

# EPC2034 – Enhancement Mode Power Transistor

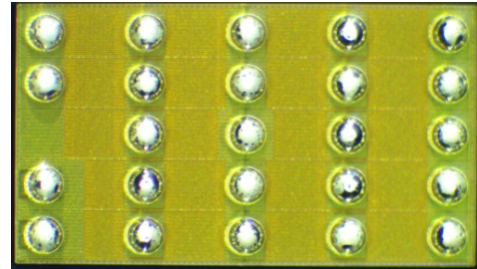
## Preliminary Specification Sheet



**Status: Engineering**

**Features:**

- $V_{DS}$ , 200 V
- Maximum  $R_{DS(on)}$ , 10 m $\Omega$
- $I_D$ , 31 A
- Pb-Free (RoHS Compliant), Halogen Free



**Applications:**

- High Frequency DC-DC Conversion
- Motor Drive
- Industrial Automation
- Class-D Audio

EPC2034 eGaN® FETs are supplied only in passivated die form with solder balls

Die Size: 2.6 mm x 4.6 mm

**MAXIMUM RATINGS**

Parameter		Value
$V_{DS}$	Maximum Drain – Source Voltage	200 V
$V_{GS}$	Gate – Source Maximum Voltage Range	-4 V < $V_{GS}$ < 6 V
$I_D$	Continuous Drain Current, ( $T_A = 25\text{ }^\circ\text{C}$ , $R_{\theta JA} = 7\text{ }^\circ\text{C/W}$ )	31 A
	Maximum Pulsed Drain Current, 25 $^\circ\text{C}$ , $T_{pulse} = 300\text{ }\mu\text{s}$	140 A
$T_J$	Optimum Temperature Range	-40 $^\circ\text{C}$ < $T_J$ < 150 $^\circ\text{C}$

**STATIC CHARACTERISTICS**

Parameter		Conditions	Value
$I_{DSS}$	Maximum Drain – Source Leakage	$V_{DS} = 160\text{ V}$ , $V_{GS} = 0\text{ V}$	0.4 mA
$R_{DS(on)}$	Maximum $R_{DS(on)}$	$V_{GS} = 5\text{ V}$ , $I_D = 20\text{ A}$	10 m $\Omega$
	Typical $R_{DS(on)}$	$V_{GS} = 5\text{ V}$ , $I_D = 20\text{ A}$	7 m $\Omega$
$V_{GS(th)}$	Gate – Source Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 7\text{ mA}$	0.8 V < $V_{GS(th)}$ < 2.5 V
$I_{GSS}$	Gate – Source Maximum Positive Leakage	$V_{GS} = 5\text{ V}$	7 mA
	Gate – Source Maximum Negative Leakage	$V_{GS} = -4\text{ V}$	-0.4 mA

$T_J = 25\text{ }^\circ\text{C}$  unless otherwise stated  
 Specifications are with Substrate shorted to Source

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### DYNAMIC CHARACTERISTICS

Parameter		Conditions	Typical Value
$C_{ISS}$	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	940 pF
$C_{OSS}$	Output Capacitance		530 pF
$C_{RSS}$	Reverse Transfer Capacitance		5 pF
$R_G$	Gate Resistance		0.5 $\Omega$
$Q_G$	Total Gate Charge	$V_{DS} = 100\text{ V}, I_D = 20\text{ A}, V_{GS} = 5\text{ V}$	8.5 nC
$Q_{GS}$	Gate to Source Charge	$V_{DS} = 100\text{ V}, I_D = 20\text{ A}$	2.6 nC
$Q_{GD}$	Gate to Drain Charge		1.4 nC
$Q_{G(th)}$	Gate Charge at Threshold		1.8 nC
$Q_{OSS}$	Output Charge	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	80 nC
$Q_{RR}$	Source-Drain Recovery Charge		0

$T_J = 25\text{ }^\circ\text{C}$  unless otherwise stated

Specifications are with Substrate shorted to Source

### THERMAL CHARACTERISTICS

		TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.45	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction to Board	3.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	45	$^\circ\text{C}/\text{W}$

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

See [http://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details

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Figure 1: Typical Output Characteristics at 25°C

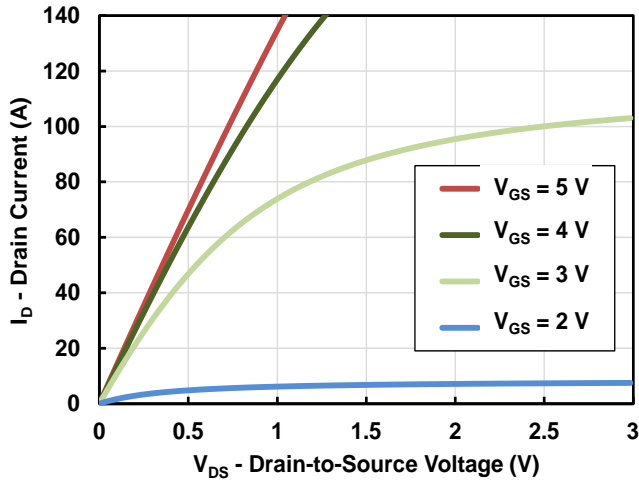


Figure 2: Transfer Characteristics

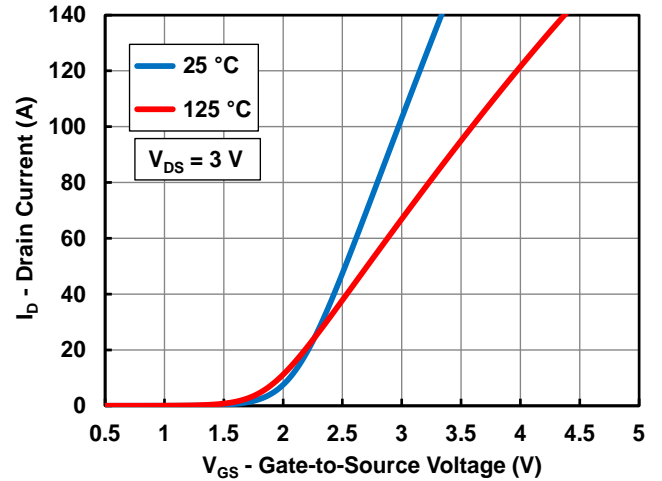


Figure 3:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

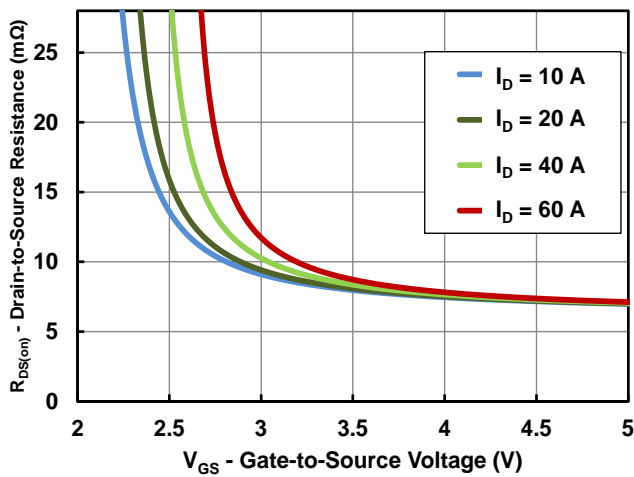


Figure 4:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Temperatures

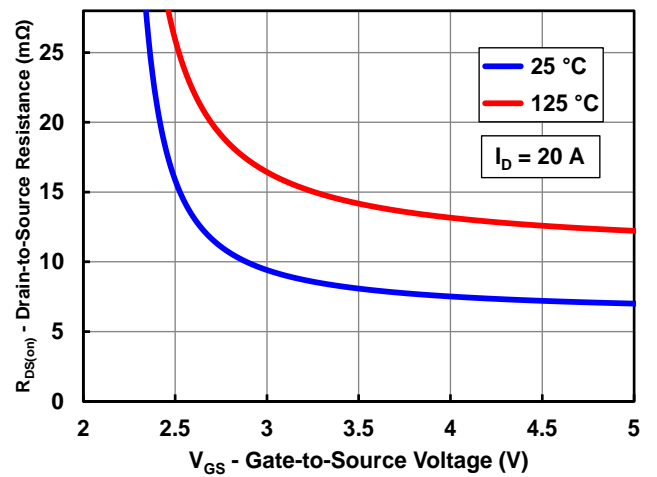


Figure 5a: Capacitance (Linear Scale)

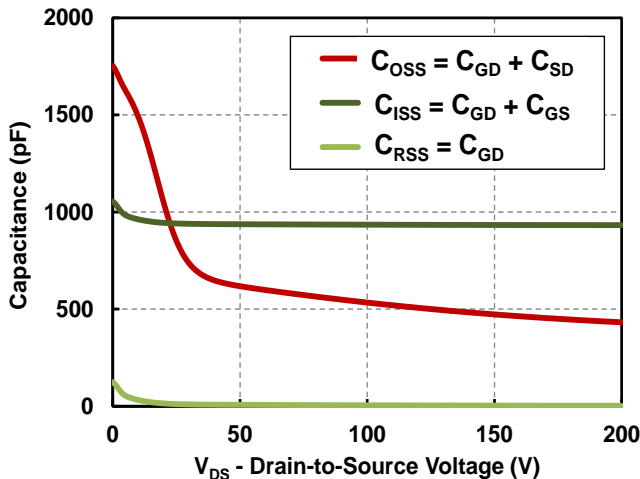
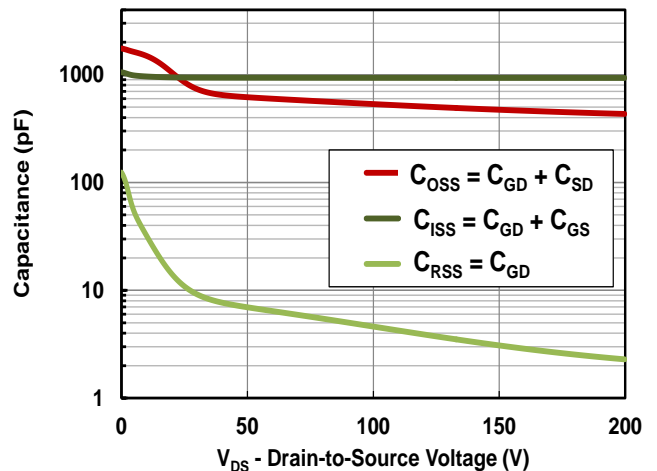


Figure 5b: Capacitance (Log Scale)



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Figure 6: Gate Charge

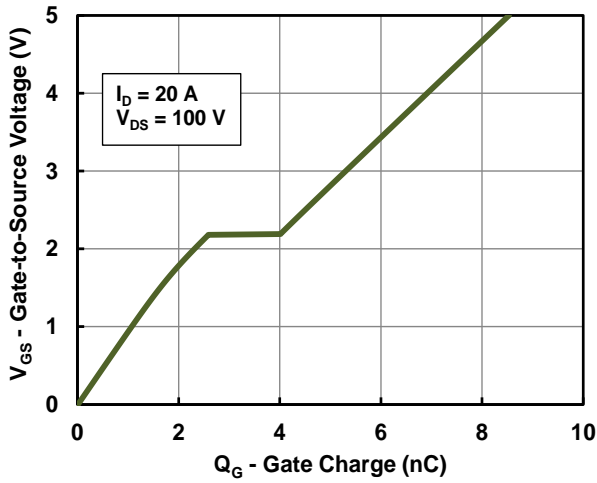


Figure 7: Reverse Drain-Source Characteristics

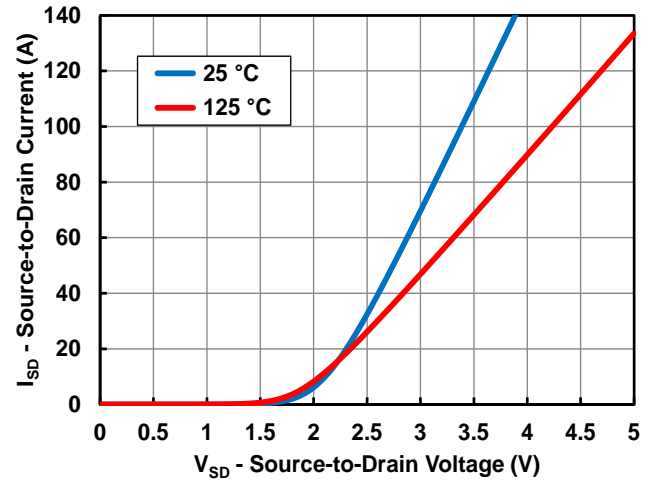


Figure 8: Normalized On Resistance vs. Temperature

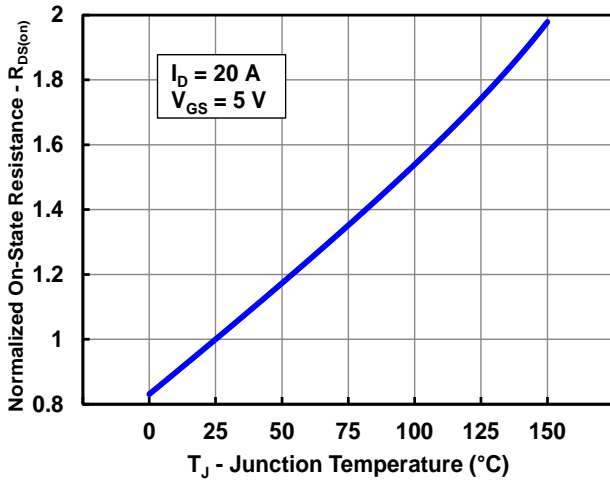


Figure 9: Normalized Threshold Voltage vs. Temperature

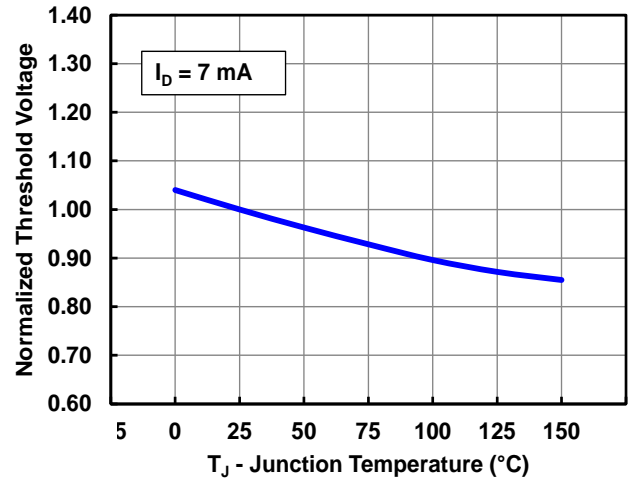
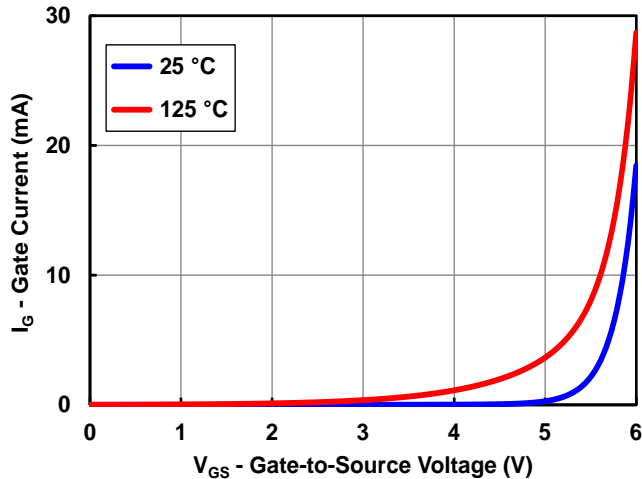


Figure 10: Gate Current



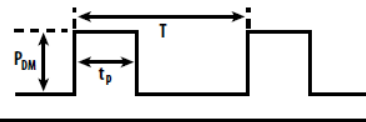
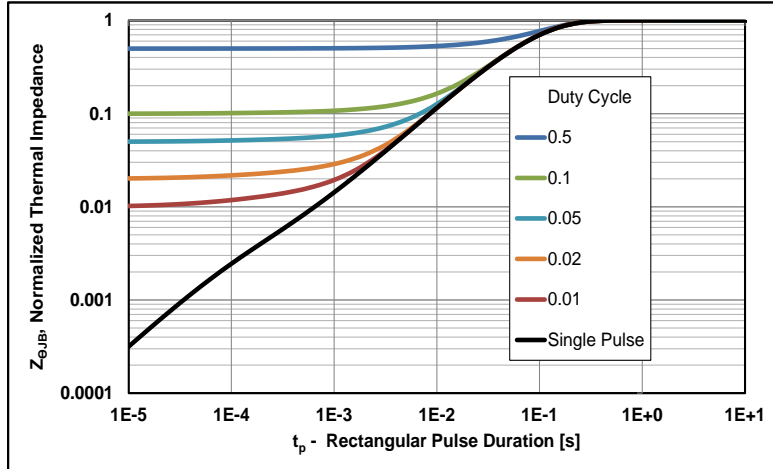
All measurements were done with substrate shorted to source

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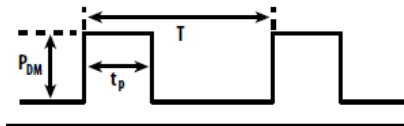
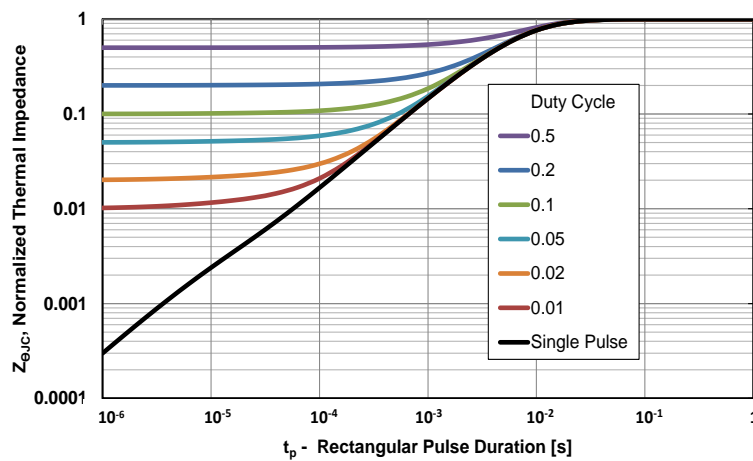
Figure 11: Transient Thermal Response Curves

### Junction-to-Board



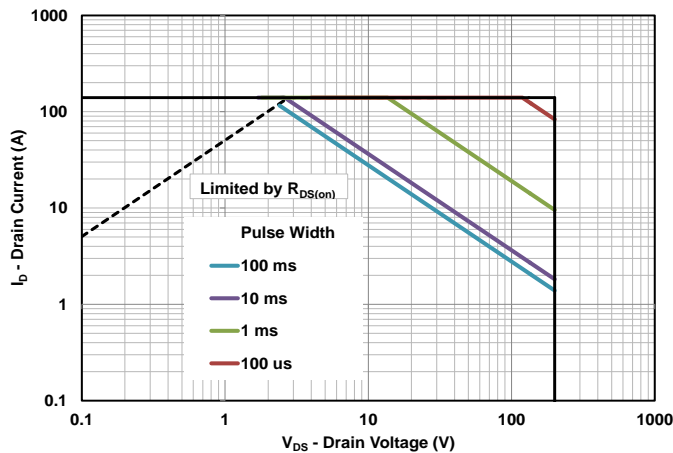
Notes:  
 Duty Factor =  $t_p/T$   
 Peak  $T_J = P_{DM} \times Z_{\Theta JB} \times R_{\Theta JB} + T_B$

### Junction-to-Case



Notes:  
 Duty Factor =  $t_p/T$   
 Peak  $T_J = P_{DM} \times Z_{\Theta JC} \times R_{\Theta JC} + T_C$

Figure 12: Safe Operating Area



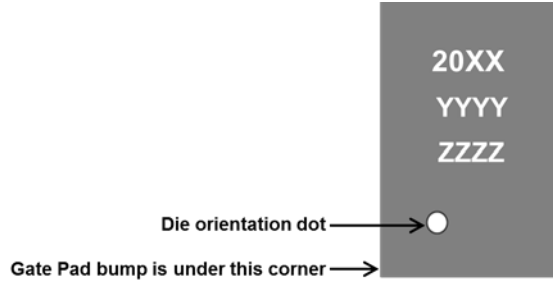
$T_J = \text{Max Rated}, T_C = +25^\circ\text{C}, \text{Single Pulse}$

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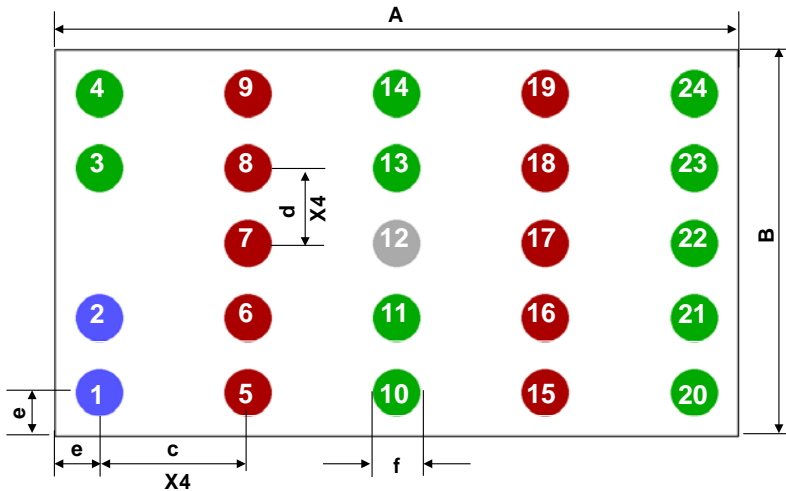
### DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2034ENGR	20XX	YYYY	ZZZZ

### DIE OUTLINE

#### Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	4570	4600	4630
B	2570	2600	2630
c	1000	1000	1000
d	500	500	500
e	285	300	315
f	332	369	406

All

Pads 1 and 2 are Gate;  
 Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;  
 Pads 3, 4, 10, 11, 13, 14, 20, 21, 22, 23, 24 are Source;  
 Pad 12 is Substrate.

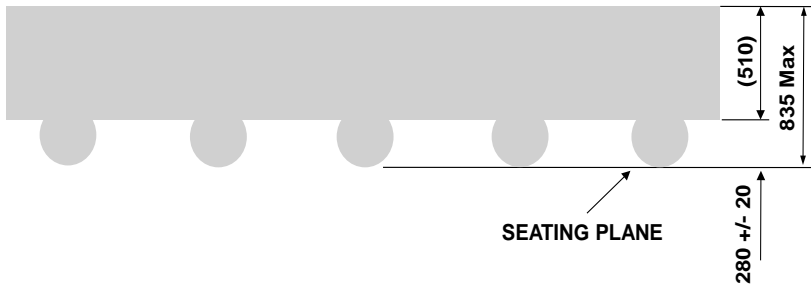
measurements in micrometers ( $\mu\text{m}$ )

### Side View

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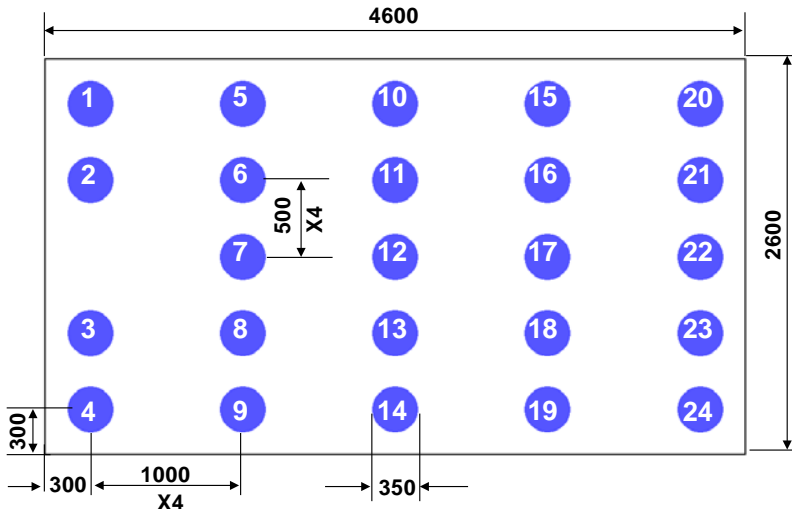


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### RECOMMENDED LAND PATTERN

(Units in  $\mu\text{m}$ )



Pads 1 and 2 are Gate;

Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;

Pads 3, 4, 10, 11, 13, 14, 20, 21, 22, 23, 24 are Source;

Pad 12 is Substrate.

Land pattern is solder mask defined

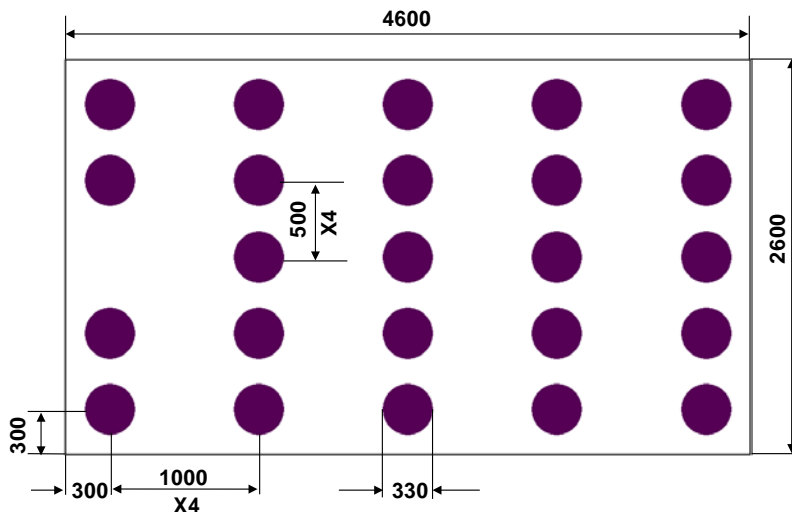
Solder mask opening is 350  $\mu\text{m}$

It is recommended to have on-Cu trace PCB vias

It is recommended to connect the substrate pin to source pin on the PCB in most high frequency switching applications

### RECOMMENDED STENCIL

(Units in  $\mu\text{m}$ )



Recommended stencil should be 4mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

For assembly recommendations please visit [www.epc-co.com/epc/DesignSupport/AssemblyBasics.aspx](http://www.epc-co.com/epc/DesignSupport/AssemblyBasics.aspx)

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012

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