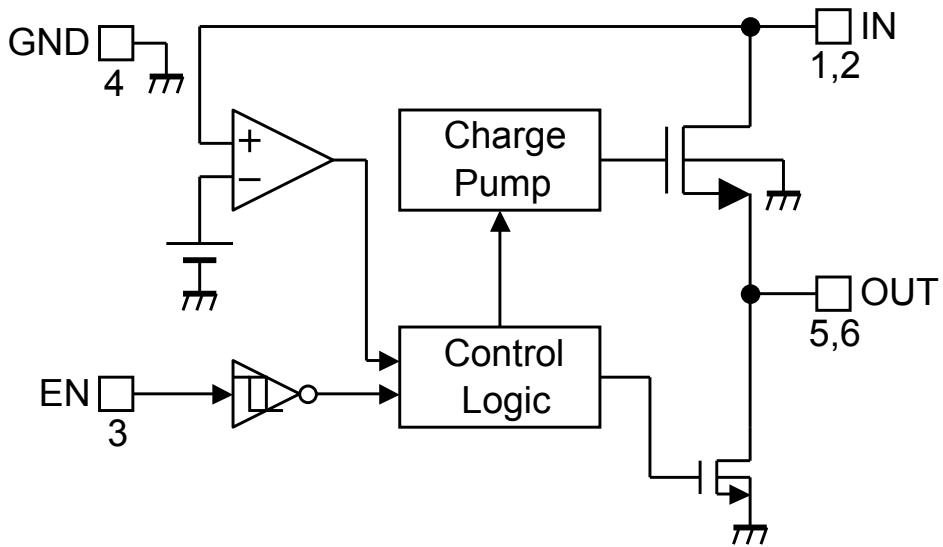
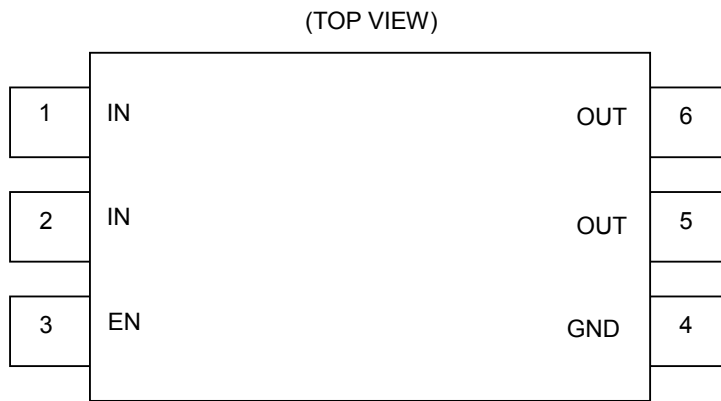


Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	Pin Function
1	IN	Switch input pin. When in use, connect each pin outside.
2		
3	EN	Switch control input pin (hysteresis input) Switch ON at High.
4	GND	Ground
5	OUT	Switch output pin When in use, connect each pin outside.
6		

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{IN}	-0.3 to +6.0	V
Control Input Voltage	V_{EN}	-0.3 to $V_{IN} + 0.3$	V
Switch Output Voltage	V_{OUT}	-0.3 to +6.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	0.85 ^(Note 1)	W

(Note 1) Mounted on 70mm x 70mm x 1.6mm glass-epoxy PCB. Derating : 6.8mW/°C above Ta=25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	V_{IN}	3.0	-	5.5	V
Operating Temperature	Topr	-25	-	+75	°C
Switch Current	I_{OUT}	-	-	500	mA

Electrical Characteristics (Unless otherwise specified, Ta = 25°C, $V_{IN} = 5V$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Operating Current	I_{DD}	-	50	75	μA	$V_{EN} = 5V, V_{OUT} = \text{Open}$
Standby Current	I_{STB}	-	0.1	1	μA	$V_{EN} = 0V, V_{OUT} = \text{Open}$
EN Input Voltage	V_{ENH}	-	-	2.5	V	High Level Input Voltage
	V_{ENL}	0.7	-	-	V	Low Level Input Voltage
EN Input Leak Current	I_{EN}	-1	+0.01	+1	μA	
Switch ON-Resistance	R_{ON}	-	200	255	m Ω	$V_{IN} = 5V$
		-	250	335	m Ω	$V_{IN} = 3.3V$
Switch Leak Current	I_{LEAK}	-	-	10	μA	At Switch OFF
Switch Rise Time	t_{ON1}	-	0.4	0.8	ms	$R_L = 10\Omega$. Refer to the Timing Diagram in Figure 2.
Switch Rise Delay Time	t_{ON2}	-	0.5	1.0	ms	$R_L = 10\Omega$. Refer to the Timing Diagram in Figure 2.
Switch Fall Time	t_{OFF1}	-	1	2	μs	$R_L = 10\Omega$. Refer to the Timing Diagram in Figure 2.
Switch Fall Delay Time	t_{OFF2}	-	2	4	μs	$R_L = 10\Omega$. Refer to the Timing Diagram in Figure 2.
UVLO Threshold Voltage	V_{UVLO}	1.9	2.2	2.5	V	V_{IN} Increasing
		1.8	2.1	2.4	V	V_{IN} Decreasing
Discharge Resistance	R_{DISC}	-	200	350	Ω	$V_{EN} = 0V, I_L = 1mA$
Discharge Current	I_{DISC}	0.8	1.8	-	mA	$V_{EN} = 0V, V_{IN} = V_{OUT} = 1.8V$

Measurement Circuit

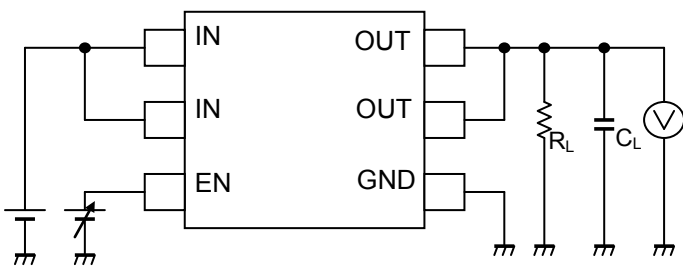


Figure 1. Measurement Circuit

Timing Diagram

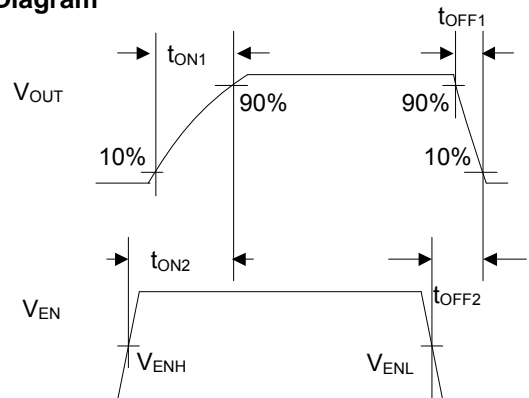


Figure 2. Timing Diagram

Typical Performance Curves

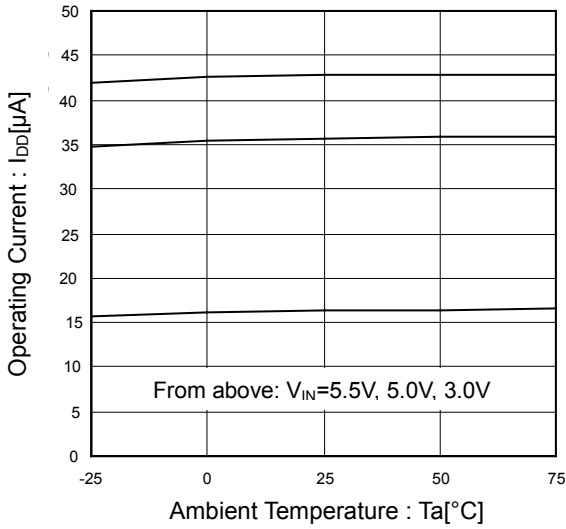


Figure 3. Operating Current vs Ambient Temperature

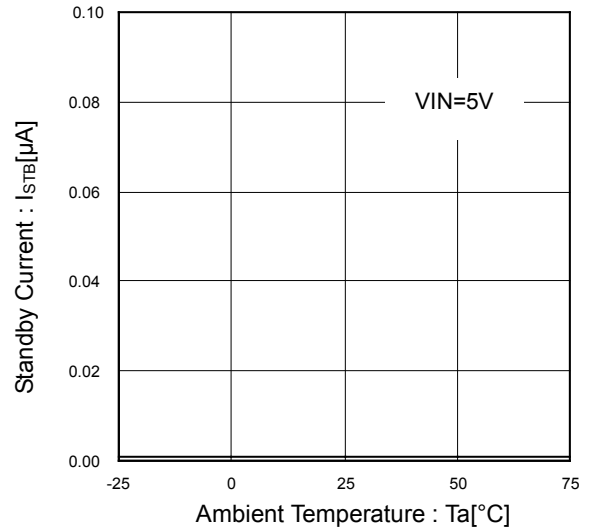


Figure 4. Standby Current vs Ambient Temperature

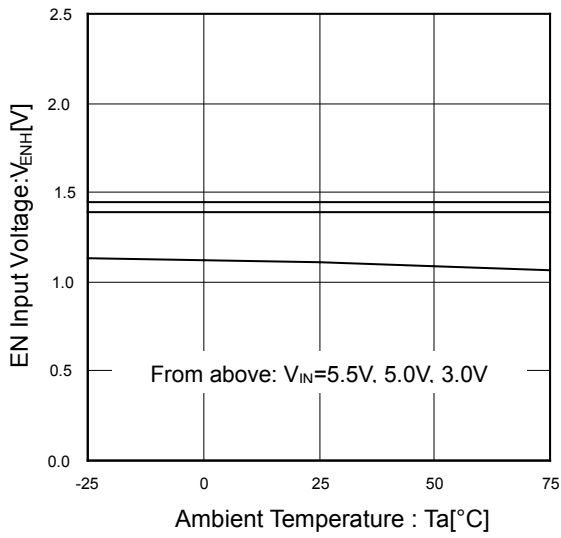


Figure 5. EN Input Voltage vs Ambient Temperature (High Level Input Voltage)

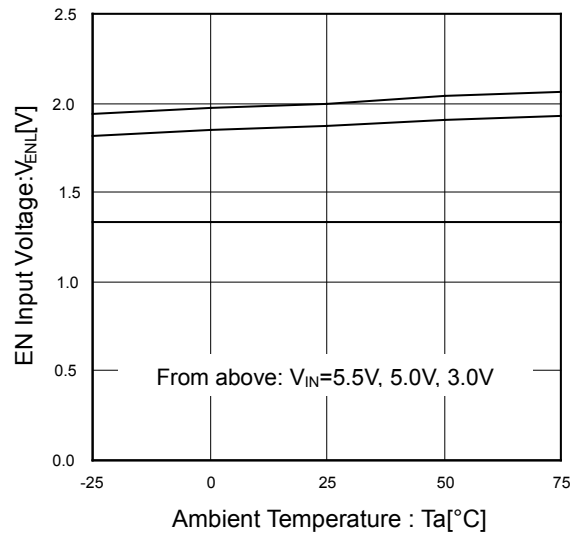


Figure 6. EN Input Voltage vs Ambient Temperature (Low Level Input Voltage)

Typical Performance Curves - continued

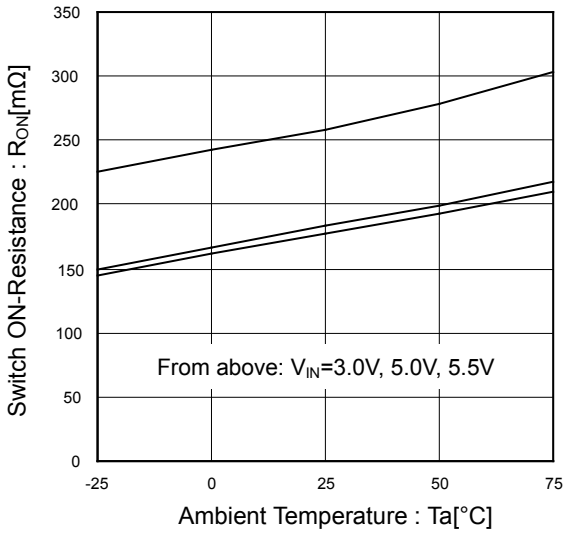


Figure 7. Switch ON-Resistance vs Ambient Temperature

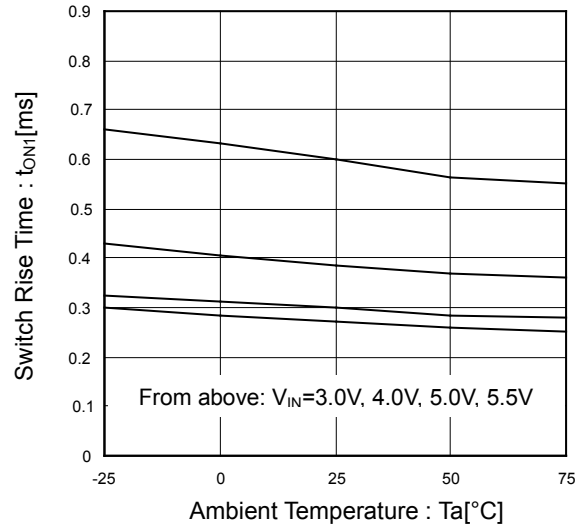


Figure 8. Switch Rise Time vs Ambient Temperature

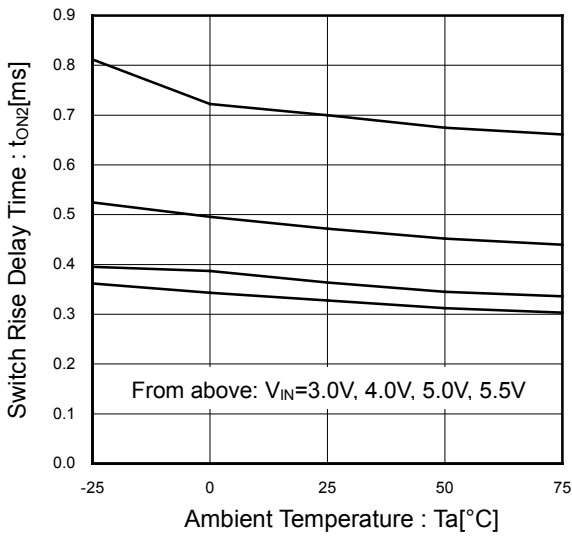


Figure 9. Switch Rise Delay Time vs Ambient Temperature

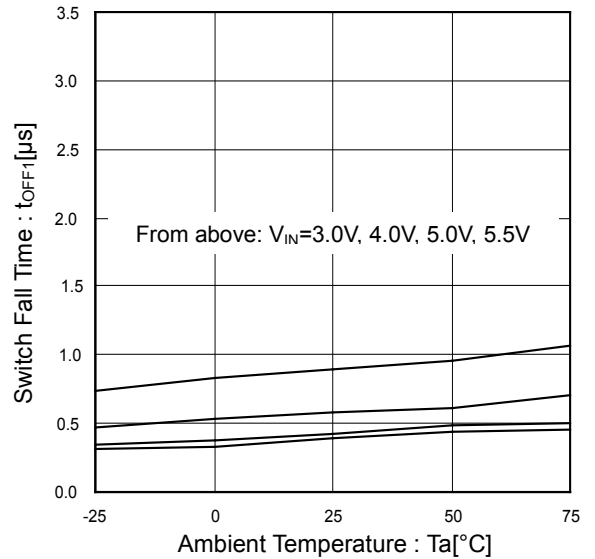


Figure 10. Switch Fall Time vs Ambient Temperature

Typical Performance Curves - continued

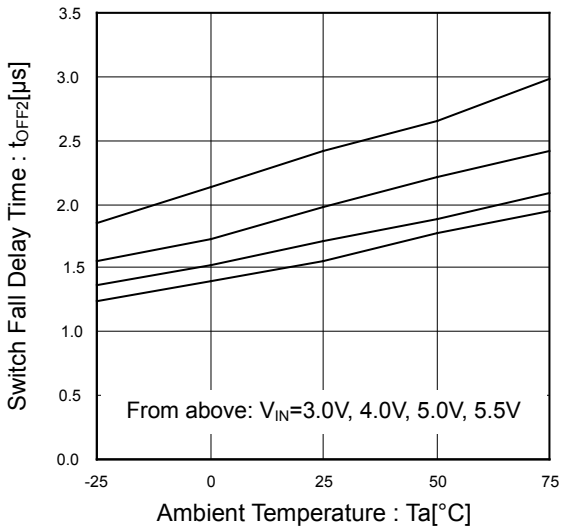


Figure 11. Switch Fall Delay Time vs Ambient Temperature

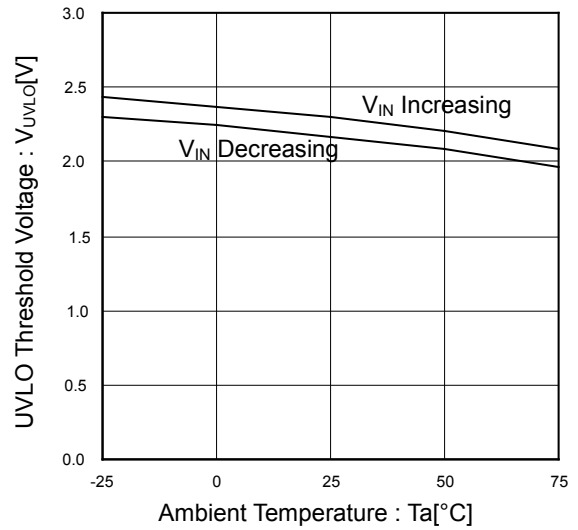


Figure 12. UVLO Threshold Voltage vs Ambient Temperature

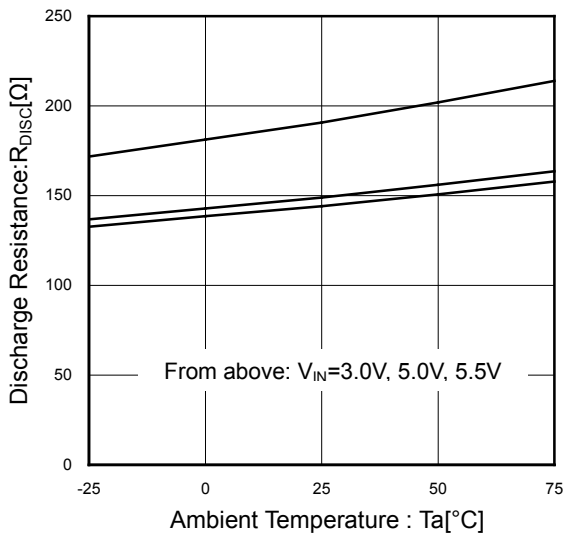


Figure 13. Discharge Resistance vs Ambient Temperature

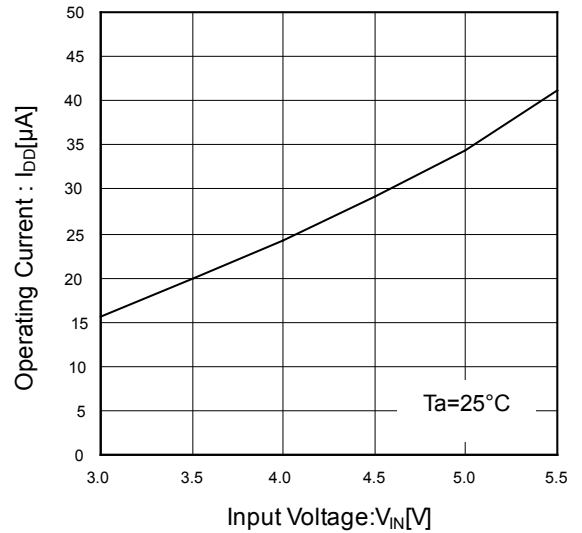


Figure 14. Operating Current vs Input Voltage

Typical Performance Curves - continued

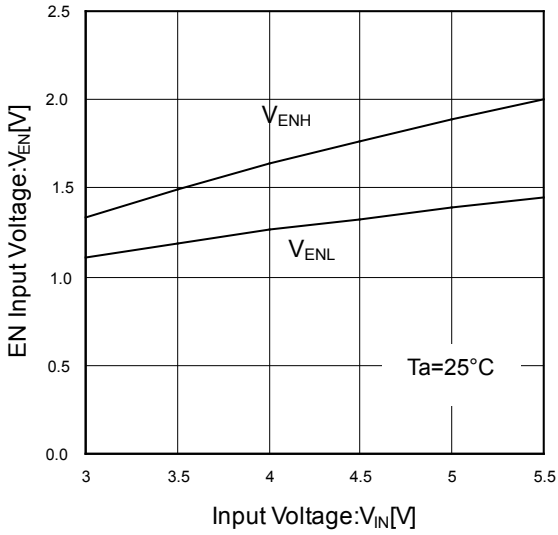


Figure 15. EN Input Voltage vs Input Voltage

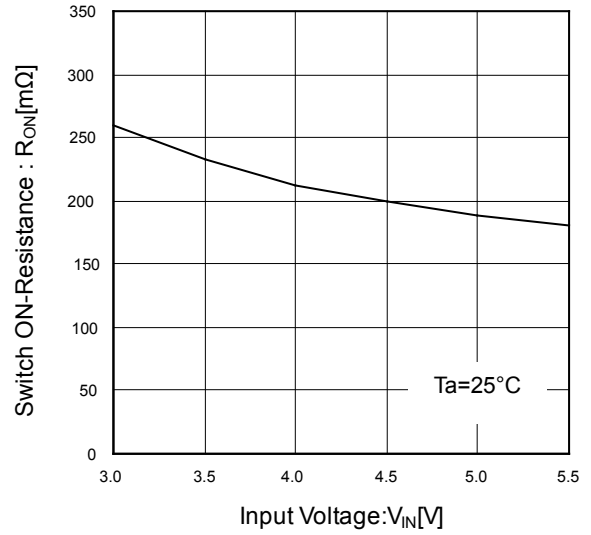


Figure 16. Switch ON-Resistance vs Input Voltage

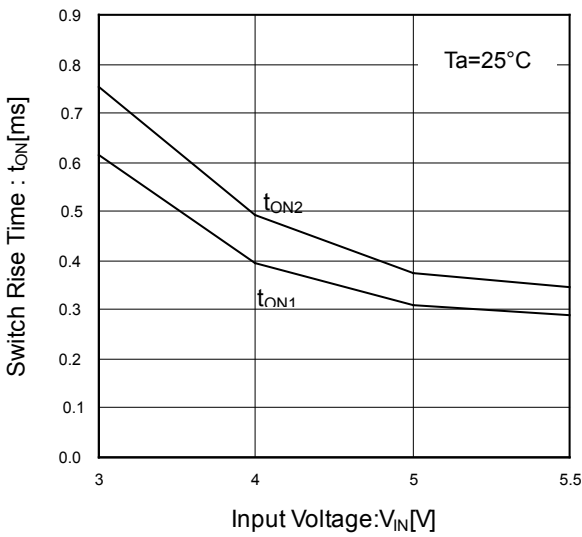


Figure 17. Switch Rise Time vs Input Voltage

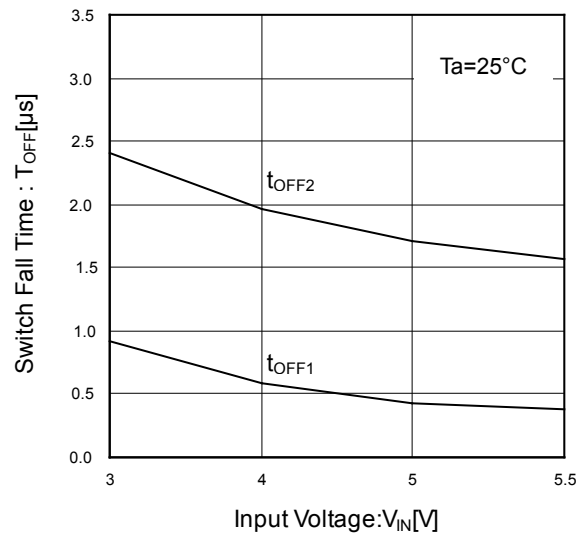


Figure 18. Switch Fall Time vs Input Voltage

Typical Performance Curves - continued

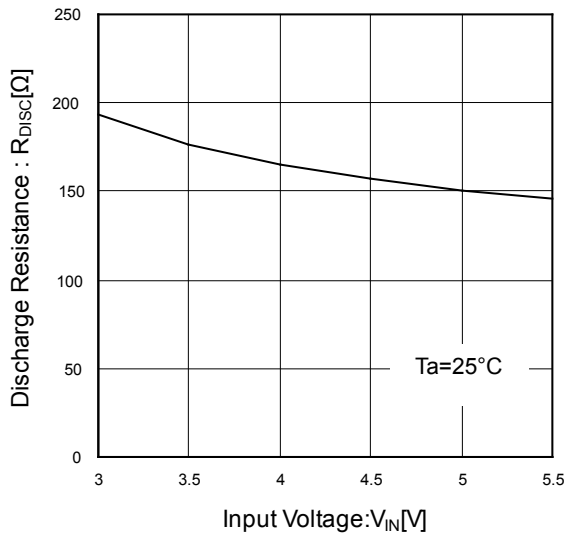


Figure 19. Discharge Resistance vs Input Voltage

Typical Wave Forms

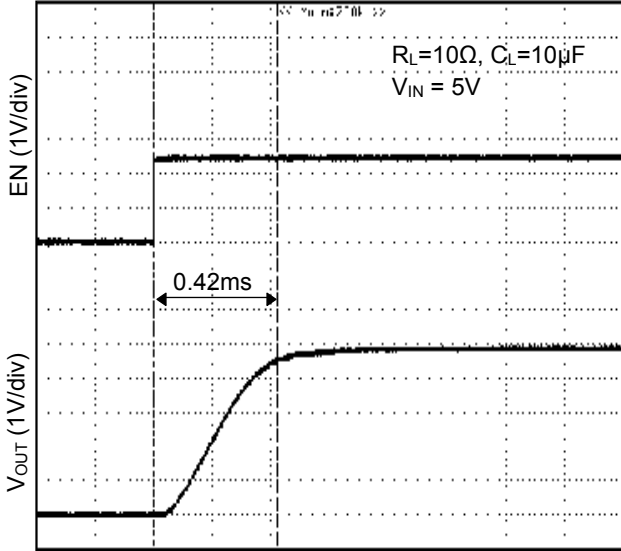


Figure 20. Switch Rise Time

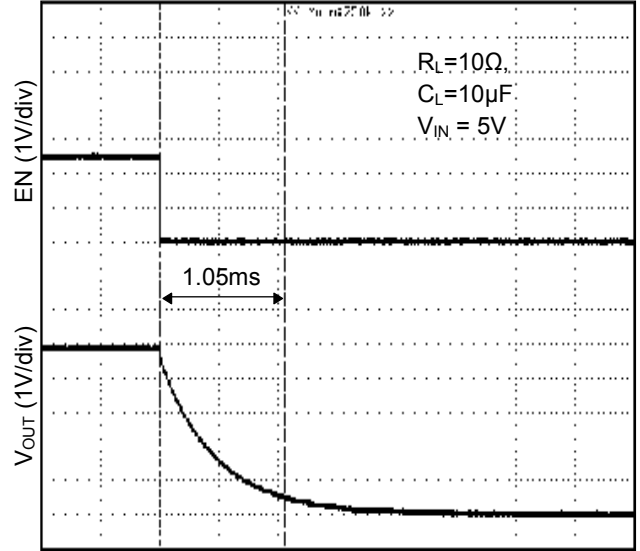


Figure 21. Switch Fall Time

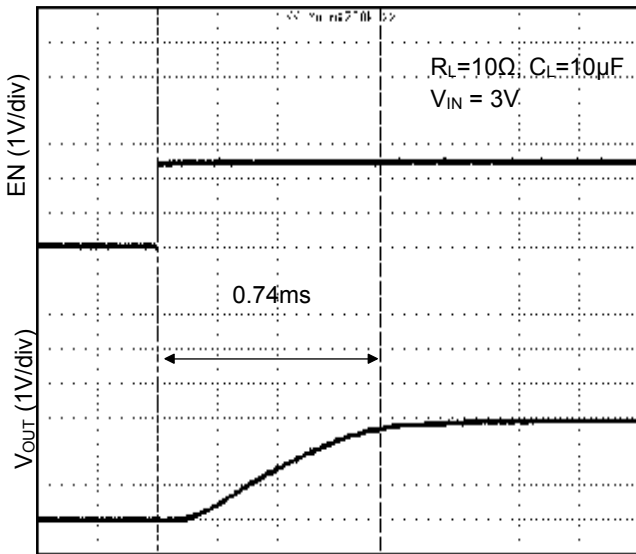


Figure 22. Switch Rise Time

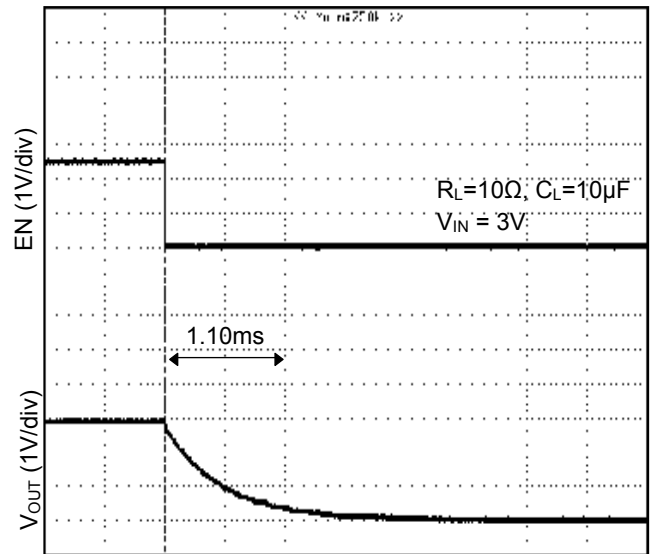


Figure 23. Switch Fall Time

Typical Wave Forms – continued

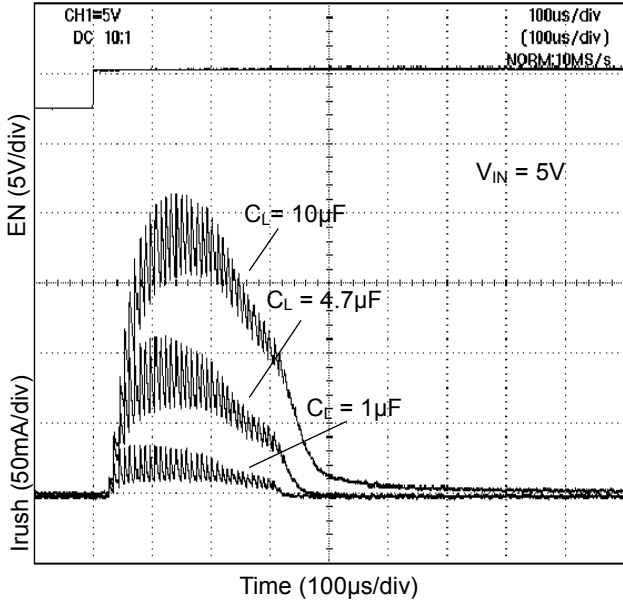


Figure 24. Inrush Current

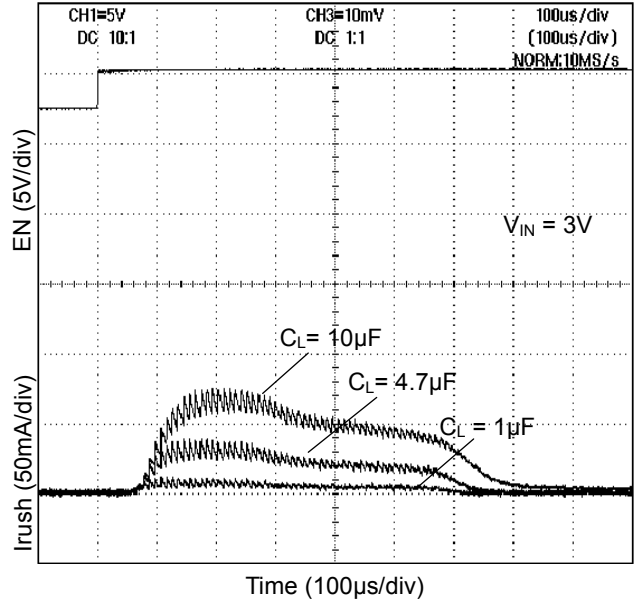


Figure 25. Inrush Current

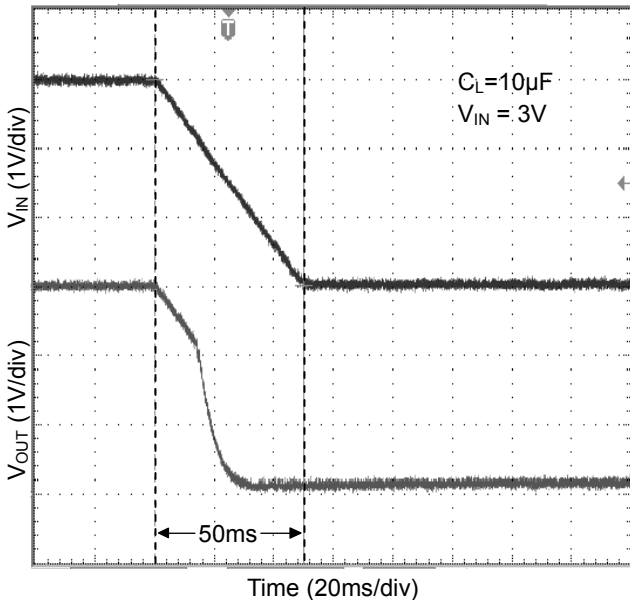


Figure 26. UVLO

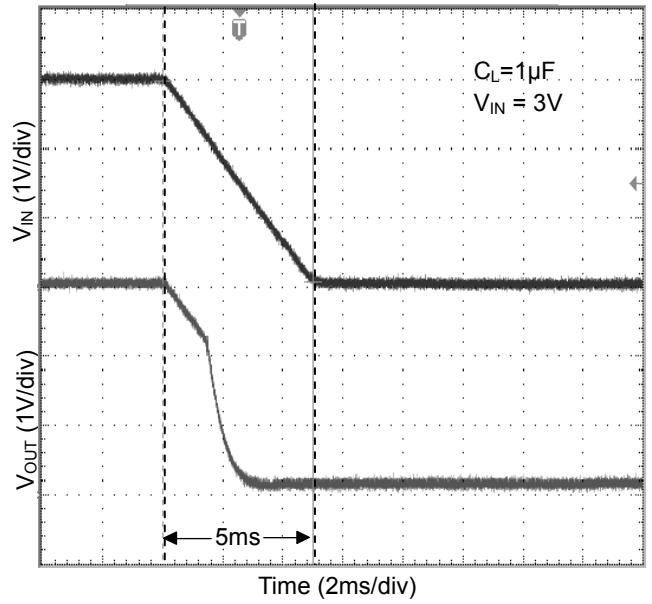
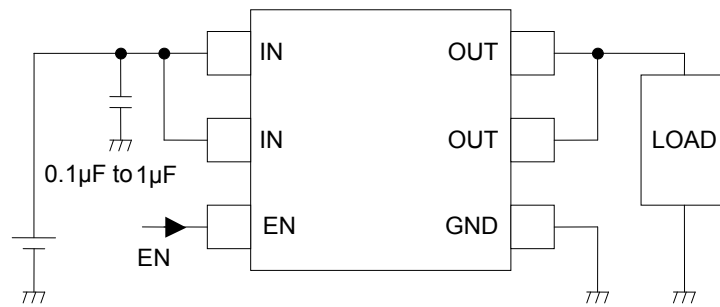


Figure 27. UVLO

Typical Application Circuit



Functional Description

1. Input / Output

The IN and OUT pins are connected to the drain and the source of the N-MOS switch respectively. The IN pin is also used as power supply input to the internal control circuit.

When EN input is set to High level and the switch is turned ON, the IN and OUT pins are connected by a 200mΩ switch. Under normal conditions, current flows from IN to OUT. If voltage at pin OUT pin is higher than pin IN, current flows from OUT to IN since the switch is bidirectional. There is no parasitic diode between the drain and the source, so it is possible to prevent current from flowing reversely from OUT pin to IN pin when the switch is disabled.

2. Discharge Circuit

When the switch between the IN and the OUT is turned OFF, the 200Ω(Typ) discharge switch between OUT and GND turns on. By turning on this switch, electric charge at capacitive load is discharged.

3. Under Voltage Lockout (UVLO)

The UVLO circuit monitors the voltage of the IN pin when the EN input is active. UVLO circuit prevents the switch from turning ON until the IN exceeds 2.2V (Typ). If the IN drops below 2.1V (Typ) while the switch turns on, then UVLO shuts off the switch.

While the switch between the IN pin and OUT pin is OFF due to UVLO operations, the switch of the discharge circuit turns ON. However, when the voltage of IN declines tremendously, then the OUT pin becomes Hi-Z.

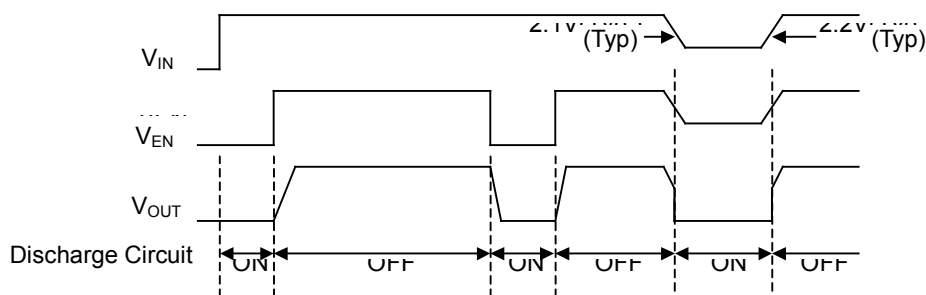
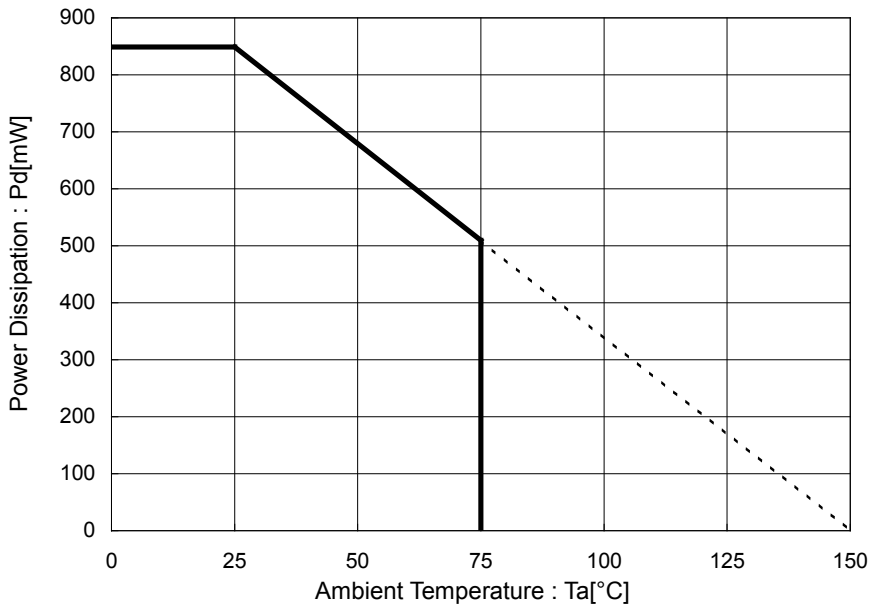


Figure 28. Operation Timing

Power Dissipation

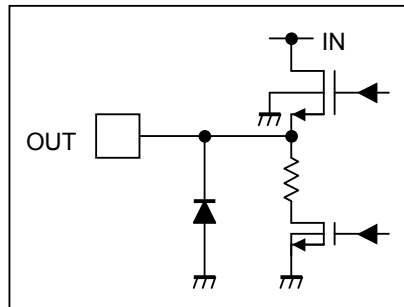
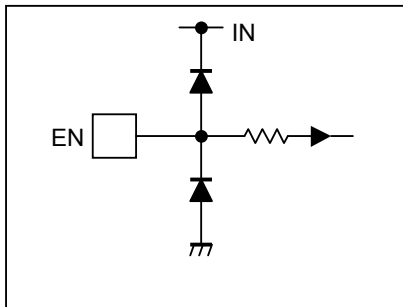
(HVSOF6 package)



70mm x 70mm x 1.6mm Glass Epoxy Board

Figure 29. Power dissipation curve (Pd-Ta Curve)

I/O Equivalence Circuit



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes - continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

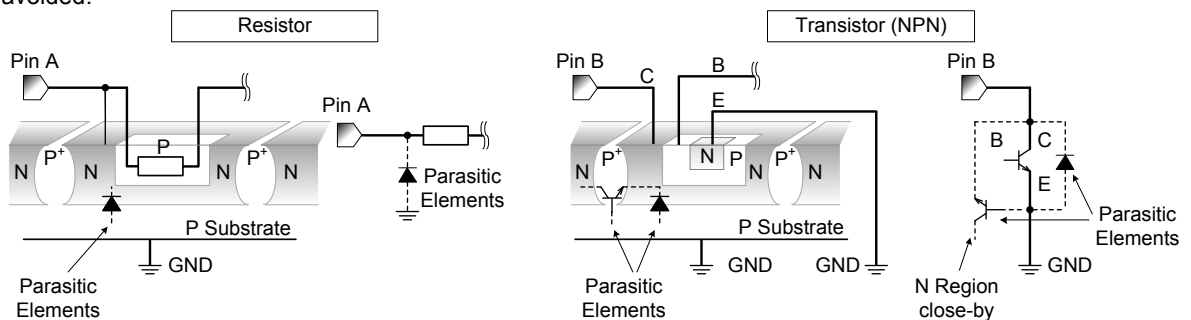
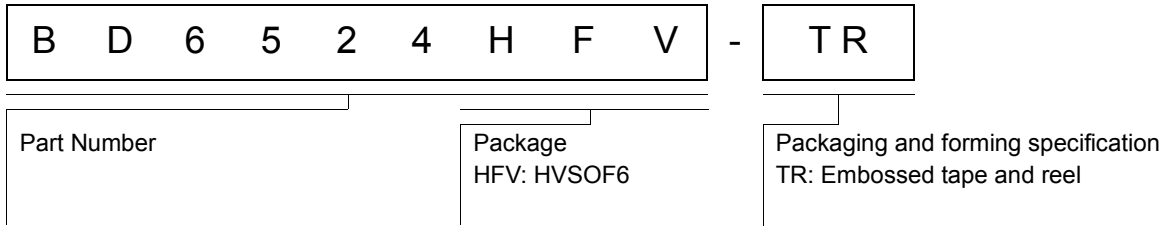


Figure 30. Example of monolithic IC structure

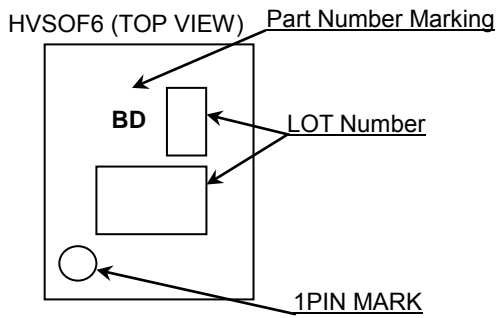
13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

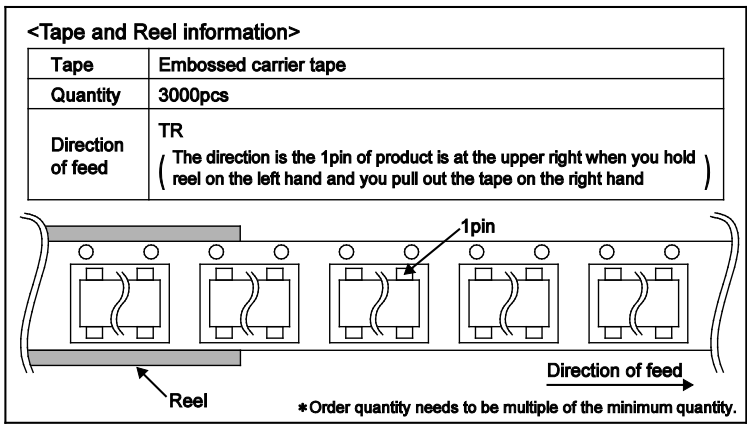
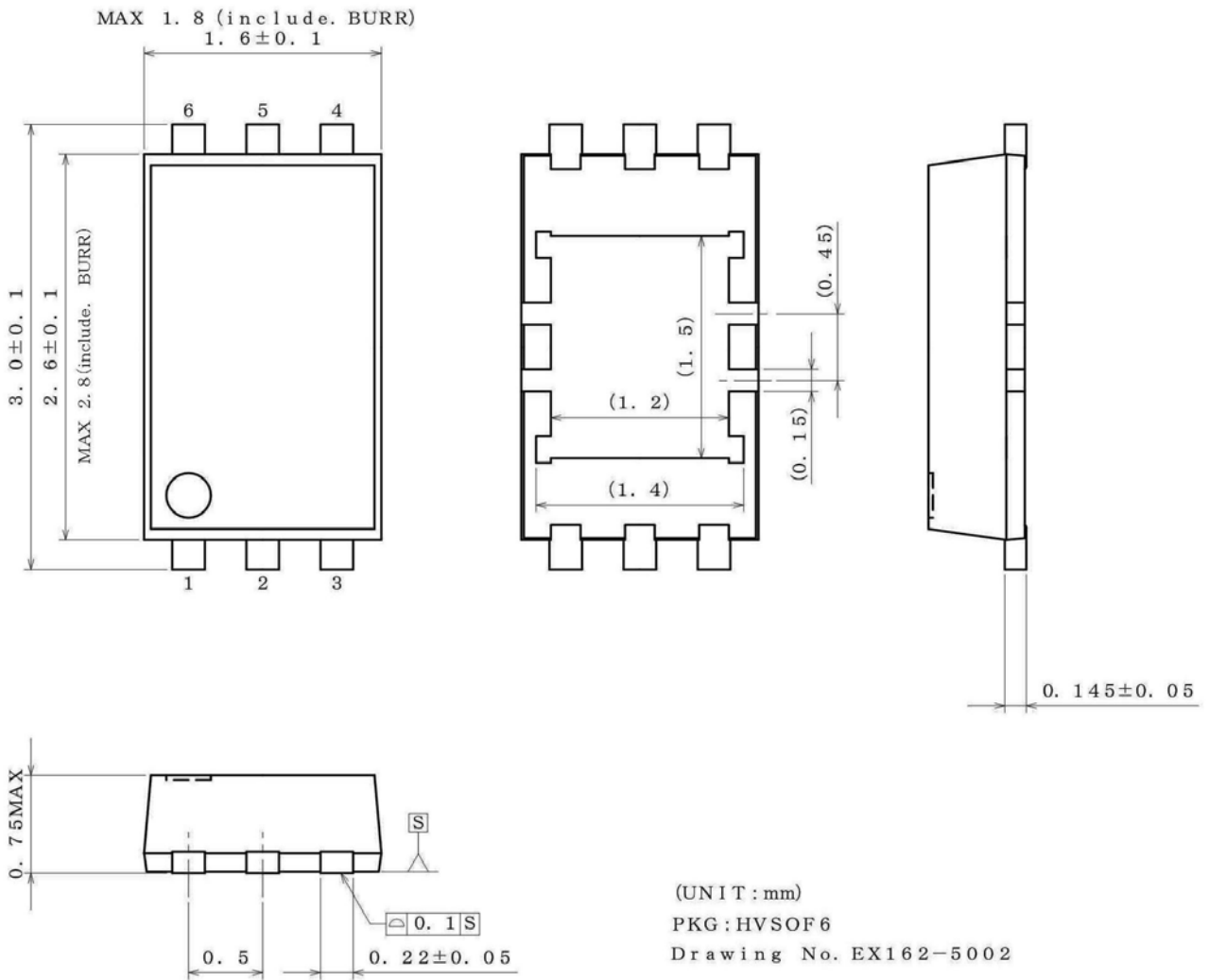


Marking Diagram



Physical Dimension, Tape and Reel Information

Package Name	HVSOF6
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Revision History

Date	Revision	Changes
11.Mar.2013	001	New Release
21.Aug.2014	002	Applied the ROHM Standard Style and improved understandability.

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

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Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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