Nonreflective, Silicon SP4T Switch, 0.1 GHz to 6.0 GHz

Data Sheet **HMC7992**

FEATURES

Nonreflective, 50 Ω design
High isolation: 45 dB typical at 2 GHz
Low insertion loss: 0.6 dB at 2 GHz
High power handling
- **33 dBm through path**
- **27 dBm terminated path**

High linearity
- **1 dB compression (P1dB): 35 dBm typical**
- **Input third-order intercept (IIP3): 58 dBm typical**

ESD rating: 2 kV human body model (HBM), Class 2
Single positive supply: 3.3 V to 5.0 V
Standard TTL-, CMOS-, and 1.8 V-compatible control
16-lead, 3 mm × 3 mm LFCSP package (9 mm²)
Pin compatible with the HMC241ALP3E

APPLICATIONS

Cellular/4G infrastructure
Wireless infrastructure
Automotive telematics
Mobile radios
Test equipment

FUNCTIONAL BLOCK DIAGRAM

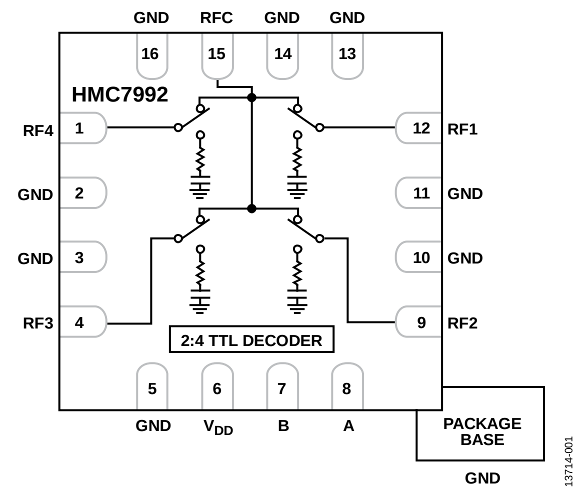


Figure 1.

GENERAL DESCRIPTION

The HMC7992 is a general-purpose, nonreflective, 0.1 GHz to 6.0 GHz, silicon, single-pole, four-throw (SP4T) switch in a leadless, surface-mount package. The switch is ideal for cellular infrastructure applications, offers high isolation of 45 dB typical at 2 GHz, and a low insertion loss of 0.6 dB at 2 GHz. It offers excellent power handling capability up to 6.0 GHz, with input power of 1 dB compression point (P1dB) of 35 dBm at 5 V operation. The HMC7992 has good low frequency input power handling below 0.1 GHz and can operate well down to 10 kHz, with a typical 1 dB compression of 21 dBm (see Figure 21) and an IIP3 of 37 dBm (see Figure 22) at 1 MHz.

The on-chip circuitry allows the HMC7992 to operate at a single, positive supply voltage range from 3.3 V to 5 V, and as well as a single, positive control voltage from 0 V to 1.8 V/3.3 V/5.0 V. A 2:4 decoder integrated in the switch requires only two controlled input signals, with a positive control voltage range from 0 V to 1.8 V/3.3 V/5.0 V, to select one of the four radio frequency (RF) paths.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support **www.analog.com**

HMC7992* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- HMC7992 Evaluation Board

Documentation

Data Sheet

- HMC7992: Nonreflective, Silicon SP4T Switch, 0.1 GHz to 6.0 GHz Data Sheet

Design Resources

- HMC7992 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all HMC7992 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

TABLE OF CONTENTS

REVISION HISTORY

1/16—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V to 5.0 V, V_{CTL} = 0 V/V_{DD}, T_A = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INSERTION LOSS		0.1 GHz to 2.0 GHz		0.6	0.9	dB
		2.0 GHz to 4.0 GHz		0.7	1.1	dB
		4.0 GHz to 6.0 GHz		1.0	1.5	dB
ISOLATION						
RFC to RF1to RF4 (Worst Case)		0.1 GHz to 2.0 GHz	40	45		dB
		2.0 GHz to 4.0 GHz	32	37		dB
		4.0 GHz to 6.0 GHz	25	30		dB
RETURN LOSS						
On State		0.1 GHz to 2.0 GHz		25		dB
		2.0 GHz to 4.0 GHz		24		dB
		4.0 GHz to 6.0 GHz		17		dB
Off State		0.1 GHz to 2.0 GHz		7		dB
		0.4 GHz to 1.0 GHz		15		dB
		1.0 GHz to 6.0 GHz		20		dB
SWITCHING SPEED						
Rise Time and Fall Time	t_{RISE}, t_{FALL}			30		ns
On Time and Off Time	t_{ON}, t_{OFF}	10%/90% RF_{OUT}		150		ns
RADIO FREQUENCY (RF) SETTLING TIME		50% V_{CTL} to 0.1 dB margin of final RF_{OUT}		320		ns
INPUT POWER		0.1 GHz to 6.0 GHz				
1 dB Compression	P1dB	V_{DD} = 5 V		35		dB
		V_{DD} = 3.3 V		33		dB
0.1 dB Compression	P0.1dB	V_{DD} = 5 V		33		dB
		V_{DD} = 3.3 V		31		dB
INPUT THIRD-ORDER INTERCEPT	IIP3	0.1 GHz to 6.0 GHz, two-tone input power = 14 dBm/tone				
		V_{DD} = 5 V		58		dBm
		V_{DD} = 3.3 V		56		dBm
RECOMMENDED OPERATING CONDITIONS						
Bias Voltage Range	V_{DD}		3.0		5.4	V
Control Voltage Range	V_{CTL}		0		V_{DD}	V
Case Temperature Range	T_{CASE}		−40		+105	°C
Maximum RF Input Power		0.1 GHz to 6.0 GHz				
Through Path		V_{DD}/V_{CTL} = 5 V, T_{CASE} = 105°C		30		dBm
		V_{DD}/V_{CTL} = 5 V, T_{CASE} = −40°C to +85°C		33		dBm
		V_{DD}/V_{CTL} = 3.3 V, T_{CASE} = 105°C		29		dBm
		V_{DD}/V_{CTL} = 3.3 V, T_{CASE} = −40°C to +85°C		32		dBm
Terminated Path		V_{DD}/V_{CTL} = 3.3 V to 5 V, T_{CASE} = 105°C		21		dBm
		V_{DD}/V_{CTL} = 3.3 V to 5 V, T_{CASE} = 85°C		24		dBm
		V_{DD}/V_{CTL} = 3.3 V to 5 V, T_{CASE} = 25°C		27		dBm
		V_{DD}/V_{CTL} = 3.3 V to 5 V, T_{CASE} = −40°C		27		dBm
Hot Switching		V_{DD}/V_{CTL} = 3.3 V to 5 V, T_{CASE} = 105°C		24		dBm
		V_{DD}/V_{CTL} = 3.3 V to 5 V, T_{CASE} = −40°C to +85°C		27		dBm

DIGITAL CONTROL VOLTAGES

T_{CASE} = −40°C to +105°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CONTROL VOLTAGE						<1 µA typical
Low Voltage	V_{IL}	0		8.5	V	V_{DD} = 3.3 V (±5% V_{DD})
		0		1.2	V	V_{DD} = 5 V (±5% V_{DD})
High Voltage	V_{IH}	1.15		3.3	V	V_{DD} = 3.3 V (±5% V_{DD})
		1.55		5.0	V	V_{DD} = 5 V (±5% V_{DD})

BIAS AND SUPPLY CURRENT

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
SUPPLY CURRENT	I_{DD}				
V_{DD} = 3.3 V			0.16	0.20	mA
V_{DD} = 5 V			0.18	0.23	mA

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Bias Voltage Range (V_{DD})	−0.3 V to +5.5 V
Control Voltage Range (A, B)	−0.5 V to V_{DD} + (+0.5 V)
RF Input Power,[1] 3.3 V to 5 V (see Figure 2 and Figure 3)	
Through Path	34 dBm
Terminated Path	28 dBm
Hot Switching	30 dBm
Channel Temperature	135°C
Storage Temperature Range	−65°C to +150°C
Maximum Peak Reflow Temperature (MSL3)	260°C
Thermal Resistance (Channel to Package Bottom)	
Through Path	115°C
Terminated Path	200°C
ESD Sensitivity	
Human Body Model (HBM)	2 kV (Class 2)
Charged Device Model (CDM)	1.25 kV

[1] For recommended operating conditions, see Table 1.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

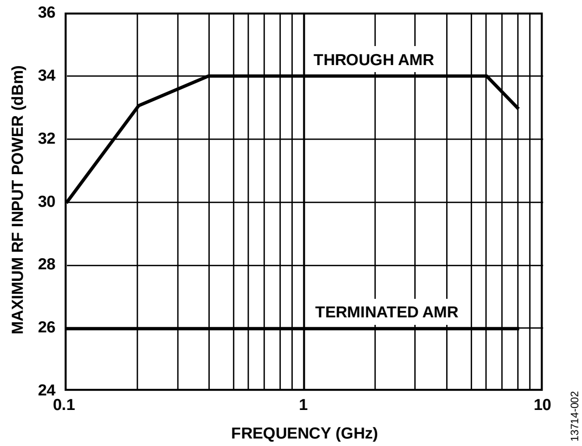


Figure 2. Maximum RF Input Power vs. Frequency

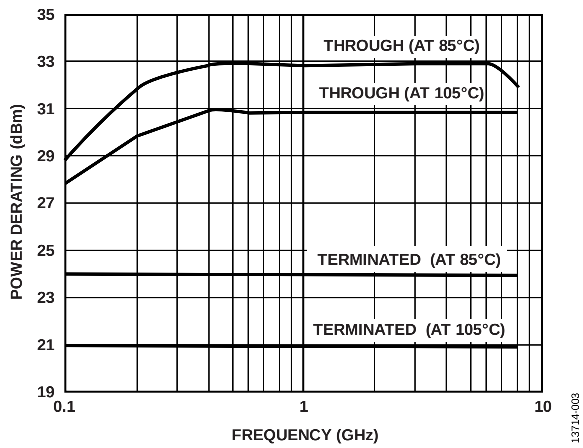
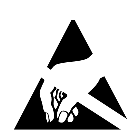


Figure 3. Power Derating vs. Frequency

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

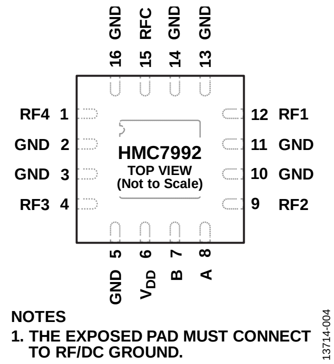


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RF4	RF Port 4. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
2, 3, 5, 10, 11, 13, 14, 16	GND	Ground. The package bottom has an exposed metal pad that must connect to the printed circuit board (PCB) RF/dc ground. See Figure 5 for the GND interface schematic.
4	RF3	RF Port 3. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
6	V_{DD}	Supply Voltage.
7	B	Logic Control Input B. See Figure 6 for the control input interface schematic. See Table 6 and the recommended input control voltages range in Table 2.
8	A	Logic Control Input A. See Figure 6 for the control input interface schematic. See Table 6 and the recommended input control voltages range in Table 2.
9	RF2	RF Port 2. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
12	RF1	RF Port 1. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
15	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
	EPAD	Exposed Pad. The exposed pad must connect to RF/dc ground.

Table 6. Truth Table

Control Input		Signal Path State
A	B	RFC to
Low	Low	RF1
High	Low	RF2
Low	High	RF3
High	High	RF4

INTERFACE SCHEMATICS

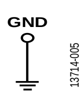


Figure 5. GND Interface Schematic

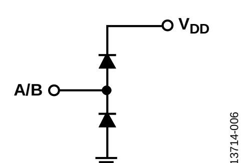


Figure 6. Logic Control (A/B) Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, ISOLATION, AND RETURN LOSS

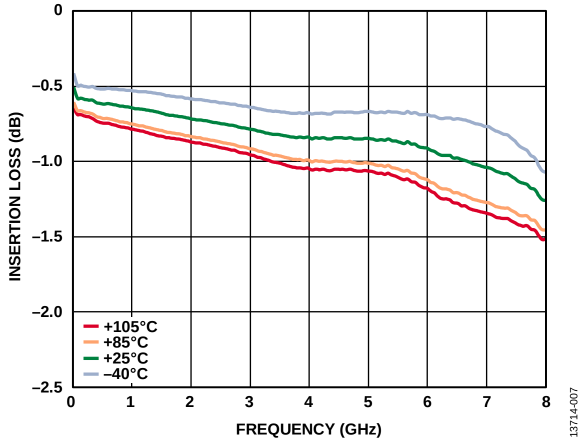


Figure 7. Insertion Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V

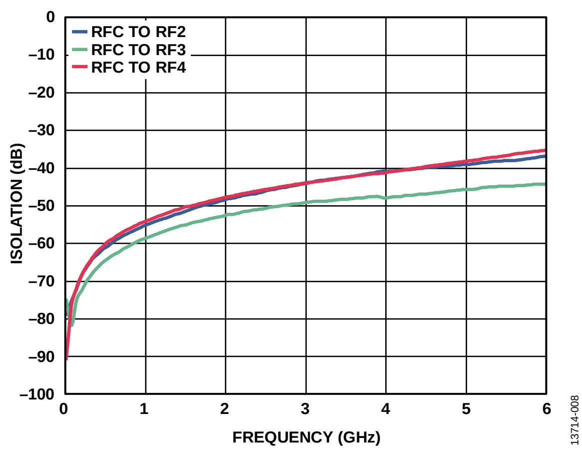


Figure 8. Isolation vs. Frequency, V_{DD} = 3.3 V to 5 V, RFC to RF1 = On

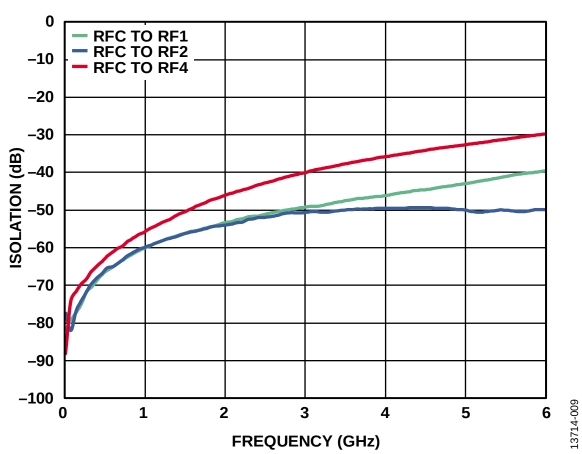


Figure 9. Isolation vs. Frequency, V_{DD} = 3.3 V to 5 V, RFC to RF3 = On

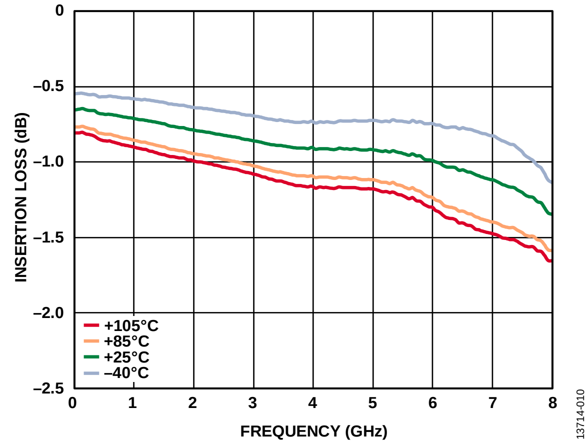


Figure 10. Insertion Loss vs. Frequency for Various Temperatures, V_{DD} = 3.3 V

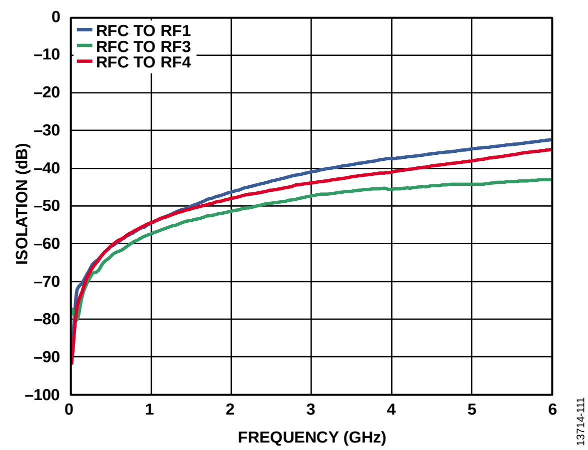


Figure 11. Isolation vs. Frequency, V_{DD} = 3.3 V to 5 V, RFC to RF2 = On

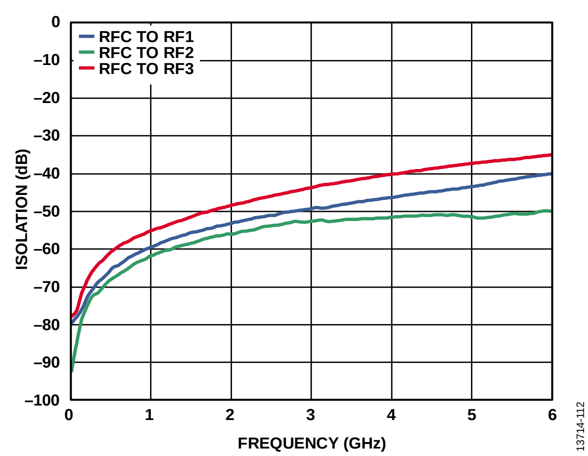


Figure 12. Isolation vs. Frequency, V_{DD} = 3.3 V to 5 V, RFC to RF4 = On

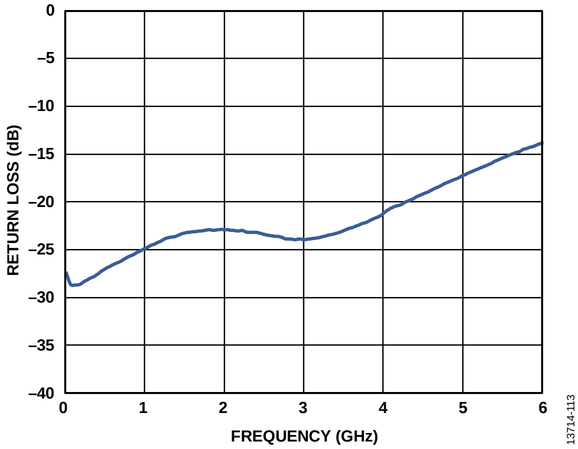


Figure 13. Return Loss for RFC vs. Frequency, V_{DD} = 3.3 V to 5 V

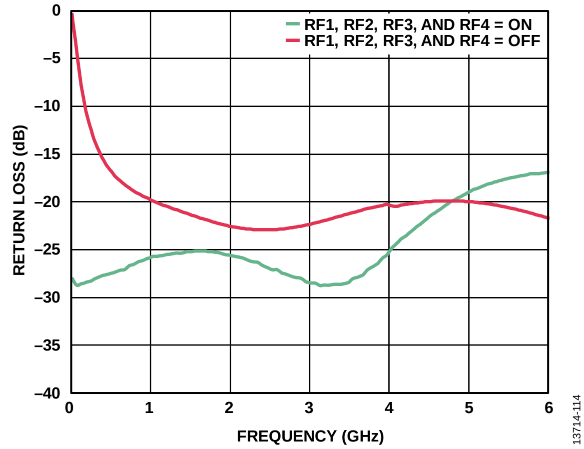


Figure 14. Return Loss for RF1, RF2, RF3, and RF4 vs. Frequency, V_{DD} = 3.3 V to 5 V

INPUT COMPRESSION AND INPUT THIRD-ORDER INTERCEPT (0.1 GHz TO 6.0 GHz)

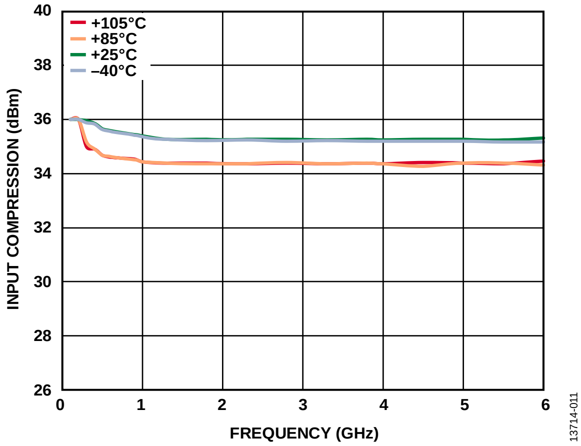


Figure 15. Input Compression 1 dB Point vs. Frequency for Various Temperatures, V_{DD} = 5 V

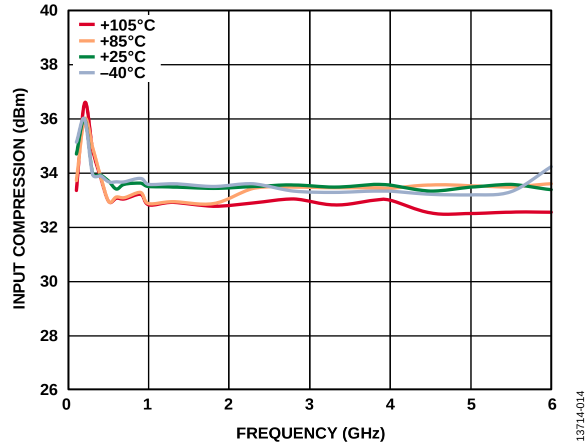


Figure 18. Input Compression 1 dB Point vs. Frequency for Various Temperatures, V_{DD} = 3.3 V

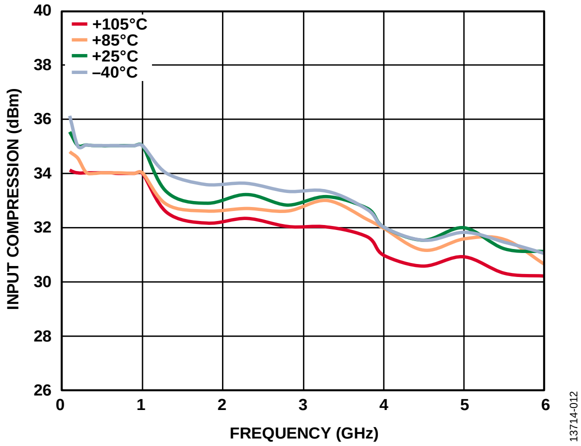


Figure 16. Input Compression 0.1 dB Point vs. Frequency for Various Temperatures, V_{DD} = 5 V

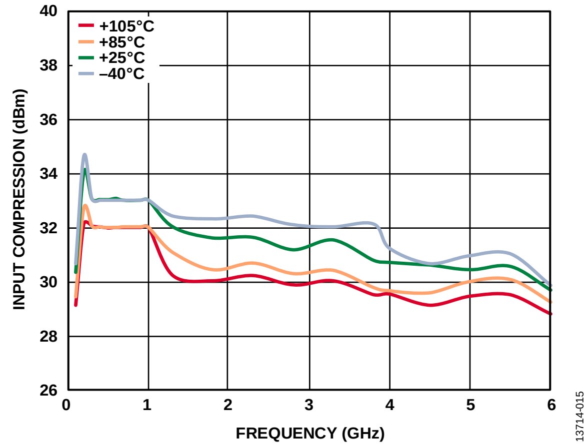


Figure 19. Input Compression 0.1 dB Point vs. Frequency for Various Temperatures, V_{DD} = 3.3 V

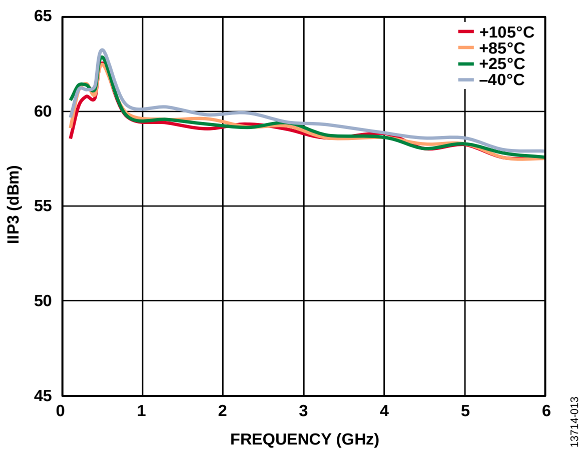


Figure 17. Input Third-Order Intercept (IIP3) Point vs. Frequency for Various Temperatures, V_{DD} = 5 V

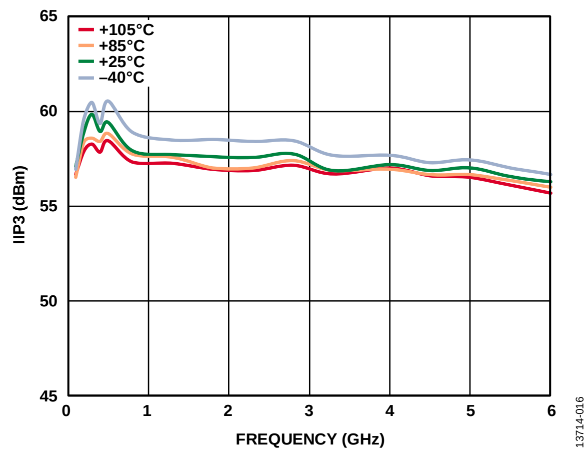


Figure 20. Input Third-Order Intercept (IIP3) Point vs. Frequency for Various Temperatures, V_{DD} = 3.3 V

INPUT COMPRESSION AND INPUT THIRD-ORDER INTERCEPT (10 kHz TO 1 GHz)

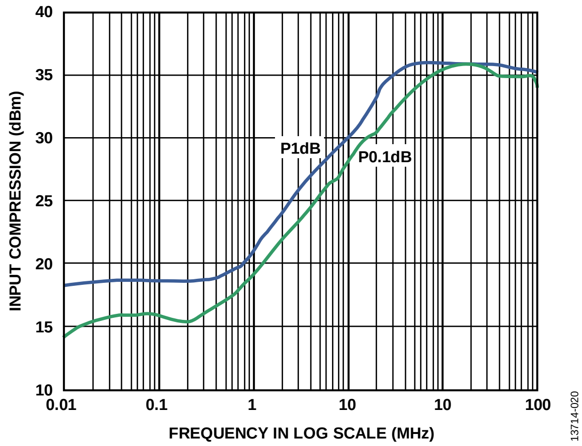


Figure 21. Input Compression (P1dB and P0.1dB Points) vs. Frequency in Log Scale, V_{DD} = 5 V at 25°C

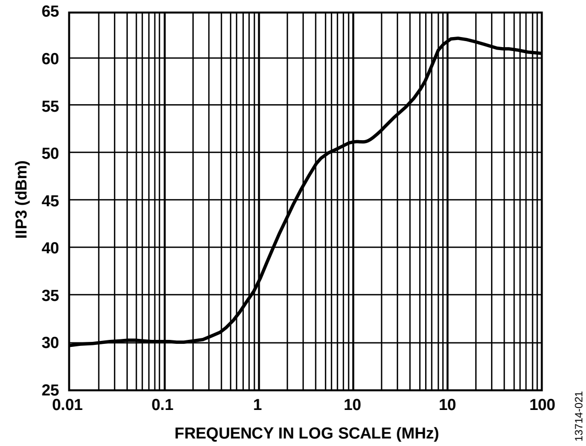


Figure 22. Input Third-Order Intercept (IIP3) vs. Frequency in Log Scale, V_{DD} = 5 V at 25°C

THEORY OF OPERATION

The HMC7992 requires a single positive supply voltage applied to the V_{DD} pin. A bypassing capacitor is recommended on the supply line to minimize RF coupling.

The HMC7992 integrates with an internal 2:4 decoder; the four RF paths are selected via the two digital control voltages applied to the A and B control inputs. A small value bypassing capacitor is recommended on these digital signal lines to improve the RF signal isolation.

The HMC7992 is internally matched to 50 Ω at the RF common port (RFC) and the RF ports (RF1, RF2, RF3, and RF4); therefore, no external matching components are required. The RF pins are dc-coupled and dc blocking capacitors are required on the RF paths. The design is bidirectional; the RF input signals can apply at the RFC port or the RF1 to RF4 ports. The inputs and outputs are interchangeable.

Depending on the logic level applied to the control input pins, A and B, one RF output port (for example, RF1) is set to on mode, by which an insertion loss path is provided from the input to the output. The other RF output ports (for example, RF2, RF3, and RF4) are then set to off mode, by which the outputs are isolated from the input. When the RF output ports (RF1, RF2, RF3, and RF4) are in isolation mode, they are internally terminated to 50 Ω, and thereby can absorb the applied RF signal.

The ideal power-up sequence is as follows:

1. Power up GND.
2. Power up V_{DD}.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. Powering the logic control inputs before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures.
4. Apply the RF input.

Table 7. Switch Mode Operation

Digital Control Inputs		Signal Mode
A	**B**	**RFC to RFx**
Low	Low	RF Port 1 is in on mode, providing a low insertion loss path from the RFC port to the RF1 port. The remaining RF ports (RF2, RF3, and RF4) are in off mode; they are isolated from the RFC port and internally terminated to a 50 Ω load.
High	Low	RF Port 2 is in on mode, providing a low insertion loss path from the RFC port to the RF2 port. The remaining RF ports (RF1, RF3, and RF4) are in off mode; they are isolated from the RFC port and internally terminated to a 50 Ω load.
Low	High	RF Port 3 is in on mode, providing a low insertion loss path from the RFC port to the RF3 port. The remaining RF ports (RF1, RF2, and RF4) are in off mode; they are isolated from the RFC port and internally terminated to a 50 Ω load.
High	High	RF Port 4 is in on mode, providing a low insertion loss path from the RFC port to the RF4 port. The remaining RF ports (RF1, RF2, and RF3) are in off mode; they are isolated from the RFC port and internally terminated to a 50 Ω load.

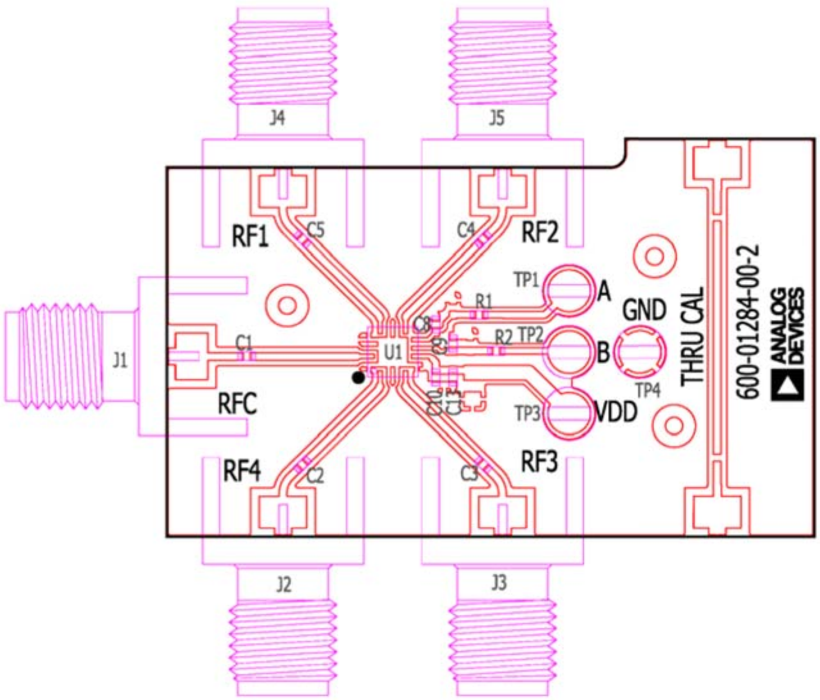
APPLICATIONS INFORMATION

Generate the evaluation PCB with proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω impedance, and the package ground leads and backside ground slug must connect directly to the ground plane, as shown in Figure 23. The evaluation board shown in Figure 23 is available from Analog Devices, Inc., upon request.

Table 8. Bill of Materials for the EV1HMC7992LP3D[1] Evaluation Board

Reference Designator	Description
J1 to J5	PCB mount SMA connectors
C1 to C5	100 pF capacitors, 0402 package
C8 to C10	100 pF capacitors, 0402 package
C13	0.1 µF capacitor, 0402 package
R1 to R2	0 Ω resistors, 0402 package
U1	HMC7992LP3DE SP4T switch
PCB[2]	600-01284-00 evaluation PCB

[1] Reference this evaluation board number when ordering the complete evaluation board.
[2] Circuit board material: Roger 4350 or Arlon 25FR.



13714-017

Figure 23. EV1HMC7992LP3D Evaluation Board

OUTLINE DIMENSIONS

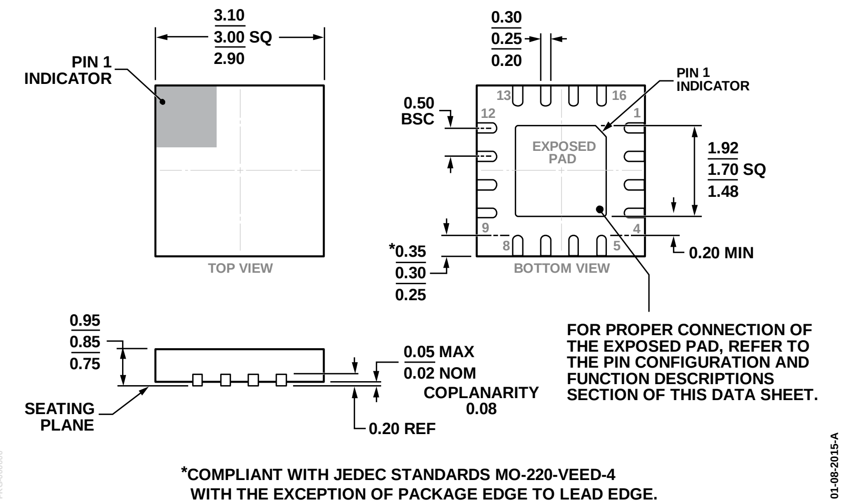


Figure 24. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.85 mm Package Height
(CP-16-38)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option	Branding[3]
HMC7992LP3DE	−40°C to +105°C	MSL3	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-38	7992 / XXXX
HMC7992LP3DETR	−40°C to +105°C	MSL3	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-38	7992 / XXXX
EV1HMC7992LP3D			Evaluation Board		

[1] The HMC7992LP3DE and HMC7992LP3DETR are RoHS Compliant Parts.
[2] See the Absolute Maximum Ratings section for MSL rating information.
[3] 4-digit lot number XXXX.

D13714-0-1/16(0)