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# HMC837\* Product Page Quick Links

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## [Evaluation Kits](#)

- HMC837LP6CE Evaluation Board

## [Documentation](#)

### **Application Notes**

- Frequency Hopping with Hittite PLLVCOs Application Note
- PLL & PLLVCO Serial Programming Interface Mode Selection Application Note
- Power-Up & Brown-Out Design Considerations for RF PLL+VCO Products Application Note
- Wideband RF PLL+VCO and Clock Generation Products FAQs

### **Data Sheet**

- HMC837 Data Sheet

### **User Guides**

- PLLs with Integrated VCO - RF Applications Product & Operating Guide

## [Reference Materials](#)

### **Quality Documentation**

- HMC Legacy PCN: LP6CE and LP6GE QFN - Alternate assembly source
- Package/Assembly Qualification Test Report: LP6, LP6C, LP6G (QTR: 2014-00368)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

## [Design Resources](#)

- HMC837 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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## FRACTIONAL-N PLL WITH INTEGRATED VCO 1025 - 1150, 2050 - 2300, 4100 - 4600 MHz

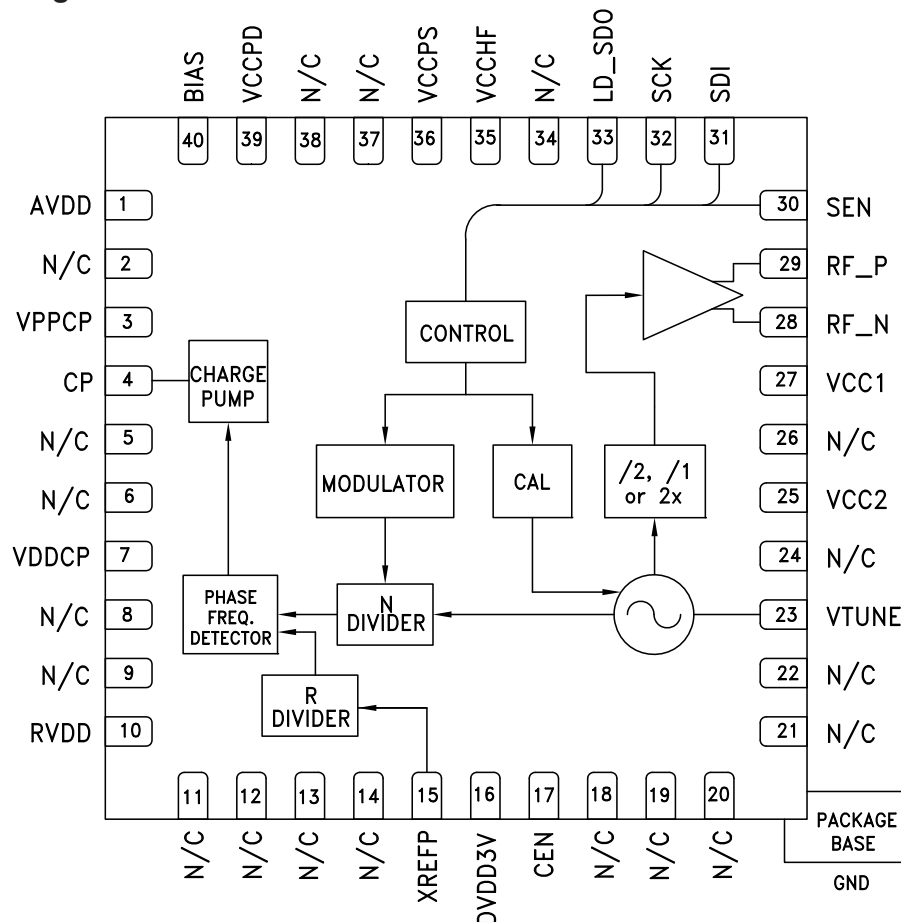
### Features

- RF Bandwidth:  
1025-1150, 2050-2300, 4100-4600 MHz
- Ultra Low Phase Noise  
-112 dBc/Hz in Band Typ.
- Figure of Merit (FOM) -230 dBc/Hz
- <180 fs RMS Jitter
- 24-bit Step Size, Resolution 3 Hz typ
- Exact Frequency Mode
- Built in Digital Self Test
- 40 Lead 6x6 mm SMT Package: 36 mm<sup>2</sup>

### Typical Applications

- Cellular/4G Infrastructure
- Repeaters and Femtocells
- Communications Test Equipment
- CATV Equipment
- Phased Array Applications
- DDS Replacement
- Very High Data Rate Radios

### Functional Diagram





## FRACTIONAL-N PLL WITH INTEGRATED VCO

### 1025 - 1150, 2050 - 2300, 4100 - 4600 MHz

### General Description

The HMC837LP6CE is a fully featured Fractional-N Phase-Locked-Loop (PLL) Frequency Synthesizer with an Integrated Voltage Controlled Oscillator (VCO). The synthesizer consists of an integrated low noise VCO with a tri-band output, an autocalibration subsystem for low voltage VCO tuning, a very low noise digital Phase Detector (PD), a precision controlled charge pump, a low noise reference path divider and a fractional divider.

The fractional synthesizer features an advanced delta-sigma modulator design that allows both ultra-fine step sizes and low spurious products. The phase detector (PD) features cycle slip prevention (CSP) technology to allow faster frequency hopping times. Ultra low in-close phase noise and low spurious also allows wider loop bandwidths for faster frequency hopping and low micro-phonics.

For theory of operation and register map refer to the “[PLLs with Integrated VCOs - RF VCOs Operating Guide](#)”. To view the Operating Guide, please visit [www.hittite.com](http://www.hittite.com) and choose HMC837LP6CE from the “Search by Part Number” pull down menu.

### Electrical Specifications

**VPPCP, VDDCP, VCC1, VCC2 = 5V; RVDD, AVDD, DVDD3V, VCCPD, VCCHF, VCCPS = 3.3V**  
**GNDCP = GNDLS = Ground Paddle = 0V, Min and Max Specified across Temp**

| Parameter                           | Condition  | Min. | Typ.            | Max.    | Units |
|-------------------------------------|--|------|-----------------|---------|-------|
| <b>RF Output Characteristics</b>    |  |      |                 |         |       |
| VCO Frequency at PLL Input          |  | 2050 |                 | 2300    | MHz   |
| RF Output Frequency at $f_{VCO}/2$  |  | 1025 |                 | 1150    | MHz   |
| RF Output Frequency at $f_{VCO}$    |  | 2050 |                 | 2300    | MHz   |
| RF Output Frequency at $2f_{VCO}$   |  | 4100 |                 | 4600    | MHz   |
| <b>Output Power</b>                 |  |      |                 |         |       |
| RF Output Power at $f_{VCO}/2$      | matched at the frequency of interest, vs temperature             | 11   | 12              | 13      | dBm   |
| RF Output Power at $f_{VCO}$        |  | 9    | 10.5            | 12      | dBm   |
| RF Output Power at $2f_{VCO}$       |  | -3   | -0.5            | 2       | dBm   |
| VCO Tuning Sensitivity              | Measured at $f_o$ , 2V   | 9.7  | 12.4            | 16.5    | MHz/V |
| VCO Supply Pushing                  | Measured at $f_o$ , 2V   |      | 1               |         | MHz/V |
| <b>Harmonics</b>                    |  |      |                 |         |       |
| RF Output $f_{out}/2$ Harmonic      | Doubler Mode   |      | -26             |         | dBc   |
| RF Output 3 $f_{out}/2$ Harmonic    | Doubler Mode   |      | -47             |         | dBc   |
| RF Output 2nd Harmonic              | $f_o/2/f_o/2f_o$   |      | -26 / -21 / -46 |         | dBc   |
| RF Output 5 $f_{out}/2$ Harmonic    | Doubler Mode   |      | -55             |         | dBc   |
| RF Output 3rd Harmonic              | $f_o/2/f_o/2f_o$   |      | -26 / -34 / -44 |         | dBc   |
| RF Output 7 $f_{out}/2$ Harmonic    | Doubler Mode   |      | -61             |         | dBc   |
| RF Output 4th Harmonic              | $f_o/2/f_o/2f_o$   |      | -25 / -52 / -61 |         | dBc   |
| <b>RF Divider Characteristics</b>   |  |      |                 |         |       |
| 19-Bit N-Divider Range (Integer)    | Max = $2^{19} - 1$   |      |                 | 524,287 |       |
| 19-Bit N-Divider Range (Fractional) | Fractional nominal divide ratio varies (-3 / +4) dynamically max |      |                 | 524,283 |       |
| <b>REF Input Characteristics</b>    |  |      |                 |         |       |
| Max Ref Input Frequency             |  |      | 50              | 200     | MHz   |
| Ref Input Range                     | AC Coupled   | 1    | 2               | 3.3     | Vp-p  |
| Ref Input Capacitance               |  |      |                 | 5       | pF    |
| 14-Bit R-Divider Range              |  | 1    |                 | 16,383  |       |


**FRACTIONAL-N PLL WITH INTEGRATED VCO**  
**1025 - 1150, 2050 - 2300, 4100 - 4600 MHz**
**Electrical Specifications (Continued)**

| Parameter   | Condition                             | Min.       | Typ. | Max.   | Units   |
|---|---------------------------------------|------------|------|--------|---------|
| <b>Phase Detector (PD)</b>  |                                       |            |      |        |         |
| PD Frequency Fractional Feedback Mode                                     | [1]                                   | 0.1        |      | 100    | MHz     |
| PD Frequency Fractional Feedforward Mode<br>(and Register 6 [17:16] = 10) |                                       | 0.1        |      | 80     | MHz     |
| PD Frequency Integer Mode   |                                       | 0.1        |      | 125    | MHz     |
| <b>Charge Pump</b>  |                                       |            |      |        |         |
| Output Current  |                                       | 0.02       |      | 2.54   | mA      |
| Charge Pump Gain Step Size  |                                       |            | 20   |        | $\mu$ A |
| PD/Charge Pump SSB Phase Noise  | 50 MHz Ref, Input Referred            |            |      |        |         |
| 1 kHz   |                                       |            | -143 |        | dBc/Hz  |
| 10 kHz  | Add 1 dB for Fractional               |            | -150 |        | dBc/Hz  |
| 100 kHz   | Add 3 dB for Fractional               |            | -153 |        | dBc/Hz  |
| <b>Logic Inputs</b>   |                                       |            |      |        |         |
| VIH Input High Voltage  |                                       | DVDD3V-0.4 |      | DVDD3V | V       |
| VIL Input Low Voltage   |                                       | 0          |      | 0.4    | V       |
| <b>Logic Outputs</b>  |                                       |            |      |        |         |
| VOH Output High Voltage   |                                       | DVDD3V-0.4 |      | DVDD3V | V       |
| VOL Output Low Voltage  |                                       | 0          |      | 0.4    | V       |
| <b>Power Supply Voltages</b>  |                                       |            |      |        |         |
| Analog 3.3V Supplies  | AVDD, VCCHF, VCCPS,<br>VCCPD, RVDD    | 3.0        | 3.3  | 3.5    | V       |
| Digital Supply  | DVDD3V                                | 3.0        | 3.3  | 3.5    | V       |
| Analog 5V Supplies  | VPPCP, VDDCP, VCC1, VCC2              | 4.8        | 5    | 5.2    | V       |
| <b>Power Supply Currents</b>  |                                       |            |      |        |         |
| +5V Analog Charge Pump  | VPPCP, VDDCP                          |            | 5.3  |        | mA      |
| +5V VCO Core and PLL Buffer   | VCC2                                  |            | 56   |        | mA      |
| +5V VCO Divider and RF Buffer   | VCC1                                  |            | 36   |        | mA      |
| +3.3V Analog  | AVDD, VCCHF, VCCPS,<br>VCCPD, RVDD    |            | 41   |        | mA      |
| +3.3V Digital   | DVDD3V                                |            | 6.5  |        | mA      |
| Power Down - Crystal Off  | Reg 01h=0,<br>Crystal Not Clocked     |            | 10   |        | $\mu$ A |
| Power Down - Crystal On, 100 MHz  | Reg 01h=0,<br>Crystal Clocked 100 MHz |            | 10   | 200    | $\mu$ A |
| <b>Power on Reset</b>   |                                       |            |      |        |         |
| Typical Reset Voltage on DVDD   |                                       |            | 700  |        | mV      |
| Min DVDD Voltage for No Reset   |                                       | 1.5        |      |        | V       |
| Power on Reset Delay  |                                       |            | 250  |        | $\mu$ s |
| <b>VCO Open Loop Phase Noise at fo/2</b>                                  |                                       |            |      |        |         |
| 10 kHz Offset   |                                       |            | -91  |        | dBc/Hz  |
| 100 kHz Offset  |                                       |            | -120 |        | dBc/Hz  |

[1] This maximum phase detector frequency can only be achieved if the minimum N value is respected. eg. In the case of fractional feedback mode, the maximum PFD rate =  $f_{vco}/20$  or 100 MHz, whichever is less.


**FRACTIONAL-N PLL WITH INTEGRATED VCO  
1025 - 1150, 2050 - 2300, 4100 - 4600 MHz**
**Electrical Specifications (Continued)**

| Parameter   | Condition             | Min. | Typ.  | Max. | Units  |
|---|-----------------------|------|-------|------|--------|
| 1 MHz Offset  |                       |      | -147  |      | dBc/Hz |
| 10 MHz Offset   |                       |      | -161  |      | dBc/Hz |
| 100 MHz Offset  |                       |      | -168  |      | dBc/Hz |
| <b>VCO Open Loop Phase Noise at fo</b>  |                       |      |       |      |        |
| 10 kHz Offset   |                       |      | -85   |      | dBc/Hz |
| 100 kHz Offset  |                       |      | -114  |      | dBc/Hz |
| 1 MHz Offset  |                       |      | -141  |      | dBc/Hz |
| 10 MHz Offset   |                       |      | -162  |      | dBc/Hz |
| 100 MHz Offset  |                       |      | -171  |      | dBc/Hz |
| <b>VCO Open Loop Phase Noise at 2fo</b>   |                       |      |       |      |        |
| 10 kHz Offset   |                       |      | -79   |      | dBc/Hz |
| 100 kHz Offset  |                       |      | -108  |      | dBc/Hz |
| 1 MHz Offset  |                       |      | -135  |      | dBc/Hz |
| 10 MHz Offset   |                       |      | -153  |      | dBc/Hz |
| 100 MHz Offset  |                       |      | -166  |      | dBc/Hz |
| <b>Closed Loop Phase Noise PLL + VCO at f<sub>vco</sub> with 93 KHz BW Loop Filter Design<sup>[3]</sup></b> |                       |      |       |      |        |
| Integer, 100 MHz PD   | 1 kHz Offset          |      | -113  |      | dBc/Hz |
| Integer, 100 MHz PD   | 10 kHz Offset         |      | -111  |      | dBc/Hz |
| Integer, 100 MHz PD   | 100 kHz Offset        |      | -112  |      | dBc/Hz |
| Integer, 100 MHz PD   | 1 MHz Offset          |      | -141  |      | dBc/Hz |
| Integer, 100 MHz PD   | 10 MHz Offset         |      | -162  |      | dBc/Hz |
| Integer, 100 MHz PD   | 100 MHz Offset        |      | -171  |      | dBc/Hz |
| Integrated Phase Noise  | from 10 KHz to 100MHz |      | -58.1 |      | dBc    |
| RMS Jitter  |                       |      | 132.5 |      | fsec   |
| Fractional, 100 MHz PD  | 1 kHz Offset          |      | -112  |      | dBc/Hz |
| Fractional, 100 MHz PD  | 10 kHz Offset         |      | -111  |      | dBc/Hz |
| Fractional, 100 MHz PD  | 100 kHz Offset        |      | -112  |      | dBc/Hz |
| Fractional, 100 MHz PD  | 1 MHz Offset          |      | -141  |      | dBc/Hz |
| Fractional, 100 MHz PD  | 10 MHz Offset         |      | -162  |      | dBc/Hz |
| Fractional, 100 MHz PD  | 100 MHz Offset        |      | -171  |      | dBc/Hz |
| Integrated Phase Noise  | from 10 KHz to 100MHz |      | -58.4 |      | dBc    |
| RMS Jitter  |                       |      | 128.5 |      | fsec   |
| <b>Closed Loop Phase Noise PLL + VCO at f<sub>vco</sub> with 176K Hz Loop Filter Design<sup>[4]</sup></b>   |                       |      |       |      |        |
| Integer, 100 MHz PD   | 1 kHz Offset          |      | -115  |      | dBc/Hz |
| Integer, 100 MHz PD   | 10 kHz Offset         |      | -118  |      | dBc/Hz |
| Integer, 100 MHz PD   | 100 kHz Offset        |      | -114  |      | dBc/Hz |
| Integer, 100 MHz PD   | 1 MHz Offset          |      | -141  |      | dBc/Hz |
| Integer, 100 MHz PD   | 10 MHz Offset         |      | -162  |      | dBc/Hz |
| Integer, 100 MHz PD   | 100 MHz Offset        |      | -171  |      | dBc/Hz |
| Integrated Phase Noise  | from 10 KHz to 100MHz |      | -62   |      | dBc    |
| RMS Jitter  |                       |      | 87.5  |      | fsec   |
| Fractional, 100 MHz PD  | 1 kHz Offset          |      | -113  |      | dBc/Hz |


**FRACTIONAL-N PLL WITH INTEGRATED VCO  
1025 - 1150, 2050 - 2300, 4100 - 4600 MHz**
**Electrical Specifications (Continued)**

| Parameter   | Condition             | Min. | Typ.  | Max. | Units  |
|---|-----------------------|------|-------|------|--------|
| Fractional, 100 MHz PD  | 10 kHz Offset         |      | -117  |      | dBc/Hz |
| Fractional, 100 MHz PD  | 100 kHz Offset        |      | -114  |      | dBc/Hz |
| Fractional, 100 MHz PD  | 1 MHz Offset          |      | -139  |      | dBc/Hz |
| Fractional, 100 MHz PD  | 10 MHz Offset         |      | -161  |      | dBc/Hz |
| Fractional, 100 MHz PD  | 100 MHz Offset        |      | -171  |      | dBc/Hz |
| Integrated Phase Noise  | from 10 KHz to 100MHz |      | -61.2 |      | dBc    |
| RMS Jitter  |                       |      | 92.5  |      | fsec   |
| <b>Closed Loop Phase Noise PLL + VCO at f<sub>vco</sub> with 78 KHz BW Loop Filter Design<sup>[5]</sup></b> |                       |      |       |      |        |
| Integer, 50 MHz PD  | 1 kHz Offset          |      | -112  |      | dBc/Hz |
| Integer, 50 MHz PD  | 10 kHz Offset         |      | -108  |      | dBc/Hz |
| Integer, 50 MHz PD  | 100 kHz Offset        |      | -111  |      | dBc/Hz |
| Integer, 50 MHz PD  | 1 MHz Offset          |      | -141  |      | dBc/Hz |
| Integer, 50 MHz PD  | 10 MHz Offset         |      | -163  |      | dBc/Hz |
| Integer, 50 MHz PD  | 100 MHz Offset        |      | -171  |      | dBc/Hz |
| Integrated Phase Noise  | from 10 KHz to 100MHz |      | -55.6 |      | dBc    |
| RMS Jitter  |                       |      | 177   |      | fsec   |
| Fractional, 50 MHz PD   | 1 kHz Offset          |      | -110  |      | dBc/Hz |
| Fractional, 50 MHz PD   | 10 kHz Offset         |      | -108  |      | dBc/Hz |
| Fractional, 50 MHz PD   | 100 kHz Offset        |      | -110  |      | dBc/Hz |
| Fractional, 50 MHz PD   | 1 MHz Offset          |      | -141  |      | dBc/Hz |
| Fractional, 50 MHz PD   | 10 MHz Offset         |      | -163  |      | dBc/Hz |
| Fractional, 50 MHz PD   | 100 MHz Offset        |      | -171  |      | dBc/Hz |
| Integrated Phase Noise  | from 10 KHz to 100MHz |      | -55.8 |      | dBc    |
| RMS Jitter  |                       |      | 171   |      | fsec   |
| <b>Closed Loop Phase Noise PLL + VCO at f<sub>vco</sub> with 142 KHz Loop Filter Design<sup>[6]</sup></b>   |                       |      |       |      |        |
| Integer, 50 MHz PD  | 1 kHz Offset          |      | -114  |      | dBc/Hz |
| Integer, 50 MHz PD  | 10 kHz Offset         |      | -112  |      | dBc/Hz |
| Integer, 50 MHz PD  | 100 kHz Offset        |      | -114  |      | dBc/Hz |
| Integer, 50 MHz PD  | 1 MHz Offset          |      | -141  |      | dBc/Hz |
| Integer, 50 MHz PD  | 10 MHz Offset         |      | -162  |      | dBc/Hz |
| Integer, 50 MHz PD  | 100 MHz Offset        |      | -171  |      | dBc/Hz |
| Integrated Phase Noise  | from 10 KHz to 100MHz |      | -60   |      | dBc    |
| RMS Jitter  |                       |      | 106.8 |      | fsec   |
| Fractional, 50 MHz PD   | 1 kHz Offset          |      | -111  |      | dBc/Hz |
| Fractional, 50 MHz PD   | 10 kHz Offset         |      | -112  |      | dBc/Hz |
| Fractional, 50 MHz PD   | 100 kHz Offset        |      | -113  |      | dBc/Hz |
| Fractional, 50 MHz PD   | 1 MHz Offset          |      | -135  |      | dBc/Hz |
| Fractional, 50 MHz PD   | 10 MHz Offset         |      | -154  |      | dBc/Hz |
| Fractional, 50 MHz PD   | 100 MHz Offset        |      | -171  |      | dBc/Hz |
| Integrated Phase Noise  | from 10 KHz to 100MHz |      | -59.4 |      | dBc    |
| RMS Jitter  |                       |      | 114   |      | fsec   |
| <b>Figure of Merit</b>  | Normalized 1 Hz       |      |       |      |        |
| Floor Integer Mode  |                       |      | -230  |      | dBc/Hz |





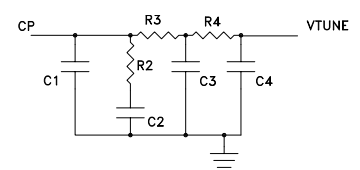
**FRACTIONAL-N PLL WITH INTEGRATED VCO**  
**1025 - 1150, 2050 - 2300, 4100 - 4600 MHz**

**Electrical Specifications (Continued)**

| Parameter             | Condition | Min. | Typ. | Max. | Units  |
|-----------------------|-----------|------|------|------|--------|
| Floor Fractional Mode |           |      | -227 |      | dBc/Hz |
| Flicker (Both Modes)  |           |      | -268 |      | dBc/Hz |

[2] The Close Loop Phase Noise PLL+VCO at  $f_{vco}/2$  can be calculated by subtracting 6dB. The Close Loop Phase Noise PLL+VCO at  $2f_{vco}$  can be calculated by adding 6dB.

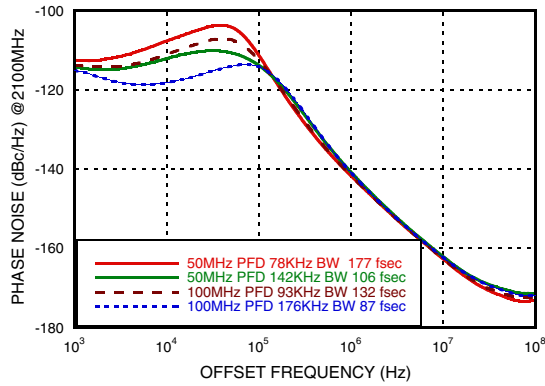
**Loop Filter Configuration Table**

| Loop Filter Configuration | C1 (pF) | C2 (nF) | C3 (pF) | C4 (pF) | R2 (kΩ) | R3 (kΩ) | R4 (kΩ) | Loop Filter Design   |
|---------------------------|---------|---------|---------|---------|---------|---------|---------|--|
| [3]                       | 820     | 15      | 130     | 130     | 0.39    | 1       | 1       |  |
| [4]                       | 120     | 5.1     | 82      | 82      | 0.75    | 1       | 1       |  |
| [5]                       | 270     | 10      | 150     | 150     | 0.68    | 2       | 2       |  |
| [6]                       | 120     | 5.6     | 68      | 68      | 1.2     | 1       | 1       |  |

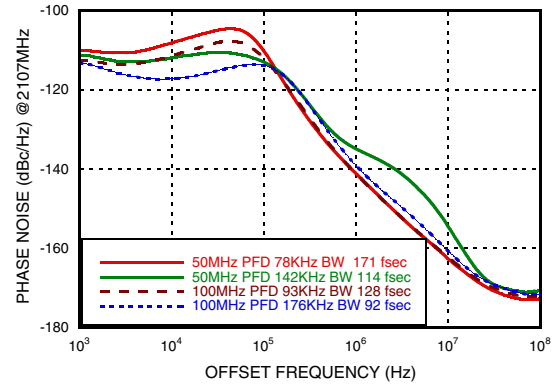


## FRACTIONAL-N PLL WITH INTEGRATED VCO 1025 - 1150, 2050 - 2300, 4100 - 4600 MHz

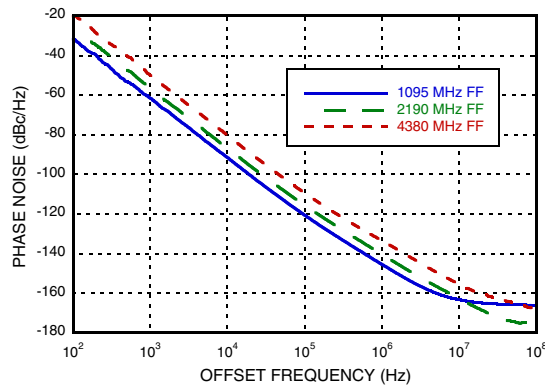
**Closed Loop Integer Phase Noise**



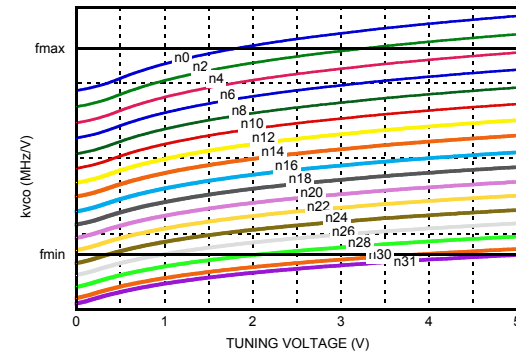
**Typical Closed Loop Fractional Phase Noise [1]**



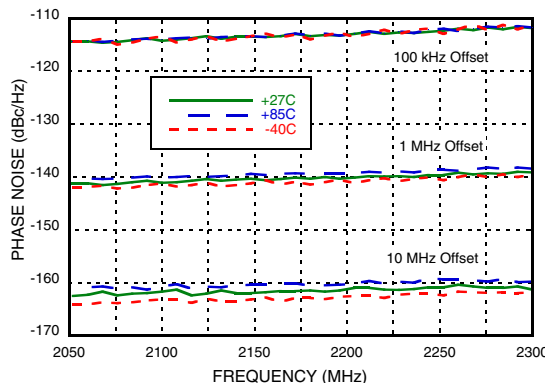
**Free Running Phase Noise**



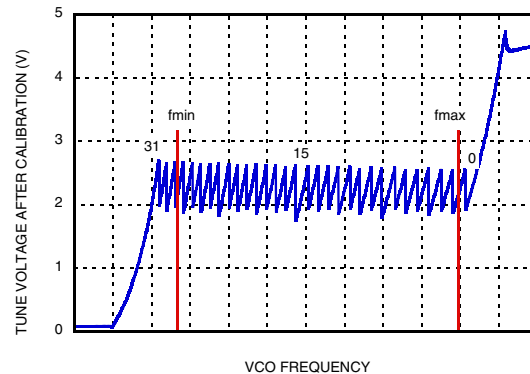
**Typical Tuning Curves vs. Switch Position**



**Free Running VCO Phase Noise Over Temperature**



**Typical VCO Tuning Voltage After Calibration**

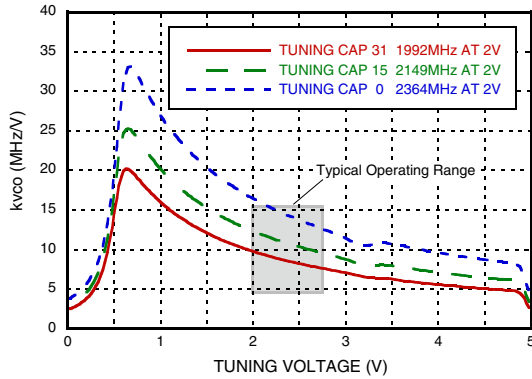


[1] RMS Jitter data are measured from 10KHz to 100MHz bandwidth.

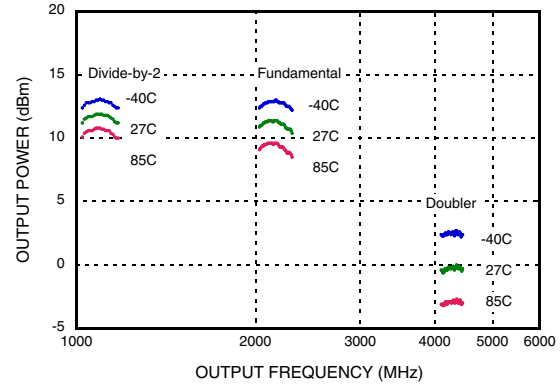


## FRACTIONAL-N PLL WITH INTEGRATED VCO 1025 - 1150, 2050 - 2300, 4100 - 4600 MHz

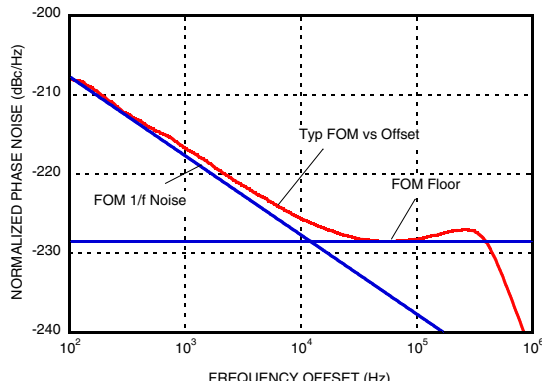
**Typical VCO Sensitivity vs. Cap @  
Fo Voltage**



**Typical Output Power - Narrow Band  
Match**



**Figure of Merit**




**FRACTIONAL-N PLL WITH INTEGRATED VCO**  
**1025 - 1150, 2050 - 2300, 4100 - 4600 MHz**
**Pin Descriptions**

| Pin Number  | Function            | Description  |
|---|---------------------|--|
| 1   | AVDD                | DC Power Supply for analog circuitry.  |
| 2, 5, 6, 8, 9,<br>11 - 14, 18 - 22, 24,<br>26, 34, 37, 38 | N/C                 | The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.   |
| 3   | VPPCP               | Power Supply for charge pump analog section  |
| 4   | CP                  | Charge Pump Output   |
| 7   | VDDCP               | Power Supply for the charge pump digital section   |
| 10  | RVDD                | Reference Supply   |
| 15  | XREFP               | Reference Oscillator Input   |
| 16  | DVDD3V              | DC Power Supply for Digital (CMOS) Circuitry   |
| 17  | CEN                 | Chip Enable. Connect to logic high for normal operation.   |
| 23  | VTUNE               | VCO Varactor. Tuning Port Input.   |
| 25  | VCC2                | VCO Analog Supply 2  |
| 27  | VCC1                | VCO Analog Supply 1  |
| 28  | RF_N <sup>[1]</sup> | RF Positive Output   |
| 29  | RF_P <sup>[1]</sup> | RF Negative Output   |
| 30  | SEN                 | PLL Serial Port Enable (CMOS) Logic Input  |
| 31  | SDI                 | PLL Serial Port Data (CMOS) Logic Input  |
| 32  | SCK                 | PLL Serial Port Clock (CMOS) Logic Input   |
| 33  | LD_SDO              | Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO)  |
| 35  | VCCHF               | DC Power Supply for Analog Circuitry   |
| 36  | VCCPS               | DC Power Supply for Analog Prescaler   |
| 39  | VCCPD               | DC Power Supply for Phase Detector   |
| 40  | BIAS                | External bypass decoupling for precision bias circuits.<br>Note: 1.920V $\pm$ 20mV reference voltage (BIAS) is generated internally and cannot drive an external load. Must be measured with 10G $\Omega$ meter such as Agilent 34410A, normal 10M $\Omega$ DVM will read erroneously. |

[1] For doubler mode of operation, pin 28 (RF\_N) and pin 29 (RF\_P) outputs must be shorted together.



## FRACTIONAL-N PLL WITH INTEGRATED VCO

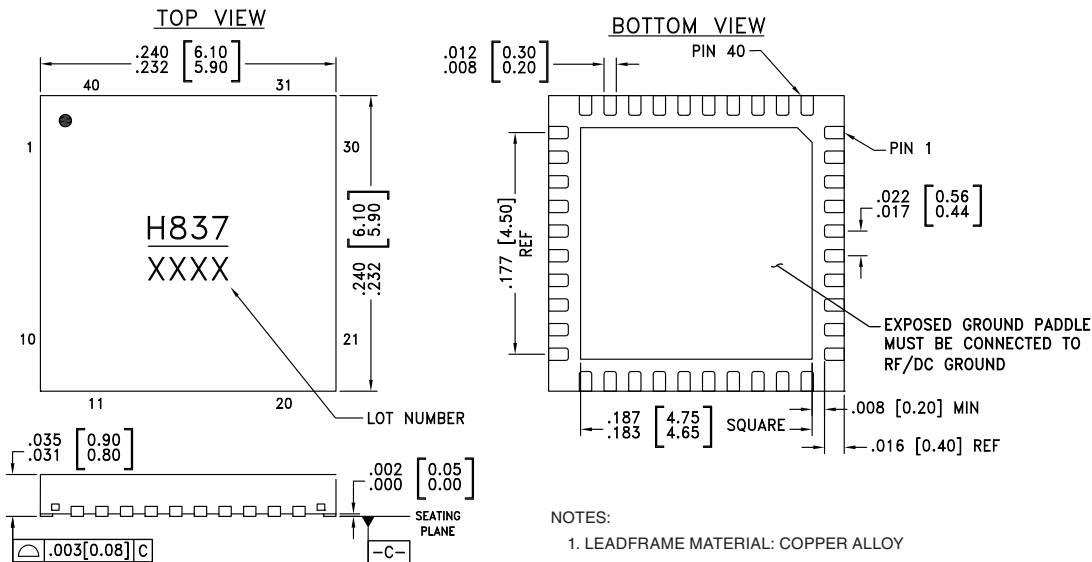
### 1025 - 1150, 2050 - 2300, 4100 - 4600 MHz

### Absolute Maximum Ratings

|  |                |
|--|----------------|
| AVDD, RVDD, DVDD3V, VCCPD, VCCHF, VCCPS                              | -0.3V to +3.6V |
| VPPCP, VDDCP, VCC1   | -0.3V to +5.8V |
| VCC2   | -0.3V to +5.5V |
| Operating Temperature  | -40°C to +85°C |
| Storage Temperature  | -65°C to 125°C |
| Maximum Junction Temperature   | 125 °C         |
| Thermal Resistance (R <sub>TH</sub> )<br>(junction to ground paddle) | 20 °C/W        |
| Reflow Soldering   |                |
| Peak Temperature   | 260°C          |
| Time at Peak Temperature   | 40 sec         |
| ESD Sensitivity (HBM)  | Class 1B       |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Outline Drawing



#### NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

### Package Information

| Part Number | Package Body Material                              | Lead Finish   | MSL Rating | Package Marking <sup>[1]</sup> |
|-------------|--|---------------|------------|--------------------------------|
| HMC837LP6CE | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1       | H837<br>XXXX                   |

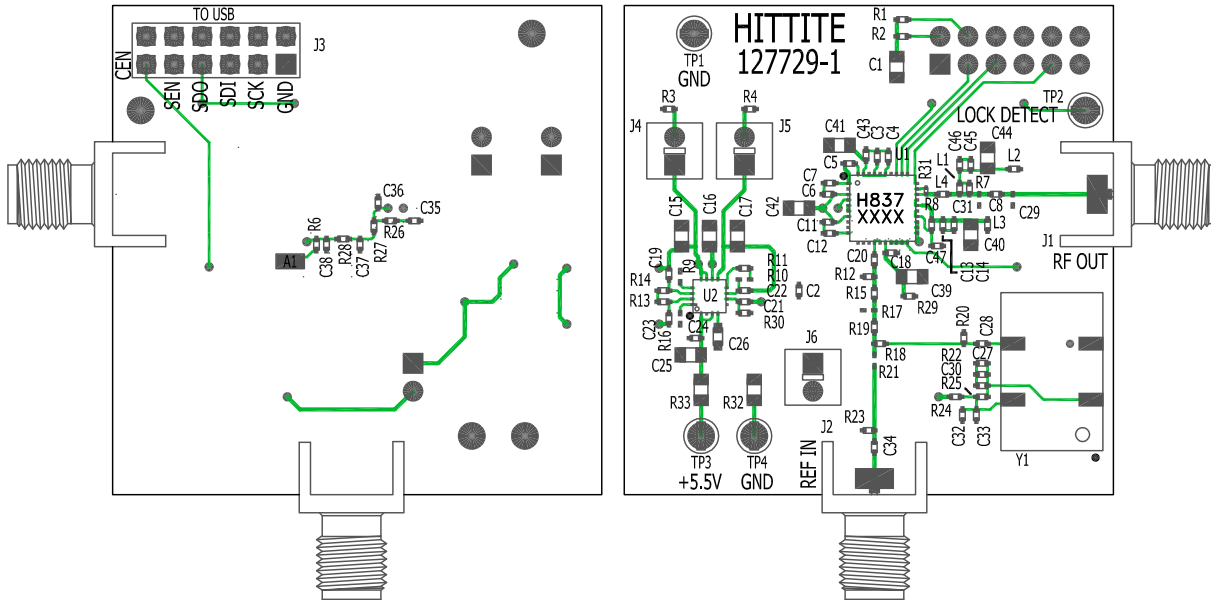
[1] 4-Digit lot number XXXX

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:  
 20 Alpha Road, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373  
 Order On-line at [www.hittite.com](http://www.hittite.com)



## FRACTIONAL-N PLL WITH INTEGRATED VCO 1025 - 1150, 2050 - 2300, 4100 - 4600 MHz

### Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

### Evaluation PCB Schematic

To view this [Evaluation PCB Schematic](#) please visit [www.hittite.com](http://www.hittite.com) and choose HMC837LP6CE from the "Search by Part Number" pull down menu to view the product splash page.

### Evaluation Order Information

| Item                | Contents  | Part Number        |
|---------------------|---|--------------------|
| Evaluation PCB Only | HMC837LP6CE $F_0/2$ & $F_0$ Evaluation PCB  | EVAL01-HMC837LP6CE |
|                     | HMC837LP6CE $2xF_0$ Evaluation PCB  | EVAL02-HMC837LP6CE |
| Evaluation Kit      | HMC837LP6CE $F_0/2$ & $F_0$ Evaluation PCB<br>USB Interface Board<br>6' USB A Male to USB B Female Cable<br>CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software) | 131995-HMC837LP6CE |
|                     | HMC837LP6CE $2xF_0$ Evaluation PCB<br>USB Interface Board<br>6' USB A Male to USB B Female Cable<br>CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)         | 131997-HMC837LP6CE |



**FRACTIONAL-N PLL WITH INTEGRATED VCO**  
**1025 - 1150, 2050 - 2300, 4100 - 4600 MHz**

**Notes:**