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FAIRCHILD SEMICONDUCTOR®

April 2007

74VHC374
Octal D-Type Flip-Flop with 3-STATE Outputs

Features

- High Speed: t_{PD} = 5.4ns (typ) at V_{CC} = 5V
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power down protection is provided on all inputs
- Low power dissipation: I_{CC} = 4μA (Max) @ T_A = 25°C
- Pin and function compatible with 74HC374

General Description

The VHC374 is an advanced high speed CMOS octal flip-flop with 3-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type flip-flop is controlled by a clock input (CP) and an output enable input ($\overline{OE}$). When the $\overline{OE}$ input is HIGH, the eight outputs are in a HIGH impedance state.

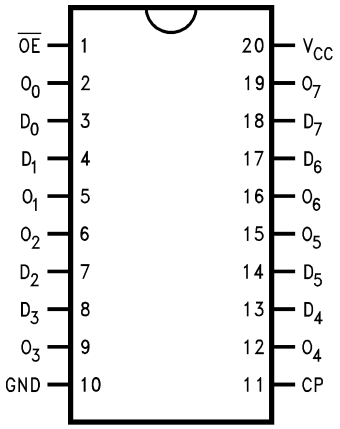
An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Ordering Information

Order Number	Package Number	Package Description
74VHC374M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC374MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter “X” to the ordering number. Pb-Free package per JEDEC J-STD-020B.

Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O_0–O_7	3-STATE Outputs

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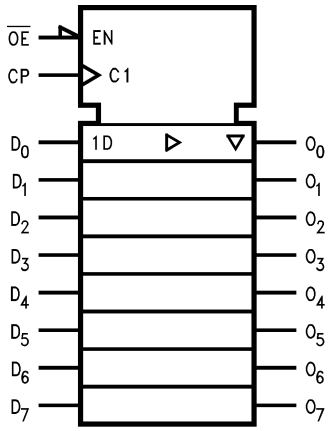
Logic Symbol

IEEE/IEC



Functional Description

The VHC374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⎍	L	H
L	⎍	L	L
X	X	H	Z

H = HIGH Voltage Level

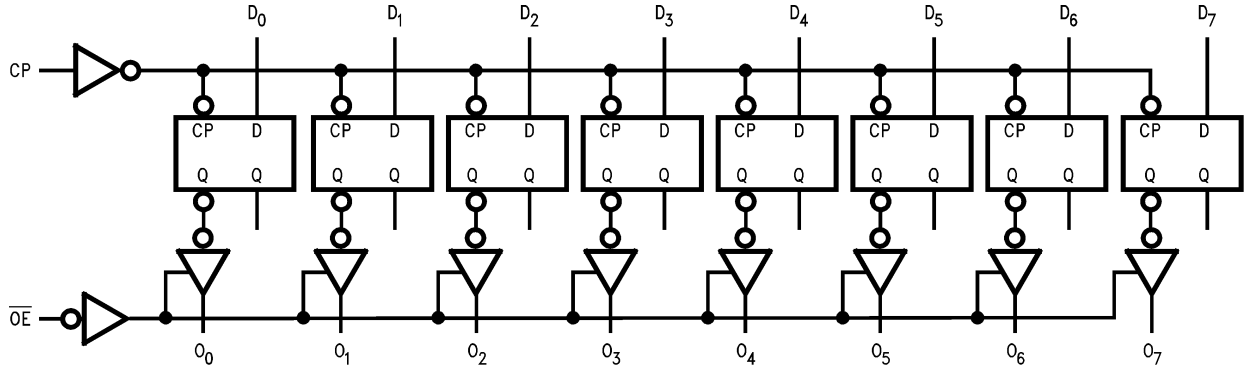
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

⎍ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_{IN}	DC Input Voltage	–0.5V to +7.0V
V_{OUT}	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_{IK}	Input Diode Current	–20mA
I_{OK}	Output Diode Current	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC}/GND Current	±75mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_{OPR}	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time,	
	V_{CC} = 3.3V ± 0.3V	0ns/V ~ 100ns/V
	V_{CC} = 5.0V ± 0.5V	0ns/V ~ 20ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C Min.	T_A = 25°C Typ.	T_A = 25°C Max.	T_A = –40°C to +85°C Min.	T_A = –40°C to +85°C Max.	Units
V_{IH}	HIGH Level Input Voltage	2.0			1.50			1.50		V
		3.0–5.5			0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V
		3.0–5.5					0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = –50\mu A$	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		$I_{OH} = –4mA$	2.58			2.48		
		4.5		$I_{OH} = –8mA$	3.94			3.80		
V_{OL}	LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu A$		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		$I_{OL} = 4mA$			0.36		0.44	
		4.5		$I_{OL} = 8mA$			0.36		0.44	
I_{OZ}	3-STATE Output Off-State Current	5.5	$V_{IN} = V_{IH}$ or V_{IL}; $V_{OUT} = V_{CC}$ or GND				±0.25		±2.5	μA
I_{IN}	Input Leakage Current	0–5.5	V_{IN} = 5.5V or GND				±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND				4.0		40.0	μA

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C Typ.	T_A = 25°C Limits	Units
V_{OLP}(2)	Quiet Output Maximum Dynamic V_{OL}	5.0	C_L = 50pF	0.6	0.9	V
V_{OLV}(2)	Quiet Output Minimum Dynamic V_{OL}	5.0	C_L = 50pF	–0.6	–0.9	V
V_{IHD}(2)	Minimum HIGH Level Dynamic Input Voltage	5.0	C_L = 50pF		3.5	V
V_{ILD}(2)	Maximum LOW Level Dynamic Input Voltage	5.0	C_L = 50pF		1.5	V

Note:

2. Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C			T_A = –40°C to +85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay Time (CP to O_n)	3.3 ± 0.3		C_L = 15pF		8.1	12.7	1.0	15.0	ns
				C_L = 50pF		10.6	16.2	1.0	18.5	
		5.0 ± 0.5		C_L = 15pF		5.4	8.1	1.0	9.5	ns
				C_L = 50pF		6.9	10.1	1.0	11.5	
t_{PZL}, t_{PZH}	3-STATE Output Enable Time	3.3 ± 0.3	R_L = 1kΩ	C_L = 15pF		7.1	11.0	1.0	13.0	ns
				C_L = 50pF		9.6	14.5	1.0	16.5	
		5.0 ± 0.5		C_L = 15pF		5.1	7.6	1.0	9.0	ns
				C_L = 50pF		6.6	9.6	1.0	11.0	
t_{PLZ}, t_{PHZ}	3-STATE Output Disable Time	3.3 ± 0.3	R_L = 1kΩ	C_L = 50pF		10.2	14.0	1.0	16.0	ns
		5.0 ± 0.5		C_L = 50pF		6.1	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	3.3 ± 0.3	(3)	C_L = 50pF			1.5		1.5	ns
		5.0 ± 0.5		C_L = 50pF			1.0		1.0	
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3		C_L = 15pF	80	130		70		MHz
				C_L = 50pF	55	85		50		
		5.0 ± 0.5		C_L = 15pF	130	185		110		
				C_L = 50pF	85	120		75		
C_{IN}	Input Capacitance		V_{CC} = Open			4	10		10	pF
C_{OUT}	Output Capacitance		V_{CC} = 5.0V			6				pF
C_{PD}	Power Dissipation Capacitance		(4)			32				pF

Notes:

3. Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL\ min}|$
4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per F/F). The total C_{PD} when n pcs. of the Octal D Flip-Flop operates can be calculated by the equation: C_{PD} (total) = 20 + 12n.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = –40°C to +85°C		Units
			Min.	Typ.	Max.	Min.	Max.	
$t_W(H)$, $t_W(L)$	Minimum Pulse Width (CP)	3.3 ± 0.3	5.0			5.5		ns
		5.0 ± 0.5	5.0			5.0		
t_S	Minimum Set-Up Time	3.3 ± 0.3	4.5			4.5		ns
		5.0 ± 0.5	3.0			3.0		
t_H	Minimum Hold Time	3.3 ± 0.3	2.0			2.0		ns
		5.0 ± 0.5	2.0			2.0		

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

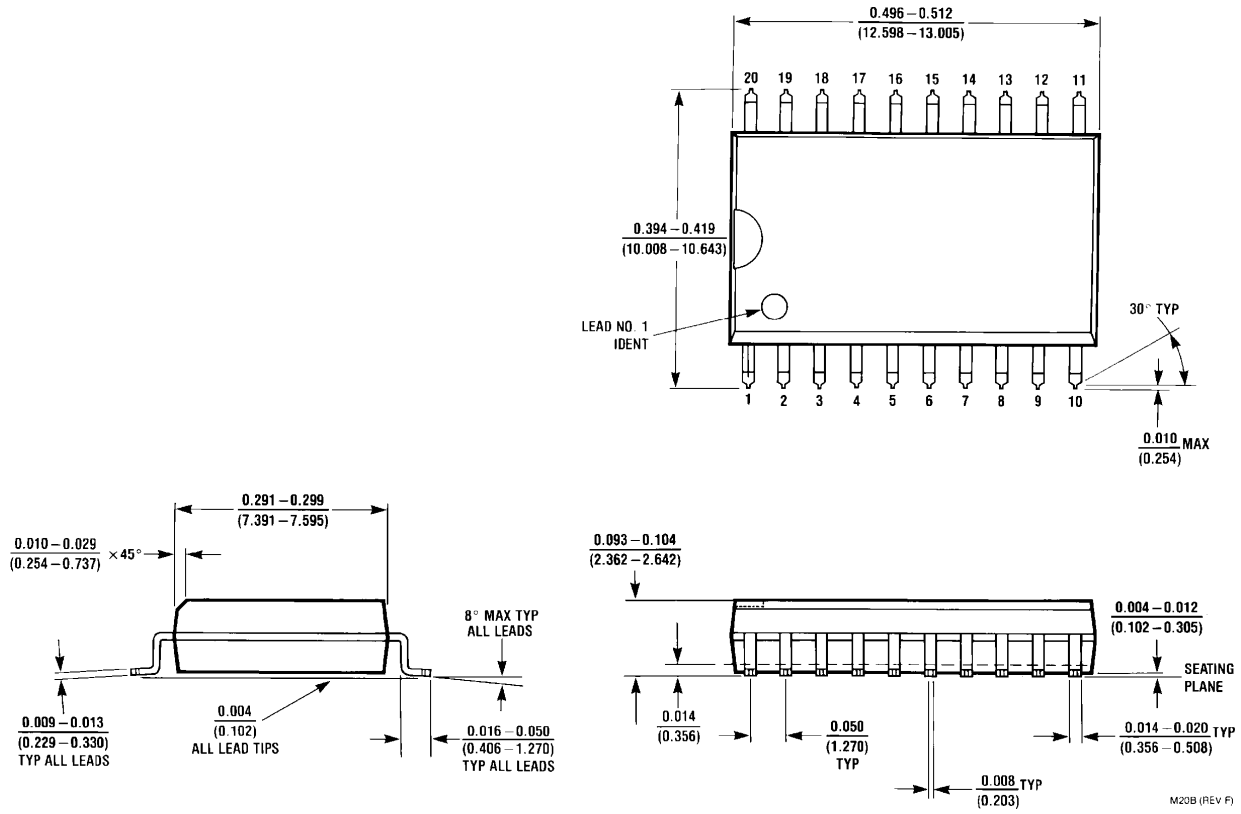


Figure 2. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

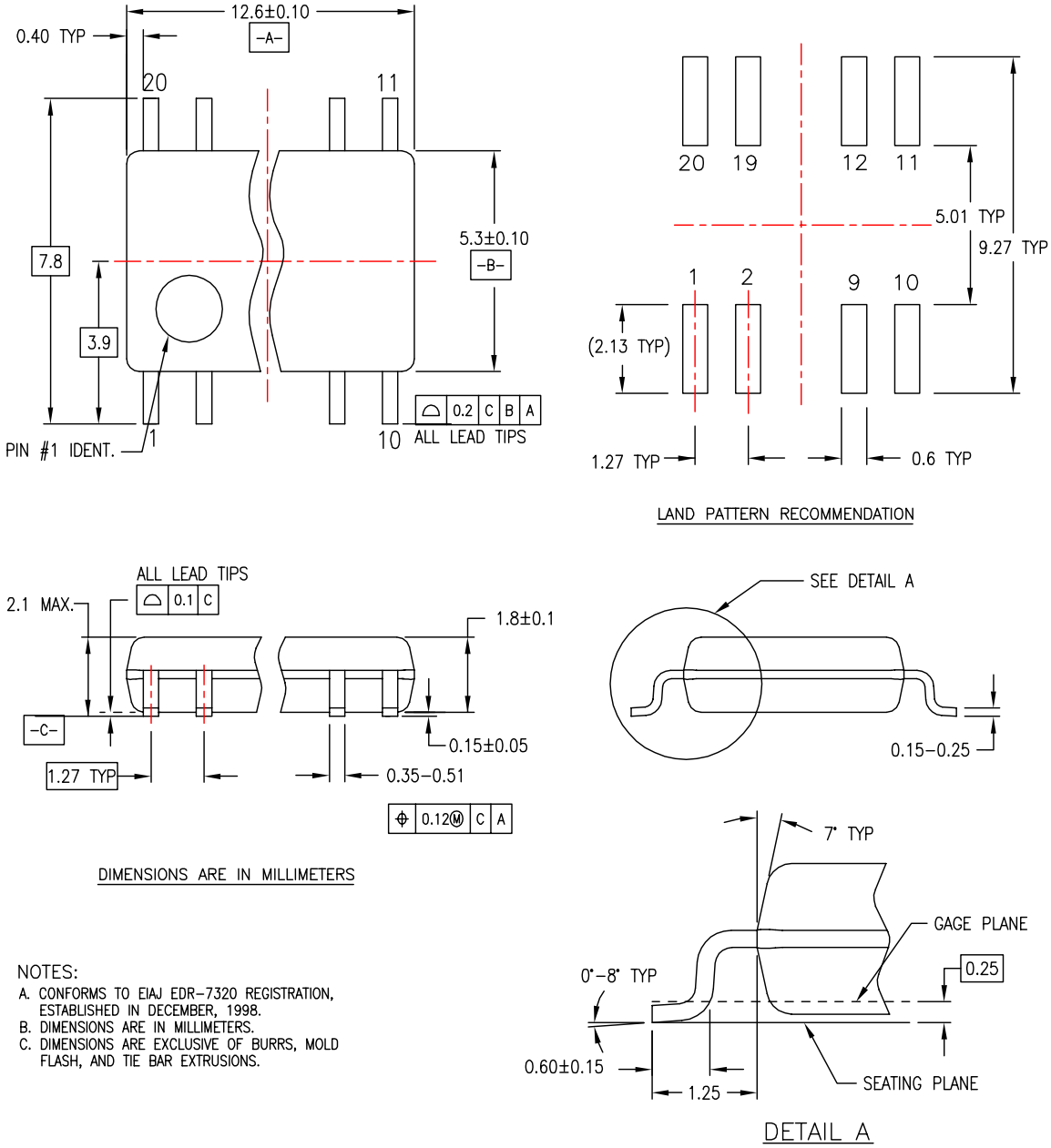


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Figure 3. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

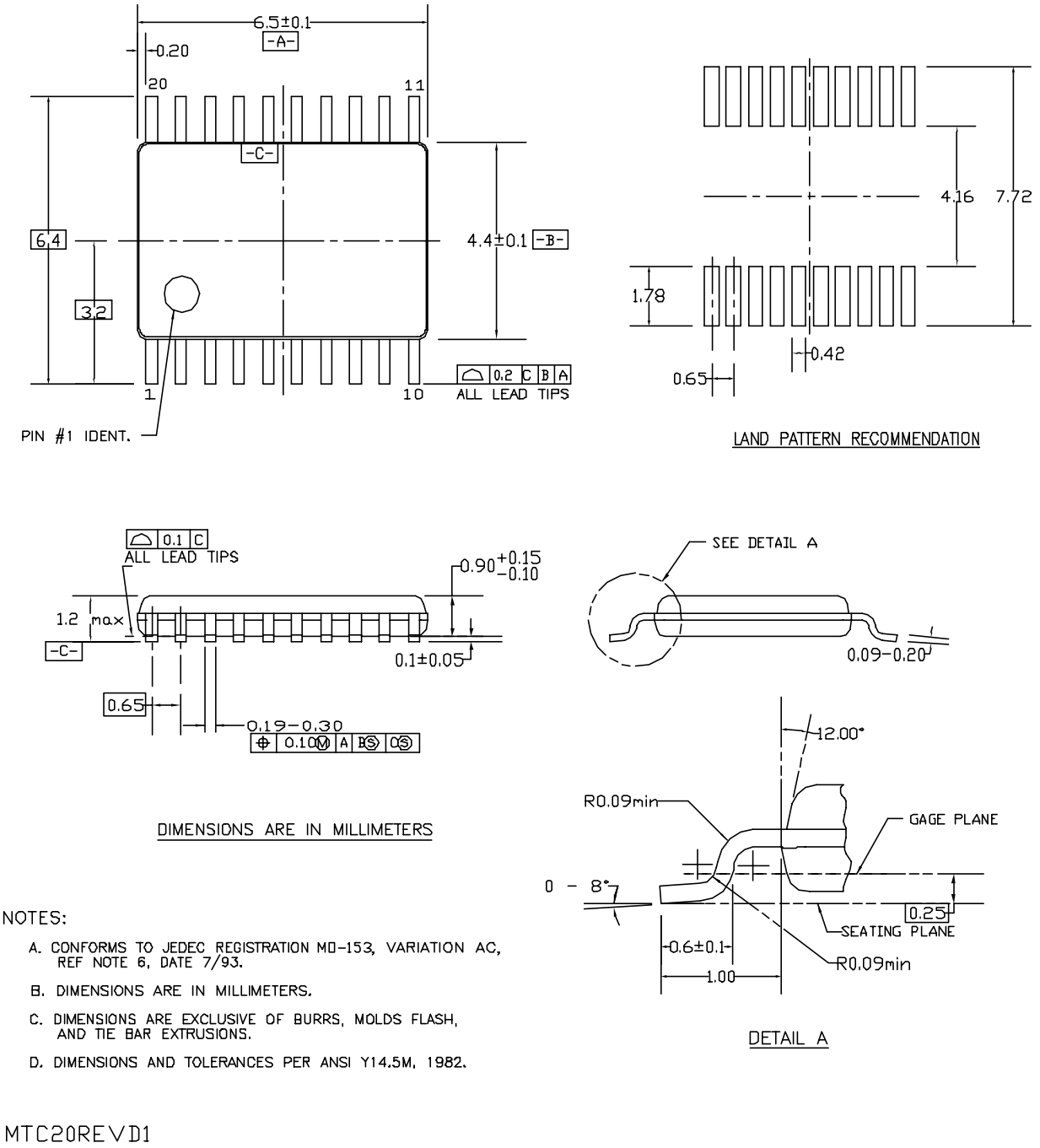

Figure 4. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

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