

### FEATURES

Fault and overvoltage protection up to  $\pm 40$  V

Signal paths open circuit with power off

Signal path resistance of  $R_{ON}$  with power on

44 V supply maximum ratings

Low on resistance: 62  $\Omega$  typical

$\pm 1$  nA maximum path current leakage @ +25°C

Low  $R_{ON}$  match (5  $\Omega$  maximum)

Low power dissipation 0.8  $\mu$ W typical

Latch-up proof construction

### APPLICATIONS

ATE equipment

Sensitive measurement equipment

Hot insertion rack systems

### GENERAL DESCRIPTION

The ADG467 is an octal channel protector. The channel protector is placed in series with the signal path. The channel protector protects sensitive components from voltage transience in the signal path regardless if the power supplies are present or not. For this reason, the channel protectors are ideal for use in applications where correct power sequencing cannot always be guaranteed (for example, hot insertion rack systems) to protect analog inputs. This is described further, and some example circuits are given in the Applications Information section.

Each channel protector has an independent operation and consists of an N-channel MOSFET, a P-channel MOSFET, and an N-channel MOSFET, connected in series. The channel protector behaves just like a series resistor during normal operation, that is,  $(V_{SS} + 1.5 \text{ V}) < V_{IN} < (V_{DD} - 1.5 \text{ V})$ . When a channel's analog input exceeds the power supplies (including  $V_{DD}$  and  $V_{SS} = 0 \text{ V}$ ), one of the MOSFETs switches off, clamping the output to either  $V_{SS} + 1.5 \text{ V}$  or  $V_{DD} - 1.5 \text{ V}$ . Circuitry and signal source protection is provided in the event of an overvoltage or power loss. The channel protectors can withstand overvoltage inputs from  $-40 \text{ V}$  to  $+40 \text{ V}$ . See the Circuit Information section.

The ADG467 can operate off both bipolar and unipolar supplies. The channels are normally on when power is

### FUNCTIONAL BLOCK DIAGRAM

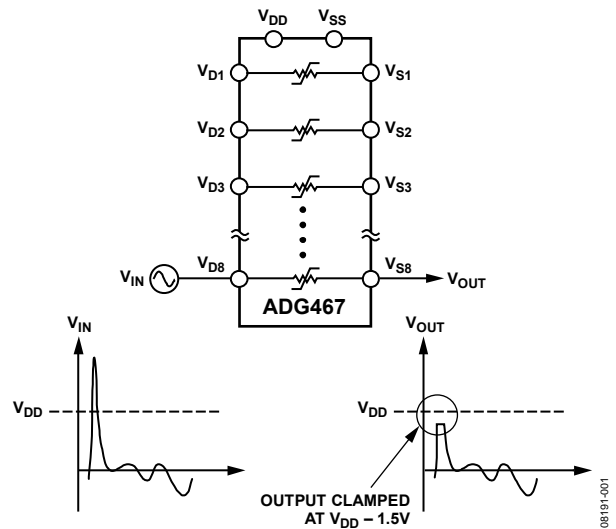


Figure 1.

connected and open circuit when power is disconnected. With power supplies of  $\pm 15 \text{ V}$ , the on resistance of the ADG467 is 62  $\Omega$  typical with a leakage current of  $\pm 1 \text{ nA}$  maximum. When power is disconnected, the input leakage current is approximately  $\pm 0.5 \text{ nA}$  typical.

The ADG467 is available in an 18-lead SOIC package and a 20-lead SSOP package.

### PRODUCT HIGHLIGHTS

1. Fault Protection.  
The ADG467 can withstand continuous voltage inputs from  $-40 \text{ V}$  to  $+40 \text{ V}$ . When a fault occurs due to the power supplies being turned off or due to an overvoltage being applied to the ADG467, the output is clamped. When power is turned off, current is limited to the microampere level.
2. Low Power Dissipation.
3. Low  $R_{ON}$ . 62  $\Omega$  typical.
4. Trench Isolation Latch-Up Proof Construction.  
A dielectric trench separates the p- and n-channel MOSFETs thereby preventing latch-up.

#### Rev. B

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**REVISION HISTORY**

<b>2/11—Rev. A to Rev. B</b>		Added Test Circuits Section and Figure 16 to Figure 20.....	8
Updated Format.....	Universal	Changes to Overvoltage Protection Section and Figure 23 .....	9
Deleted ADG466 .....	Universal	Changes to Figure 24.....	10
Changes to Features Section, General Description Section, Figure 1, and Product Highlights Section .....	1	Change to Figure 26 .....	11
Changes to Power Requirements, $V_{DD}/V_{SS}$ Parameter, Table 1... 3		Changes to Overvoltage and Power Supply Sequencing Protection Section and Figure 27 .....	12
Deleted 8-Lead DIP, SOIC, and $\mu$ SOIC Pin Configuration .....	3	Changes to High Voltage Surge Suppression Section and Figure 28 .....	13
Deleted Figure 12; Renumbered Sequentially .....	5	Changes to Outline Dimensions .....	14
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Added Figure 7; Renumbered Sequentially .....	6		
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## SPECIFICATIONS

### DUAL SUPPLY

$V_{DD} = +15\text{ V}$ ,  $V_{SS} = -15\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	ADG467		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>FAULT PROTECTED CHANNEL</b>				
Fault-Free Analog Signal Range	$V_{SS} + 1.5$ $V_{DD} - 1.5$		V typ V typ	Output open circuit
	$V_{SS} + 1.7$ $V_{DD} - 1.7$		V typ V typ	Output loaded, 1 mA
$R_{ON}$	62	80	$\Omega$ typ	$-10\text{ V} \leq V_{Sx} \leq +10\text{ V}$ , $I_{Sx} = 1\text{ mA}$
		95	$\Omega$ max	
$R_{ON}$ Flatness		6	$\Omega$ max	$-5\text{ V} \leq V_{Sx} \leq +5\text{ V}$
$R_{ON}$ Match between Channels	5	6	$\Omega$ max	$V_{Sx} = \pm 10\text{ V}$ , $I_{Sx} = 1\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Channel Output Leakage, $I_{S(ON)}$ (Without Fault Condition)	$\pm 0.04$ $\pm 1$	$\pm 0.2$ $\pm 5$	nA typ nA max	$V_{Sx} = V_{Dx} = \pm 10\text{ V}$
Channel Input Leakage, $I_{D(ON)}$ (with Fault Condition)	$\pm 0.2$ $\pm 2$	$\pm 0.4$ $\pm 5$	nA typ nA max	$V_{Sx} = \pm 25\text{ V}$ $V_{Dx} = \text{open circuit}$
Channel Input Leakage, $I_{D(OFF)}$ (with Power Off and Fault)	$\pm 0.5$ $\pm 2$	$\pm 2$ $\pm 10$	nA typ nA max	$V_{DD} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_{Sx} = \pm 35\text{ V}$ $V_{Dx} = \text{open circuit}$
Channel Input Leakage, $I_{D(OFF)}$ (with Power Off and Output Short Circuit)	$\pm 0.006$ $\pm 0.015$	$\pm 0.16$ $\pm 0.5$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_{Sx} = \pm 35\text{ V}$ , $V_{Dx} = 0\text{ V}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	$\pm 0.05$ $\pm 0.5$	$\pm 8$	$\mu\text{A}$ typ $\mu\text{A}$ max	
$I_{SS}$	$\pm 0.05$ $\pm 0.5$	$\pm 8$	$\mu\text{A}$ typ $\mu\text{A}$ max	
$V_{DD}/V_{SS}$		$\pm 4.5/\pm 20$	V min/max	

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = +25°C, unless otherwise noted.

**Table 2.**

Parameter	Rating
V <sub>DD</sub> to V <sub>SS</sub>	+44 V
V <sub>SX</sub> , V <sub>DX</sub> , Analog Input Overvoltage with Power On <sup>1</sup>	V <sub>SS</sub> – 20V to V <sub>DD</sub> + 20 V
V <sub>SX</sub> , V <sub>DX</sub> , Analog Input Overvoltage with Power Off <sup>1</sup>	–40 V to +40 V
Continuous Current, V <sub>SX</sub> , V <sub>DX</sub>	20 mA
Peak Current, V <sub>SX</sub> , V <sub>DX</sub> (Pulsed at 1 ms, 10% Duty Cycle Maximum)	40 mA
Operating Temperature Range Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +125°C
Junction Temperature	+150°C
SOIC Package	
θ <sub>JA</sub> , Thermal Impedance	160°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C
SSOP Package	
θ <sub>JA</sub> , Thermal Impedance	130°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

<sup>1</sup> Overvoltages at V<sub>SX</sub> or V<sub>DX</sub> are clamped by the channel protector; see the Circuit Information section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

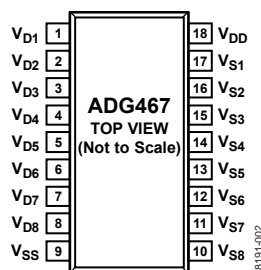


Figure 2. 18-Lead SOIC Pin Configuration

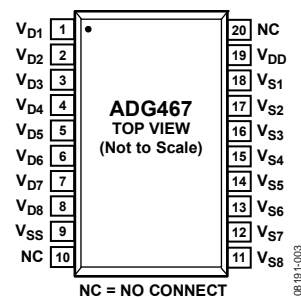


Figure 3. 20-Lead SSOP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.		Mnemonic	Description
SOIC	SSOP		
1	1	VD1	Drain Terminal 1. This pin can be an input or an output.
2	2	VD2	Drain Terminal 2. This pin can be an input or an output.
3	3	VD3	Drain Terminal 3. This pin can be an input or an output.
4	4	VD4	Drain Terminal 4. This pin can be an input or an output.
5	5	VD5	Drain Terminal 5. This pin can be an input or an output.
6	6	VD6	Drain Terminal 6. This pin can be an input or an output.
7	7	VD7	Drain Terminal 7. This pin can be an input or an output.
8	8	VD8	Drain Terminal 8. This pin can be an input or an output.
9	9	VSS	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
N/A	10	NC	No Connect.
10	11	VS8	Source Terminal 1. This pin can be an input or an output.
11	12	VS7	Source Terminal 2. This pin can be an input or an output.
12	13	VS6	Source Terminal 3. This pin can be an input or an output.
13	14	VS5	Source Terminal 4. This pin can be an input or an output.
14	15	VS4	Source Terminal 5. This pin can be an input or an output.
15	16	VS3	Source Terminal 6. This pin can be an input or an output.
16	17	VS2	Source Terminal 7. This pin can be an input or an output.
17	18	VS1	Source Terminal 8. This pin can be an input or an output.
18	19	VDD	Most Positive Power Supply Potential.
N/A	20	NC	No Connect. Do not connect to this pin.

## TYPICAL PERFORMANCE CHARACTERISTICS

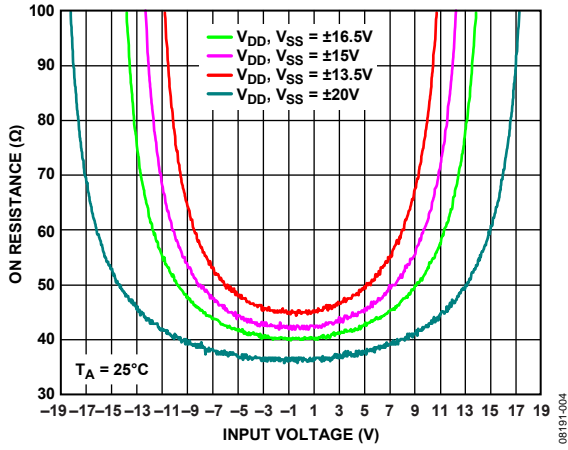


Figure 4. On Resistance as a Function of  $V_{DD}$  and  $V_{SS}$  (Input Voltage), Dual Supply

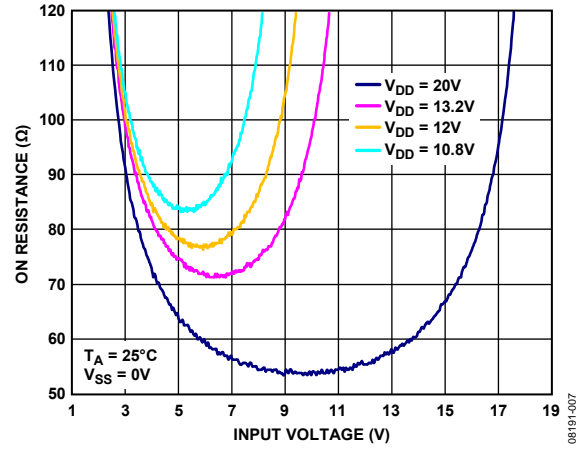


Figure 7. On Resistance as a Function of  $V_{DD}$  and  $V_{SS}$  (Input Voltage), Single Supply

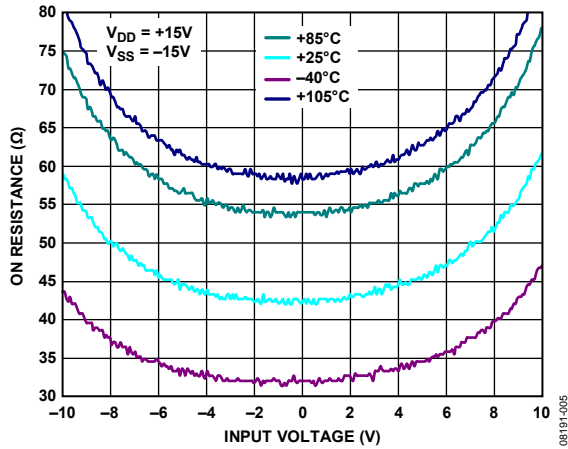


Figure 5. On Resistance as a Function of Temperature and  $V_{SS}$  (Input Voltage)

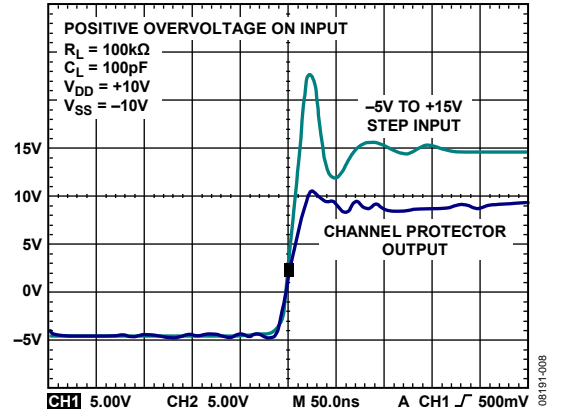


Figure 8. Positive Overvoltage Transience Response

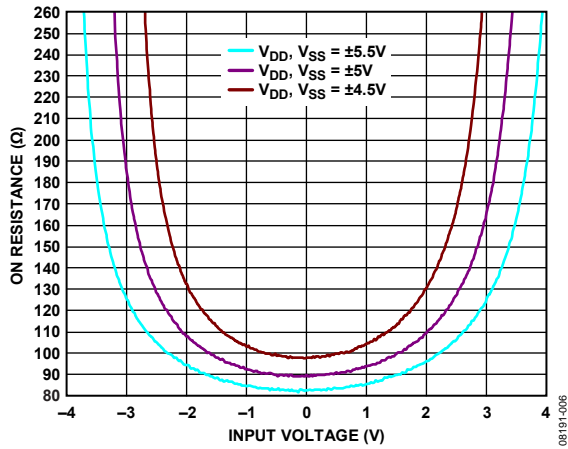


Figure 6. On Resistance as a Function of  $V_{DD}$  and  $V_{SS}$  (Input Voltage), 5V Dual Supply

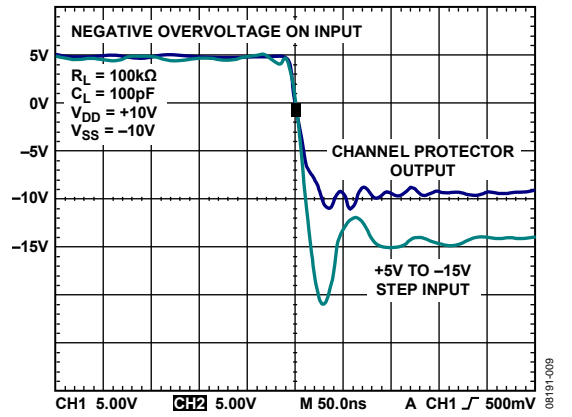


Figure 9. Negative Overvoltage Transience Response

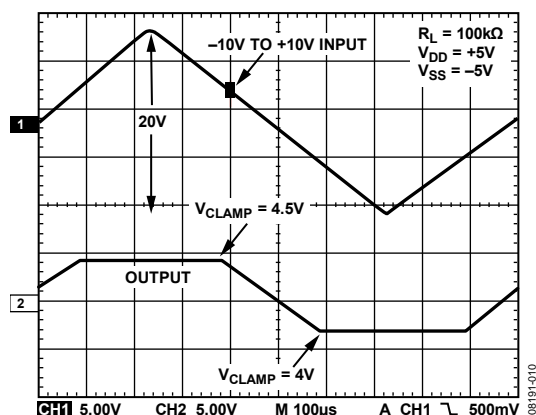


Figure 10. Overvoltage Ramp

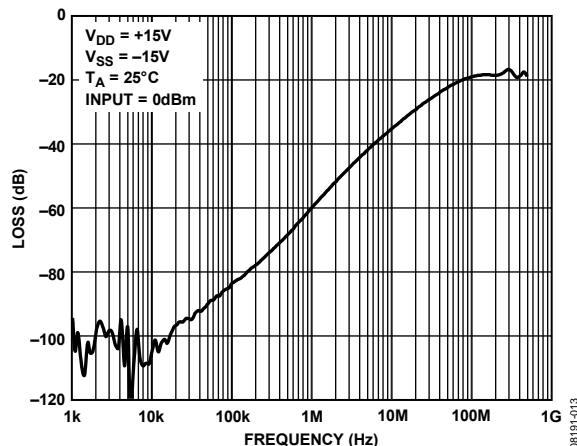


Figure 13. Crosstalk Between Adjacent Channels

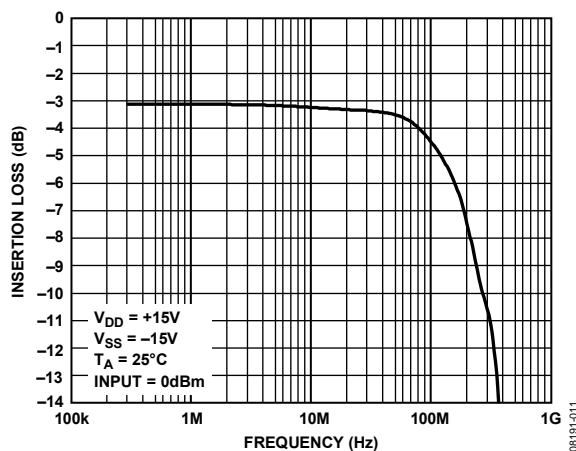


Figure 11. Frequency Response (Magnitude)

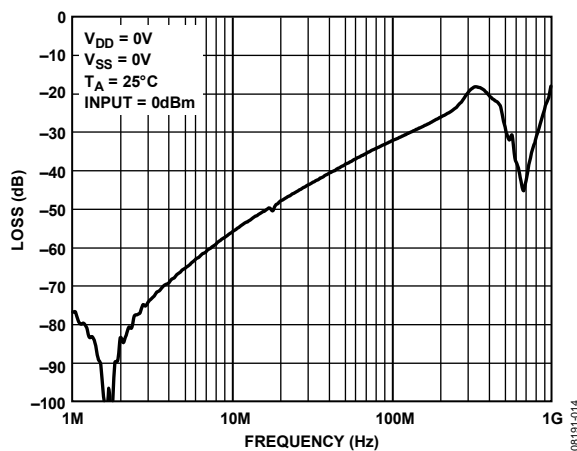


Figure 14. Off Isolation

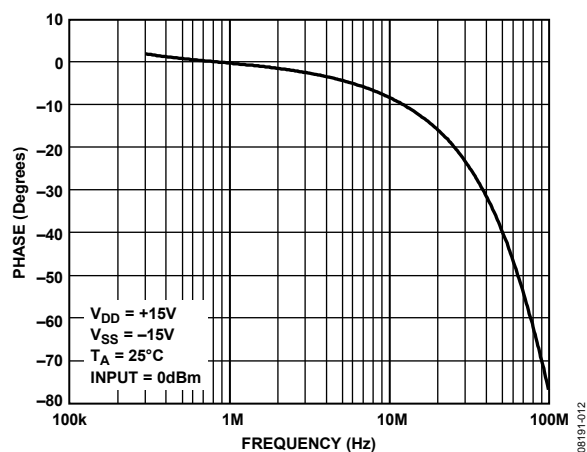


Figure 12. Frequency Response (Phase)

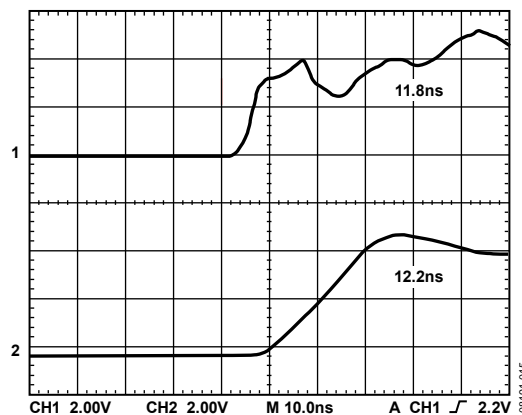


Figure 15. Propagation Delay



## TEST CIRCUITS

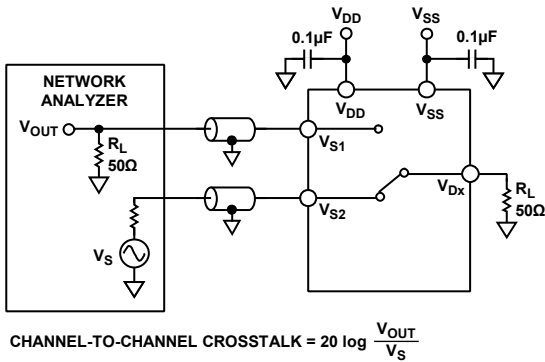
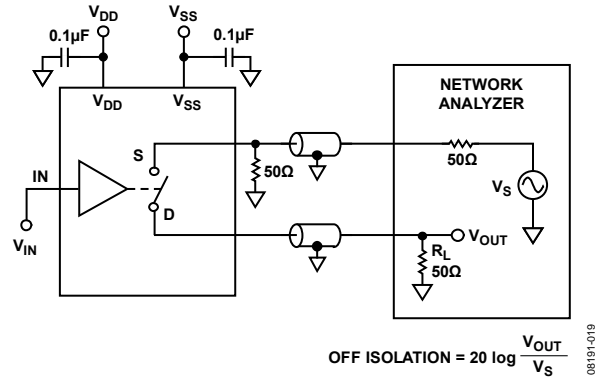
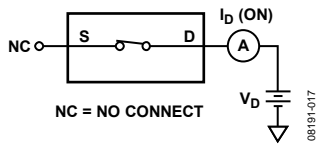
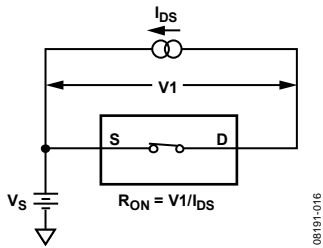


Figure 18. Channel-to-Channel Crosstalk

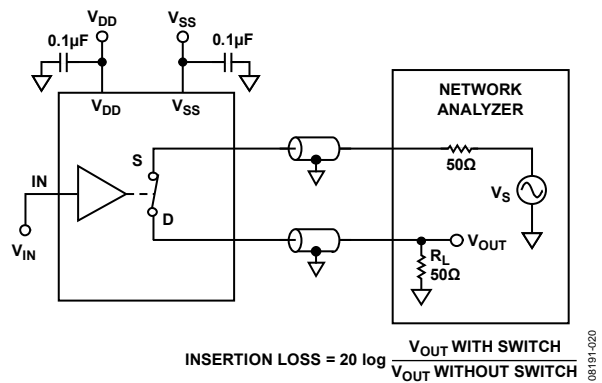


Figure 20. Bandwidth

## CIRCUIT INFORMATION

Figure 21 shows a simplified schematic of a channel protector circuit. The circuit is made up of four MOS transistors—two NMOS and two PMOS. One of the PMOS devices does not lie directly in the signal path but is used to connect the source of the second PMOS device to its backgate. This has the effect of lowering the threshold voltage and thus increasing the input signal range of the channel for normal operation. The source and backgate of the NMOS devices are connected for the same reason. During normal operation, the channel protectors have an on resistance of 62 Ω typical. The channel protectors are very low power devices, and even under fault conditions, the supply current is limited to sub microampere levels. All transistors are dielectrically isolated from each other using a trench isolation method. This makes it impossible to latch up the channel protectors. For further details, see the Trench Isolation section.

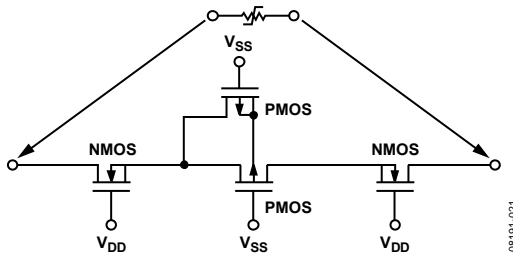


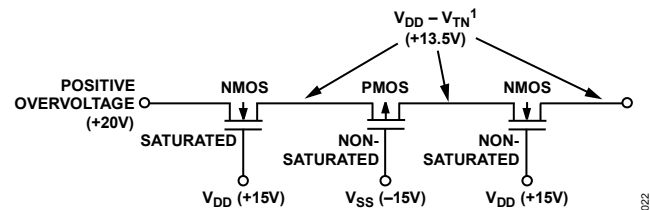
Figure 21. The Channel Protector Circuit

## OVERVOLTAGE PROTECTION

When a fault condition occurs on the input of a channel protector, the voltage on the input has exceeded some threshold voltage set by the supply rail voltages. The threshold voltages are related to the supply rails as follows. For a positive overvoltage, the threshold voltage is given by  $V_{DD} - V_{TN}$ , where  $V_{TN}$  is the threshold voltage of the NMOS transistor (1.5 V typical). In the case of a negative overvoltage, the threshold voltage is given by  $V_{SS} - V_{TP}$ , where  $V_{TP}$  is the threshold voltage of the PMOS device (-1.5 V typical). If the input voltage exceeds these threshold voltages,

the output of the channel protector (no load) is clamped at these threshold voltages. However, the channel protector output clamps at a voltage value that is inside these thresholds if the output is loaded. For example, with an output load of 1 kΩ,  $V_{DD} = 15$  V, and a positive overvoltage on the input, the output clamps at  $V_{DD} - V_{TN} - \Delta V = 15$  V - 1.5 V - 0.6 V = 12.9 V, where  $\Delta V$  is due to an  $I \times R$  voltage drop across the channels of the MOS devices (see Figure 23). As can be seen from Figure 23, the current during fault condition is determined by the load on the output (that is,  $V_{CLAMP}/R_L$ ). However, if the supplies are off, the fault current is limited to the nano-ampere level.

Figure 22, Figure 24, and Figure 25 show the operating conditions of the signal path transistors during various fault conditions. Figure 22 shows how the channel protectors operate when a positive overvoltage is applied to the channel protector.



<sup>1</sup> $V_{TN}$  = NMOS THRESHOLD VOLTAGE (+1.5V).

Figure 22. Positive Overvoltage on the Channel Protector

The first NMOS transistor goes into a saturated mode of operation as the voltage on its drain exceeds the gate voltage ( $V_{DD}$ ) - the threshold voltage ( $V_{TN}$ ). This situation is shown in Figure 23. The potential at the source of the NMOS device is equal to  $V_{DD} - V_{TN}$ . The other MOS devices are in a nonsaturated mode of operation.

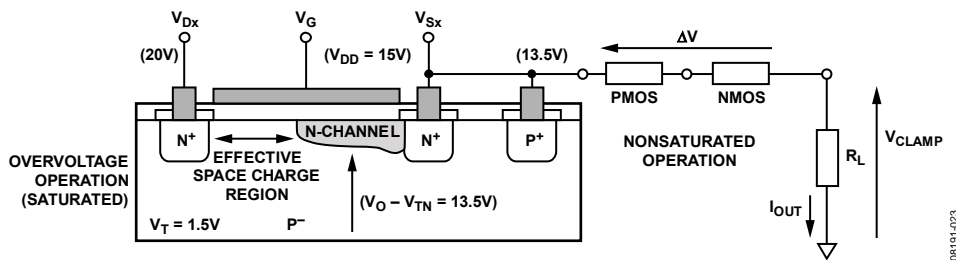


Figure 23. Positive Overvoltages Operation of the Channel Protector

# ADG467

When a negative overvoltage is applied to the channel protector circuit, the PMOS transistor enters a saturated mode of operation as the drain voltage exceeds  $V_{SS} - V_{TP}$  (see Figure 24). As in the case of the positive overvoltage, the other MOS devices are nonsaturated.

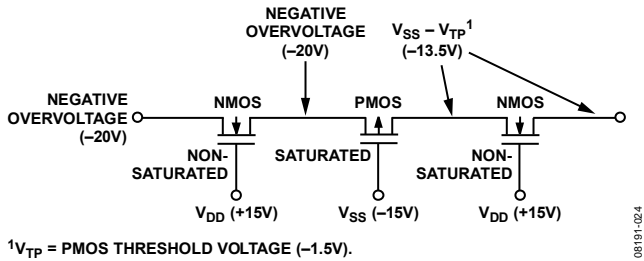


Figure 24. Negative Overvoltage on the Channel Protector

The channel protector is also functional when the supply rails are down (for example, power failure) or momentarily unconnected (for example, rack system). This is where the channel protector has an advantage over more conventional protection methods such as diode clamping (see the Applications Information section). When  $V_{DD}$  and  $V_{SS}$  equal 0 V, all transistors are off and the current is limited to subnano-ampere levels (see Figure 25).

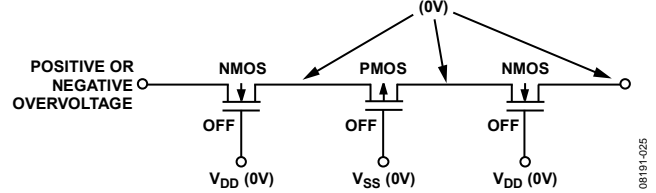


Figure 25. Channel Protector Supplies Equal to 0 V

## TRENCH ISOLATION

The MOS devices that make up the channel protector are isolated from each other by an oxide layer (trench) (see Figure 26). When the NMOS and PMOS devices are not electrically isolated from each other, parasitic junctions between CMOS transistors may cause latch-up. Latch-up is caused when P-N junctions that are normally reverse biased become forward biased, causing large currents to flow, which can be destructive.

CMOS devices are normally isolated from each other by junction isolation. In junction isolation, the N and P wells of the CMOS transistors form a diode that is reverse biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed; the result is a latch-up-proof circuit.

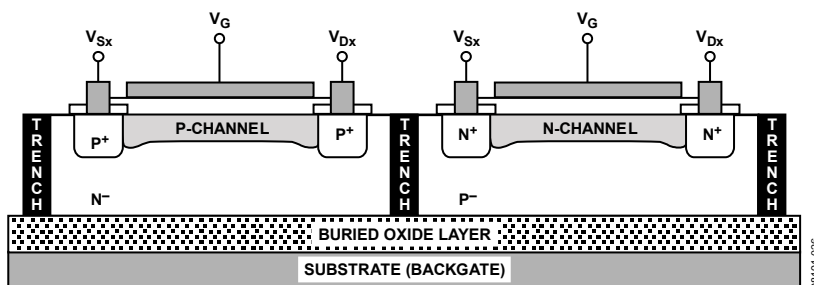


Figure 26. Trench Isolation

## APPLICATIONS INFORMATION

### OVERVOLTAGE AND POWER SUPPLY SEQUENCING PROTECTION

The ADG467 is ideal for use in applications where input overvoltage protection is required and correct power supply sequencing cannot always be guaranteed. The overvoltage protection ensures that the output voltage of the channel protector does not exceed the threshold voltages set by the supplies (see the Circuit Information section) when there is an overvoltage on the input. When the input voltage does not exceed these threshold voltages, the channel protector behaves like a series resistor (62  $\Omega$  typical). The resistance of the channel protector does vary slightly with operating conditions (see the Typical Performance Characteristics section).

The power sequencing protection is provided by the channel protector, which becomes a high resistance device when the supplies to the channel protector are not connected. Under this condition, all transistors in the channel protector are off and the only currents that flow are leakage currents, which are at the microampere level.

Figure 27 shows a typical application that requires overvoltage and power supply sequencing protection. The application shows a hot insertion rack system. This involves plugging a circuit board or module into a live rack via an edge connector. In this type of application, it is not possible to guarantee correct power supply sequencing. Correct power supply sequencing means that the power supplies should be connected before any external signals. Incorrect power sequencing can cause a CMOS device to latch up. This is true of most CMOS devices regardless of the functionality. RC networks are used on the supplies of the channel protector (see Figure 27) to ensure that the rest of the circuitry is powered up before the channel protectors. In this way, the outputs of the channel protectors are clamped well below  $V_{DD}$  and  $V_{SS}$  until the capacitors are charged. The diodes ensure that the supplies on the channel protector never exceed the supply rails of the board when it is being disconnected. This ensures that signals on the inputs of the CMOS devices never exceed the supplies.

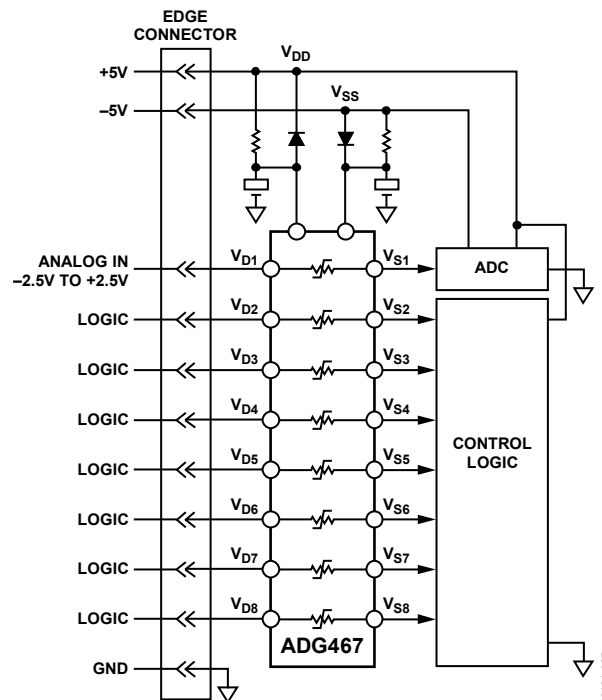


Figure 27. Overvoltage and Power Supply Sequencing Protection

### HIGH VOLTAGE SURGE SUPPRESSION

The ADG467 is not intended for use in high voltage applications like surge suppression. The ADG467 has breakdown voltages in excess of  $V_{SS} - 20\text{ V}$  and  $V_{DD} + 20\text{ V}$  on the inputs when the power supplies are connected. When the power supplies are disconnected, the breakdown voltages on the input of the channel protector are  $\pm 40\text{ V}$ . In applications where inputs are likely to be subject to overvoltages exceeding the breakdown voltages specified for the channel protectors, transient voltage suppressors (TVSs) should be used. These devices are commonly used to protect vulnerable circuits from electric overstress such as that caused by electrostatic discharge, inductive load switching, and induced lightning. However, TVSs can have a substantial standby (leakage) current ( $300\text{ }\mu\text{A}$  typical) at the reverse standoff voltage. The reverse stand-off

voltage of a TVS is the normal peak operating voltage of the circuit. Also, a TVS offers no protection against latch-up of sensitive CMOS devices when the power supplies are off. The ideal solution is to use a channel protector in conjunction with a TVS to provide the optimal leakage current specification and circuit protection.

Figure 28 shows an input protection scheme that uses both a TVS and a channel protector. The TVS is selected with a reverse standoff voltage that is much greater than the operating voltage of the circuit (TVSs with higher breakdown voltages tend to have better standby leakage current specifications) but is inside the breakdown voltage of the channel protector. This circuit protects the circuitry regardless of whether the power supplies are present.

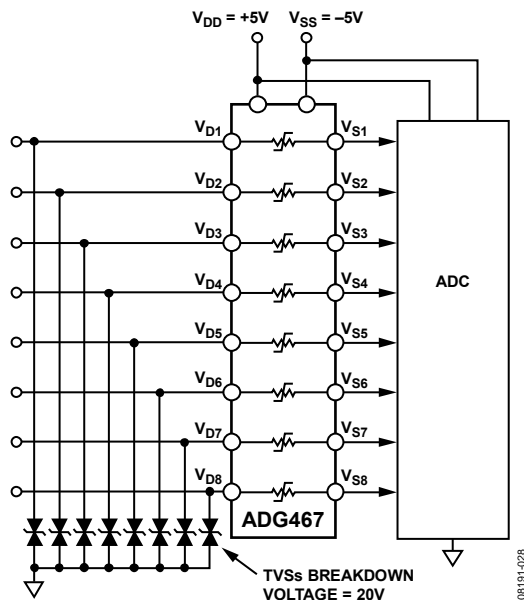
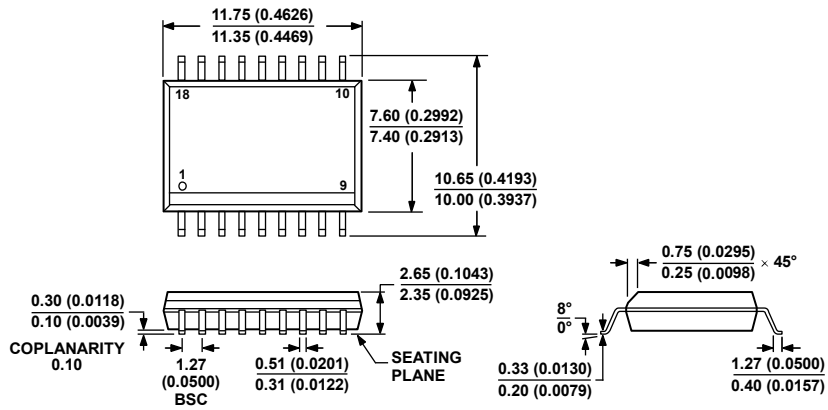


Figure 28. High Voltage Protection

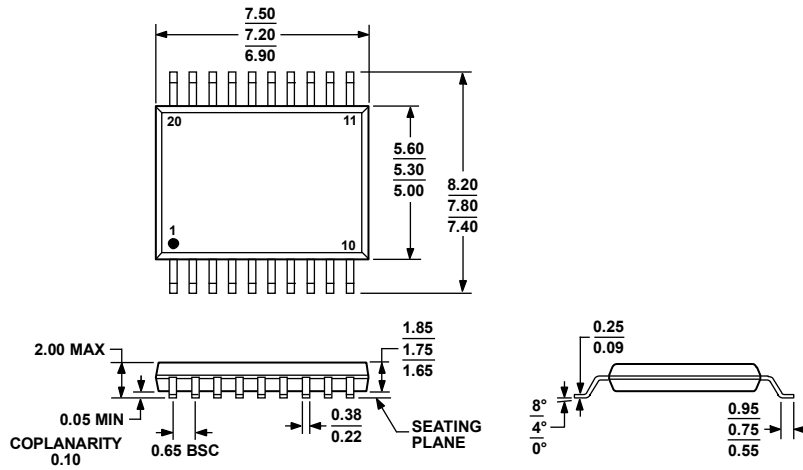
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AB  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 29. 18-Lead Standard Small Outline Package [SOIC\_W]  
 Wide Body (RW-18)  
 Dimensions shown in millimeters and (inches)

060706-A



COMPLIANT TO JEDEC STANDARDS MO-150-AE

Figure 30. 20-Lead Shrink Small Outline Package [SSOP]  
 (RS-20)  
 Dimensions shown in millimeters

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**ORDERING GUIDE**

<b>Model<sup>1</sup></b>	<b>Temperature Range</b>	<b>Package Description</b>	<b>Package Option</b>
ADG467BR	-40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BR-REEL	-40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BR-REEL7	-40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BRZ	-40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BRZ-REEL	-40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BRZ-REEL7	-40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BRS	-40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADG467BRS-REEL	-40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADG467BRSZ	-40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADG467BRSZ-REEL	-40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20

<sup>1</sup> Z = RoHS Compliant Part.



**ADG467**

**NOTES**