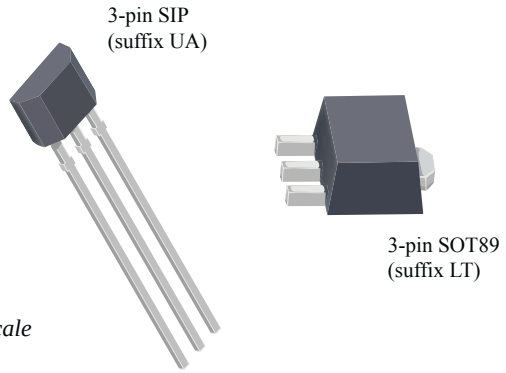
Hall Effect Latch for High Temperature Operation

Features and Benefits

- Symmetrical switchpoints
- Superior temperature stability
- Operation from unregulated supply
- Open-drain 25 mA output
- Reverse Battery protection
- Activate with small, commercially available permanent magnets
- Solid-state reliability
- Small size
- Resistant to physical stress
- Enhanced ESD structures result in 8 kV HBM ESD performance without external protection components
- Internal protection circuits enable 40 V load dump compliance without external protection components

Packages:



Not to scale

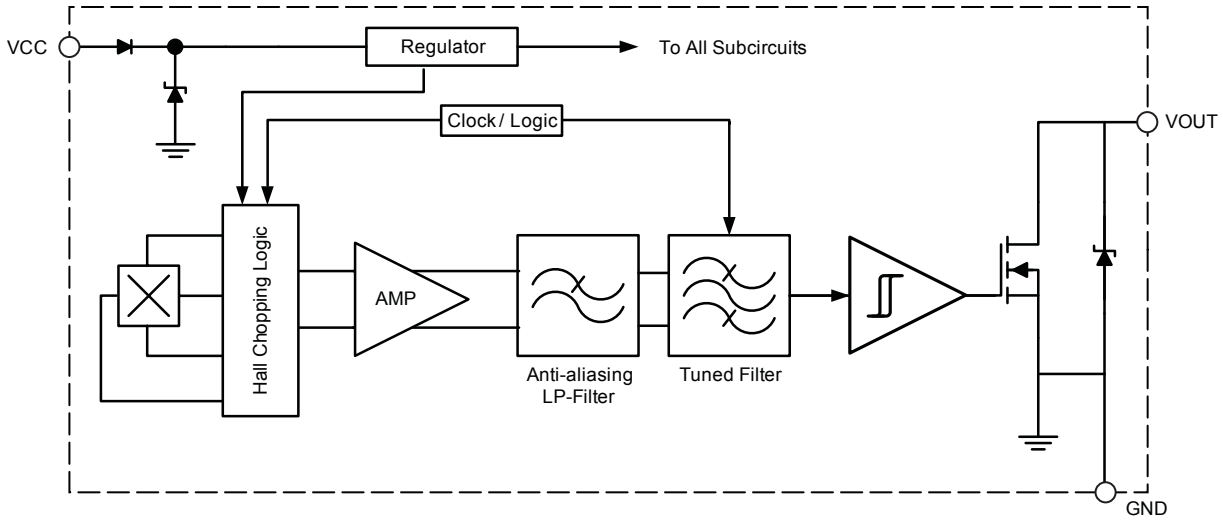
Description

These Hall-effect latches are extremely temperature-stable and stress resistant sensor ICs especially suited for operation over extended temperature ranges to 150°C. Superior high-temperature performance is made possible through a novel Schmitt trigger circuit that maintains operate and release point symmetry by compensating for temperature changes in the Hall element. Additionally, internal compensation provides magnetic switchpoints that become more sensitive with temperature, hence offsetting the usual degradation of the magnetic field with temperature. The symmetry capability makes these devices ideal for use in pulse-counting applications where duty cycle is an important parameter. The three basic devices (A1225, A1227, and A1229) are identical except for magnetic switchpoints.

Each device includes on a single silicon chip a voltage regulator, Hall-voltage generator, temperature compensation circuit, signal amplifier, Schmitt trigger, and a buffered open-drain output to sink up to 25 mA. The on-board regulator permits operation with supply voltages of 3.8 to 24 V.

The first character of the part number suffix determines the device operating temperature range. Suffix L is for –40°C to 150°C. Two package styles provide a magnetically optimized package for most applications. Suffix LT is a miniature SOT89/TO-243AA transistor package for surface-mount applications, suffix UA is a three-lead ultra-mini-SIP. Both packages are lead (Pb) free with 100% matte tin leadframe plating.

Functional Block Diagram



Selection Guide

Part Number	Packing*	Package	Ambient Temperature, T_A	B_{RP}(min) (G)	B_{OP}(max) (G)
A1225LLTTK-T	13-in. reel, 4000 pieces/reel	3-pin SOT89 surface mount	–40°C to 150°C	–300	300
A1225LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1227LLTTK-T	13-in. reel, 4000 pieces/reel	3-pin SOT89 surface mount	–40°C to 150°C	–175	175
A1227LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1229LLTTK-T	13-in. reel, 4000 pieces/reel	3-pin SOT89 surface mount	–40°C to 150°C	–200	200
A1229LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			

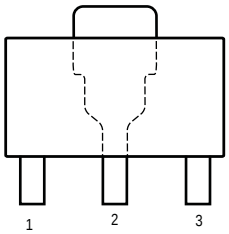
*Contact Allegro™ for additional packaging options.

Absolute Maximum Ratings

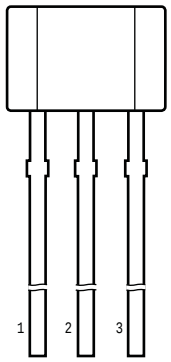
Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		30	V
Reverse Supply Voltage	V_{RCC}		–30	V
Output Off Voltage	V_{OUT}		30	V
Reverse Output Voltage	V_{ROUT}		–0.5	V
Continuous Output Current	$I_{OUT(SINK)}$		25	mA
Operating Ambient Temperature	T_A	Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Pin-out Diagrams

Package LT



Package UA



Terminal List Table

Number	Name	Function
1	VCC	Input power supply
2	GND	Ground
3	VOUT	Output signal

ELECTRICAL CHARACTERISTICS Valid at T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, V_{CC} = 12 V; unless otherwise noted

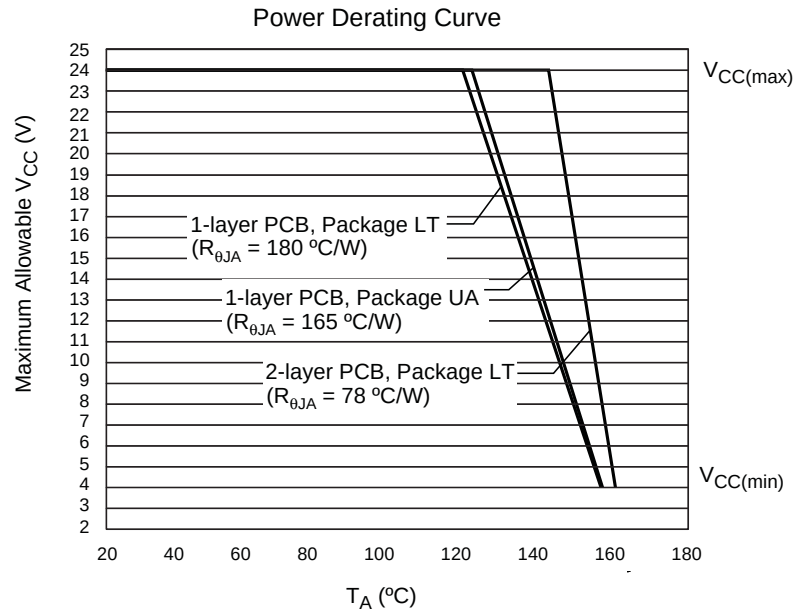
Characteristics	Symbol	Test Conditions		Min.	Typ.[1]	Max.	Unit[2]
Electrical Characteristics							
Supply Voltage	V_{CC}	Operating; $T_J \le 165°C$		3.8		24	V
Supply Current	I_{CC}	$B < B_{RP}$ (Output off)		–	–	6	mA
		$B > B_{OP}$ (Output on)		–	–	6	mA
Supply Zener Voltage	$V_{Z(sup)}$	I_{CC} = 9 mA, T_A = 25°C		28	–	–	V
Reverse Battery Current	$I_{Z(sup)}$	V_{RCC} = –28 V, T_A = 25°C		–	–	– 5	mA
Power-On Time[3]	t_{PO}			–	–	12	µs
Power-On State	POS	$B < B_{OP}$		–	HIGH	–	–
Chopping Frequency	f_{chop}			–	400	–	kHz
Output Stage Characteristics							
Output Saturation Voltage	$V_{OUT(sat)}$	I_{OUT} = 20 mA		–	175	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, $B < B_{RP}$		–	< 1	10	µA
Output Rise Time[3,4]	t_r	R_L= 820 Ω, C_L= 20 pF		–	200	2000	ns
Output Fall Time[3,4]	t_f	R_L= 820 Ω, C_L= 20 pF		–	200	2000	ns
Output Zener Voltage	$V_{Z(out)}$	I_{OUT} = 3 mA, T_A = 25°C		30	–	–	V
Magnetic Characteristics							
Operate Point	B_{OP}	A1225	T_A = 25°C	170	–	270	G
			Over operating temperature range	140	–	300	G
		A1227	T_A = 25°C	50	–	150	G
			Over operating temperature range	50	–	175	G
		A1229	T_A = 25°C	100	–	180	G
			Over operating temperature range	80	–	200	G
Release Point	B_{RP}	A1225	T_A = 25°C	–270	–	–170	G
			Over operating temperature range	–300	–	–140	G
		A1227	T_A = 25°C	–150	–	–50	G
			Over operating temperature range	–175	–	–50	G
		A1229	T_A = 25°C	–180	–	–100	G
			Over operating temperature range	–200	–	–80	G
Hysteresis ($B_{OP} – B_{RP}$)	B_{HYS}	A1225	T_A = 25°C	340	–	540	G
			Over operating temperature range	280	–	600	G
		A1227	T_A = 25°C	100		300	G
			Over operating temperature range	100	–	350	G
		A1229	T_A = 25°C	200	–	360	G
			Over operating temperature range	160	–	400	G

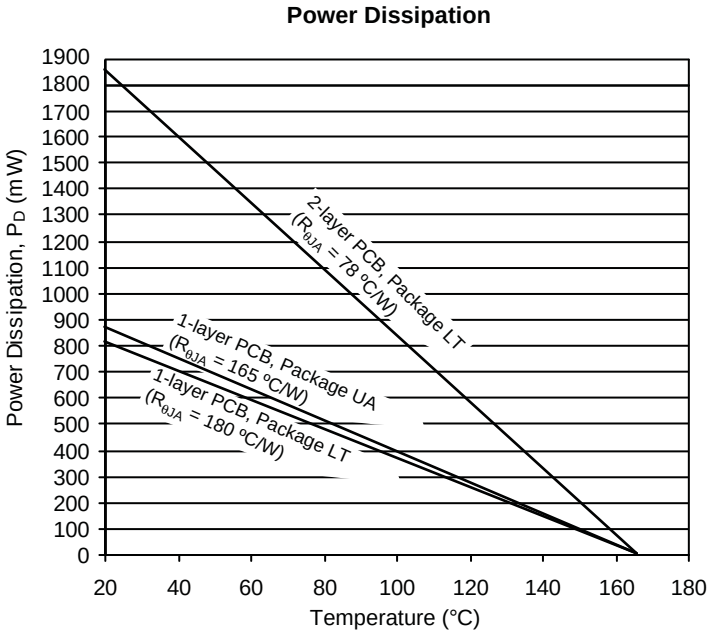
[1]Typical data are at T_A = 25°C and V_{CC} = 12 V, and are for design estimations only.
[2]1 G (gauss) = 0.1 mT (millitesla).
[3]Minimum and maximum specifications verified by bench characterization and not guaranteed by Allegro final test.
[4]C_L = oscilloscope probe capacitance.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LT, 1-layer PCB with copper limited to solder pads	180	ºC/W
		Package LT, 2-layer PCB with 0.94 in^2 copper each side	78	ºC/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	ºC/W

*Additional thermal information available on Allegro website.

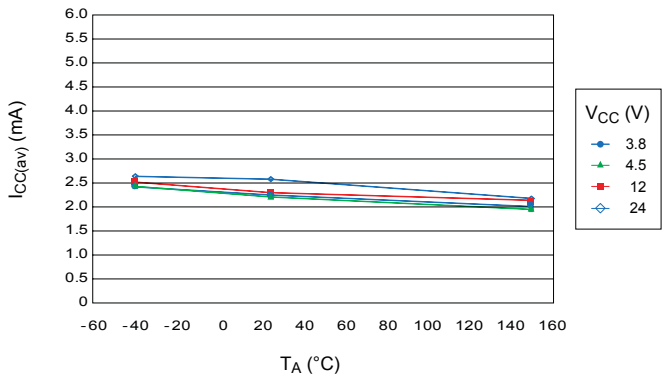




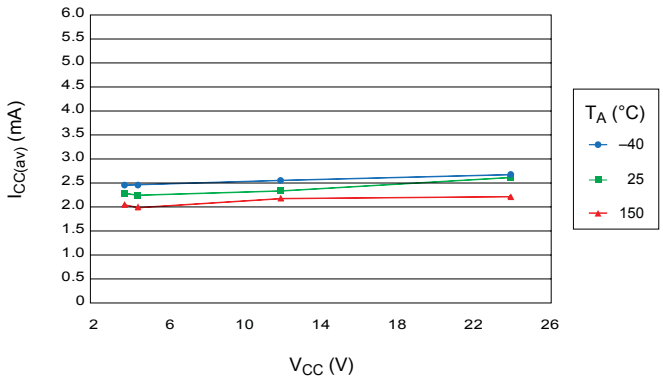
Characteristic Performance

A1225, A1227, and A1229 Electrical Characteristics

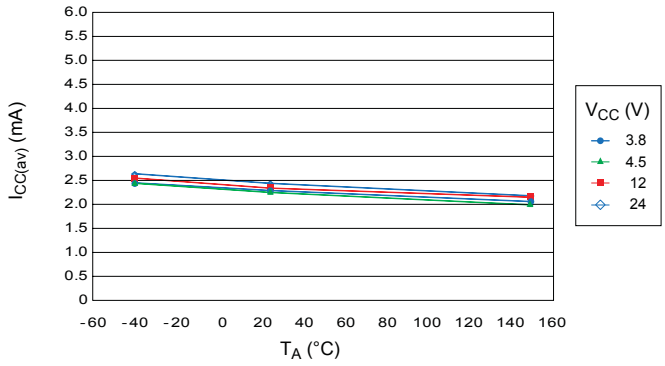
Average Supply Current (On) versus Ambient Temperature



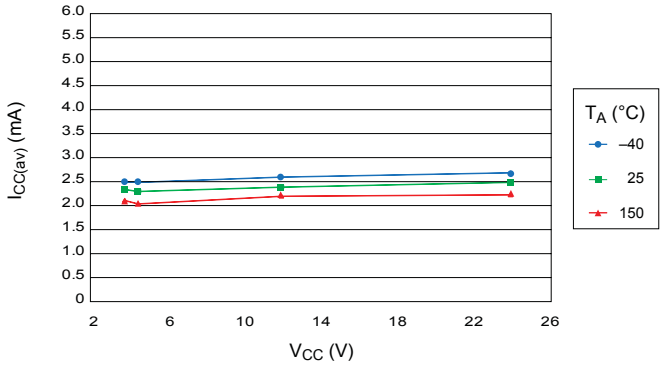
Average Supply Current (On) versus Supply Voltage



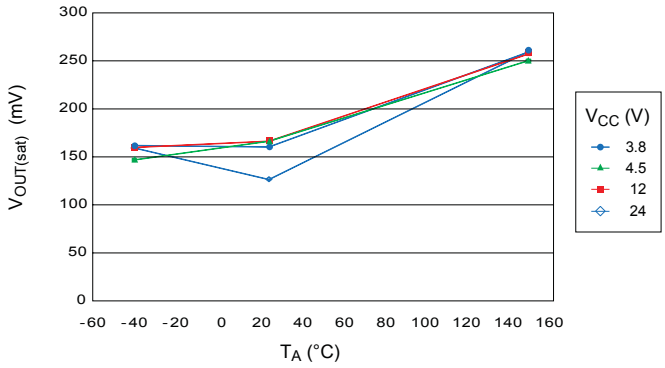
Average Supply Current (Off) versus Ambient Temperature



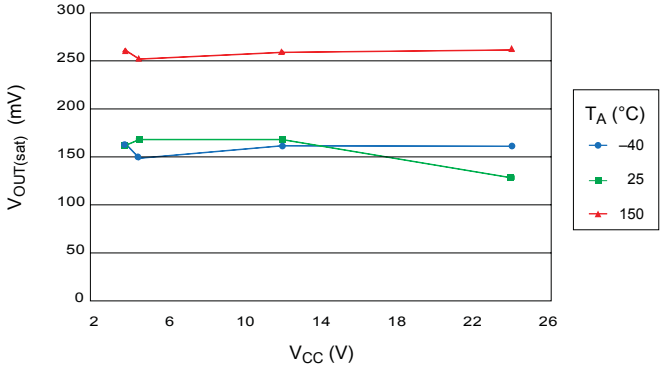
Average Supply Current (Off) versus Supply Voltage



Average Output Saturation Voltage versus Ambient Temperature

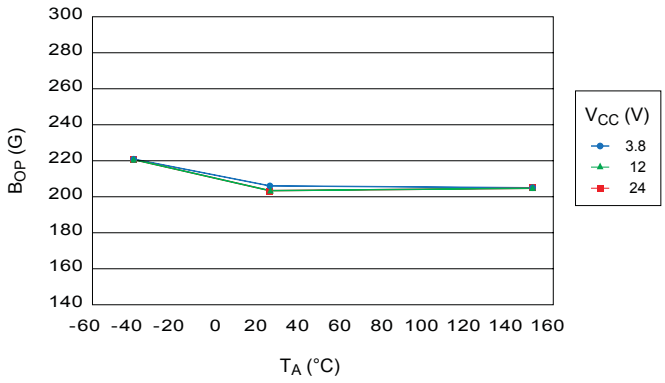


Average Output Saturation Voltage versus Supply Voltage

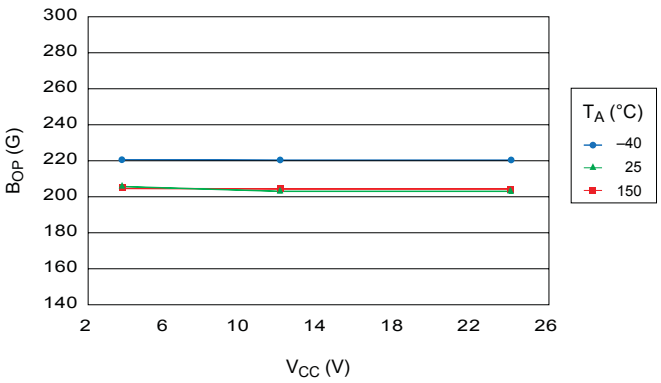


A1225 Magnetic Characteristics

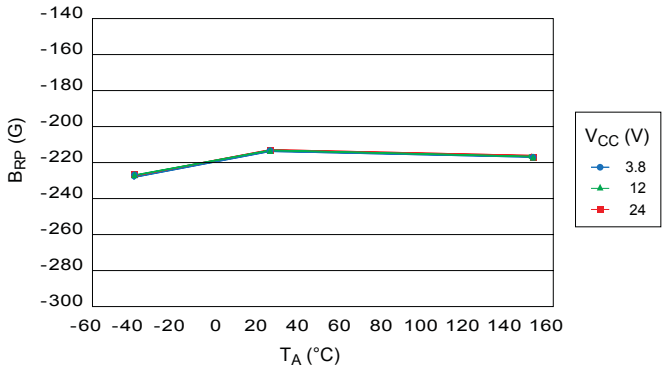
Operate Point versus Ambient Temperature



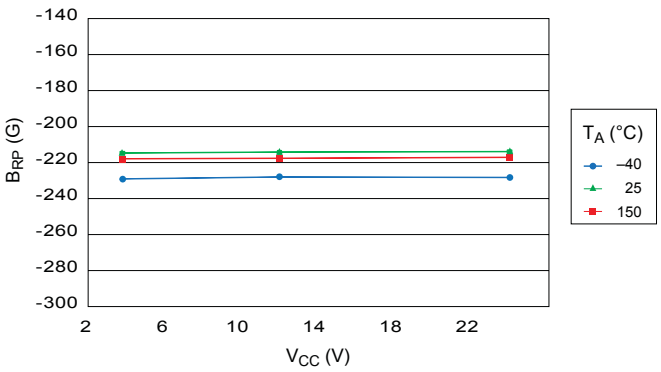
Operate Point versus Supply Voltage



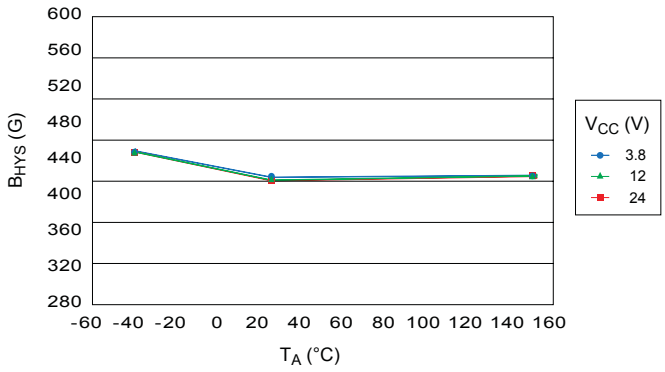
Release Point versus Ambient Temperature



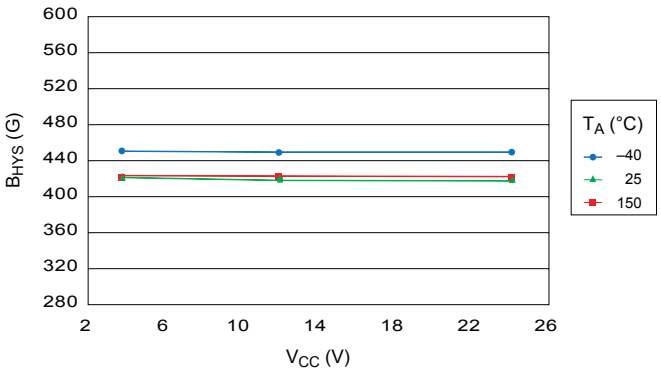
Release Point versus Supply Voltage



Switchpoint Hysteresis versus Ambient Temperature

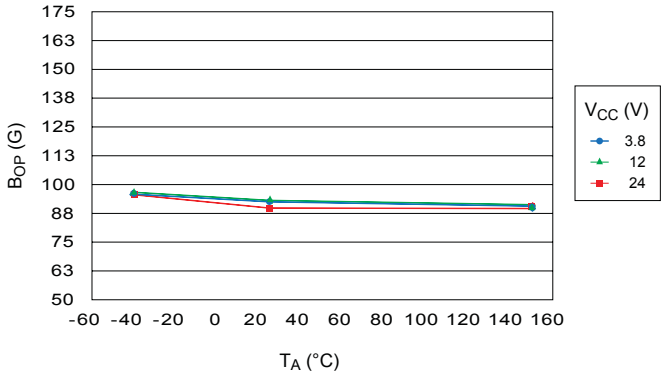


Switchpoint Hysteresis versus Supply Voltage

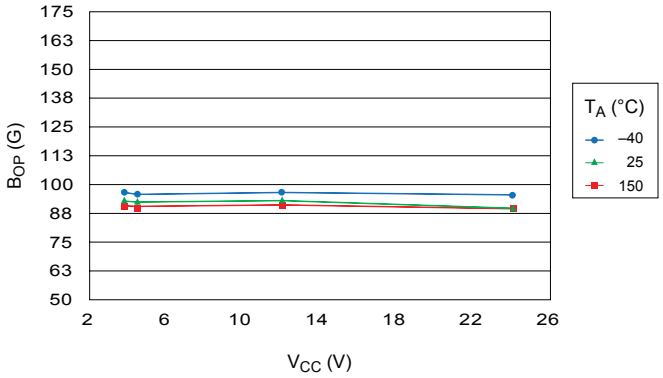


A1227 Magnetic Characteristics

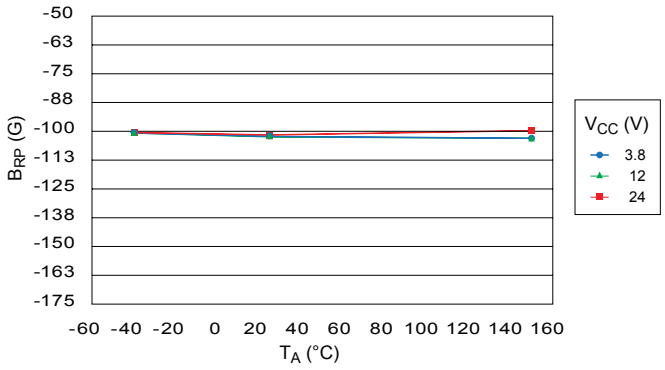
Operate Point versus Ambient Temperature



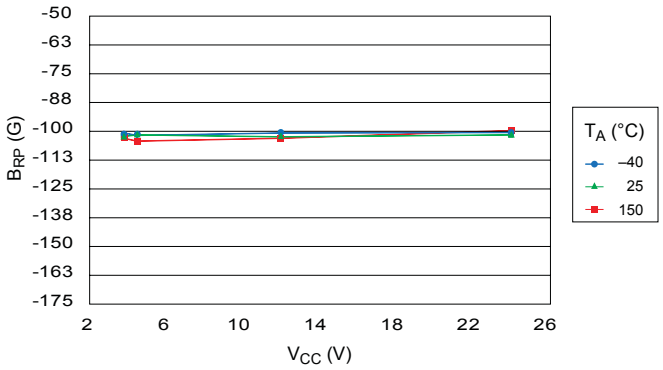
Operate Point versus Supply Voltage



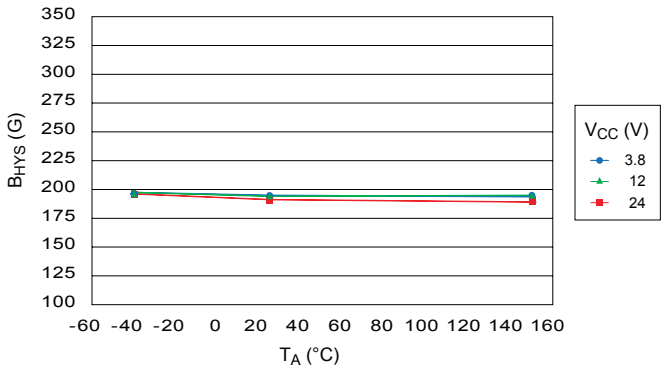
Release Point versus Ambient Temperature



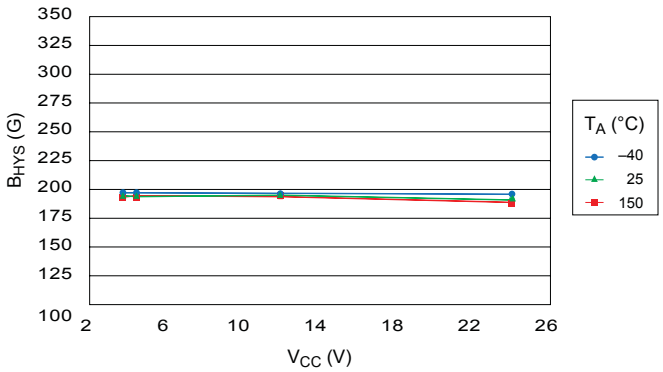
Release Point versus Supply Voltage



Switchpoint Hysteresis versus Ambient Temperature

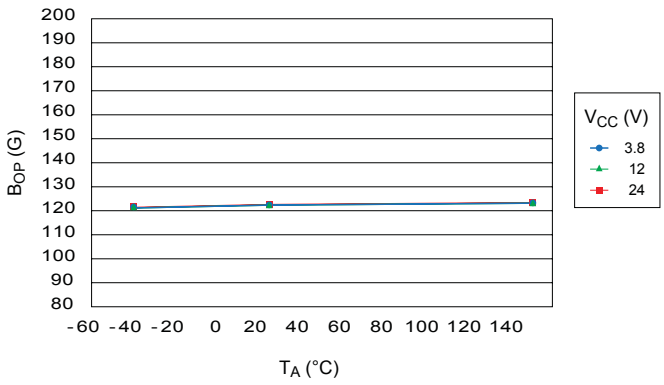


Switchpoint Hysteresis versus Supply Voltage

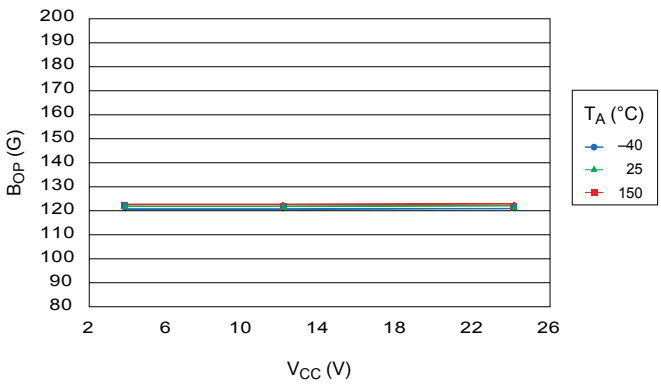


A1229 Magnetic Characteristics

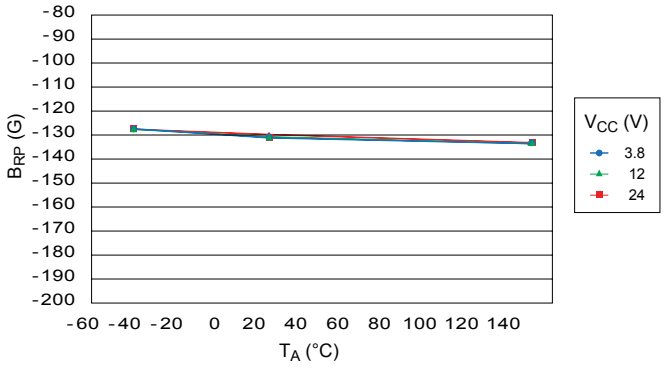
Operate Point versus Ambient Temperature



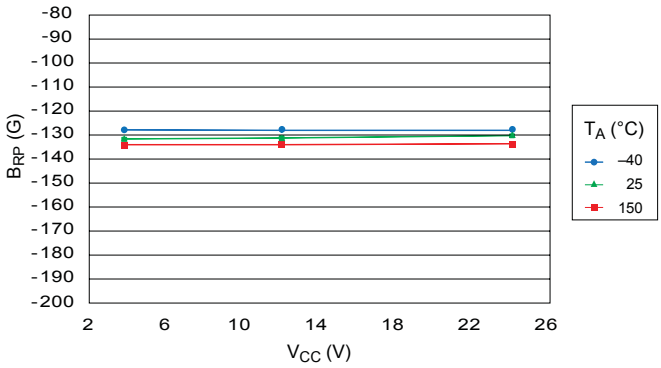
Operate Point versus Supply Voltage



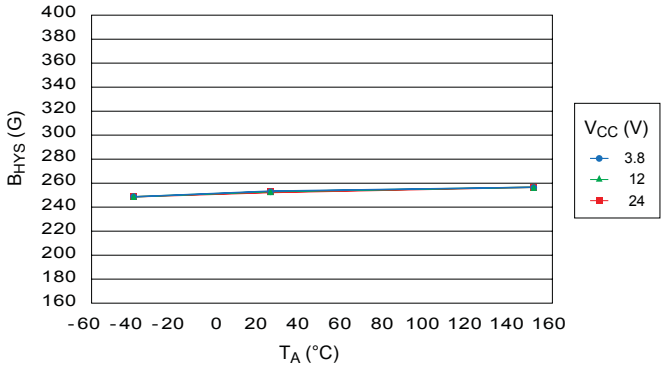
Release Point versus Ambient Temperature



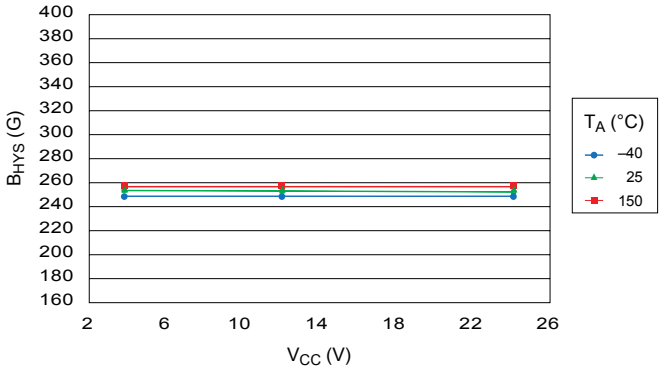
Release Point versus Supply Voltage



Switchpoint Hysteresis versus Ambient Temperature



Switchpoint Hysteresis versus Supply Voltage



Functional Description and Application Information

Switching Behavior

The output of the A1225, A1227, and A1229 devices switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point threshold, B_{OP} (see figure 1). After turn-on, the output is capable of sinking 25 mA and the output voltage is $V_{OUT(sat)}$. Notice that the device latches; that is, a south pole of sufficient strength towards the branded surface of the device turns the device on, and the device remains on with removal of the south pole.

When the magnetic field is reduced below the release point, B_{RP}, the device output goes high (turns off). The difference between the magnetic operate point and release point is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output, even in the presence of external mechanical vibration and electrical noise.

When the device is powered-on in the hysteresis range, less than B_{OP} and higher than B_{RP}, the device output goes high. The correct output state is attained after the first excursion beyond B_{OP} or B_{RP}.

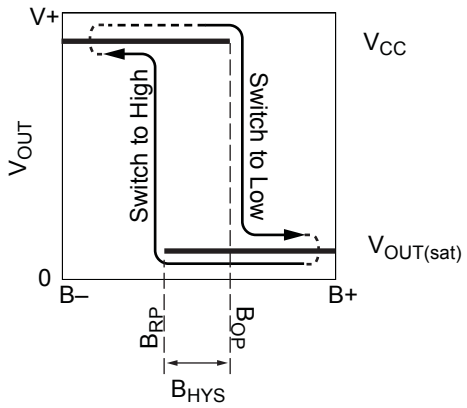


Figure 1. Output switching characteristics

Application Information

The simplest form of magnet that will operate these devices is a ring magnet, as shown in figure 2. Other methods of operation are possible.

In three-wire applications the device output is connected through a pull-up resistor to the supply pin or separate battery voltage (figure 3). Switching of the output signal indicates sufficient change of the magnetic field.

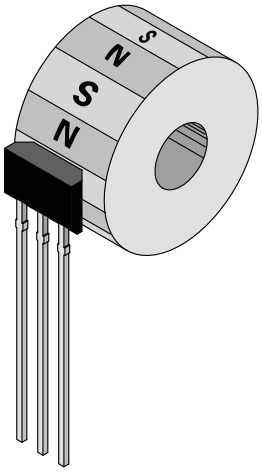


Figure 2. Typical magnetic target configuration using a ring magnet

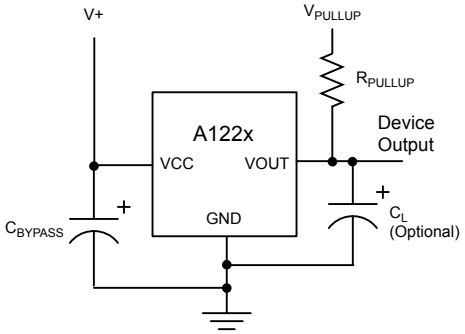


Figure 3. Typical 3-wire application circuit

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a patented technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal and stress related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high-frequency sampling clock. For the demodulation process, a sample-and-hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

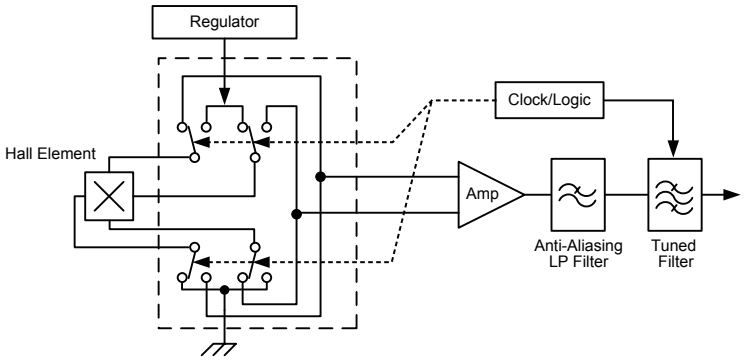
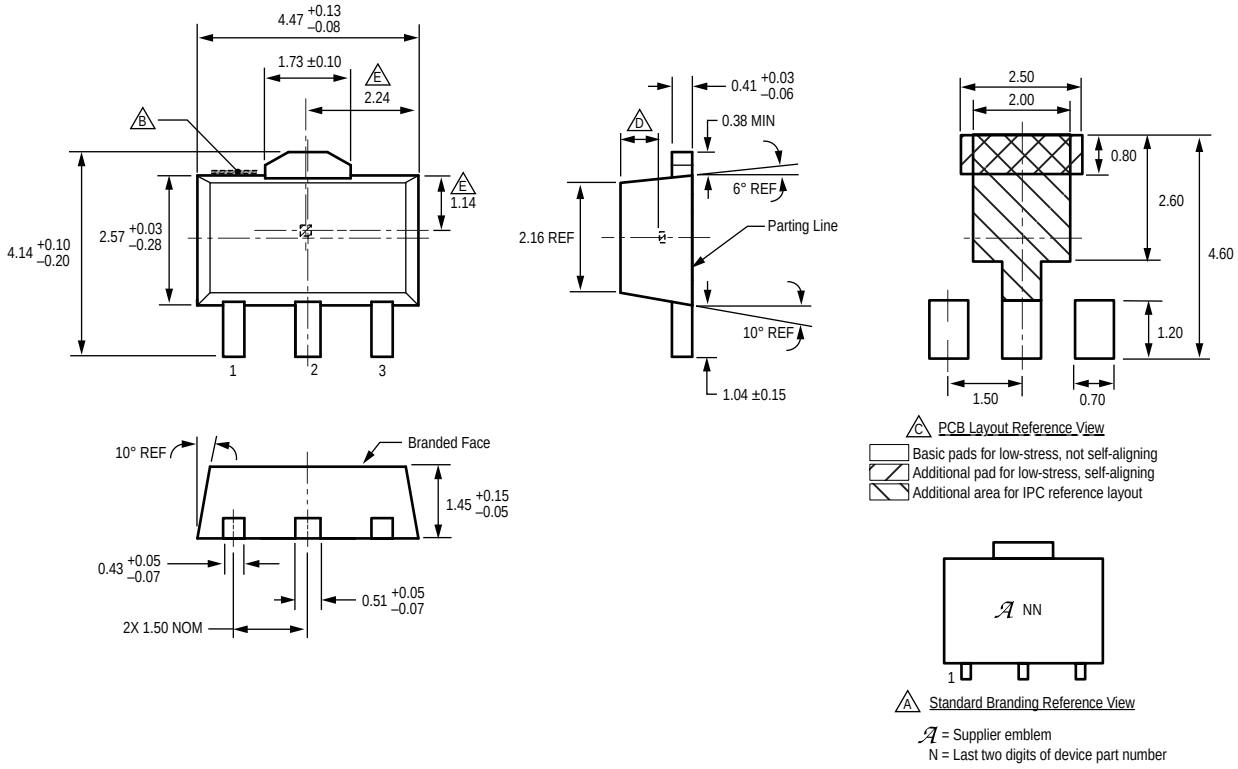


Figure 4. Chopper stabilization technique

Package LT 3-Pin SOT-89



Updated package drawing only. Allegro package assembly tooling has not changed.
For Reference Only; not for tooling use (reference DWG-9064)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Branding scale and appearance at supplier discretion

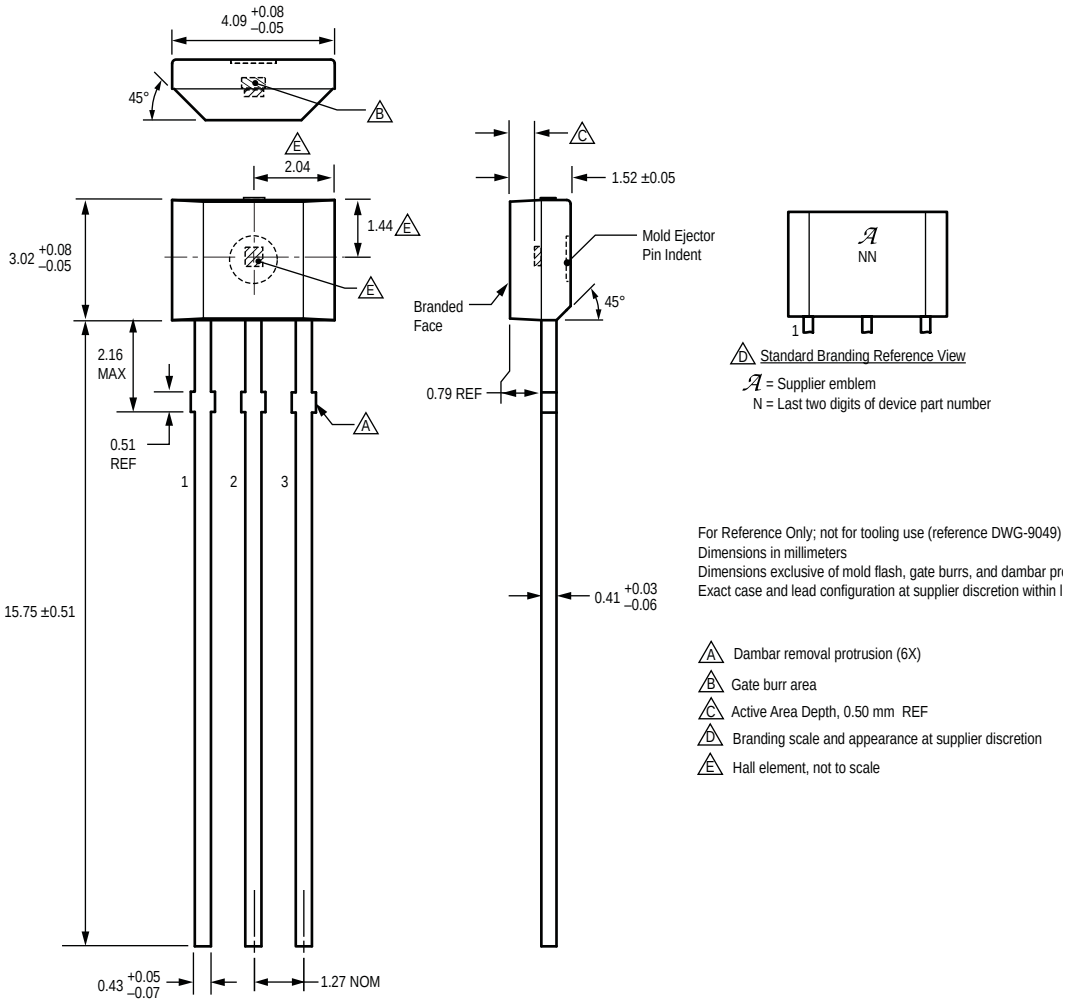
B Gate and tie bar burr area

C Reference land pattern layout;
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

D Active Area Depth, 0.77 mm

E Hall element; not to scale

Package UA 3-Pin SIP



Revision History

Revision	Revision Date	Description of Revision
Rev. 2	May 8, 2013	Update product offerings, editorial correction to $I_{Z(sup)}$

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www.allegromicro.com