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August 2014

FDPC4044

Common Drain N-Channel PowerTrench® MOSFET

30 V, 27 A, 4.3 mΩ

Features

- Max $r_{S1S2(on)} = 4.3 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_{S1S2} = 27 \text{ A}$
- Max $r_{S1S2(on)} = 6.4 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_{S1S2} = 23 \text{ A}$
- Pakage size/height: 3.3 x 3.3 x 0.8 mm
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- RoHS Compliant

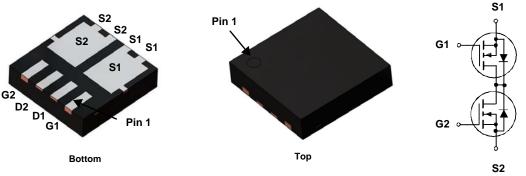


General Description

This device is designed specifically as a single package solution for Li-lon battery pack protection circuit and other ultra-portable applications. It features two common drain N-channel MOSFETs, which enables bidirectional current flow. FDPC4044 combines Fairchild's advanced PowerTrench® process with state of the art packaging process to minimize the on-state resistance.

Applications

- Battery management
- Load switch
- Battery protection



Power Clip 33

MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units		
V _{S1S2}	Source1 to Source2 Voltage	30	V		
V_{GS}	Gate to Source Voltage	±20	V		
I _{S1S2}	Source1 to Source2 Current -Continuous TA:	= 25 °C (Note 1a)	27	^	
	-Pulsed (Note 2)		120	A	
В	Power Dissipation T _A =	= 25 °C (Note 1a)	2.7	W	
P_{D}	Power Dissipation $T_A = 25 ^{\circ}\text{C}$ (Note 1b)		1	T VV	
T _J , T _{STG}	Operating and Storage Junction Temperature Ra	-55 to +150	°C		

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	47	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	127	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
40CF	FDPC4044	Power Clip 33	13 "	12 mm	3000 units

Units

Max

Electrical Characteristics T_J = 25 °C unless otherwise noted

Parameter

			71		
Off Chara	cteristics				
I _{S1S2}	Zero Gate Voltage Source1 to Source2 Current	V _{S1S2} = 24 V, V _{GS} = 0 V		1	μА
I _{GSS}	Gate to Source Leakage Current	V _{GS} = 20 V, V _{S1S2} = 0 V		100	nA

Test Conditions

On Characteristics

Symbol

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{S1S2}, I_{S1S2} = 250 \mu A$	1.2	1.5	3	V
1	V _{GS} =10 V, I _{S1S2} = 27 A		3.2	4.3		
r	Static Source1 to Source2 On Resistance	V _{GS} = 4.5 V, I _{S1S2} = 23 A		4.6	6.4	mΩ
r _{S1S2(on)}	Static Course 1 to Gource 2 of Tresistance	$V_{GS} = 10 \text{ V}, I_{S1S2} = 27 \text{ A},$ $T_{J} = 125 {}^{\circ}\text{C}$		4.5	7	11122
9 _{FS}	Forward Transconductance	V _{S1S2} = 10 V, I _{S1S2} = 27 A		150		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 45 V V 6 V	2295	3215	pF
C _{oss}	Output Capacitance	V _{S1S2} = 15 V, V _{GS} = 0 V, f = 1 MHz	627	880	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12	66	95	pF

Switching Characteristics

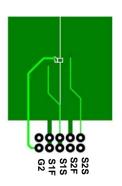
t _{d(on)}	Turn-On Delay Time		8.5	17	ns
t _r	Rise Time	V _{S1S2} = 15 V, I _{S1S2} = 27 A,	4.8	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	32	52	ns
t _f	Fall Time		5.2	10	ns
Q_g	Total Gate Charge	V 45.V.I 07.A	35	49	nC
Q_{gs}	Gate to Source1 Gate Charge	$V_{S1S2} = 15 \text{ V}, I_{S1S2} = 27 \text{ A},$ $V_{G1S1} = 10 \text{ V}, V_{G2S2} = 0 \text{ V}$	5.7		nC
Q_{gd}	Gate to Source2 "Miller" Charge	VG1S1 - 10 V, VG2S2 - 0 V	4.7		nC

Source1 to Source2 Diode Characteristics

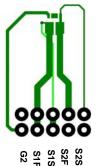
I _{fss}	Maximum Continuous Source1 to Source2 Diode Forward Current			1	Α
V		$V_{G1S1} = 0 \text{ V}, V_{G2S2} = 4.5 \text{ V},$	0.8	12	V
V _{fss}	Voltage	$I_{fss} = 27 \text{ A}$ (Note 2)	0.0	1.2	•

Notes:

^{1.} R_{0,JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0,JC} is guaranteed by design while R_{0,CA} is determined by the user's board design.



a. 47 °C/W when mounted on a 1 in² pad of 2 oz copper.



b.127 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 us, Duty cycle < 2.0%.
- 3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

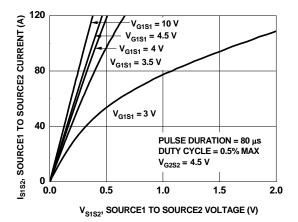


Figure 1. On-Region Characteristics

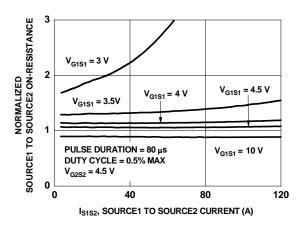


Figure 3. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

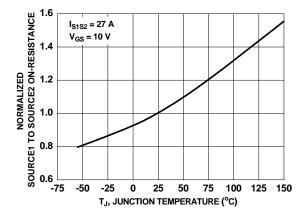


Figure 5. Normalized On-Resistance vs Junction Temperature

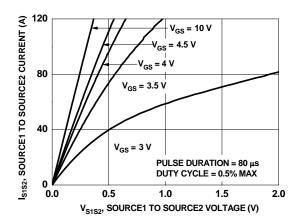


Figure 2. On-Region Characteristics

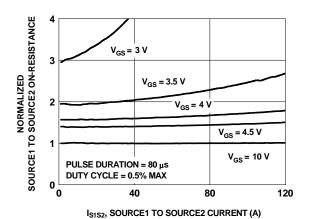


Figure 4. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

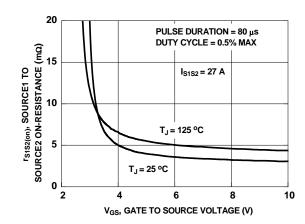


Figure 6. On-Resistance vs Gate to Source Voltage

Typical Characteristics $T_J = 25$ °C unless otherwise noted

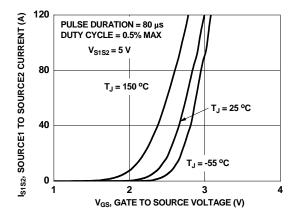


Figure 7. Transfer Characteristics

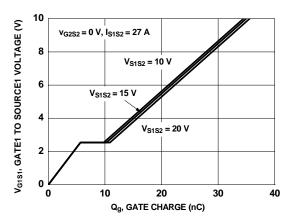


Figure 9. Gate Charge Characteristics

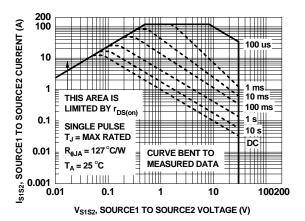


Figure 11. Forward Bias Safe Operating Area

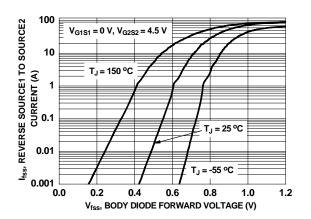


Figure 8. Source1 to Source2 Diode Forward Voltage vs Source Current

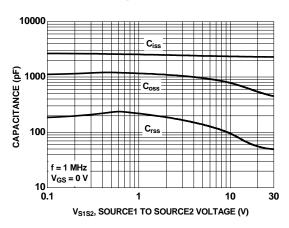


Figure 10. Capacitance vs Source1 to Source2 Voltage

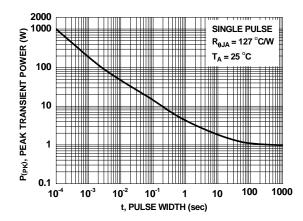


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

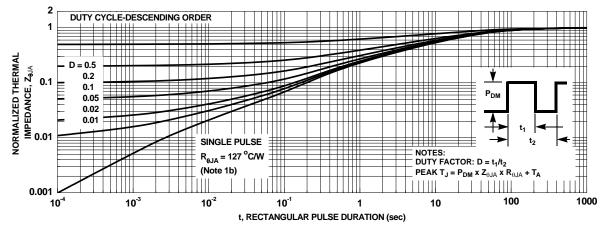
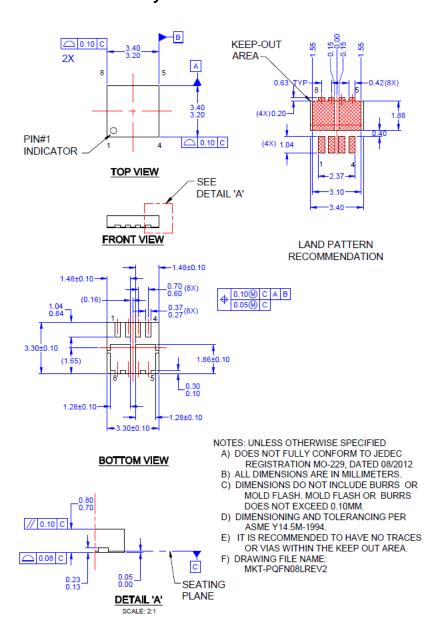


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



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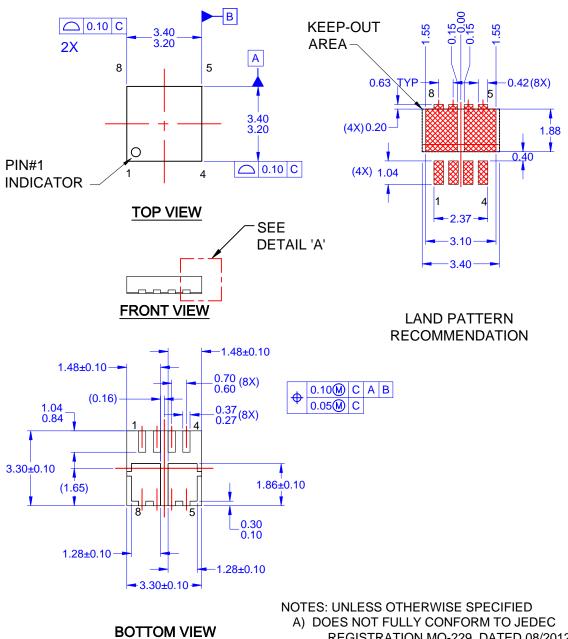
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Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 171



0.80 // 0.10 C △ 0.08 C С 0.05 0.23 0.13 **SEATING PLANE DETAIL 'A'** SCALE: 2:1

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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F) DRAWING FILE NAME: MKT-PQFN08LREV2

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