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April 2015

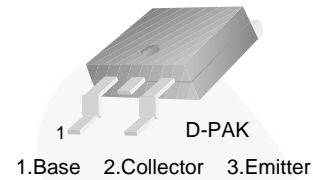


MJD44H11 — NPN Epitaxial Silicon Transistor

MJD44H11 NPN Epitaxial Silicon Transistor

Features

- General-Purpose Power and Switching such as Output or Driver Stages in Applications
- D-PAK for Surface-Mount Applications
- Lead-Formed for Surface Mount Application (No Suffix)
- Fast Switching Speeds
- Low Collector Emitter Saturation Voltage



Ordering Information

Part Number	Top Mark	Package	Packing Method
MJD44H11TF	MJD44H11	TO-252 3L (DPAK)	Tape and Reel
MJD44H11TM	MJD44H11	TO-252 3L (DPAK)	Tape and Reel

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter Voltage	80	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current (DC)	8	A
I_{CP}	Collector Current (Pulse)	16	A
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	- 65 to +150	$^\circ\text{C}$

Thermal Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Max.	Unit
P_D	Total Device Dissipation	$T_C = 25^\circ\text{C}$	20
		$T_A = 25^\circ\text{C}$	1.75
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	6.25	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	71.4	$^\circ\text{C/W}$

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage ⁽¹⁾	$I_C = 30\text{ mA}, I_B = 0$	80			V
I_{CEO}	Collector Cut-Off Current	$V_{CE} = 80\text{ V}, I_B = 0$			10	μA
I_{EBO}	Emitter Cut-Off Current	$V_{EB} = 5\text{ V}, I_C = 0$			50	μA
h_{FE}	DC Current Gain ⁽¹⁾	$V_{CE} = 1\text{ V}, I_C = 2\text{ A}$	60			
		$V_{CE} = 1\text{ V}, I_C = 4\text{ A}$	40			
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage ⁽¹⁾	$I_C = 8\text{ A}, I_B = 0.4\text{ A}$			1	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage ⁽¹⁾	$I_C = 8\text{ A}, I_B = 0.8\text{ A}$			1.5	V
f_T	Current Gain Bandwidth Product	$V_{CE} = 10\text{ V}, I_C = 0.5\text{ A}$		50		MHz
C_{ob}	Output Capacitance	$V_{CB} = 10\text{ V}, f = 1\text{ MHz}$		130		pF
t_{ON}	Turn-On Time	$I_C = 5\text{ A},$ $I_{B1} = - I_{B2} = 0.5\text{ A}$		300		ns
t_{STG}	Storage Time			500		ns
t_F	Fall Time			140		ns

Note:

1. Pulse test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Performance Characteristics

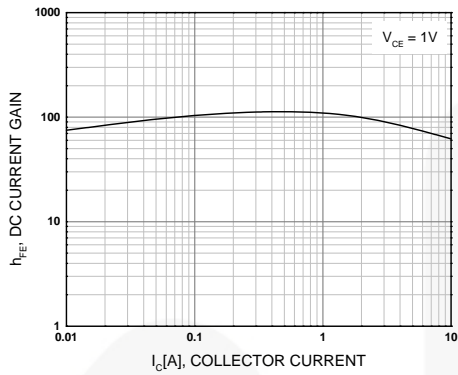


Figure 1. DC Current Gain

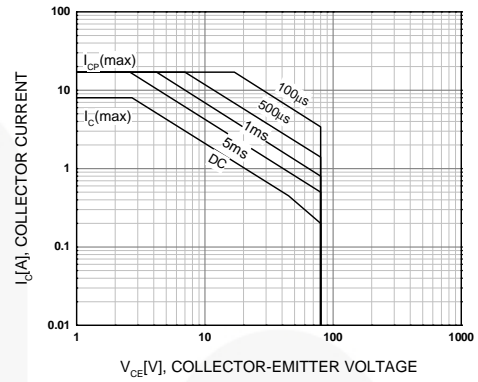


Figure 2. Safe Operating Area

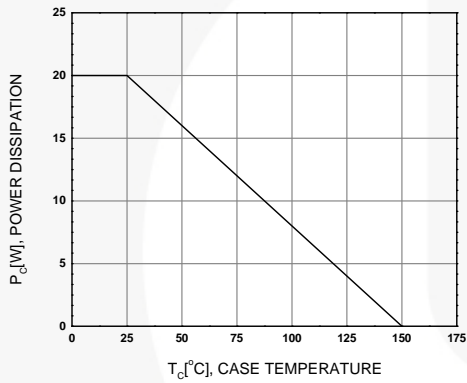
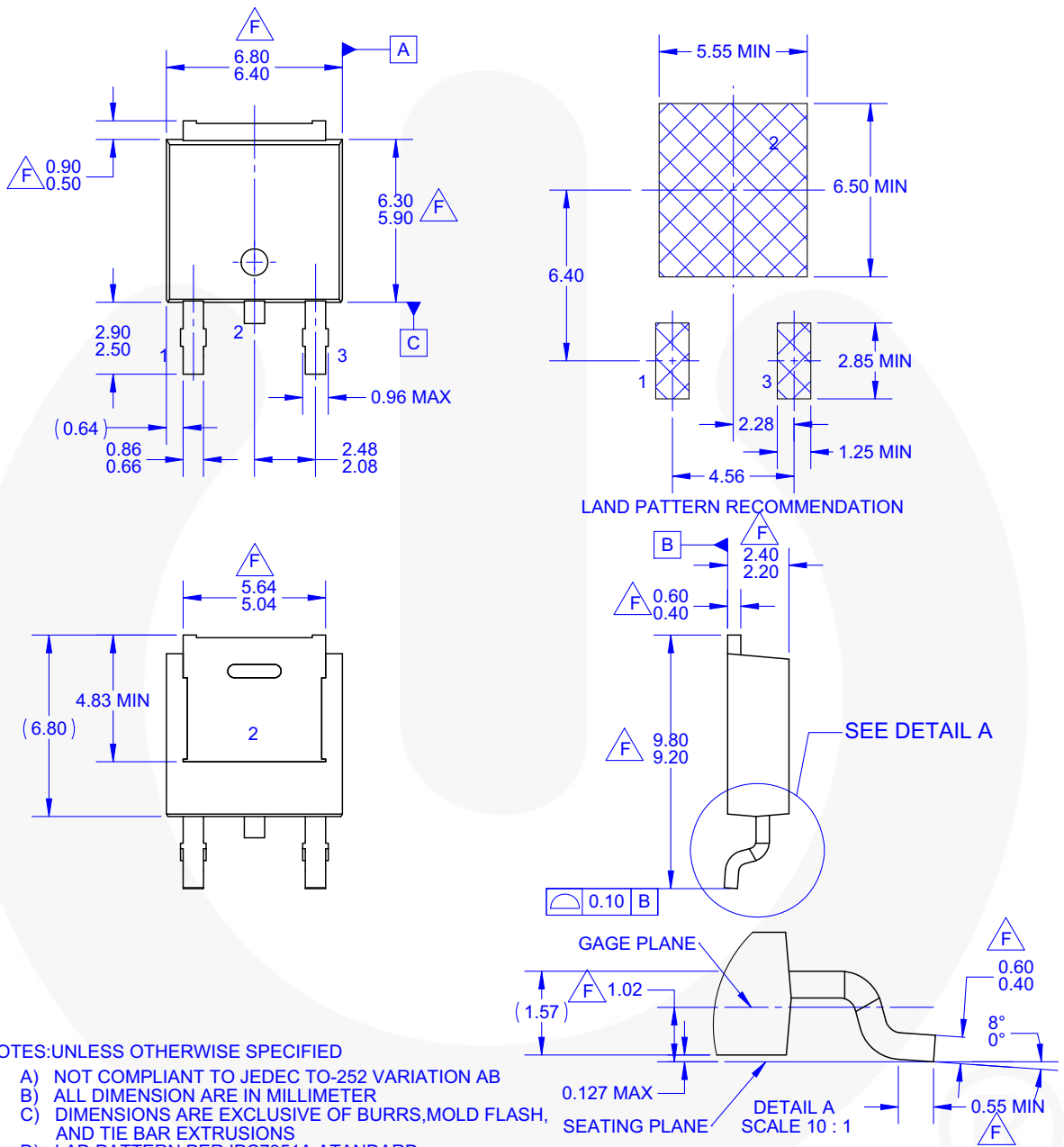


Figure 3. Power Derating

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) NOT COMPLIANT TO JEDEC TO-252 VARIATION AB
- B) ALL DIMENSION ARE IN MILLIMETER
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D) LAD PATTERN PER IPC7351A ATANDARD TO228P991X239-3N
- E) DRAWING FILE NAME: MKT-TO252D03REV3.
- F) DOES NOT COMPLY JEDEC STANDARD VALUE.
- G) FAIRCHILD SEMICONDUCTOR.

Figure 4. 3-LEAD, TO-252, NOT COMPLIANT TO JEDEC TO-252 VAR. AB, SURFACE MOUNT (DPAK)



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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