Quad-Channel, 12-Bit, Serial Input, 4 mA to 20 mA and Voltage Output DAC with Dynamic Power Control

Data Sheet **AD5735**

FEATURES

- **12-bit resolution and monotonicity**
- **Dynamic power control for thermal management**
- **Current and voltage output pins connectable to a single terminal**
- **Current output ranges: 0 mA to 20 mA, 4 mA to 20 mA, and 0 mA to 24 mA**
  - **±0.1% total unadjusted error (TUE) maximum**
- **Voltage output ranges (with 20% overrange): 0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V**
  - **±0.09% total unadjusted error (TUE) maximum**
- **User-programmable offset and gain**
- **On-chip diagnostics**
- **On-chip reference: ±10 ppm/°C maximum**
- **–40°C to +105°C temperature range**

APPLICATIONS

- **Process control**
- **Actuator control**
- **PLCs**

GENERAL DESCRIPTION

The AD5735 is a quad-channel voltage and current output DAC that operates with a power supply range from −26.4 V to +33 V.

On-chip dynamic power control minimizes package power dissipation in current mode. This reduced power dissipation is achieved by regulating the voltage on the output driver from 7.4 V to 29.5 V using a dc-to-dc boost converter optimized for minimum on-chip power dissipation.

The AD5735 uses a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with standard SPI, QSPI™, MICROWIRE®, DSP, and microcontroller interface standards. The serial interface also features optional CRC-8 packet error checking, as well as a watchdog timer that monitors activity on the interface.

PRODUCT HIGHLIGHTS

1. Dynamic power control for thermal management.
2. 12-bit performance.
3. Quad channel.

COMPANION PRODUCTS

Product Family: AD5755, AD5755-1, AD5757, AD5737
External References: ADR445, ADR02
Digital Isolators: ADuM1410, ADuM1411
Power: ADP2302, ADP2303
Additional companion products on the AD5735 product page

FUNCTIONAL BLOCK DIAGRAM

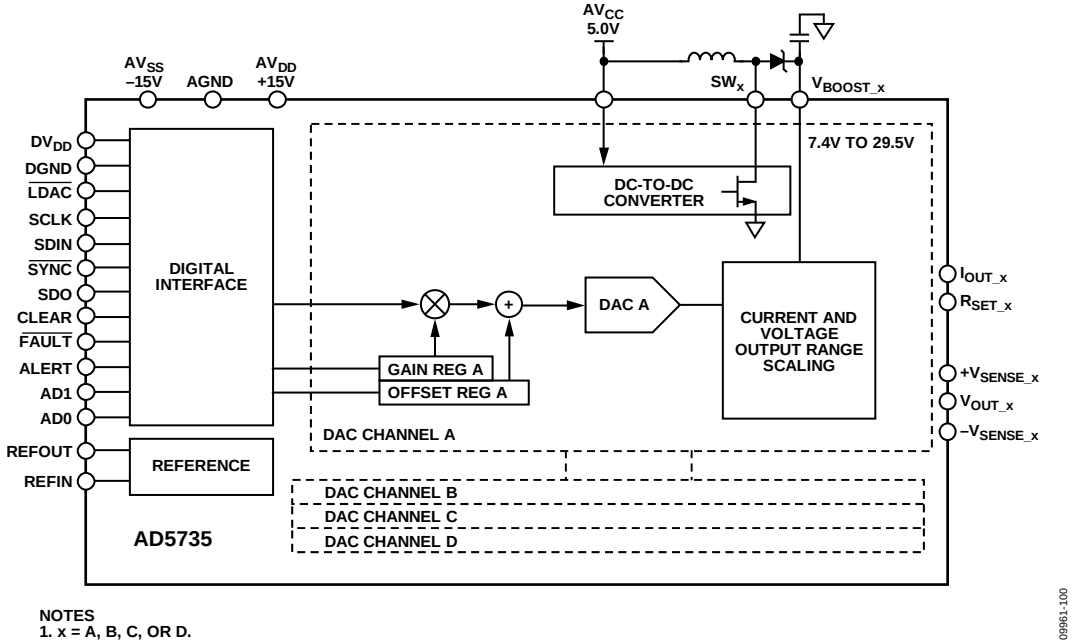

Figure 1.

Rev. D **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD5735* Product Page Quick Links

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Comparable Parts

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Evaluation Kits

- AD5755 Evaluation Board

Documentation

Application Notes

- AN-1289: Using the AD5755 and Similar Dynamic Power Control DACs in Applications Without Dynamic Power Control

Data Sheet

- AD5735: Quad-Channel, 12-Bit, Serial Input, 4 mA to 20 mA and Voltage Output DAC with Dynamic Power Control Data Sheet

Software and Systems Requirements

- AD5755 IIO Multi-Channel DAC Linux Driver

Reference Materials

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

Design Resources

- AD5735 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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Changes to Power-On State of the AD5735 Section 29
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7/11—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

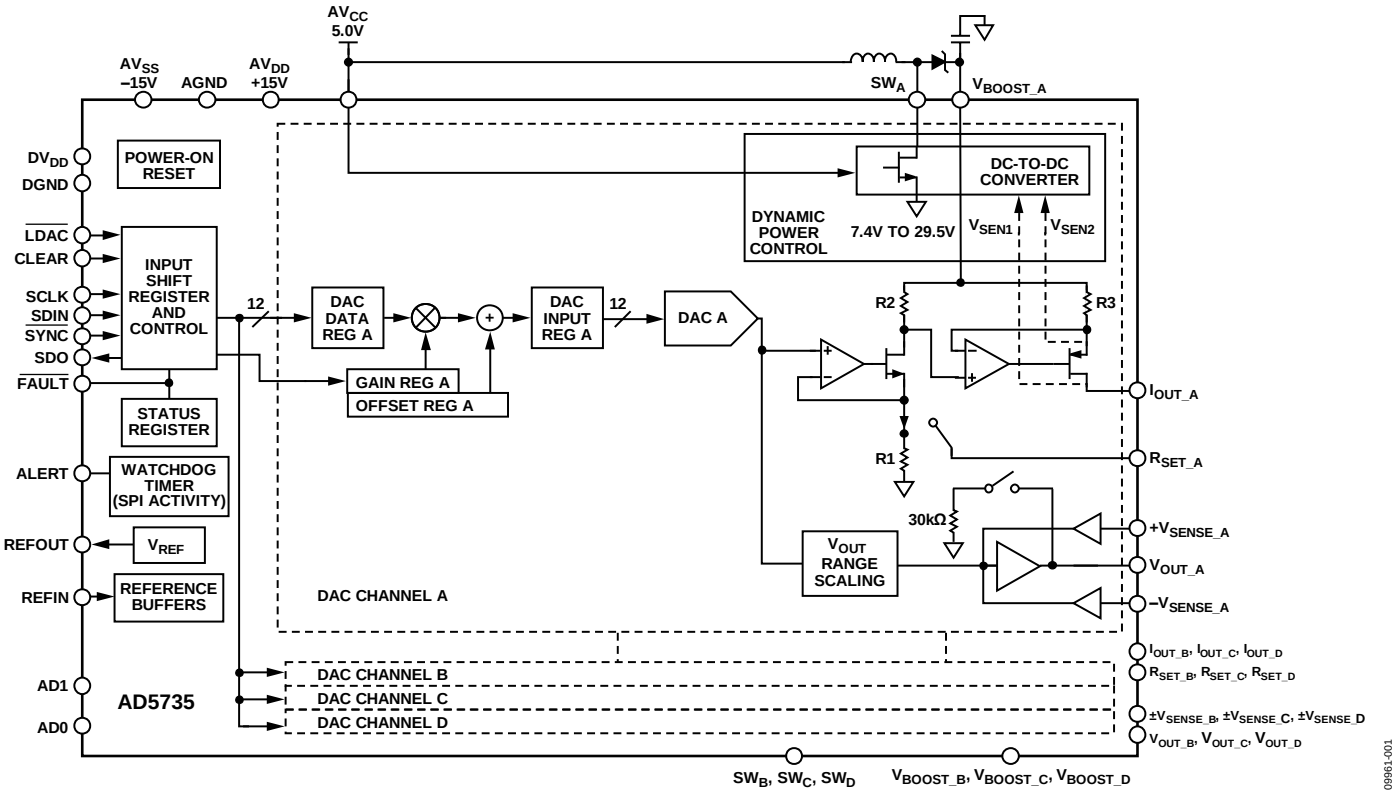


Figure 2.

SPECIFICATIONS

AV_{DD} = V_{BOOST_x} = 15 V; AV_{SS} = −15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; voltage outputs: R_L = 1 kΩ, C_L = 220 pF; current outputs: R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					
Output Voltage Ranges	0		5	V	
	0		10	V	
	−5		+5	V	
	−10		+10	V	
	0		6	V	
	0		12	V	
	−6		+6	V	
	−12		+12	V	
Resolution	12			Bits	
ACCURACY, VOLTAGE OUTPUT					
Total Unadjusted Error (TUE)	−0.09	±0.012	+0.09	% FSR	0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V ranges
	−0.13	±0.05	+0.13	% FSR	On overranges (0 V to 6 V, 0 V to 12 V, ±6 V, ±12 V)
TUE Long-Term Stability		35		ppm FSR	Drift after 1000 hours, T_J = 150°C
Relative Accuracy (INL)	−0.032	±0.006	+0.032	% FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.05	±0.004	+0.05	% FSR	0 V to 5 V, 0 V to 10 V ranges
	−0.08	±0.004	+0.08	% FSR	On overranges (0 V to 6 V, 0 V to 12 V)
Zero-Scale TC[2]		±2		ppm FSR/°C	
Bipolar Zero Error	−0.05	±0.003	+0.05	% FSR	±5 V, ±10 V ranges
	−0.08	±0.03	+0.08	% FSR	On overranges (±6 V, ±12 V)
Bipolar Zero TC[2]		±2		ppm FSR/°C	
Offset Error	−0.065	±0.005	+0.065	% FSR	0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V ranges
	−0.09	±0.03	+0.09	% FSR	On overranges (0 V to 6 V, 0 V to 12 V, ±6 V, ±12 V)
Offset TC[2]		±2		ppm FSR/°C	
Gain Error	−0.08	±0.004	+0.08	% FSR	0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V ranges
	−0.15	±0.004	+0.15	% FSR	On overranges (0 V to 6 V, 0 V to 12 V, ±6 V, ±12 V)
Gain TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.09	±0.01	+0.09	% FSR	0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V ranges
	−0.13	±0.05	+0.13	% FSR	On overranges (0 V to 6 V, 0 V to 12 V, ±6 V, ±12 V)
Full-Scale TC[2]		±2		ppm FSR/°C	
OUTPUT CHARACTERISTICS, VOLTAGE OUTPUT[2]					
Headroom		1	2.2	V	With respect to V_{BOOST} supply
Footroom		1	1.4	V	With respect to the AV_{SS} supply
Output Voltage Drift vs. Time		20		ppm FSR	Drift after 1000 hours, ¾ scale output, T_J = 150°C, AV_{SS} = −15 V
Short-Circuit Current	12/6	16/8		mA	Programmable by user; defaults to 16 mA typical
Resistive Load	1			kΩ	For specified performance
Capacitive Load Stability			10	nF	
			2	µF	External 220 pF compensation capacitor connected
DC Output Impedance		0.06		Ω	
DC PSRR		50		µV/V	
DC Crosstalk		24		µV	
CURRENT OUTPUT					
Output Current Ranges	0		24	mA	
	0		20	mA	
	4		20	mA	
Resolution	12			Bits	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY, CURRENT OUTPUT (EXTERNAL R_{SET})					Assumes ideal resistor, see External Current Setting Resistor section for more information.
Total Unadjusted Error (TUE)	−0.1	±0.019	+0.1	% FSR	
TUE Long-Term Stability		100		ppm FSR	Drift after 1000 hours, T_J = 150°C
Relative Accuracy (INL)	−0.032	±0.006	+0.032	% FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.1	±0.012	+0.1	% FSR	
Offset Error Drift[2]		±4		ppm FSR/°C	
Gain Error	−0.1	±0.004	+0.1	% FSR	
Gain TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.1	±0.014	+0.1	% FSR	
Full-Scale TC[2]		±5		ppm FSR/°C	
DC Crosstalk		0.0005		% FSR	External R_{SET}
ACCURACY, CURRENT OUTPUT (INTERNAL R_{SET})					
Total Unadjusted Error (TUE)[3, 4]	−0.14	±0.022	+0.14	% FSR	
TUE Long-Term Stability		180		ppm FSR	Drift after 1000 hours, T_J = 150°C
Relative Accuracy (INL)	−0.032	±0.006	+0.032	% FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error[3, 4]	−0.1	±0.017	+0.1	% FSR	
Offset Error Drift[2]		±6		ppm FSR/°C	
Gain Error	−0.12	±0.004	+0.12	% FSR	
Gain TC[2]		±9		ppm FSR/°C	
Full-Scale Error[3, 4]	−0.14	±0.02	+0.14	% FSR	
Full-Scale TC[2]		±14		ppm FSR/°C	
DC Crosstalk[4]		−0.011		% FSR	Internal R_{SET}
OUTPUT CHARACTERISTICS, CURRENT OUTPUT[2]					
Current Loop Compliance Voltage		V_{BOOST_x} − 2.4	V_{BOOST_x} − 2.7	V	
Output Current Drift vs. Time					Drift after 1000 hours, ¾ scale output, T_J = 150°C
		90		ppm FSR	External R_{SET}
		140		ppm FSR	Internal R_{SET}
Resistive Load			1000	Ω	The dc-to-dc converter has been characterized with a maximum load of 1 kΩ, chosen such that compliance is not exceeded; see Figure 52 and the DC-DC MaxV bits in Table 28
DC Output Impedance		100		MΩ	
DC PSRR		0.02	1	µA/V	
REFERENCE INPUT/OUTPUT					
Reference Input[2]					
Reference Input Voltage	4.95	5	5.05	V	For specified performance
DC Input Impedance	45	150		MΩ	
Reference Output					
Output Voltage	4.995	5	5.005	V	T_A = 25°C
Reference TC[2]	−10	±5	+10	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[2]		7		µV p-p	
Noise Spectral Density[2]		100		nV/√Hz	At 10 kHz
Output Voltage Drift vs. Time[2]		180		ppm	Drift after 1000 hours, T_J = 150°C
Capacitive Load[2]		1000		nF	
Load Current		9		mA	See Figure 63
Short-Circuit Current		10		mA	
Line Regulation[2]		3		ppm/V	See Figure 64
Load Regulation[2]		95		ppm/mA	See Figure 63
Thermal Hysteresis[2]		200		ppm	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER					
Switch					
Switch On Resistance		0.425		Ω	
Switch Leakage Current		10		nA	
Peak Current Limit		0.8		A	
Oscillator					
Oscillator Frequency	11.5	13	14.5	MHz	This oscillator is divided down to provide the dc-to-dc converter switching frequency
Maximum Duty Cycle		89.6		%	At 410 kHz dc-to-dc switching frequency
DIGITAL INPUTS[2]					JEDEC compliant
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current	−1		+1	µA	Per pin
Pin Capacitance		2.6		pF	Per pin
DIGITAL OUTPUTS[2]					
SDO, ALERT Pins					
Output Low Voltage, V_{OL}			0.4	V	Sinking 200 µA
Output High Voltage, V_{OH}	DV_{DD} − 0.5			V	Sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance		2.5		pF	
$\overline{\text{FAULT}}$ Pin					
Output Low Voltage, V_{OL}			0.4	V	10 kΩ pull-up resistor to DV_{DD}
		0.6		V	At 2.5 mA
Output High Voltage, V_{OH}	3.6			V	10 kΩ pull-up resistor to DV_{DD}
POWER REQUIREMENTS					
AV_{DD}	9		33	V	
AV_{SS}	−26.4		−10.8	V	
DV_{DD}	2.7		5.5	V	
AV_{CC}	4.5		5.5	V	
AI_{DD}		8.6	10.5	mA	Voltage output mode on all channels, outputs unloaded, over supplies
		7	7.5	mA	Current output mode on all channels
AI_{SS}	−11	−8.8		mA	Voltage output mode on all channels, outputs unloaded, over supplies
	−1.7			mA	Current output mode on all channels
DI_{CC}		9.2	11	mA	$V_{IH} = DV_{DD}$, V_{IL} = DGND, internal oscillator running, over supplies
AI_{CC}			1	mA	Outputs unloaded, over supplies
I_{BOOST}[5]			2.7	mA	Per channel, voltage output mode, outputs unloaded, over supplies
			1	mA	Per channel, current output mode
Power Dissipation		173		mW	AV_{DD} = 15 V, AV_{SS} = −15 V, dc-to-dc converter enabled, current output mode, outputs disabled

[1] Temperature range: −40°C to +105°C; typical at +25°C.
[2] Guaranteed by design and characterization; not production tested.
[3] For current outputs with internal R_{SET}, the offset, full-scale, and TUE measurements exclude dc crosstalk. The measurements are made with all four channels enabled and loaded with the same code.
[4] See the Current Output Mode with Internal R_{SET} section for more information about dc crosstalk.
[5] Efficiency plots in Figure 54 through Figure 57 include the I_{BOOST} quiescent current.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = V_{BOOST_x} = 15 V; AV_{SS} = −15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; voltage outputs: R_L = 2 kΩ, C_L = 220 pF; current outputs: R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE, VOLTAGE OUTPUT					
Output Voltage Settling Time		11		µs	5 V step to ±0.03% FSR, 0 V to 5 V range
			18	µs	10 V step to ±0.03% FSR, 0 V to 10 V range
Slew Rate		1.9		V/µs	0 V to 10 V range
Power-On Glitch Energy		150		nV-sec	
Digital-to-Analog Glitch Energy		6		nV-sec	
Glitch Impulse Peak Amplitude		25		mV	
Digital Feedthrough		1		nV-sec	
DAC-to-DAC Crosstalk		2		nV-sec	0 V to 10 V range
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.01		LSB p-p	12-bit LSB, 0 V to 10 V range
Output Noise Spectral Density		150		nV/√Hz	Measured at 10 kHz, midscale output, 0 V to 10 V range
AC PSRR		83		dB	200 mV, 50 Hz/60 Hz sine wave superimposed on power supply voltage
DYNAMIC PERFORMANCE, CURRENT OUTPUT					
Output Current Settling Time		15		µs	To 0.1% FSR, 0 mA to 24 mA range
		See Test Conditions/Comments		ms	For settling times when using the dc-to-dc converter, see Figure 48, Figure 49, and Figure 50
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.01		LSB p-p	12-bit LSB, 0 mA to 24 mA range
Output Noise Spectral Density		0.5		nA/√Hz	Measured at 10 kHz, midscale output, 0 mA to 24 mA range

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

AV_{DD} = V_{BOOST_x} = 15 V; AV_{SS} = −15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; voltage outputs: R_L = 1 kΩ, C_L = 220 pF; current outputs: R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	13	ns min	24th/32nd SCLK falling edge to $\overline{SYNC}$ rising edge (see Figure 77)
t_6	198	ns min	$\overline{SYNC}$ high time after a configuration write
	5	µs min	$\overline{SYNC}$ high time after a DAC update write
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	20	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (applies to any channel that has digital slew rate control enabled; single DAC updated)
	5	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DAC updated)
t_{10}	10	ns min	$\overline{LDAC}$ pulse width low
t_{11}	500	ns max	$\overline{LDAC}$ falling edge to DAC output response time
t_{12}	See Table 2	µs max	DAC output settling time
t_{13}	10	ns min	CLEAR high time
t_{14}	5	µs max	CLEAR activation time
t_{15}	40	ns max	SCLK rising edge to SDO valid
t_{16}	5	µs min	$\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$ = 0) (Single DAC updated)
t_{17}	500	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge
t_{18}	800	ns min	$\overline{RESET}$ pulse width
t_{19}			$\overline{SYNC}$ high to next $\overline{SYNC}$ low (Single DAC updated)
	20	µs min	Digital slew rate control enabled
	5	µs min	Digital slew rate control disabled

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with t_{RISE} = t_{FALL} = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.2 V.
[3] See Figure 3, Figure 4, Figure 6, and Figure 7.

Timing Diagrams

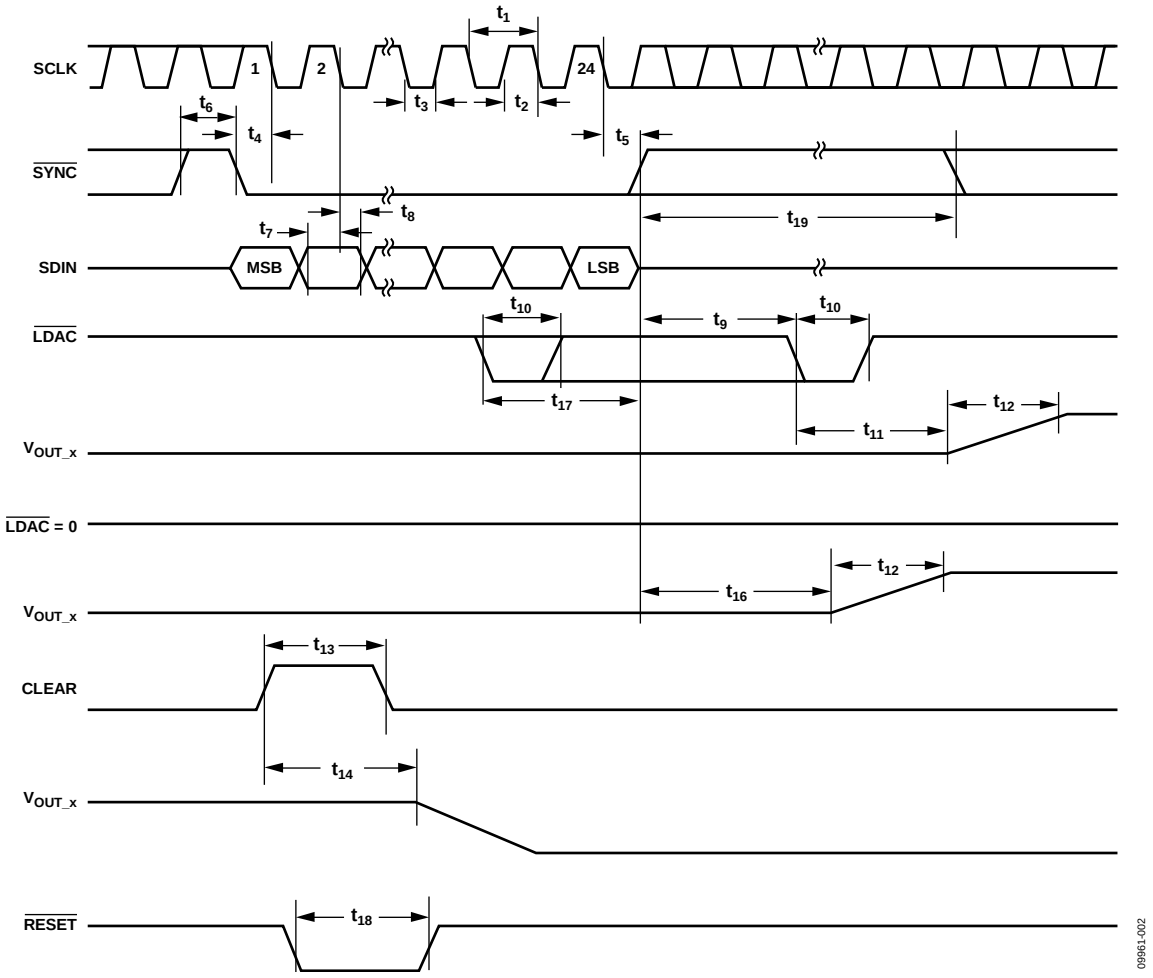
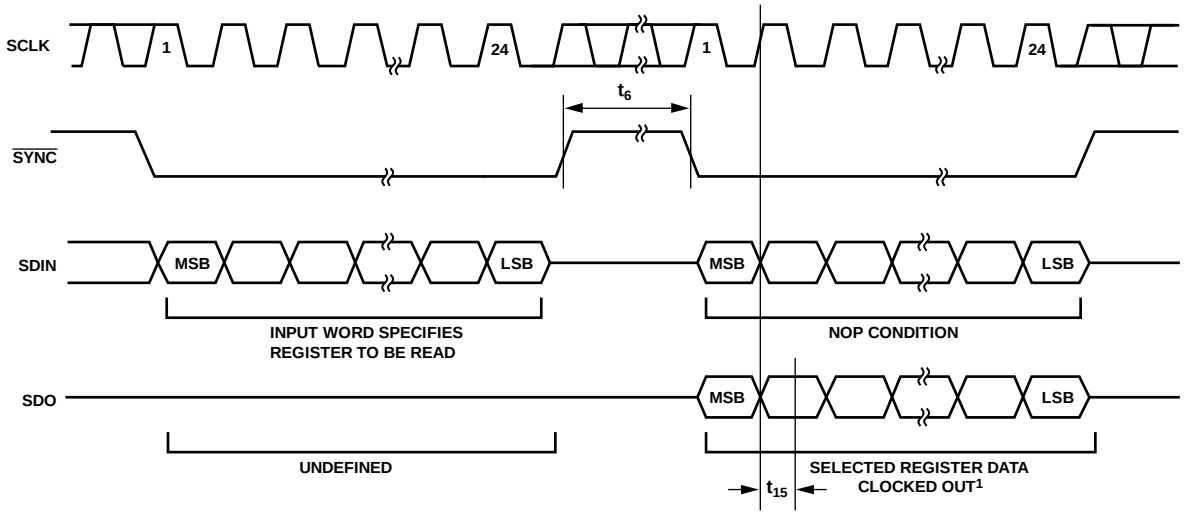
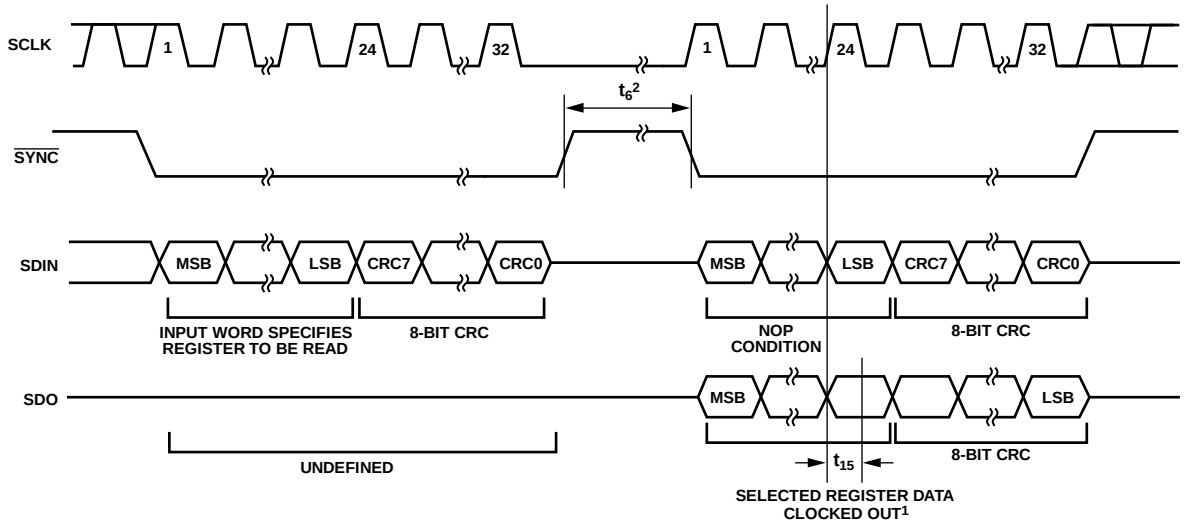


Figure 3. Serial Interface Timing Diagram



[1]IF FIRST SCLK IS NEGATIVE EDGE WITHIN $\overline{SYNC}$ FRAME OF NOP CONDITION, 7 DONT CARE BITS + 16 DATA BITS CLOCKED OUT (TOTAL 23 BITS). IF FIRST SCLK IS POSITIVE EDGE WITHIN $\overline{SYNC}$ FRAME OF NOP CONDITION, 8 DONT CARE BITS + 16 DATA BITS CLOCKED OUT (TOTAL 24 BITS). SEE THE READBACK OPERATION SECTION FOR FURTHER INFORMATION.

Figure 4. Readback Timing Diagram (Packet Error Checking Disabled)



[1]IF FIRST SCLK IS NEGATIVE EDGE WITHIN $\overline{SYNC}$ FRAME OF NOP CONDITION, 7 DONT CARE BITS + 16 DATA BITS CLOCKED OUT + 8 CRC BITS (TOTAL 31 BITS).
IF FIRST SCLK IS POSITIVE EDGE WITHIN $\overline{SYNC}$ FRAME OF NOP CONDITION, 8 DONT CARE BITS + 16 DATA BITS CLOCKED OUT + 8 CRC BITS (TOTAL 32 BITS).
[2]AVOID SCLK ACTIVITY DURING t_6 AS IT MAY RESULT IN A PEC ERROR ON READBACK.
SEE THE READBACK OPERATION AND PACKET ERROR CHECKING SECTIONS FOR FURTHER INFORMATION.

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Figure 5. Readback Timing Diagram (Packet Error Checking Enabled)

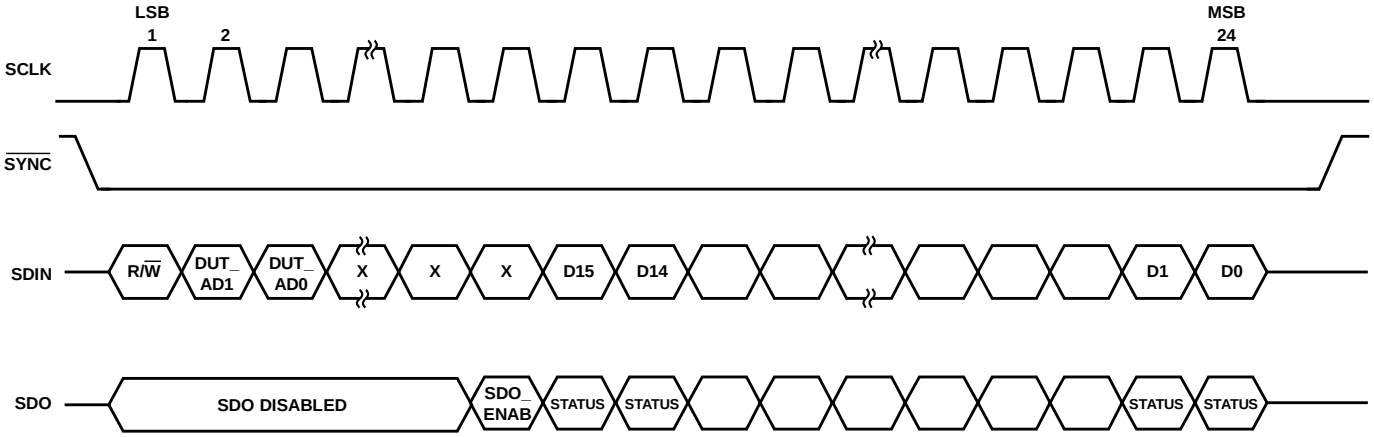

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Figure 6. Status Readback During Write, Timing Diagram

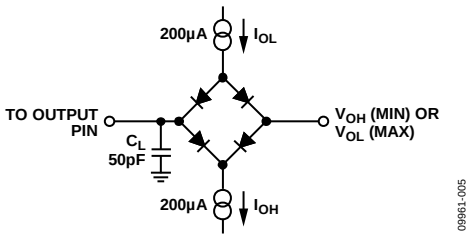

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Figure 7. Load Circuit for SDO Timing Diagrams

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
AV_{DD}, V_{BOOST_x} to AGND, DGND	−0.3 V to +33 V
AV_{SS} to AGND, DGND	+0.3 V to −28 V
AV_{DD} to AV_{SS}	−0.3 V to +60 V
AV_{CC} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{DD} + 0.3 V or +7 V (whichever is less)
Digital Outputs to DGND	−0.3 V to DV_{DD} + 0.3 V or +7 V (whichever is less)
REFIN, REFOUT to AGND	−0.3 V to AV_{DD} + 0.3 V or +7 V (whichever is less)
V_{OUT_x} to AGND	AV_{SS} to V_{BOOST_x} or 33 V if using the dc-to-dc converter
$+V_{SENSE\_x}$, $-V_{SENSE\_x}$ to AGND	AV_{SS} to V_{BOOST_x} or 33 V if using the dc-to-dc converter
I_{OUT_x} to AGND	AV_{SS} to V_{BOOST_x} or 33 V if using the dc-to-dc converter
SW_x to AGND	−0.3 V to +33 V
AGND, $GNDSW_x$ to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial[1]	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

[1] Power dissipated on chip must be derated to keep the junction temperature below 125°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Junction-to-air thermal resistance (θ_{JA}) is specified for a JEDEC 4-layer test board.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
64-Lead LFCSP (CP-64-3)	28	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

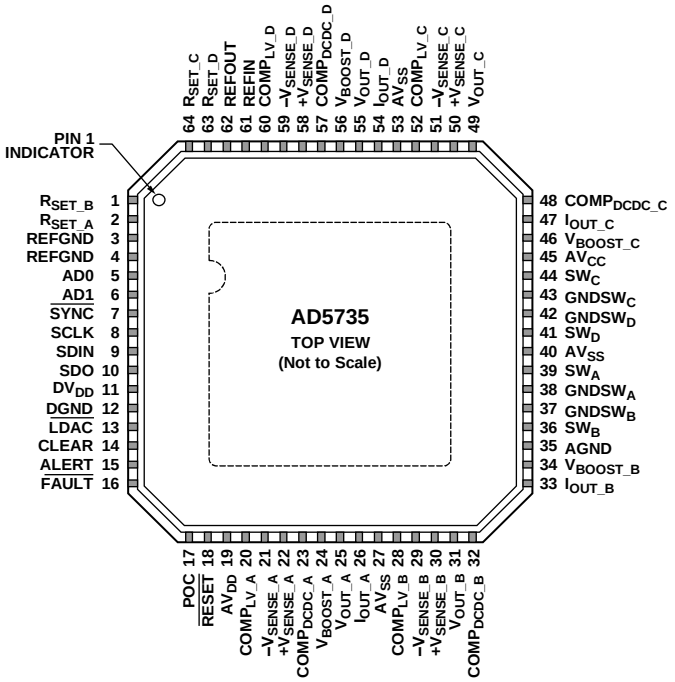


Figure 8. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{SET_B}	An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_B} temperature drift performance. For more information, see the External Current Setting Resistor section.
2	R_{SET_A}	An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_A} temperature drift performance. For more information, see the External Current Setting Resistor section.
3	REFGND	Ground Reference Point for Internal Reference.
4	REFGND	Ground Reference Point for Internal Reference.
5	AD0	Address Decode for the Device Under Test (DUT) on the Board.
6	AD1	Address Decode for the DUT on the Board. It is not recommended to tie both AD1 and AD0 low when using PEC, see the Packet Error Checking section.
7	$\overline{SYNC}$	Frame Synchronization Signal for the Serial Interface. Active low input. When $\overline{SYNC}$ is low, data is clocked into the input shift register on the falling edge of SCLK.
8	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. The serial interface operates at clock speeds of up to 30 MHz.
9	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
10	SDO	Serial Data Output. Used to clock data from the serial register in readback mode (see Figure 4 and Figure 6).
11	DV_{DD}	Digital Supply Pin. The voltage range is from 2.7 V to 5.5 V.
12	DGND	Digital Ground.
13	$\overline{LDAC}$	Load DAC. This active low input is used to update the DAC register and, consequently, the DAC outputs. When $\overline{LDAC}$ is tied permanently low, the addressed DAC data register is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle, the DAC input register is updated, but the DAC output is updated only on the falling edge of $\overline{LDAC}$ (see Figure 3). Using this mode, all analog outputs can be updated simultaneously. The $\overline{LDAC}$ pin must not be left unconnected.

Pin No.	Mnemonic	Description
14	CLEAR	Active High, Edge Sensitive Input. When this pin is asserted, the output current and voltage are set to the programmed clear code bit setting. Only channels enabled to be cleared are cleared. For more information, see the Asynchronous Clear section. When CLEAR is active, the DAC output register cannot be written to.
15	ALERT	Active High Output. This pin is asserted when there is no SPI activity on the interface pins for a preset time. For more information, see the Alert Output section.
16	$\overline{\text{FAULT}}$	Active Low, Open-Drain Output. This pin is asserted low when any of the following conditions is detected: open circuit in current mode; short circuit in voltage mode; PEC error; or an overtemperature condition (see the Fault Output section).
17	POC	Power-On Condition. This pin determines the power-on condition and is read during power-on and after a device reset. If POC = 0, the device is powered up with the voltage and current channels in tristate mode. If POC = 1, the device is powered up with a 30 kΩ pull-down resistor to ground on the voltage output channel, and the current channel is in tristate mode.
18	$\overline{\text{RESET}}$	Hardware Reset, Active Low Input.
19	AV_{DD}	Positive Analog Supply Pin. The voltage range is from 9 V to 33 V.
20	$COMP_{LV\_A}$	Optional Compensation Capacitor Connection for V_{OUT_A} Output Buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_A} pin allows the voltage output to drive up to 2 µF. Note that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
21	$-V_{SENSE\_A}$	Sense Connection for the Negative Voltage Output Load Connection for V_{OUT_A}. This pin must stay within ±3.0 V of AGND for specified operation.
22	$+V_{SENSE\_A}$	Sense Connection for the Positive Voltage Output Load Connection for V_{OUT_A}. The difference in voltage between this pin and the V_{OUT_A} pin is added directly to the headroom requirement.
23	$COMP_{DCDC\_A}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel A dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the AI_{CC} Supply Requirements—Slewing section.
24	V_{BOOST_A}	Supply for Channel A Current Output Stage (see Figure 72). This pin is also the supply for the V_{OUT_A} stage, which is regulated to 15 V by the dc-to-dc converter. To use the dc-to-dc converter, connect this pin as shown in Figure 78.
25	V_{OUT_A}	Buffered Analog Output Voltage for DAC Channel A.
26	I_{OUT_A}	Current Output Pin for DAC Channel A.
27	AV_{SS}	Negative Analog Supply Pin. The voltage range is from −10.8 V to −26.4 V.
28	$COMP_{LV\_B}$	Optional Compensation Capacitor Connection for V_{OUT_B} Output Buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_B} pin allows the voltage output to drive up to 2 µF. Note that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
29	$-V_{SENSE\_B}$	Sense Connection for the Negative Voltage Output Load Connection for V_{OUT_B}. This pin must stay within ±3.0 V of AGND for specified operation.
30	$+V_{SENSE\_B}$	Sense Connection for the Positive Voltage Output Load Connection for V_{OUT_B}. The difference in voltage between this pin and the V_{OUT_B} pin is added directly to the headroom requirement.
31	V_{OUT_B}	Buffered Analog Output Voltage for DAC Channel B.
32	$COMP_{DCDC\_B}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel B dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the AI_{CC} Supply Requirements—Slewing section.
33	I_{OUT_B}	Current Output Pin for DAC Channel B.
34	V_{BOOST_B}	Supply for Channel B Current Output Stage (see Figure 72). This pin is also the supply for the V_{OUT_B} stage, which is regulated to 15 V by the dc-to-dc converter. To use the dc-to-dc converter, connect this pin as shown in Figure 78.
35	AGND	Ground Reference Point for Analog Circuitry. This pin must be connected to 0 V.
36	SW_B	Switching Output for Channel B DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 78.
37	$GNDSW_B$	Ground Connection for DC-to-DC Switching Circuit. This pin should always be connected to ground.
38	$GNDSW_A$	Ground Connection for DC-to-DC Switching Circuit. This pin should always be connected to ground.
39	SW_A	Switching Output for Channel A DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 78.
40	AV_{SS}	Negative Analog Supply Pin. The voltage range is from −10.8 V to −26.4 V.
41	SW_D	Switching Output for Channel D DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 78.
42	$GNDSW_D$	Ground Connection for DC-to-DC Switching Circuit. This pin should always be connected to ground.

Pin No.	Mnemonic	Description
43	$GNDSW_C$	Ground Connection for DC-to-DC Switching Circuit. This pin should always be connected to ground.
44	SW_C	Switching Output for Channel C DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 78.
45	AV_{CC}	Supply for DC-to-DC Circuitry. The voltage range is from 4.5 V to 5.5 V.
46	V_{BOOST_C}	Supply for Channel C Current Output Stage (see Figure 72). This pin is also the supply for the V_{OUT_C} stage, which is regulated to 15 V by the dc-to-dc converter. To use the dc-to-dc converter, connect this pin as shown in Figure 78.
47	I_{OUT_C}	Current Output Pin for DAC Channel C.
48	$COMP_{DCDC\_C}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel C dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the AI_{CC} Supply Requirements—Slewing section.
49	V_{OUT_C}	Buffered Analog Output Voltage for DAC Channel C.
50	$+V_{SENSE\_C}$	Sense Connection for the Positive Voltage Output Load Connection for V_{OUT_C}. The difference in voltage between this pin and the V_{OUT_C} pin is added directly to the headroom requirement.
51	$-V_{SENSE\_C}$	Sense Connection for the Negative Voltage Output Load Connection for V_{OUT_C}. This pin must stay within ±3.0 V of AGND for specified operation.
52	$COMP_{LV\_C}$	Optional Compensation Capacitor Connection for V_{OUT_C} Output Buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_C} pin allows the voltage output to drive up to 2 µF. Note that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
53	AV_{SS}	Negative Analog Supply Pin. The voltage range is from −10.8 V to −26.4 V.
54	I_{OUT_D}	Current Output Pin for DAC Channel D.
55	V_{OUT_D}	Buffered Analog Output Voltage for DAC Channel D.
56	V_{BOOST_D}	Supply for Channel D Current Output Stage (see Figure 72). This pin is also the supply for the V_{OUT_D} stage, which is regulated to 15 V by the dc-to-dc converter. To use the dc-to-dc converter, connect this pin as shown in Figure 78.
57	$COMP_{DCDC\_D}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel D dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the AI_{CC} Supply Requirements—Slewing section.
58	$+V_{SENSE\_D}$	Sense Connection for the Positive Voltage Output Load Connection for V_{OUT_D}. The difference in voltage between this pin and the V_{OUT_D} pin is added directly to the headroom requirement.
59	$-V_{SENSE\_D}$	Sense Connection for the Negative Voltage Output Load Connection for V_{OUT_D}. This pin must stay within ±3.0 V of AGND for specified operation.
60	$COMP_{LV\_D}$	Optional Compensation Capacitor Connection for V_{OUT_D} Output Buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_D} pin allows the voltage output to drive up to 2 µF. Note that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
61	REFIN	External Reference Voltage Input.
62	REFOUT	Internal Reference Voltage Output. It is recommended that a 0.1 µF capacitor be placed between REFOUT and REFGND.
63	R_{SET_D}	An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_D} temperature drift performance. For more information, see the External Current Setting Resistor section.
64	R_{SET_C}	An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_C} temperature drift performance. For more information, see the External Current Setting Resistor section.
	EPAD	Exposed Pad. The exposed paddle should be connected to the potential of the AV_{SS} pin, or, alternatively, it can be left electrically unconnected. It is recommended that the paddle be thermally connected to a copper plane for enhanced thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE OUTPUTS

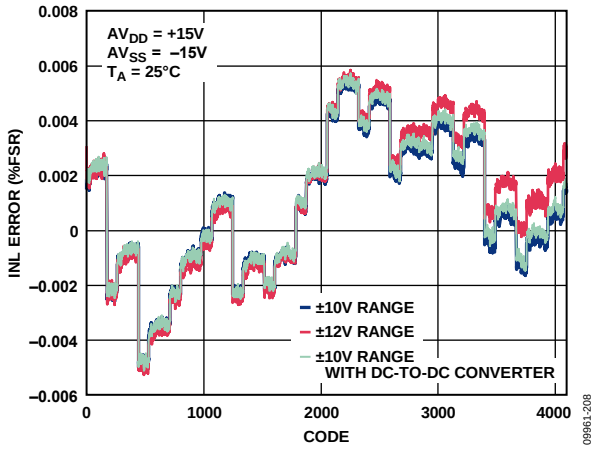


Figure 9. Integral Nonlinearity Error vs. DAC Code

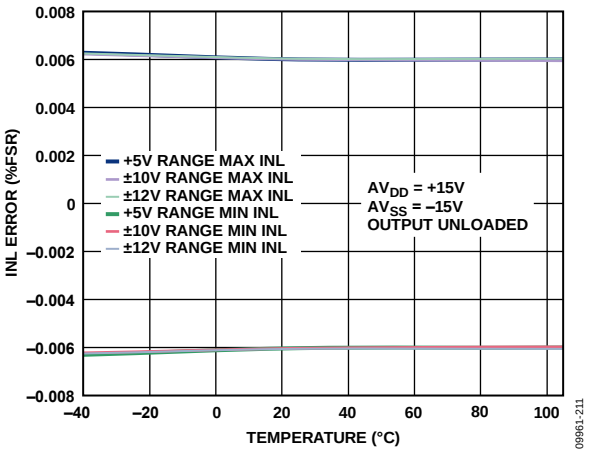


Figure 12. Integral Nonlinearity Error vs. Temperature

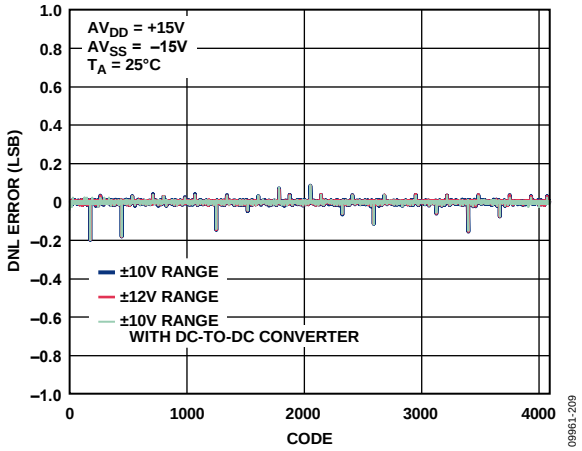


Figure 10. Differential Nonlinearity Error vs. DAC Code

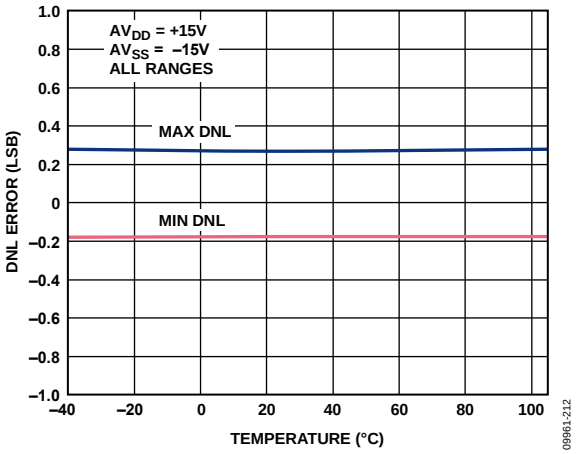


Figure 13. Differential Nonlinearity Error vs. Temperature

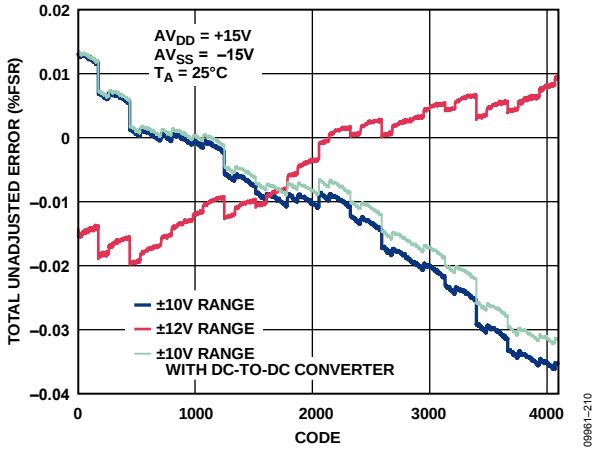


Figure 11. Total Unadjusted Error vs. DAC Code

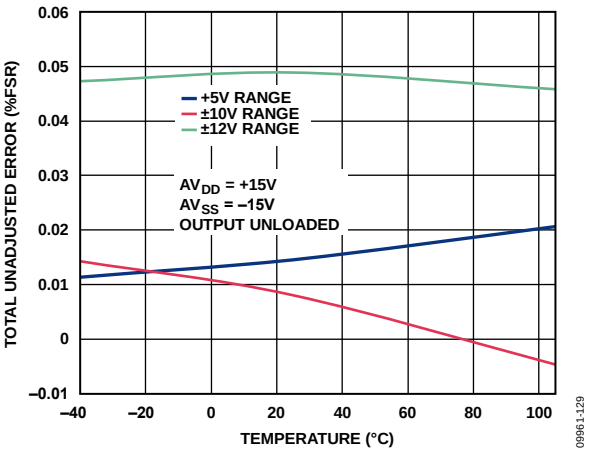


Figure 14. Total Unadjusted Error vs. Temperature

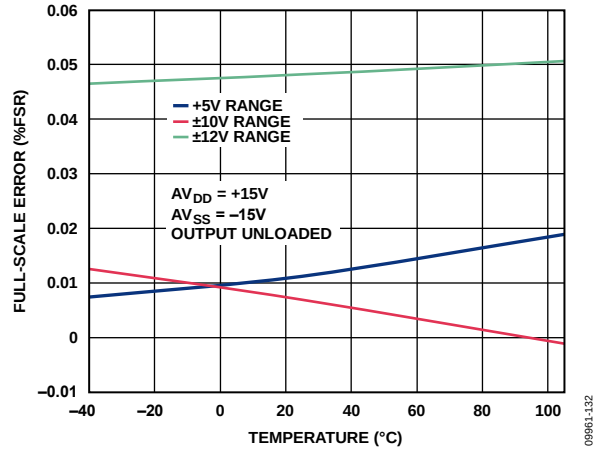


Figure 15. Full-Scale Error vs. Temperature

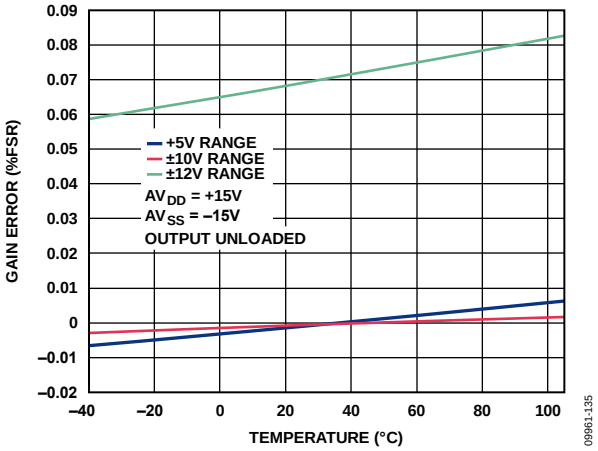


Figure 18. Gain Error vs. Temperature

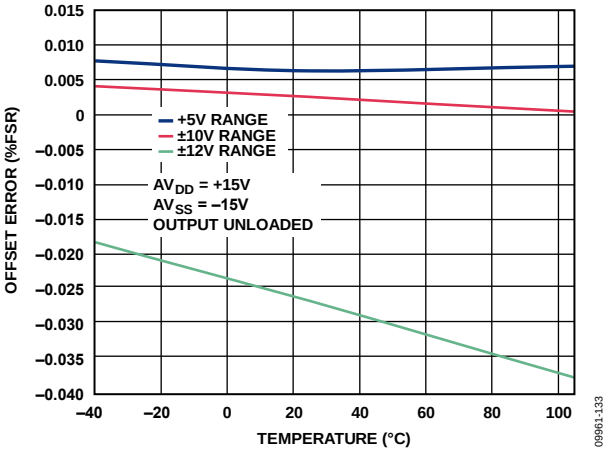


Figure 16. Offset Error vs. Temperature

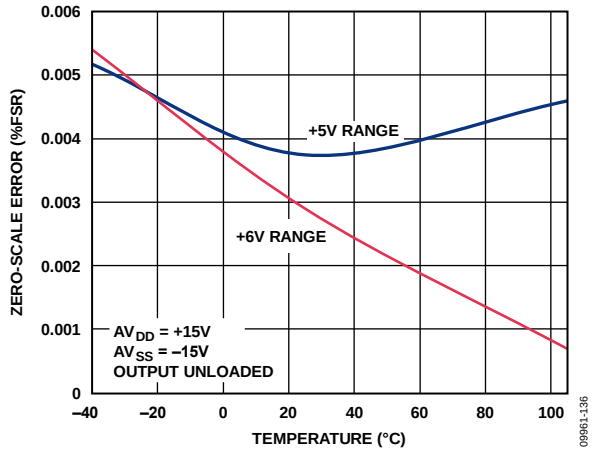


Figure 19. Zero-Scale Error vs. Temperature

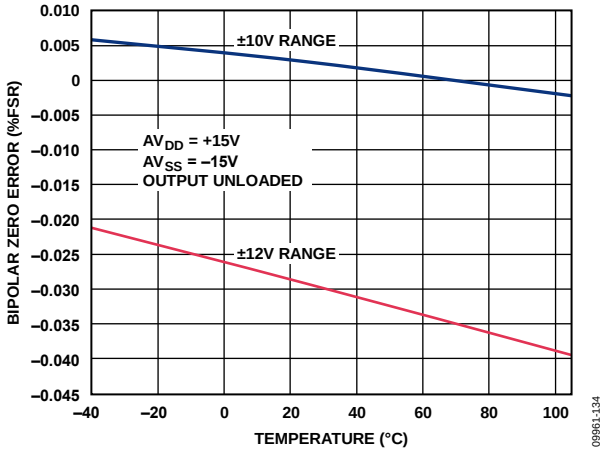


Figure 17. Bipolar Zero Error vs. Temperature

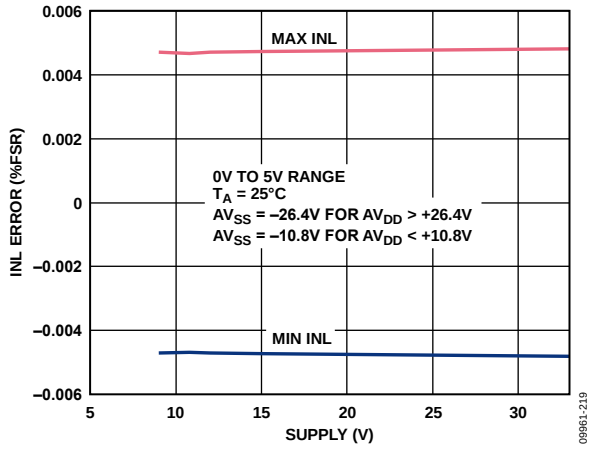


Figure 20. Integral Nonlinearity Error vs. Supply

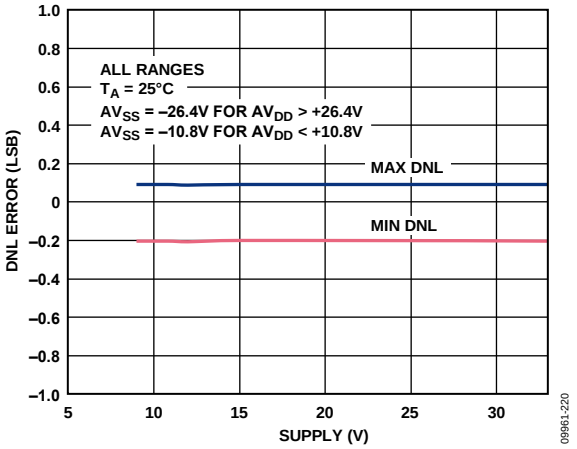


Figure 21. Differential Nonlinearity Error vs. Supply

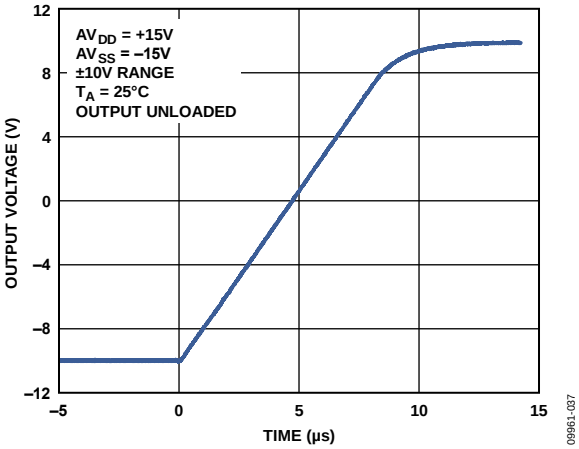


Figure 24. Full-Scale Positive Step

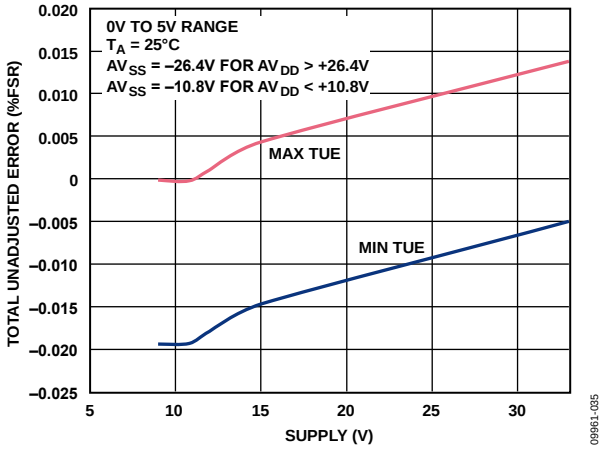


Figure 22. Total Unadjusted Error vs. Supply

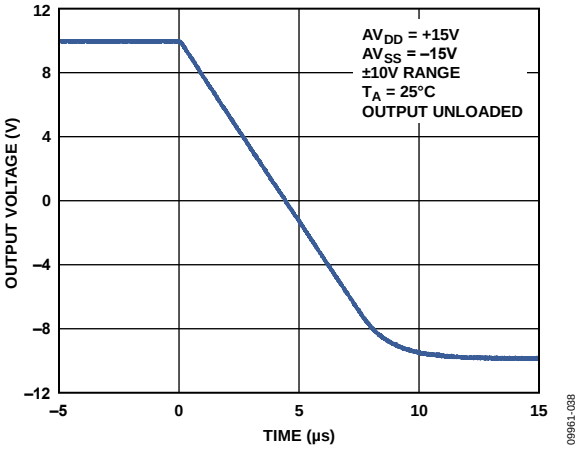


Figure 25. Full-Scale Negative Step

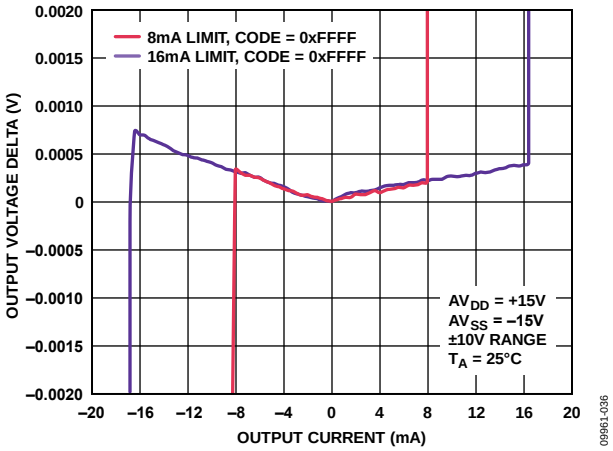


Figure 23. Source and Sink Capability of the Output Amplifier

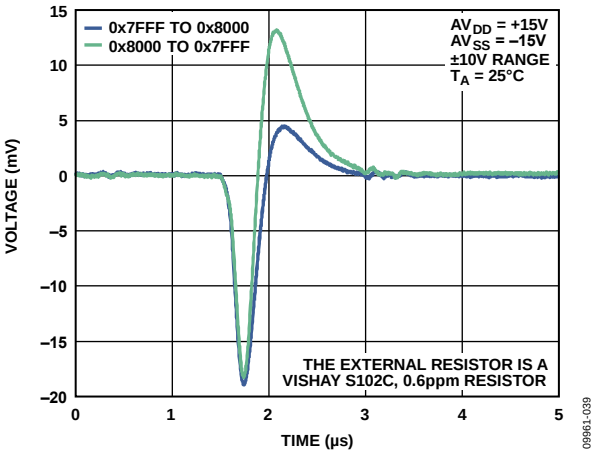


Figure 26. Digital-to-Analog Glitch

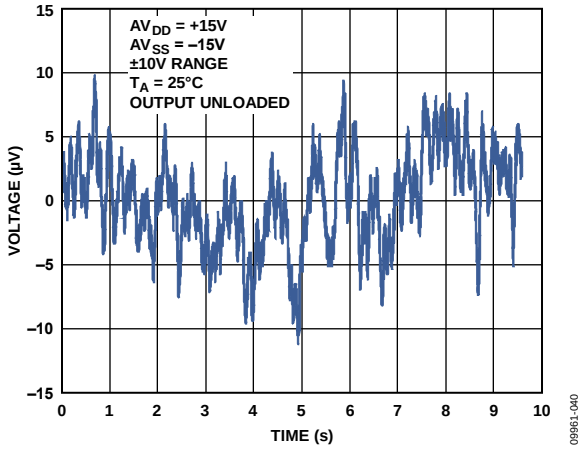


Figure 27. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

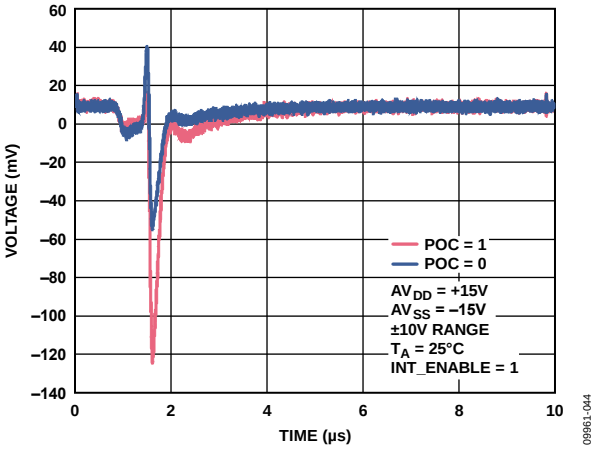


Figure 30. Voltage vs. Time on Output Enable

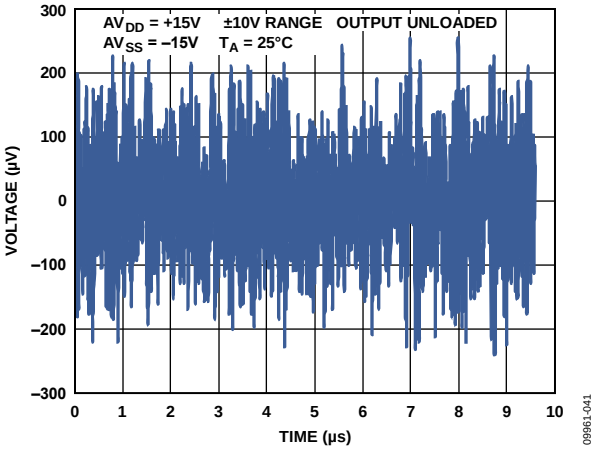


Figure 28. Peak-to-Peak Noise (100 kHz Bandwidth)

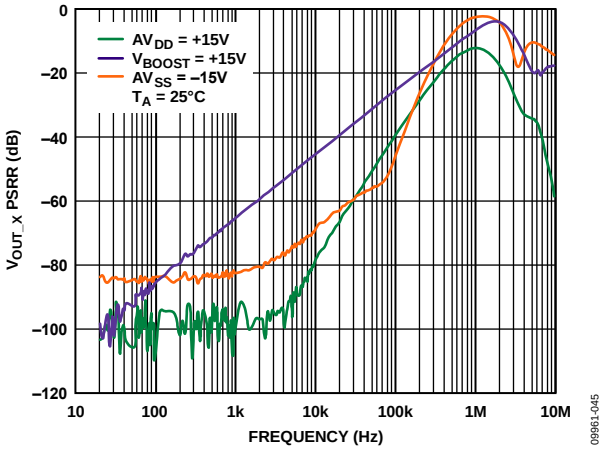


Figure 31. V_{OUT_x} PSRR vs. Frequency

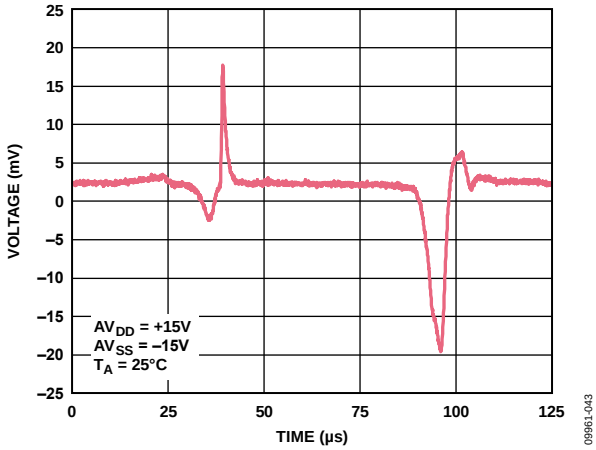


Figure 29. Voltage vs. Time on Power-Up

CURRENT OUTPUTS

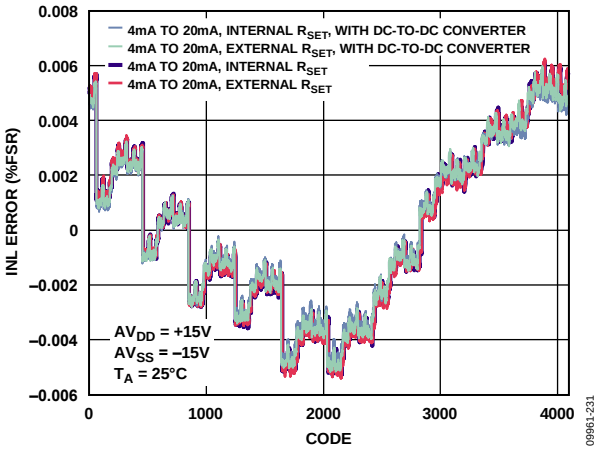


Figure 32. Integral Nonlinearity Error vs. DAC Code

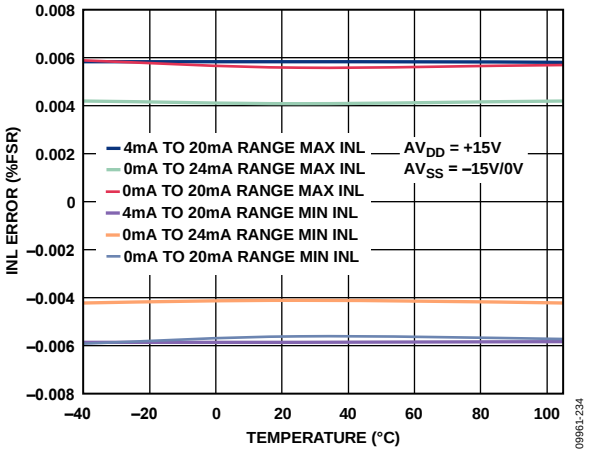


Figure 35. Integral Nonlinearity Error vs. Temperature, Internal R_{SET}

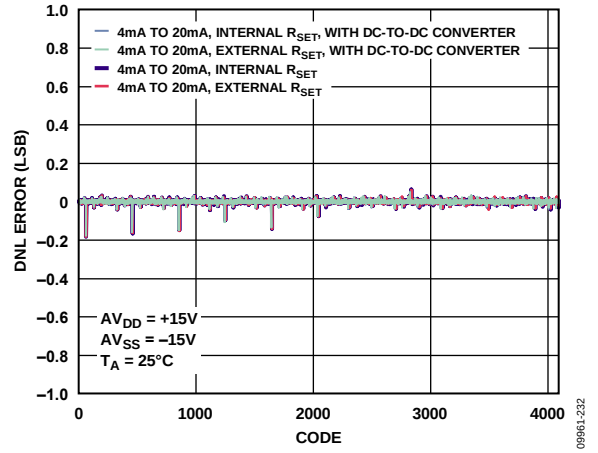


Figure 33. Differential Nonlinearity Error vs. DAC Code

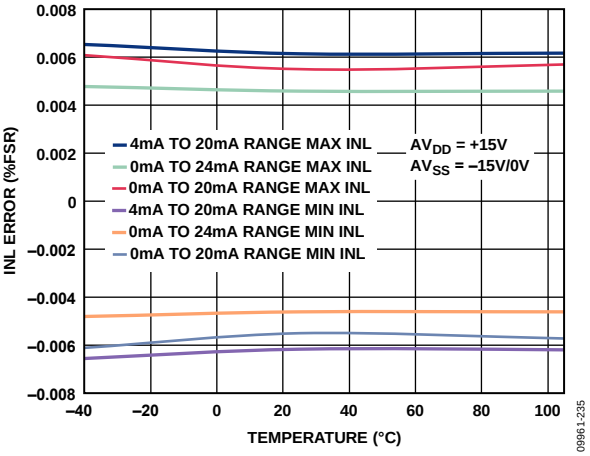


Figure 36. Integral Nonlinearity Error vs. Temperature, External R_{SET}

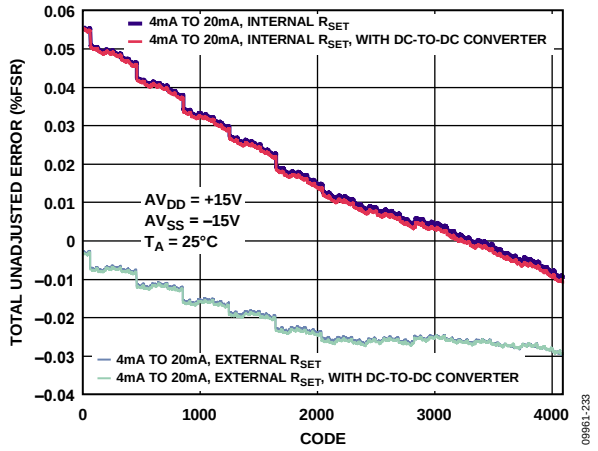


Figure 34. Total Unadjusted Error vs. DAC Code

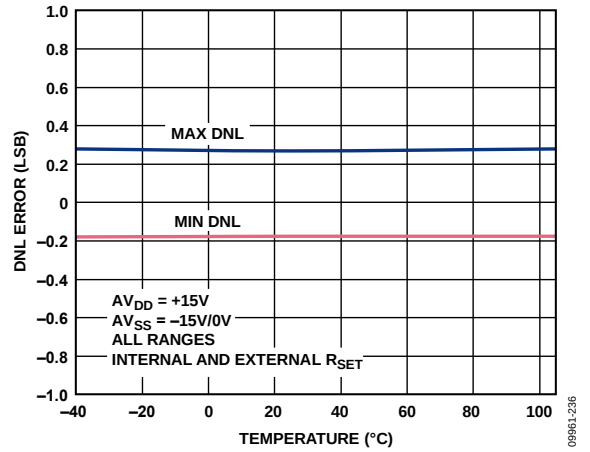


Figure 37. Differential Nonlinearity Error vs. Temperature

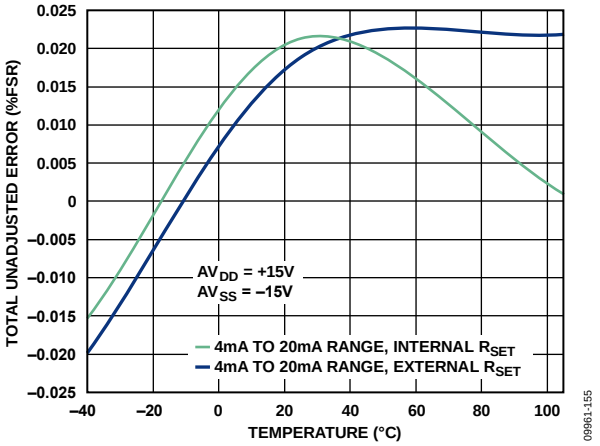


Figure 38. Total Unadjusted Error vs. Temperature

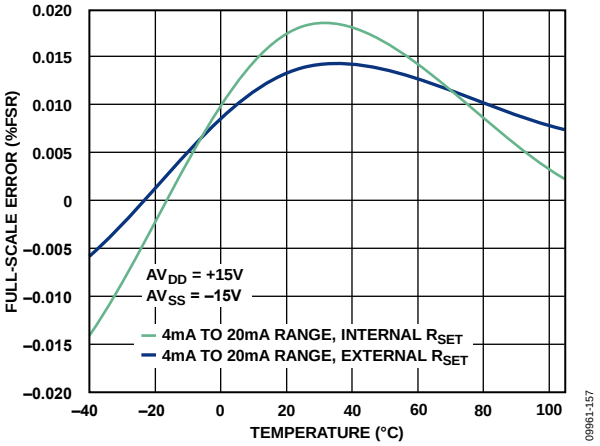


Figure 39. Full-Scale Error vs. Temperature

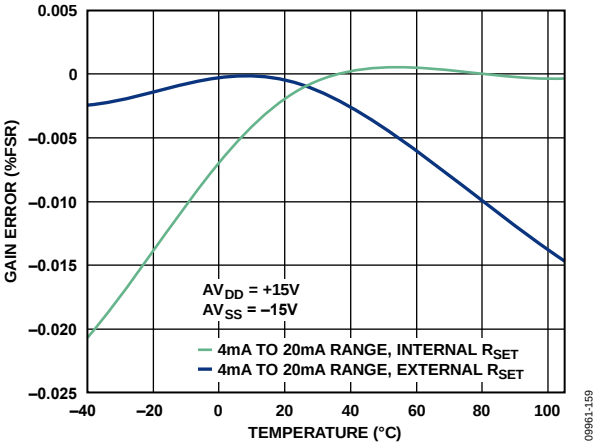


Figure 40. Gain Error vs. Temperature

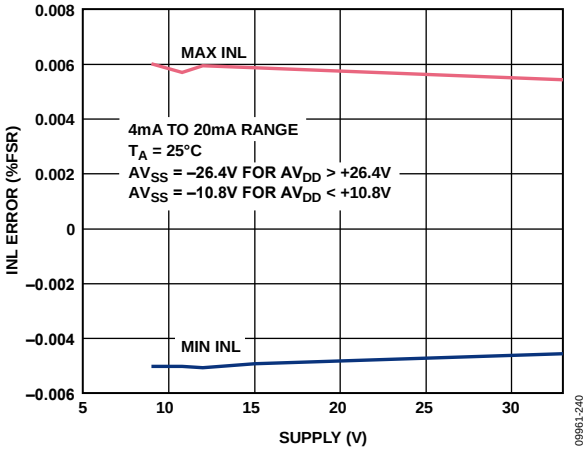


Figure 41. Integral Nonlinearity Error vs. Supply, External R_{SET}

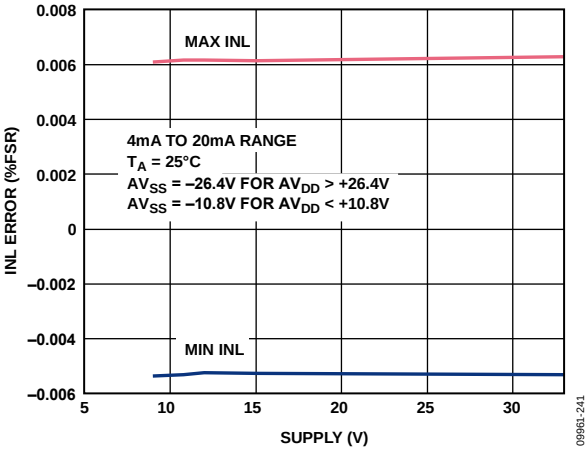


Figure 42. Integral Nonlinearity Error vs. Supply, Internal R_{SET}

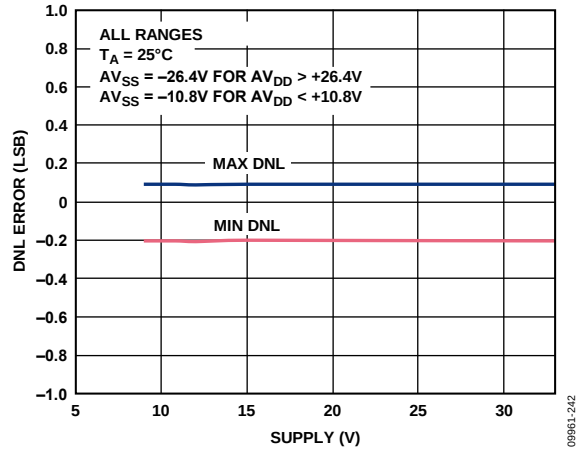


Figure 43. Differential Nonlinearity Error vs. Supply

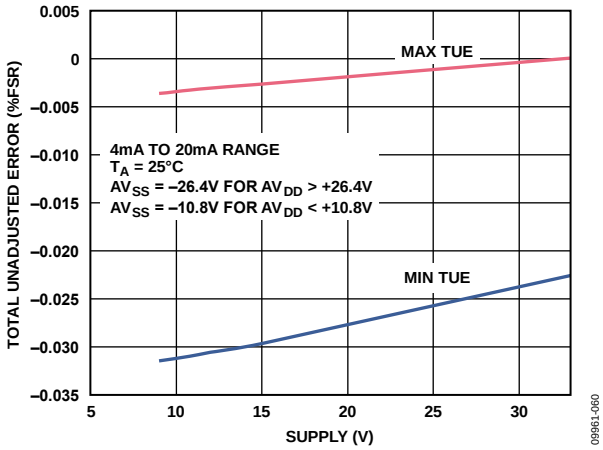


Figure 44. Total Unadjusted Error vs. Supply, External R_{SET}

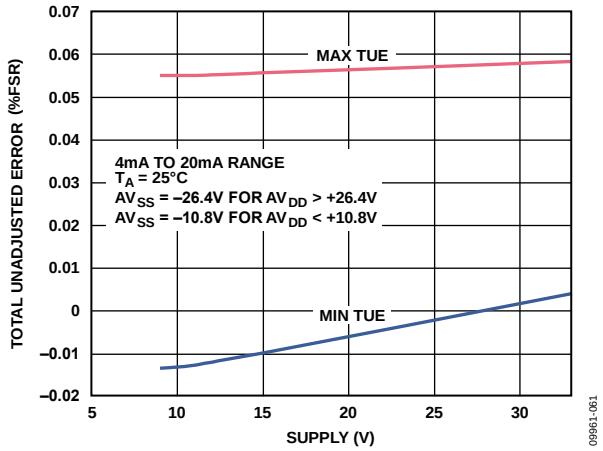


Figure 45. Total Unadjusted Error vs. Supply, Internal R_{SET}

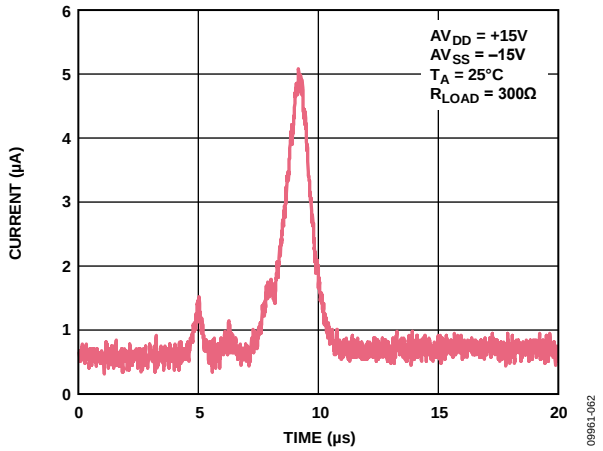


Figure 46. Current vs. Time on Power-Up

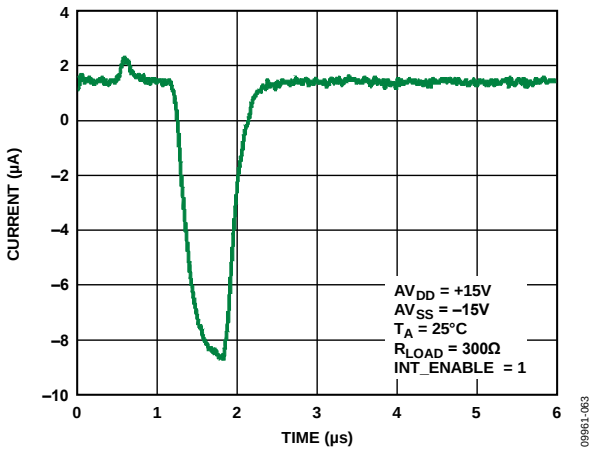


Figure 47. Current vs. Time on Output Enable

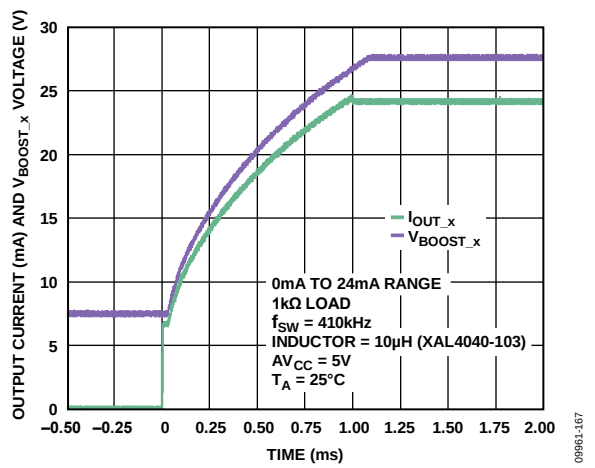


Figure 48. Output Current and V_{BOOST_x} Settling Time with DC-to-DC Converter (See Figure 78)

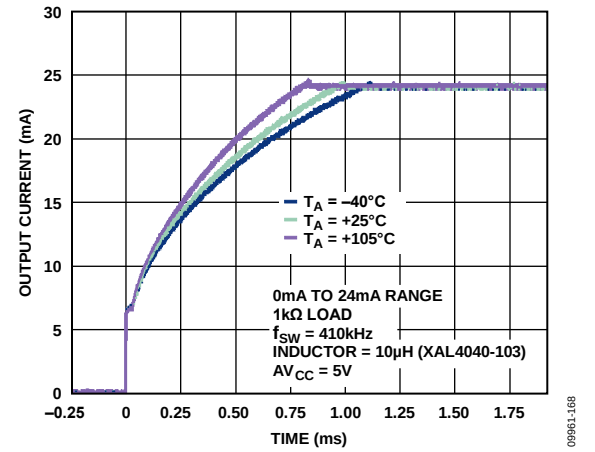


Figure 49. Output Current Settling Time with DC-to-DC Converter over Temperature (See Figure 78)

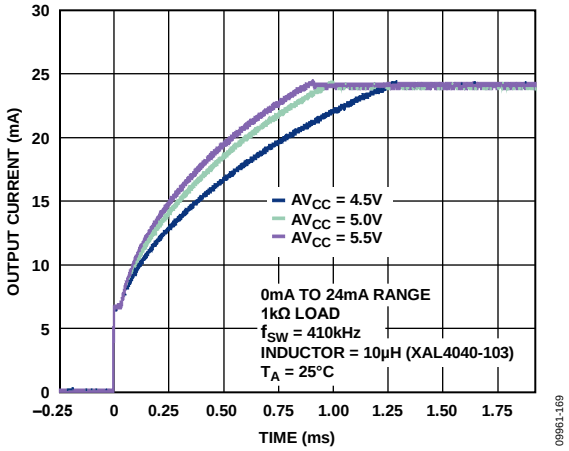


Figure 50. Output Current Settling Time with DC-to-DC Converter over AV_{CC} (See Figure 78)

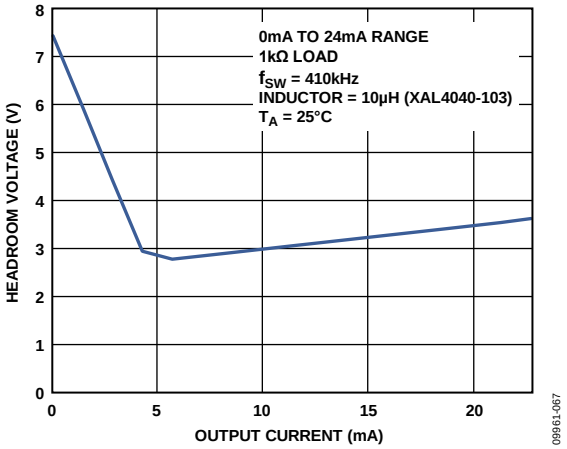


Figure 52. DC-to-DC Converter Headroom vs. Output Current (See Figure 78)

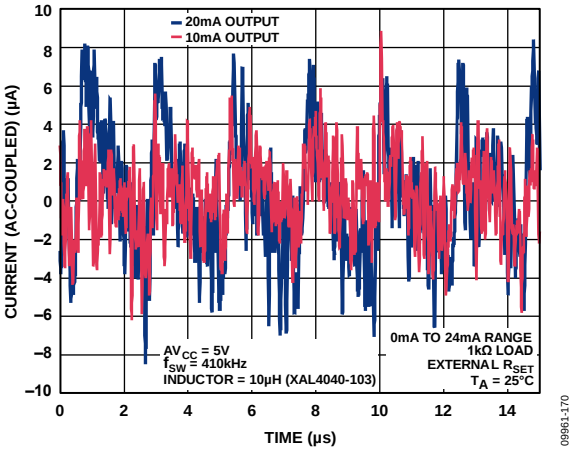


Figure 51. Output Current, AC-Coupled vs. Time with DC-to-DC Converter (See Figure 78)

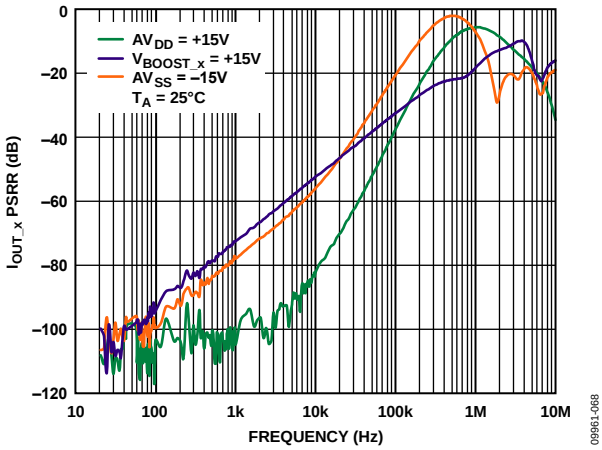


Figure 53. I_{OUT_x} PSRR vs. Frequency

DC-TO-DC CONVERTER

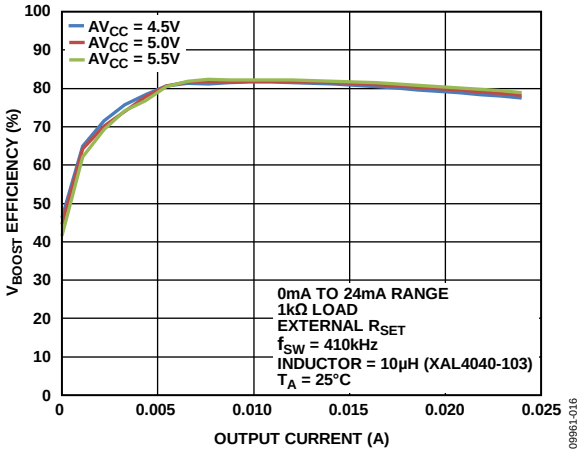


Figure 54. Efficiency at V_{BOOST_x} vs. Output Current (See Figure 78)

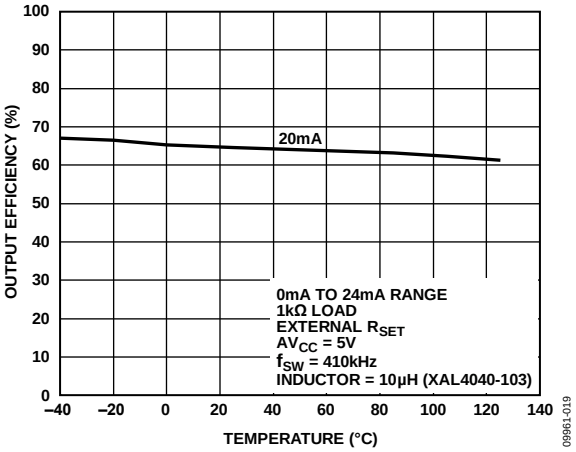


Figure 57. Output Efficiency vs. Temperature (See Figure 78)

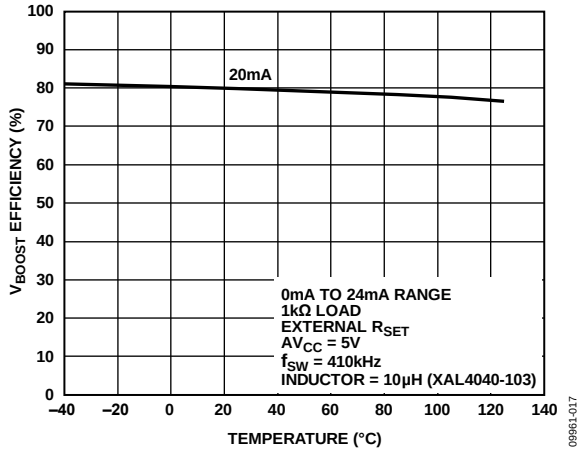


Figure 55. Efficiency at V_{BOOST_x} vs. Temperature (See Figure 78)

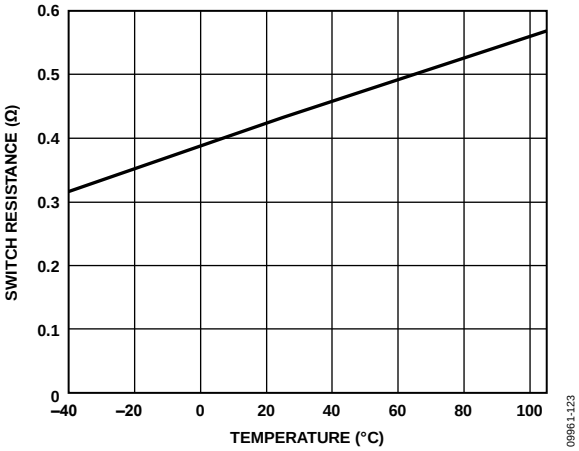


Figure 58. Switch Resistance vs. Temperature

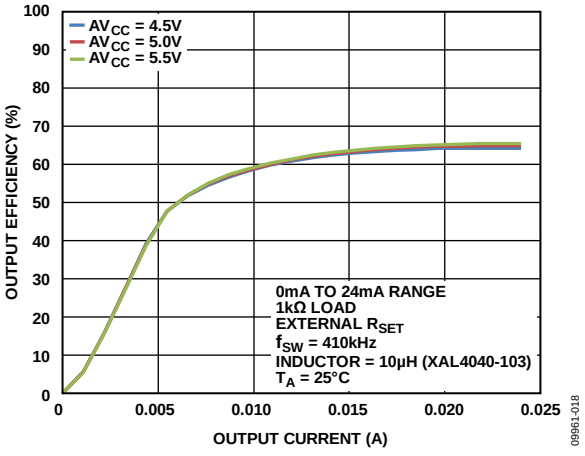


Figure 56. Output Efficiency vs. Output Current (See Figure 78)

REFERENCE

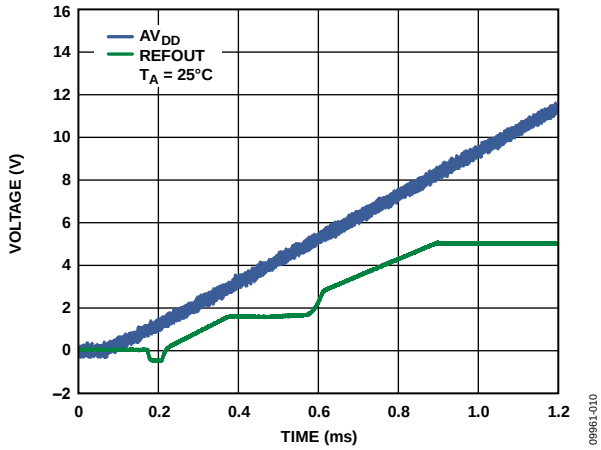


Figure 59. REFOUT Voltage Turn-On Transient

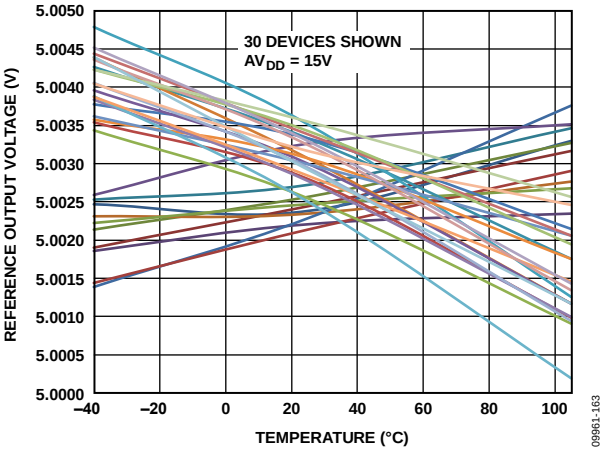


Figure 62. REFOUT Voltage vs. Temperature (When the AD5735 is soldered onto a PCB, the reference shifts due to thermal shock on the package. The average output voltage shift is −4 mV. Measurement of these parts after seven days shows that the outputs typically shift back 2 mV toward their initial values. This second shift is due to the relaxation of stress incurred during soldering.)

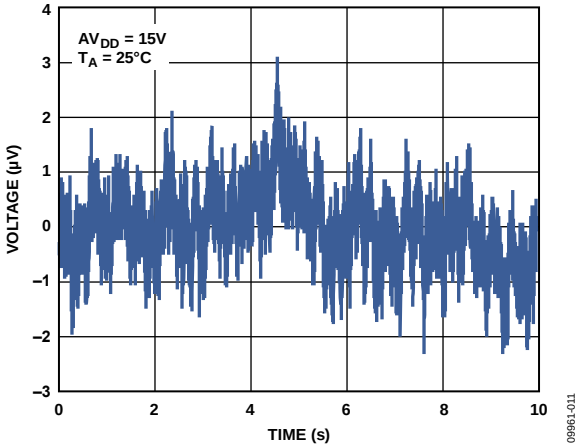


Figure 60. REFOUT Output Noise (0.1 Hz to 10 Hz Bandwidth)

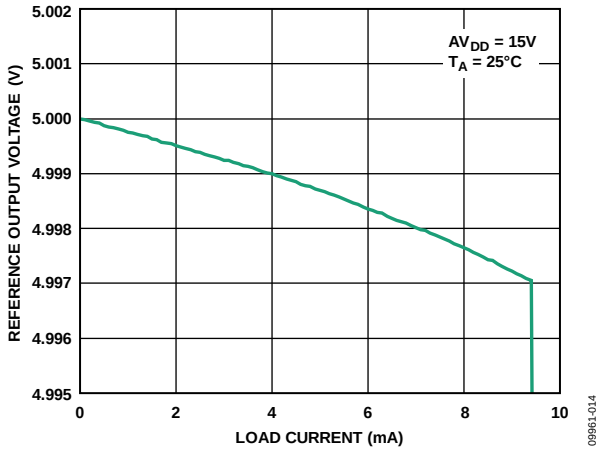


Figure 63. REFOUT Voltage vs. Load Current

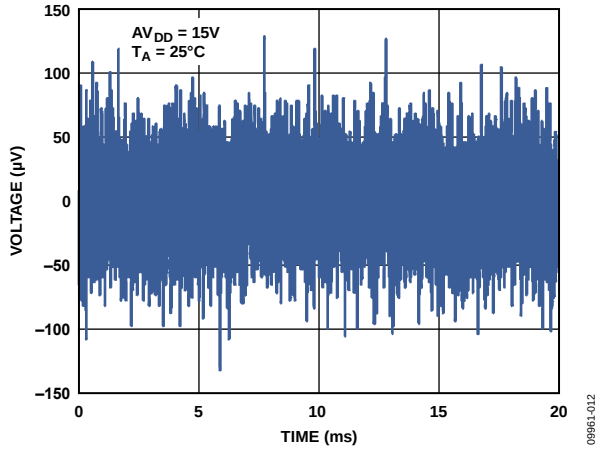


Figure 61. REFOUT Output Noise (100 kHz Bandwidth)

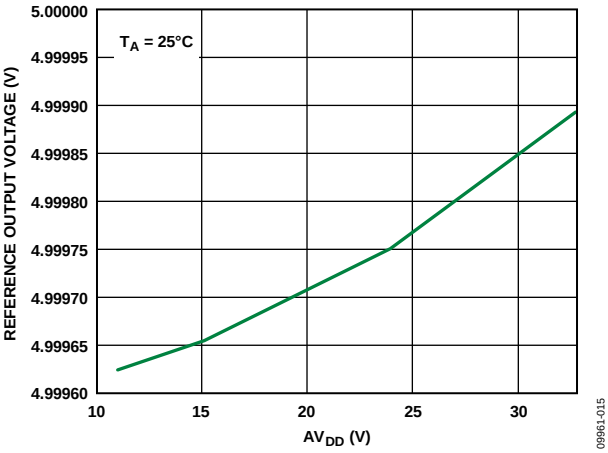


Figure 64. REFOUT Voltage vs. AV$_{DD}$

GENERAL

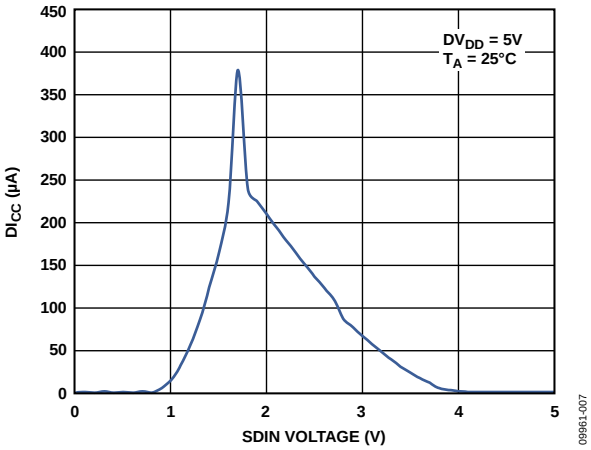


Figure 65. DI$_{CC}$ vs. Logic Input Voltage

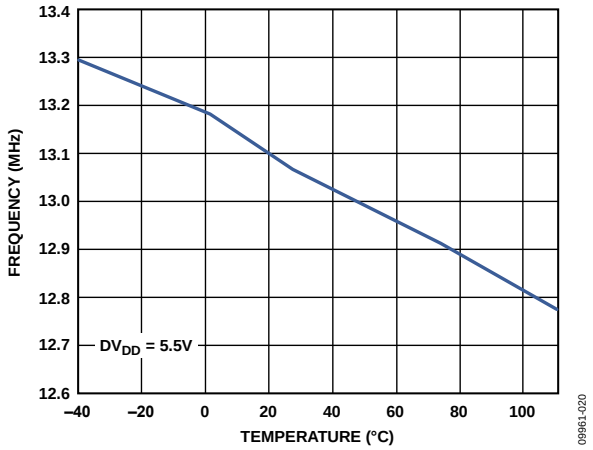


Figure 68. Internal Oscillator Frequency vs. Temperature

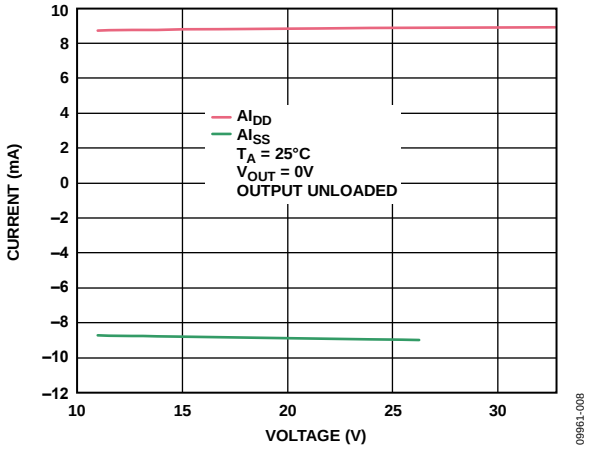


Figure 66. Supply Current (AI$_{DD}$/AI$_{SS}$) vs. Supply Voltage (AV$_{DD}$/|AV$_{SS}$|)

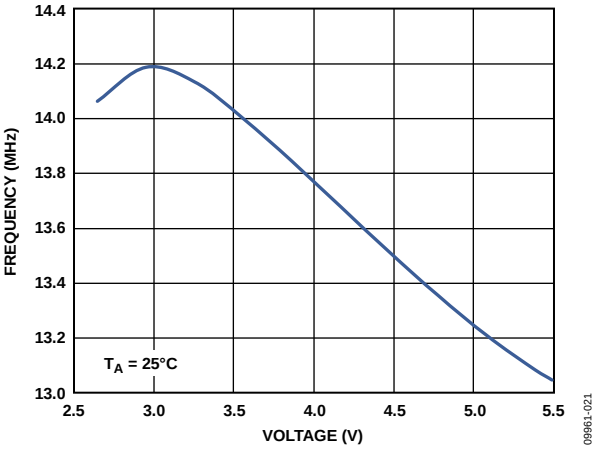


Figure 69. Internal Oscillator Frequency vs. DV$_{DD}$ Supply Voltage

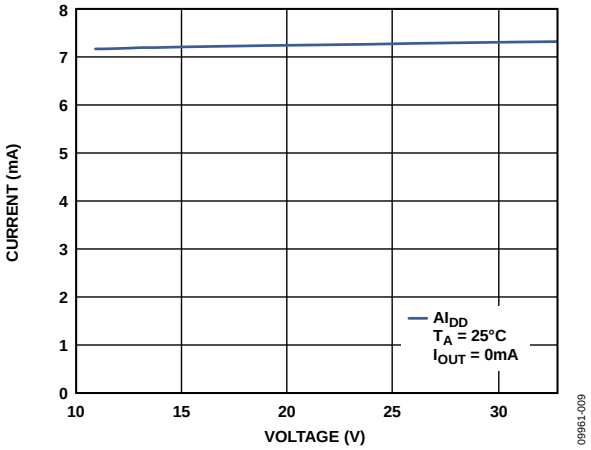


Figure 67. Supply Current (AI$_{DD}$) vs. Supply Voltage (AV$_{DD}$)

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
Relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation from the best fit line through the DAC transfer function. INL is expressed in percent of full-scale range (% FSR). Typical INL vs. code plots are shown in Figure 9 and Figure 32.

Differential Nonlinearity (DNL)
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity. The AD5735 is guaranteed monotonic by design. Typical DNL vs. code plots are shown in Figure 10 and Figure 33.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5735 is monotonic over its full operating temperature range.

Negative Full-Scale Error or Zero-Scale Error
Negative full-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) is loaded to the DAC register.

Zero-Scale Temperature Coefficient (TC)
Zero-scale TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale TC is expressed in ppm FSR/°C.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (straight binary coding).

Bipolar Zero Temperature Coefficient (TC)
Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/°C.

Offset Error
In voltage output mode, offset error is the deviation of the analog output from the ideal quarter-scale output when the DAC is configured for a bipolar output range and the DAC register is loaded with 0x4000 (straight binary coding).

In current output mode, offset error is the deviation of the analog output from the ideal zero-scale output when all DAC registers are loaded with 0x0000.

Offset Error Drift or Offset TC
Offset error drift, or offset TC, is a measure of the change in offset error with changes in temperature and is expressed in ppm FSR/°C.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer function from the ideal, expressed in % FSR.

Gain Temperature Coefficient (TC)
Gain TC is a measure of the change in gain error with changes in temperature and is expressed in ppm FSR/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output should be full-scale − 1 LSB. Full-scale error is expressed in % FSR.

Full-Scale Temperature Coefficient (TC)
Full-scale TC is a measure of the change in full-scale error with changes in temperature and is expressed in ppm FSR/°C.

Total Unadjusted Error (TUE)
Total unadjusted error (TUE) is a measure of the output error that includes all the error measurements: INL error, offset error, gain error, temperature, and time. TUE is expressed in % FSR.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC, which is at midscale.

Current Loop Compliance Voltage
The current loop compliance voltage is the maximum voltage at the I_{OUT_x} pin for which the output current is equal to the programmed value.

Voltage Reference Thermal Hysteresis
Voltage reference thermal hysteresis is the difference in output voltage measured at +25°C compared to the output voltage measured at +25°C after cycling the temperature from +25°C to −40°C to +105°C and back to +25°C. The hysteresis is specified in ppm.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change. Plots of settling time are shown in Figure 24, Figure 49, and Figure 50.

Slew Rate
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage output DAC is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in V/µs.

Power-On Glitch Energy
Power-on glitch energy is the impulse injected into the analog output when the AD5735 is powered on. It is specified as the area of the glitch in nV-sec (see Figure 29 and Figure 46).

Digital-to-Analog Glitch Energy
Digital-to-analog glitch energy is the impulse injected into the analog output when the input code in the DAC register changes state but the output voltage remains constant. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (~0x7FFF to 0x8000). See Figure 26.

Glitch Impulse Peak Amplitude
Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the amplitude of the glitch in mV and is measured when the digital input code is changed by 1 LSB at the major carry transition (~0x7FFF to 0x8000). See Figure 26.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and a subsequent output change of another DAC. DAC-to-DAC crosstalk includes both digital and analog crosstalk. It is measured by loading one DAC with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low while monitoring the output of another DAC. The energy of the glitch is expressed in nV-sec.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

Reference Temperature Coefficient (TC)
Reference TC is a measure of the change in the reference output voltage with changes in temperature. It is expressed in ppm/°C.

Line Regulation
Line regulation is the change in the reference output voltage due to a specified change in supply voltage. It is expressed in ppm/V.

Load Regulation
Load regulation is the change in the reference output voltage due to a specified change in load current. It is expressed in ppm/mA.

DC-to-DC Converter Headroom
DC-to-DC converter headroom is the difference between the voltage required at the current output and the voltage supplied by the dc-to-dc converter (see Figure 52).

Output Efficiency
Output efficiency is defined as the ratio of the power delivered to a channel's load and the power delivered to the channel's dc-to-dc input. The V_{BOOST_x} quiescent current is considered part of the dc-to-dc converter's losses.

$$\frac{I_{OUT}{}^2 \times R_{LOAD}}{AV_{CC} \times AI_{CC}}$$

Efficiency at VBOOST_x
The efficiency at V_{BOOST_x} is defined as the ratio of the power delivered to a channel's V_{BOOST_x} supply and the power delivered to the channel's dc-to-dc input. The V_{BOOST_x} quiescent current is considered part of the dc-to-dc converter's losses.

$$\frac{I_{OUT} \times V_{BOOST\_x}}{AV_{CC} \times AI_{CC}}$$

THEORY OF OPERATION

The AD5735 is a quad, precision digital-to-current loop and voltage output converter designed to meet the requirements of industrial process control applications. It provides a high precision, fully integrated, low cost, single-chip solution for generating current loop and unipolar/bipolar voltage outputs.

The current ranges available are 0 mA to 20 mA, 4 mA to 20 mA, and 0 mA to 24 mA. The voltage ranges available are 0 V to 5 V, ±5 V, 0 V to 10 V, and ±10 V. The current and voltage outputs are available on separate pins, and only one output is active at any one time. The output configuration is user-selectable via the DAC control register.

On-chip dynamic power control minimizes package power dissipation in current mode (see the Dynamic Power Control section).

DAC ARCHITECTURE

The DAC core architecture of the AD5735 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 70. The four MSBs of the 12-bit data-word are decoded to drive 15 switches, E1 to E15. Each switch connects one of 15 matched resistors either to ground or to the reference buffer output. The remaining eight bits of the data-word drive Switch S0 to Switch S7 of an 8-bit voltage mode R-2R ladder network.

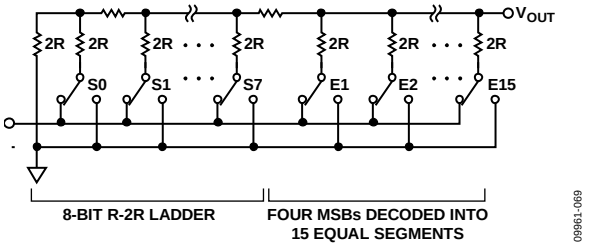


Figure 70. DAC Ladder Structure

The voltage output from the DAC core can be

- Buffered and scaled to output a software selectable unipolar or bipolar voltage range (see Figure 71)
- Converted to a current, which is then mirrored to the supply rail so that the application sees only a current source output (see Figure 72)

Both the voltage and current outputs are supplied by V_{BOOST_x}. The current and voltage are output on separate pins and cannot be output simultaneously. The current and voltage output pins of a channel can be tied together (see the Voltage and Current Output Pins on the Same Terminal section).

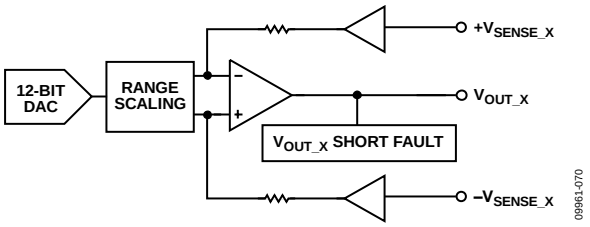


Figure 71. Voltage Output

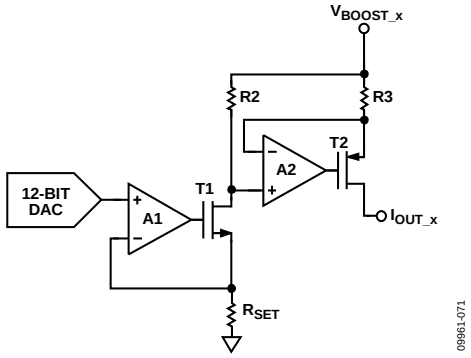


Figure 72. Voltage-to-Current Conversion Circuitry

Voltage Output Amplifier

The voltage output amplifier is capable of generating both unipolar and bipolar output voltages. It is capable of driving a load of 1 kΩ in parallel with 1 µF (with an external compensation capacitor) to AGND. The source and sink capabilities of the output amplifier are shown in Figure 23. The slew rate is 1.9 V/µs with a full-scale settling time of 18 µs max (10 V step). If remote sensing of the load is not required, connect $+V_{SENSE\_x}$ directly to V_{OUT_x}, and connect $-V_{SENSE\_x}$ directly to AGND. $-V_{SENSE\_x}$ must stay within ±3.0 V of AGND for specified operation. The difference in voltage between $+V_{SENSE\_x}$ and V_{OUT_x} should be added directly to the headroom requirement.

Driving Large Capacitive Loads

The voltage output amplifier is capable of driving capacitive loads of up to 2 µF with the addition of a 220 pF, nonpolarized compensation capacitor on each channel. The 220 pF capacitor is connected between the $COMP_{LV\_x}$ pin and the V_{OUT_x} pin.

Care should be taken to choose an appropriate value of compensation capacitor. This capacitor, while allowing the AD5735 to drive higher capacitive loads and reduce overshoot, increases the settling time of the part and, therefore, affects the bandwidth of the system. Without the compensation capacitor, capacitive loads of up to 10 nF can be driven.

Reference Buffers

The AD5735 can operate with either an external or internal reference. The reference input requires a 5 V reference for specified performance. This input voltage is then buffered before it is applied to the DAC.

POWER-ON STATE OF THE AD5735

On initial power-up of the AD5735, the state of the power-on reset circuit is dependent on the power-on condition (POC) pin.

- If POC = 0, both the voltage output and current output channels power up in tristate mode.
- If POC = 1, the voltage output channel powers up with a 30 kΩ pull-down resistor to ground, and the current output channel powers up in tristate mode.

The output ranges are not enabled, but the default output range is 0 V to 5 V, and the clear code register is loaded with all 0s. Therefore, if the user clears the part after power-up, the output is actively driven to 0 V if the channel has been enabled for clear.

After device power on, or a device reset, it is recommended to wait 100 µs or more before writing to the device to allow time for internal calibrations to take place.

SERIAL INTERFACE

The AD5735 is controlled by a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP standards. Data coding is always straight binary.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of the serial clock input, SCLK. Data is clocked in on the falling edge of SCLK.

If packet error checking (PEC) is enabled, an additional eight bits must be written to the AD5735, creating a 32-bit serial interface (see the Packet Error Checking section).

The DAC outputs can be updated in one of two ways: individual DAC updating or simultaneous updating of all DACs.

Individual DAC Updating

To update an individual DAC, $\overline{\text{LDAC}}$ is held low while data is clocked into the DAC data register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$. See Table 3 and Figure 3 for timing information.

Simultaneous Updating of All DACs

To update all DACs simultaneously, $\overline{\text{LDAC}}$ is held high while data is clocked into the DAC data register. After $\overline{\text{LDAC}}$ is taken high, only the first write to the DAC data register of each channel is valid; subsequent writes to the DAC data register are ignored, although these subsequent writes are returned if a readback is initiated. All DAC outputs are updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ is taken high.

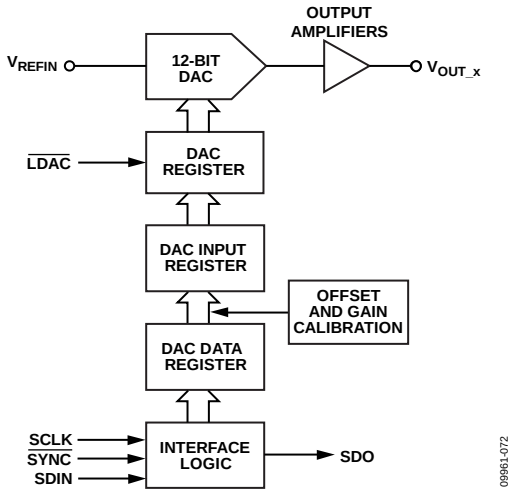


Figure 73. Simplified Serial Interface of the Input Loading Circuitry for One DAC Channel

TRANSFER FUNCTION

Table 7 shows the input code to ideal output voltage relationship for the AD5735 for straight binary data coding of the ±10 V output range.

Table 7. Input Code to Ideal Output Voltage Relationship

Digital Input				
Straight Binary Data Coding				Analog Output
MSB		LSB[1]		V_{OUT}
1111	1111	1111	XXXX	+2 V_{REF} × (2047/2048)
1111	1111	1110	XXXX	+2 V_{REF} × (2046/2048)
1000	0000	0000	XXXX	0 V
0000	0000	0001	XXXX	−2 V_{REF} × (2047/2048)
0000	0000	0000	XXXX	−2 V_{REF}

[1] X = don't care.

REGISTERS

Table 8, Table 9, and Table 10 provide an overview of the registers for the AD5735.

Table 8. Data Registers for the AD5735

Register	Description
DAC Data Registers	The four DAC data registers (one register per DAC channel) are used to write a DAC code to each DAC channel. The DAC data bits are D15 to D4.
Gain Registers	The four gain registers (one register per DAC channel) are used to program the gain trim on a per-channel basis. The gain data bits are D15 to D4.
Offset Registers	The four offset registers (one register per DAC channel) are used to program the offset trim on a per-channel basis. The offset data bits are D15 to D4.
Clear Code Registers	The four clear code registers (one register per DAC channel) are used to program the clear code on a per-channel basis. The clear code data bits are D15 to D4.

Table 9. Control Registers for the AD5735

Register	Description
Main Control Register	The main control register is used to configure functions for the entire part. These functions include the following: enabling status readback during a write; enabling the output on all four DAC channels simultaneously; power-on of the dc-to-dc converter on all four DAC channels simultaneously; and enabling and configuring the watchdog timer. For more information, see the Main Control Register section.
DAC Control Registers	The four DAC control registers (one register per DAC channel) are used to configure the following functions on a per-channel basis: output range (for example, 4 mA to 20 mA or 0 V to 10 V); selection of the internal current sense resistor or an external current sense resistor; enabling/disabling the use of a clear code; enabling/disabling overrange on a voltage channel; enabling/disabling the internal circuitry (dc-to-dc converter, DAC, and internal amplifiers); power-on/power-off of the dc-to-dc converter; and enabling/disabling the output channel.
Software Register	The software register is used to perform a reset, to toggle the user bit in the status register, and, as part of the watchdog timer feature, to verify correct data communication operation.
DC-to-DC Control Register	The dc-to-dc control register is used to set the control parameters for the dc-to-dc converter: maximum output voltage, phase, and switching frequency. This register is also used to select the internal compensation resistor or an external compensation resistor for the dc-to-dc converter.
Slew Rate Control Registers	The four slew rate control registers (one register per DAC channel) are used to program the slew rate of the DAC output.

Table 10. Readback Register for the AD5735

Register	Description
Status Register	The status register contains any fault information, as well as a user toggle bit.

ENABLING THE OUTPUT

To correctly write to and set up the part from a power-on condition, use the following sequence:

1. Perform a hardware or software reset after initial power-on.
2. Configure the dc-to-dc converter supply block. Set the dc-to-dc switching frequency, the maximum output voltage allowed, and the dc-to-dc converter phase between channels.
3. Configure the DAC control register on a per-channel basis. Select the output range, and enable the dc-to-dc converter block (DC_DC bit). Other control bits can also be configured. Set the INT_ENABLE bit, but do not set the OUTEN (output enable) bit.
4. Write the required code to the DAC data register. This step implements a full internal DAC calibration. For reduced output glitch, allow at least 200 µs before performing Step 5.
5. Write to the DAC control register again to enable the output (set the OUTEN bit).

Figure 74 provides a flowchart of this sequence.

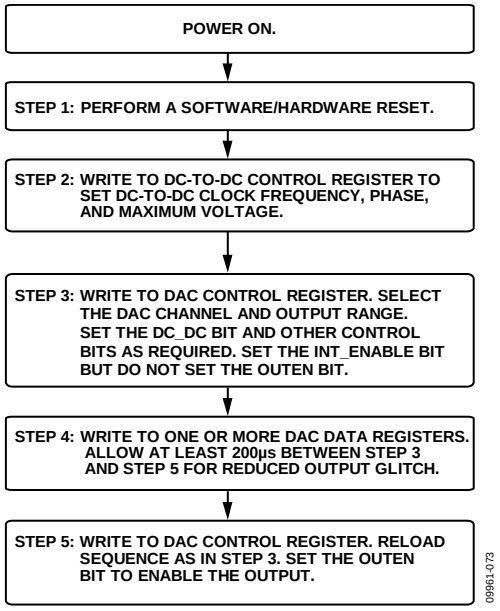


Figure 74. Programming Sequence to Correctly Enable the Output

REPROGRAMMING THE OUTPUT RANGE

When changing the range of an output, the same sequence described in the Enabling the Output section should be used. It is recommended that the range be set to 0 V (zero scale or midscale) before the output is disabled. Because the dc-to-dc switching frequency, maximum output voltage, and phase have already been selected, there is no need to reprogram these values. Figure 75 provides a flowchart of this sequence.

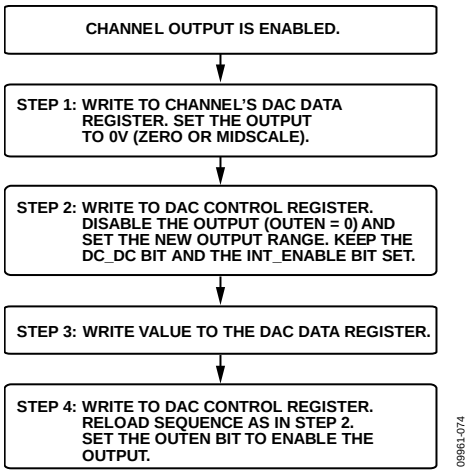


Figure 75. Programming Sequence to Change the Output Range

DATA REGISTERS

The input shift register is 24 bits wide. When PEC is enabled, the input shift register is 32 bits wide, with the last eight bits corresponding to the PEC code (see the Packet Error Checking section for more information about PEC). When writing to a data register, the format shown in Table 11 must be used.

DAC Data Register

When writing to a DAC data register, Bit D15 to Bit D4 are the DAC data bits. Table 13 shows the register format, and Table 12 describes the functions of Bit D23 to Bit D16.

Table 11. Input Shift Register for a Write Operation to a Data Register

MSB								LSB
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**D15 to D0**
R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	Data

Table 12. Descriptions of Data Register Bits[D23:D16]

Bit Name	Description			
R/$\overline{W}$	This bit indicates whether the addressed register is written to or read from. 0 = write to the addressed register. 1 = read from the addressed register.			
DUT_AD1, DUT_AD0	Used in association with the external pins AD1 and AD0, these bits determine which AD5735 device is being addressed by the system controller. It is not recommended to tie both AD1 and AD0 low when using PEC, see the Packet Error Checking section.			
	DUT_AD1	**DUT_AD0**	**Part Addressed**	
	0	0	Pin AD1 = 0, Pin AD0 = 0	
	0	1	Pin AD1 = 0, Pin AD0 = 1	
	1	0	Pin AD1 = 1, Pin AD0 = 0	
	1	1	Pin AD1 = 1, Pin AD0 = 1	
DREG2, DREG1, DREG0	These bits select the register to be written to. If a control register is selected (DREG[2:0] = 111), the CREG bits in the control register select the specific control register to be written to (see Table 20).			
	DREG2	**DREG1**	**DREG0**	**Function**
	0	0	0	Write to DAC data register (one DAC channel)
	0	0	1	Reserved
	0	1	0	Write to gain register (one DAC channel)
	0	1	1	Write to gain registers (all DAC channels)
	1	0	0	Write to offset register (one DAC channel)
	1	0	1	Write to offset registers (all DAC channels)
	1	1	0	Write to clear code register (one DAC channel)
	1	1	1	Write to a control register
DAC_AD1, DAC_AD0	These bits are used to specify the DAC channel. If a write to the part does not apply to a specific DAC channel, these bits are don't care bits.			
	DAC_AD1	**DAC_AD0**	**DAC Channel**	
	0	0	DAC A	
	0	1	DAC B	
	1	0	DAC C	
	1	1	DAC D	

Table 13. Programming the DAC Data Register

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D4	D3 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	0	0	0	DAC_AD1	DAC_AD0	DAC data	X[1]

[1] X = don't care.

Gain Register

The 12-bit gain register allows the user to adjust the gain of each channel in steps of 1 LSB. To write to the gain register of one DAC channel, set the DREG[2:0] bits to 010 (see Table 14). To write the same gain code to all four DAC channels at the same time, set the DREG[2:0] bits to 011. The gain register coding is straight binary, as shown in Table 15. The default code in the gain register is 0xFFFF. The maximum recommended gain trim is approximately 50% of the programmed range to maintain accuracy (for more information, see the Digital Offset and Gain Control section).

Offset Register

The 12-bit offset register allows the user to adjust the offset of each channel by −2048 LSB to +2047 LSB in steps of 1 LSB. To write to the offset register of one DAC channel, set the DREG[2:0] bits to 100 (see Table 16). To write the same offset code to all four DAC channels at the same time, set the DREG[2:0] bits to 101. The offset register coding is straight binary, as shown in Table 17. The default code in the offset register is 0x8000, which results in zero offset programmed to the output (for more information, see the Digital Offset and Gain Control section).

Clear Code Register

The 12-bit clear code register allows the user to set the clear value of each channel. To configure a channel to be cleared when the CLEAR pin is activated, set the CLR_EN bit in the DAC control register for that channel (see Table 24). To write to the clear code register, set the DREG[2:0] bits to 110 (see Table 18). The default clear code is 0x0000 (for more information, see the Asynchronous Clear section).

Table 14. Programming the Gain Register

R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	D15 to D4	D3 to D0
0	Device address		0	1	0	DAC channel address		Gain adjustment	1111

Table 15. Gain Register Bit Descriptions

Gain Adjustment	G15	G14	G13 to G5	G4	G3 to G0
+4096 LSB	1	1	111111111	1	1111
+4095 LSB	1	1	111111111	0	1111
…	…	…	…	…	1111
1 LSB	0	0	000000000	1	1111
0 LSB	0	0	000000000	0	1111

Table 16. Programming the Offset Register

R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	D15 to D4	D3 to D0
0	Device address		1	0	0	DAC channel address		Offset adjustment	0000

Table 17. Offset Register Bit Descriptions

Offset Adjustment	OF15	OF14	OF13	OF12 to OF5	OF4	OF3 to OF0
+2047 LSB	1	1	1	11111111	1	0000
+2046 LSB	1	1	1	11111111	0	0000
…	…	…	…	…	…	0000
No Adjustment (Default)	1	0	0	00000000	0	0000
…	…	…	…	…	…	0000
−2047 LSB	0	0	0	00000000	1	0000
−2048 LSB	0	0	0	00000000	0	0000

Table 18. Programming the Clear Code Register

R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	D15 to D4	D3 to D0
0	Device address		1	1	0	DAC channel address		Clear code	0000

CONTROL REGISTERS

When writing to a control register, the format shown in Table 19 must be used. See Table 12 for information about the configuration of Bit D23 to Bit D16. The control registers are addressed by setting the DREG[2:0] bits (Bits[D20:D18] in the input shift register) to 111 and then setting the CREG[2:0] bits to select the specific control register (see Table 20).

Main Control Register

The main control register options are shown in Table 21 and Table 22. See the Device Features section for more information about the features controlled by the main control register.

Table 19. Input Shift Register for a Write Operation to a Control Register

MSB **LSB**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	1	1	1	DAC_AD1	DAC_AD0	CREG2	CREG1	CREG0	Data

Table 20. Control Register Addresses (CREG[2:0] Bits)

CREG2 (D15)	CREG1 (D14)	CREG0 (D13)	Control Register
0	0	0	Slew rate control register (one per channel)
0	0	1	Main control register
0	1	0	DAC control register (one per channel)
0	1	1	DC-to-DC control register
1	0	0	Software register

Table 21. Programming the Main Control Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3 to D0
0	0	1	POC	STATREAD	EWD	WD1	WD0	X[1]	ShtCctLim	OUTEN_ALL	DCDC_ALL	X[1]

[1] X = don't care.

Table 22. Main Control Register Bit Descriptions

Bit Name	Description		
POC	The POC bit determines the state of the voltage output channels during normal operation. POC = 0: the output goes to the value set by the POC hardware pin when the voltage output is not enabled (default). POC = 1: the output goes to the opposite value of the POC hardware pin when the voltage output is not enabled.		
STATREAD	Enable status readback during a write. See the Status Readback During a Write section. 0 = disable status readback (default). 1 = enable status readback.		
EWD	Enable the watchdog timer. See the Watchdog Timer section. 0 = disable the watchdog timer (default). 1 = enable the watchdog timer.		
WD1, WD0	Timeout select bits. Used to select the timeout period for the watchdog timer.		
	WD1	**WD0**	**Timeout Period (ms)**
	0	0	5
	0	1	10
	1	0	100
	1	1	200
ShtCctLim	Programmable short-circuit limit on the V_{OUT_x} pin in the event of a short-circuit condition. 0 = 16 mA (default). 1 = 8 mA.		
OUTEN_ALL	Setting this bit to 1 enables the output on all four DACs simultaneously. Do not use the OUTEN_ALL bit when using the OUTEN bit in the DAC control register.		
DCDC_ALL	Setting this bit to 1 powers up the dc-to-dc converter on all four channels simultaneously. To power down the dc-to-dc converters, all channel outputs must first be disabled. Do not use the DCDC_ALL bit when using the DC_DC bit in the DAC control register.		

DAC Control Register

The DAC control register is used to configure each DAC channel. The DAC control register options are shown in Table 23 and Table 24.

Table 23. Programming the DAC Control Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	X[1]	X[1]	X[1]	X[1]	INT_ENABLE	CLR_EN	OUTEN	RSET	DC_DC	OVRNG	R2	R1	R0

[1] X = don't care.

Table 24. DAC Control Register Bit Descriptions

Bit Name	Description			
INT_ENABLE	Powers up the dc-to-dc converter, DAC, and internal amplifiers for the selected channel. This bit applies to individual channels only; it does not enable the output. After setting this bit, it is recommended that a >200 µs delay be observed before enabling the output to reduce the output enable glitch. See Figure 30 and Figure 47 for plots of this glitch.			
CLR_EN	Per-channel clear enable bit. This bit specifies whether the selected channel is cleared when the CLEAR pin is activated. 0 = channel is not cleared when the part is cleared (default). 1 = channel is cleared when the part is cleared.			
OUTEN	Enables or disables the selected output channel. 0 = channel disabled (default). 1 = channel enabled.			
RSET	Selects the internal current sense resistor or an external current sense resistor for the selected DAC channel. 0 = external resistor selected (default). 1 = internal resistor selected.			
DC_DC	Powers up or powers down the dc-to-dc converter on the selected channel. All dc-to-dc converters can be powered up simultaneously using the DCDC_ALL bit in the main control register. To power down the dc-to-dc converter, the OUTEN and INT_ENABLE bits must also be set to 0. 0 = dc-to-dc converter is powered down (default). 1 = dc-to-dc converter is powered up.			
OVRNG	Enables 20% overrange on the voltage output channel only. No current output overrange is available. 0 = overrange disabled (default). 1 = overrange enabled.			
R2, R1, R0	Selects the output range to be enabled.			
	R2	**R1**	**R0**	**Output Range Selected**
	0	0	0	0 V to 5 V voltage range (default)
	0	0	1	0 V to 10 V voltage range
	0	1	0	±5 V voltage range
	0	1	1	±10 V voltage range
	1	0	0	4 mA to 20 mA current range
	1	0	1	0 mA to 20 mA current range
	1	1	0	0 mA to 24 mA current range

Software Register

The software register allows the user to perform a software reset of the part. This register is also used to set the user toggle bit, D11, in the status register and as part of the watchdog timer feature when that feature is enabled.

Bit D12 in the software register can be used to ensure that communication has not been lost between the MCU and the AD5735 and that the datapath lines are working properly (that is, SDIN, SCLK, and $\overline{\text{SYNC}}$).

When the watchdog timer feature is enabled, the user must write 0x195 to Bits[D11:D0] of the software register within the timeout period. If this command is not received within the timeout period, the ALERT pin signals a fault condition. This command is only required when the watchdog timer feature is enabled.

DC-to-DC Control Register

The dc-to-dc control register allows the user to configure the dc-to-dc switching frequency and phase, as well as the maximum allowable dc-to-dc output voltage. The dc-to-dc control register options are shown in Table 27 and Table 28.

Table 25. Programming the Software Register

D15	D14	D13	D12	D11 to D0
1	0	0	User program	Reset code/SPI code

Table 26. Software Register Bit Descriptions

Bit Name	Description	
User Program	This bit is mapped to Bit D11 of the status register. When this bit is set to 1, Bit D11 of the status register is set to 1. When this bit is set to 0, Bit D11 of the status register is also set to 0. This feature can be used to ensure that the SPI pins are working correctly by writing a known bit value to this register and then reading back Bit D11 from the status register.	
Reset Code/SPI Code	**Option**	**Description**
	Reset code	Writing 0x555 to Bits[D11:D0] performs a software reset of the AD5735.
	SPI code	If the watchdog timer feature is enabled, 0x195 must be written to the software register (Bits[D11:D0]) within the programmed timeout period (see Table 22).

Table 27. Programming the DC-to-DC Control Register

D15	D14	D13	D12 to D7	D6	D5 to D4	D3 to D2	D1 to D0
0	1	1	X[1]	DC-DC comp	DC-DC phase	DC-DC freq	DC-DC MaxV

[1] X = don't care.

Table 28. DC-to-DC Control Register Bit Descriptions

Bit Name	Description
DC-DC Comp	Selects the internal compensation resistor or an external compensation resistor for the dc-to-dc converter. See the DC-to-DC Converter Compensation Capacitors section and the AI_{CC} Supply Requirements—Slewing section. 0 = selects the internal 150 kΩ compensation resistor (default). 1 = bypasses the internal compensation resistor. When this bit is set to 1, an external compensation resistor must be used; this resistor is placed at the $COMP_{DCDC\_x}$ pin in series with the 10 nF dc-to-dc compensation capacitor to ground. Typically, a resistor of ~50 kΩ is recommended.
DC-DC Phase	User-programmable dc-to-dc converter phase (between channels). 00 = all dc-to-dc converters clock on the same edge (default). 01 = Channel A and Channel B clock on the same edge; Channel C and Channel D clock on the opposite edge. 10 = Channel A and Channel C clock on the same edge; Channel B and Channel D clock on the opposite edge. 11 = Channel A, Channel B, Channel C, and Channel D clock 90° out of phase from each other.
DC-DC Freq	Switching frequency for the dc-to-dc converter; this frequency is divided down from the internal 13 MHz oscillator (see Figure 68 and Figure 69). 00 = 250 kHz ± 10%. 01 = 410 kHz ± 10% (default). 10 = 650 kHz ± 10%.
DC-DC MaxV	Maximum allowed V_{BOOST_x} voltage supplied by the dc-to-dc converter. 00 = 23 V + 1 V/−1.5 V (default). 01 = 24.5 V ± 1 V. 10 = 27 V ± 1 V. 11 = 29.5 V ± 1 V.

Slew Rate Control Register

This register is used to program the slew rate control for the selected DAC channel. This feature is available on both the current and voltage outputs. The slew rate control is enabled/disabled and programmed on a per-channel basis. See Table 29 and the Digital Slew Rate Control section for more information.

READBACK OPERATION

Readback mode is invoked by setting the R/$\overline{W}$ bit = 1 in the serial input register write. See Table 30 for the bits associated with a read-back operation. The DUT_AD1 and DUT_AD0 bits, in association with Bits[RD4:RD0], select the register to be read (see Table 33). The remaining data bits in the write sequence are don't care bits. During the next SPI transfer, the data that appears on the SDO output contains the data from the previously addressed register (see Figure 4). This second SPI transfer should be either a request to read another register on a third data transfer or a no operation command. The no operation command for DUT Address 00 is 0x1CE000, for other DUT addresses, Bit D22 and Bit D21 are set accordingly.

The data read back is contained in the 16 LSBs. The MSBs consist of don't care bits. The number of don't care bits is dependent on the polarity of the first clock edge within the SYNC frame of the NOP command (see Figure 4).

If the first clock edge in the NOP command is positive, the data read back will be 24 bits in length consisting of eight don't care bits prior to the16 data bits (see Table 31).

If the first clock edge in the NOP command is negative, the data read back will be 23 bits in length consisting of seven don't care bits prior to the 16 data bits (see Table 32).

In both cases, if PEC is enabled, there must be no activity on SCLK in between the read command and NOP command otherwise an incorrect PEC may be read back (see Figure 5).

Readback Example

To read back the gain register of AD5735 Device 1, Channel A, implement the following sequence:

1. Write 0xA80000 to the input register to configure Device Address 1 for read mode with the gain register of Channel A selected. The data bits, D15 to D0, are don't care bits.
2. Execute another read command or a no operation command (0x3CE000). During this command, the data from the Channel A gain register is clocked out on the SDO line.

Table 29. Programming the Slew Rate Control Register

D15	D14	D13	D12	D11 to D7	D6 to D3	D2 to D0
0	0	0	SREN	X[1]	SR_CLOCK	SR_STEP

[1] X = don't care.

Table 30. Input Shift Register for a Read Operation

MSB								LSB
D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	RD4	RD3	RD2	RD1	RD0	X[1]

[1] X = don't care.

Table 31. Decoding Data Readback on SDO (First Clock Edge within the $\overline{SYNC}$ Frame of NOP Command is Positive)

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	Data readback

[1] X = don't care.

Table 32. Decoding Data Readback on SDO (First Clock Edge within the $\overline{SYNC}$ Frame of NOP Command is Negative)

D22	D21	D20	D19	D18	D17	D16	D15 to D0
X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	Data readback

[1] X = don't care.

Table 33. Read Addresses (Bits[RD4:RD0])

RD4	RD3	RD2	RD1	RD0	Function
0	0	0	0	0	Read DAC A data register
0	0	0	0	1	Read DAC B data register
0	0	0	1	0	Read DAC C data register
0	0	0	1	1	Read DAC D data register
0	0	1	0	0	Read DAC A control register
0	0	1	0	1	Read DAC B control register
0	0	1	1	0	Read DAC C control register
0	0	1	1	1	Read DAC D control register
0	1	0	0	0	Read DAC A gain register
0	1	0	0	1	Read DAC B gain register
0	1	0	1	0	Read DAC C gain register
0	1	0	1	1	Read DAC D gain register
0	1	1	0	0	Read DAC A offset register
0	1	1	0	1	Read DAC B offset register
0	1	1	1	0	Read DAC C offset register
0	1	1	1	1	Read DAC D offset register
1	0	0	0	0	Read DAC A clear code register
1	0	0	0	1	Read DAC B clear code register
1	0	0	1	0	Read DAC C clear code register
1	0	0	1	1	Read DAC D clear code register
1	0	1	0	0	Read DAC A slew rate control register
1	0	1	0	1	Read DAC B slew rate control register
1	0	1	1	0	Read DAC C slew rate control register
1	0	1	1	1	Read DAC D slew rate control register
1	1	0	0	0	Read status register
1	1	0	0	1	Read main control register
1	1	0	1	0	Read dc-to-dc control register

Status Register

The status register is a read-only register. This register contains any fault information, as a well as a ramp active bit (Bit D9) and a user toggle bit (Bit D11). When the STATREAD bit in the main control register is set, the status register contents can be read back on the SDO pin during every write sequence. Alternatively, if the STATREAD bit is not set, the status register can be read using the normal readback operation (see the Readback Operation section).

Table 34. Decoding the Status Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DC-DCD	DC-DCC	DC-DCB	DC-DCA	User toggle	PEC error	Ramp active	Over temp	V_{OUT_D} fault	V_{OUT_C} fault	V_{OUT_B} fault	V_{OUT_A} fault	I_{OUT_D} fault	I_{OUT_C} fault	I_{OUT_B} fault	I_{OUT_A} fault

Table 35. Status Register Bit Descriptions

Bit Name	Description
DC-DCD	In current output mode, this bit is set if the dc-to-dc converter on Channel D cannot maintain compliance, for example, if the dc-to-dc converter is reaching its V_{MAX} voltage; in this case, the I_{OUT_D} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information about the operation of this bit under this condition. In voltage output mode, this bit is set if the dc-to-dc converter on Channel D is unable to regulate to 15 V as expected. When this bit is set, it does not result in the $\overline{FAULT}$ pin going high.
DC-DCC	In current output mode, this bit is set if the dc-to-dc converter on Channel C cannot maintain compliance, for example, if the dc-to-dc converter is reaching its V_{MAX} voltage; in this case, the I_{OUT_C} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information about the operation of this bit under this condition. In voltage output mode, this bit is set if the dc-to-dc converter on Channel C is unable to regulate to 15 V as expected. When this bit is set, it does not result in the $\overline{FAULT}$ pin going high.
DC-DCB	In current output mode, this bit is set if the dc-to-dc converter on Channel B cannot maintain compliance, for example, if the dc-to-dc converter is reaching its V_{MAX} voltage; in this case, the I_{OUT_B} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information about the operation of this bit under this condition. In voltage output mode, this bit is set if the dc-to-dc converter on Channel B is unable to regulate to 15 V as expected. When this bit is set, it does not result in the $\overline{FAULT}$ pin going high.
DC-DCA	In current output mode, this bit is set if the dc-to-dc converter on Channel A cannot maintain compliance, for example, if the dc-to-dc converter is reaching its V_{MAX} voltage; in this case, the I_{OUT_A} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information about the operation of this bit under this condition. In voltage output mode, this bit is set if the dc-to-dc converter on Channel A is unable to regulate to 15 V as expected. When this bit is set, it does not result in the $\overline{FAULT}$ pin going high.
User Toggle	User toggle bit. This bit is set or cleared via the software register and can be used to verify data communications, if needed.
PEC Error	Denotes a PEC error on the last data-word received over the SPI interface.
Ramp Active	This bit is set while any output channel is slewing (digital slew rate control is enabled on at least one channel).
Over Temp	This bit is set if the AD5735 core temperature exceeds approximately 150°C.
V_{OUT_D} Fault	This bit is set if a fault is detected on the V_{OUT_D} pin.
V_{OUT_C} Fault	This bit is set if a fault is detected on the V_{OUT_C} pin.
V_{OUT_B} Fault	This bit is set if a fault is detected on the V_{OUT_B} pin.
V_{OUT_A} Fault	This bit is set if a fault is detected on the V_{OUT_A} pin.
I_{OUT_D} Fault	This bit is set if a fault is detected on the I_{OUT_D} pin.
I_{OUT_C} Fault	This bit is set if a fault is detected on the I_{OUT_C} pin.
I_{OUT_B} Fault	This bit is set if a fault is detected on the I_{OUT_B} pin.
I_{OUT_A} Fault	This bit is set if a fault is detected on the I_{OUT_A} pin.

DEVICE FEATURES

FAULT OUTPUT

The AD5735 is equipped with a $\overline{\text{FAULT}}$ pin, an active low, open-drain output that allows several AD5735 devices to be connected together to one pull-up resistor for global fault detection. The $\overline{\text{FAULT}}$ pin is forced active by any one of the following fault conditions:

- The voltage at I_{OUT_x} attempts to rise above the compliance range due to an open-loop circuit or insufficient power supply voltage. The internal circuitry that develops the fault output avoids using a comparator with windowed limits because this requires an actual output error before the $\overline{\text{FAULT}}$ output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately 1 V of remaining drive capability. Thus, the $\overline{\text{FAULT}}$ output is activated slightly before the compliance limit is reached.
- A short circuit is detected on a voltage output pin. The short-circuit current is limited to 16 mA or 8 mA, which is programmable by the user. If the AD5735 is used in unipolar supply mode, a short-circuit fault may be generated if the output voltage is below 50 mV.
- An interface error is detected due to a PEC failure (see the Packet Error Checking section).
- The core temperature of the AD5735 exceeds approximately 150°C.

The V_{OUT_x} fault, I_{OUT_x} fault, PEC error, and over temp bits of the status register are used in conjunction with the $\overline{\text{FAULT}}$ output to inform the user which fault condition caused the $\overline{\text{FAULT}}$ output to be activated.

VOLTAGE OUTPUT SHORT-CIRCUIT PROTECTION

Under normal operation, the voltage output sinks/sources up to 12 mA and maintains specified operation. The maximum output current or short-circuit current is programmable by the user and can be set to 16 mA or 8 mA. If a short circuit is detected, the $\overline{\text{FAULT}}$ pin goes low, and the relevant V_{OUT_x} fault bit is set in the status register (see Table 35).

DIGITAL OFFSET AND GAIN CONTROL

Each DAC channel has a gain (M) register and an offset (C) register, which allow trimming out of the gain and offset errors of the entire signal chain. Data from the DAC data register is operated on by a digital multiplier and adder controlled by the contents of the gain and offset registers; the calibrated DAC data is then stored in the DAC input register (see Figure 76).

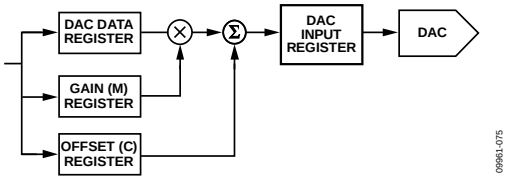


Figure 76. Digital Offset and Gain Control

Although Figure 76 indicates a multiplier and adder for each channel, the device has only one multiplier and one adder, which are shared by all four channels. This design has implications for the update speed when several channels are updated at once (see Table 3).

When data is written to the gain (M) or offset (C) register, the output is not automatically updated. Instead, the next write to the DAC channel uses the new gain and offset values to perform a new calibration and automatically updates the channel.

The output data from the calibration is routed to the DAC input register. This data is then loaded to the DAC, as described in the Serial Interface section. Both the gain register and the offset register have 12 bits of resolution. The correct order to calibrate the gain and offset is to first calibrate the gain and then calibrate the offset.

The value (in decimal) that is written to the DAC input register can be calculated as follows:

$$Code_{DACRegister} = D \times \frac{(M+1)}{2^{12}} + C - 2^{11} \quad (1)$$

where:
D is the code loaded to the DAC data register of the DAC channel.
M is the code in the gain register (default code = $2^{12} - 1$).
C is the code in the offset register (default code = 2^{11}).

STATUS READBACK DURING A WRITE

The AD5735 can be configured to read back the contents of the status register during every write sequence. This feature is enabled using the STATREAD bit in the main control register. When this feature is enabled, the user can continuously monitor the status register and act quickly in the case of a fault.

When status readback during a write is enabled, the contents of the 16-bit status register (see Table 35) are output on the SDO pin, as shown in Figure 6.

When the AD5735 is powered up, the status readback during a write feature is disabled. When this feature is enabled, readback of registers other than the status register is not available. To read back any other register, clear the STATREAD bit before following the readback sequence (see the Readback Operation section). The STATREAD bit can be set high again after the register read.

If there are multiple units on the same SDO bus which have the STATREAD feature enabled, ensure that each unit is provided a unique physical address (AD1 and AD0) in order to prevent contention on the bus.

If Packet Error Checking is enabled, the PEC values returned on a status readback during a write operation should be ignored. See the Packet Error Checking section for further information.

ASYNCHRONOUS CLEAR

CLEAR is an active high, edge sensitive input that allows the output to be cleared to a preprogrammed 12-bit code. This code is user-programmable via a per-channel 12-bit clear code register.

For a channel to be cleared, set the CLR_EN bit in the DAC control register for that channel. If the clear function on a channel is not enabled, the output remains in its current state, independent of the level of the CLEAR pin.

When the CLEAR signal returns low, the relevant outputs remain cleared until a new value is programmed to them.

PACKET ERROR CHECKING

To verify that data has been received correctly in noisy environments, the AD5735 offers the option of packet error checking based on an 8-bit cyclic redundancy check (CRC-8). The device controlling the AD5735 should generate an 8-bit frame check sequence using the following polynomial:

$$C(x) = x_8 + x_2 + x_1 + 1$$

This value is added to the end of the data-word, and 32 bits are sent to the AD5735 before $\overline{\text{SYNC}}$ goes high. If the AD5735 sees a 32-bit frame, it performs the error check when $\overline{\text{SYNC}}$ goes high. If the error check is valid, the data is written to the selected register. If the error check fails, the $\overline{\text{FAULT}}$ pin goes low and the PEC error bit in the status register is set. After the status register is read, $\overline{\text{FAULT}}$ returns high (assuming that there are no other faults), and the PEC error bit is cleared automatically. It is not recommended to tie both AD1 and AD0 low as a short low on SDIN could possibly lead to a zero-scale update for DAC A.

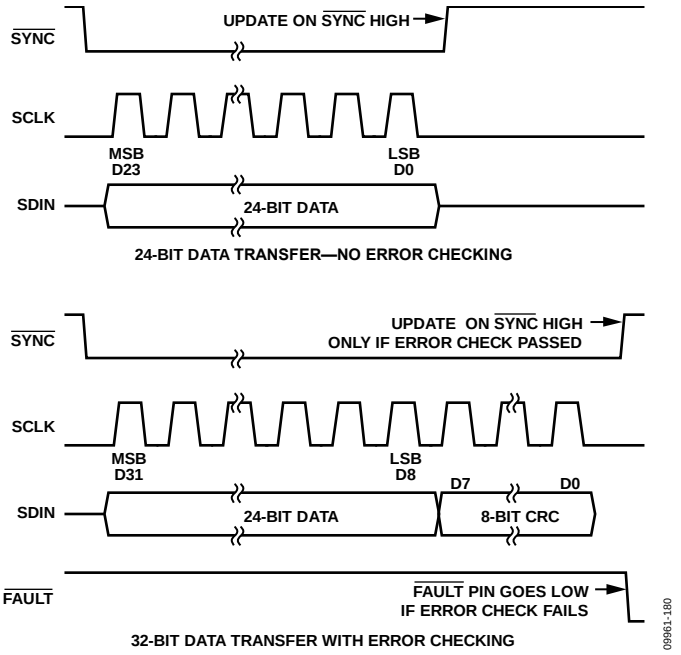


Figure 77. PEC Timing

Packet error checking can be used for transmitting and receiving data packets. If status readback during a write is enabled, the PEC values returned during the status readback operation should be ignored. If status readback during a write is disabled, the user can still use the normal readback operation to monitor status register activity with PEC.

If PEC is enabled when receiving data packets, there must be no activity on SCLK in between the read command and NOP command otherwise an incorrect PEC may be read back. See Figure 5 and the Readback Operation section for further information.

WATCHDOG TIMER

When enabled, an on-chip watchdog timer generates an alert signal if 0x195 is not written to the software register within the programmed timeout period. This feature is useful to ensure that communication has not been lost between the MCU and the AD5735 and that the datapath lines are working properly (that is, SDIN, SCLK, and $\overline{\text{SYNC}}$). If 0x195 is not received by the software register within the timeout period, the ALERT pin signals a fault condition. The ALERT pin is active high and can be connected directly to the CLEAR pin to enable a clear in the event that communication from the MCU is lost.

To enable the watchdog timer and set the timeout period (5 ms, 10 ms, 100 ms, or 200 ms), program the main control register (see Table 21 and Table 22).

ALERT OUTPUT

The AD5735 is equipped with an ALERT pin. This pin is an active high CMOS output. The AD5735 also has an internal watchdog timer. When enabled, the watchdog timer monitors SPI communications. If 0x195 is not received by the software register within the timeout period, the ALERT pin is activated.

INTERNAL REFERENCE

The AD5735 contains an integrated 5 V voltage reference with initial accuracy of ±5 mV maximum and a temperature coefficient of ±10 ppm/°C maximum. The reference voltage is buffered and is externally available for use elsewhere within the system. REFOUT must be connected to REFIN to use the internal reference.

EXTERNAL CURRENT SETTING RESISTOR

R_{SET} is an internal sense resistor that is part of the voltage-to-current conversion circuitry (see Figure 72). The stability of the output current value over temperature is dependent on the stability of the R_{SET} value. To improve the stability of the output current over temperature, the internal R_{SET} resistor, R1, can be bypassed and an external, 15 kΩ, low drift resistor can be connected to the R_{SET_x} pin of the AD5735. The external resistor is selected via the DAC control register (see Table 24).

Table 1 provides the performance specifications for the AD5735 with both the internal R_{SET} resistor and an external, 15 kΩ R_{SET} resistor. The use of an external R_{SET} resistor allows for improved performance over the internal R_{SET} resistor option. The external R_{SET} resistor specifications assume an ideal resistor; the actual performance depends on the absolute value and temperature coefficient of the resistor used. This directly affects the gain error

of the output and, thus, the total unadjusted error. To arrive at the gain/TUE error of the output with a specific external R_{SET} resistor, add the absolute error percentage of the R_{SET} resistor directly to the gain/TUE error of the AD5735 with the external R_{SET} resistor, as shown in Table 1 (expressed in % FSR).

DIGITAL SLEW RATE CONTROL

The digital slew rate control feature of the AD5735 allows the user to control the rate at which the output value changes. This feature is available on both the current and voltage outputs. With the slew rate control feature disabled, the output value changes at a rate limited by the output drive circuitry and the attached load. To reduce the slew rate, the user can enable the digital slew rate control feature using the SREN bit of the slew rate control register (see Table 29).

When slew rate control is enabled, the output, instead of slewing directly between two values, steps digitally at a rate defined by the SR_CLOCK and SR_STEP parameters. These parameters are accessible via the slew rate control register (see Table 29).

- SR_CLOCK defines the rate at which the digital slew is updated; for example, if the selected update rate is 8 kHz, the output is updated every 125 µs.
- SR_STEP defines by how much the output value changes at each update.

Together, these parameters define the rate of change of the output value. Table 36 and Table 37 list the range of values for the SR_CLOCK and SR_STEP parameters, respectively.

Table 36. Slew Rate Update Clock Options

SR_CLOCK	Update Clock Frequency[1]
0000	64 kHz
0001	32 kHz
0010	16 kHz
0011	8 kHz
0100	4 kHz
0101	2 kHz
0110	1 kHz
0111	500 Hz
1000	250 Hz
1001	125 Hz
1010	64 Hz
1011	32 Hz
1100	16 Hz
1101	8 Hz
1110	4 Hz
1111	0.5 Hz

[1] These clock frequencies are divided down from the 13 MHz internal oscillator (see Table 1, Figure 68, and Figure 69).

Table 37. Slew Rate Step Size Options

SR_STEP	Step Size (LSB)
000	1
001	2
010	4
011	16
100	32
101	64
110	128
111	256

The following equation describes the slew rate as a function of the step size, the update clock frequency, and the LSB size.

$$Slew\ Rate = \frac{Output\ Change}{Step\ Size \times Update\ Clock\ Frequency \times LSB\ Size}$$

where:
Slew Rate is expressed in seconds.
Output Change is expressed in amperes for I_{OUT_x} or in volts for V_{OUT_x}.

The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range.

When the slew rate control feature is enabled, all output changes occur at the programmed slew rate (see the DC-to-DC Converter Settling Time section for more information). For example, if the CLEAR pin is asserted, the output slews to the clear value at the programmed slew rate (assuming that the channel is enabled to be cleared).

If more than one channel is enabled for digital slew rate control, care must be taken when asserting the CLEAR pin. If a channel under slew rate control is slewing when the CLEAR pin is asserted, other channels under slew rate control may change directly to their clear code not under slew rate control.

DYNAMIC POWER CONTROL

When configured in current output mode, the AD5735 provides integrated dynamic power control using a dc-to-dc boost converter circuit. This circuit reduces power consumption compared with standard designs.

In standard current input module designs, the load resistor values can range from typically 50 Ω to 750 Ω. Output module systems must source enough voltage to meet the compliance voltage requirement across the full range of load resistor values. For example, in a 4 mA to 20 mA loop when driving 20 mA, a compliance voltage of >15 V is required. When driving 20 mA into a 50 Ω load, a compliance voltage of only 1 V is required.

The AD5735 circuitry senses the output voltage and regulates this voltage to meet the compliance requirements plus a small headroom voltage. The AD5735 is capable of driving up to 24 mA through a 1 kΩ load.

DC-TO-DC CONVERTERS

The AD5735 contains four independent dc-to-dc converters. These are used to provide dynamic control of the V_{BOOST_x} supply voltage for each channel (see Figure 72). Figure 78 shows the discrete components needed for the dc-to-dc circuitry, and the following sections describe component selection and operation of this circuitry.

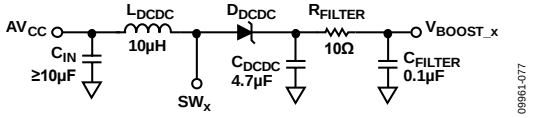


Figure 78. DC-to-DC Circuit

Table 38. Recommended Components for a DC-to-DC Converter

Symbol	Component	Value	Manufacturer
L_{DCDC}	XAL4040-103	10 µH	Coilcraft®
C_{DCDC}	GRM32ER71H475KA88L	4.7 µF	Murata
D_{DCDC}	PD3S160-7	0.55 V_F	Diodes, Inc.

It is recommended that a 10 Ω, 100 nF low-pass RC filter be placed after C_{DCDC}. This filter consumes a small amount of power but reduces the amount of ripple on the V_{BOOST_x} supply.

DC-to-DC Converter Operation

The on-board dc-to-dc converters use a constant frequency, peak current mode control scheme to step up an AV_{CC} input of 4.5 V to 5.5 V to drive the AD5735 output channel. These converters are designed to operate in discontinuous conduction mode with a duty cycle of <90% typical. Discontinuous conduction mode refers to a mode of operation where the inductor current goes to zero for an appreciable percentage of the switching cycle. The dc-to-dc converters are nonsynchronous; that is, they require an external Schottky diode.

DC-to-DC Converter Output Voltage

When a channel current output is enabled, the converter regulates the V_{BOOST_x} supply to 7.4 V (±5%) or ($I_{OUT} \times R_{LOAD}$ + Headroom), whichever is greater (see Figure 52 for a plot of headroom supplied vs. output current). In voltage output mode with the output disabled, the converter regulates the V_{BOOST_x} supply to 15 V (±5%). In current output mode with the output disabled, the converter regulates the V_{BOOST_x} supply to 7.4 V (±5%).

Within a channel, the V_{OUT_x} and I_{OUT_x} stages share a common V_{BOOST_x} supply; therefore, the outputs of the I_{OUT_x} and V_{OUT_x} stages can be tied together (see the Voltage and Current Output Pins on the Same Terminal section).

DC-to-DC Converter Settling Time

In current output mode, the settling time for a step greater than ~1 V ($I_{OUT} \times R_{LOAD}$) is dominated by the settling time of the dc-to-dc converter. The exception to this is when the required voltage at the I_{OUT_x} pin plus the compliance voltage is below 7.4 V (±5%). Figure 48 shows a typical plot of the output settling time. This plot is for a 1 kΩ load. The settling time for smaller loads is faster. The settling time for current steps less than 24 mA is also faster.

DC-to-DC Converter V_{MAX} Functionality

The maximum V_{BOOST_x} voltage is set in the dc-to-dc control register (23 V, 24.5 V, 27 V, or 29.5 V; see Table 28). When the maximum voltage is reached, the dc-to-dc converter is disabled, and the V_{BOOST_x} voltage is allowed to decay by ~0.4 V. After the V_{BOOST_x} voltage decays by ~0.4 V, the dc-to-dc converter is reenabled, and the voltage ramps up again to V_{MAX}, if still required. This operation is shown in Figure 79.

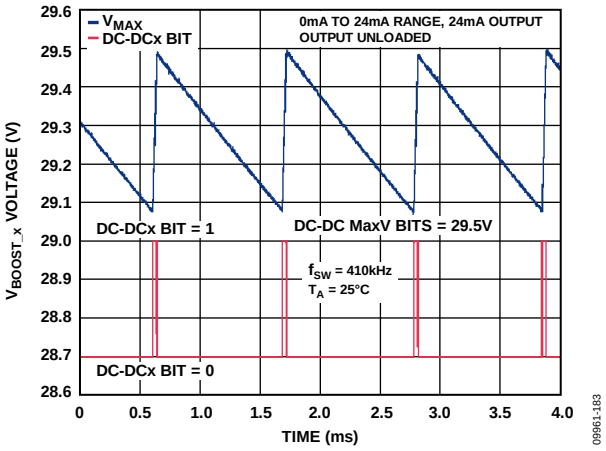


Figure 79. Operation on Reaching V_{MAX}

As shown in Figure 79, the DC-DCx bit in the status register is asserted when the AD5735 ramps up to the V_{MAX} value but is deasserted when the voltage decays to V_{MAX} − ~0.4 V.

DC-to-DC Converter On-Board Switch

The AD5735 contains a 0.425 Ω internal switch. The switch current is monitored on a pulse-by-pulse basis and is limited to 0.8 A peak current.

DC-to-DC Converter Switching Frequency and Phase

The AD5735 dc-to-dc converter switching frequency can be selected from the dc-to-dc control register (see Table 28). The phasing of the channels can also be adjusted so that the dc-to-dc converters can clock on different edges. For typical applications, a 410 kHz frequency is recommended. At light loads (low output current and small load resistor), the dc-to-dc converter enters a pulse-skipping mode to minimize switching power dissipation.

DC-to-DC Converter Inductor Selection

For typical 4 mA to 20 mA applications, a 10 µH inductor (such as the XAL4040-103 from Coilcraft), combined with a switching frequency of 410 kHz, allows up to 24 mA to be driven into a load resistance of up to 1 kΩ with an AV_{CC} supply of 4.5 V to 5.5 V. It is important to ensure that the inductor can handle the peak current without saturating, especially at the maximum ambient temperature. If the inductor enters saturation mode, efficiency decreases. The inductance value also drops during saturation and may result in the dc-to-dc converter circuit not being able to supply the required output power.

DC-to-DC Converter External Schottky Diode Selection

The AD5735 requires an external Schottky diode for correct operation. Ensure that the Schottky diode is rated to handle the maximum reverse breakdown voltage expected in operation and that the maximum junction temperature of the diode is not exceeded. The average current of the diode is approximately equal to the I_{LOAD} current. Diodes with larger forward voltage drops result in a decrease in efficiency.

DC-to-DC Converter Compensation Capacitors

Because the dc-to-dc converter operates in discontinuous conduction mode, the uncompensated transfer function is essentially a single-pole transfer function. The pole frequency of the transfer function is determined by the output capacitance, input and output voltage, and output load of the dc-to-dc converter. The AD5735 uses an external capacitor in conjunction with an internal 150 kΩ resistor to compensate the regulator loop.

Alternatively, an external compensation resistor can be used in series with the compensation capacitor by setting the DC-DC comp bit in the dc-to-dc control register (see Table 28). In this case, a resistor of ~50 kΩ is recommended. The advantages of this configuration are described in the AI_{CC} Supply Requirements—Slewing section. For typical applications, a 10 nF dc-to-dc compensation capacitor is recommended.

DC-to-DC Converter Input and Output Capacitor Selection

The output capacitor affects the ripple voltage of the dc-to-dc converter and indirectly limits the maximum slew rate at which the channel output current can rise. The ripple voltage is caused by a combination of the capacitance and the equivalent series resistance (ESR) of the capacitor. For typical applications, a ceramic capacitor of 4.7 µF is recommended. Larger capacitors or parallel capacitors improve the ripple at the expense of reduced slew rate. Larger capacitors also affect the current requirements of the AV_{CC} supply while slewing (see the AI_{CC} Supply Requirements—Slewing section). The capacitance at the output of the dc-to-dc converter should be >3 µF under all operating conditions.

The input capacitor provides much of the dynamic current required for the dc-to-dc converter and should be a low ESR component. For the AD5735, a low ESR tantalum or ceramic capacitor of 10 µF is recommended for typical applications. Ceramic capacitors must be chosen carefully because they can exhibit a large sensitivity to dc bias voltages and temperature. X5R or X7R dielectrics are preferred because these capacitors remain stable over wider operating voltage and temperature ranges. Care must be taken if selecting a tantalum capacitor to ensure a low ESR value.

AI_{CC} SUPPLY REQUIREMENTS—STATIC

The dc-to-dc converter is designed to supply a V_{BOOST_x} voltage of

$$V_{BOOST\_x} = I_{OUT} \times R_{LOAD} + Headroom \quad (2)$$

See Figure 52 for a plot of headroom supplied vs. output current. Therefore, for a fixed load and output voltage, the output current of the dc-to-dc converter can be calculated by the following formula:

$$AI_{CC} = \frac{PowerOut}{Efficiency \times AV_{CC}} = \frac{I_{OUT} \times V_{BOOST}}{\eta_{V_{BOOST}} \times AV_{CC}} \quad (3)$$

where:

I_{OUT} is the output current from I_{OUT_x} in amperes.

$\eta_{V_{BOOST}}$ is the efficiency at V_{BOOST_x} as a fraction (see Figure 54 and Figure 55).

AI_{CC} SUPPLY REQUIREMENTS—SLEWING

The AI_{CC} current requirement while slewing is greater than in static operation because the output power increases to charge the output capacitance of the dc-to-dc converter. This transient current can be quite large (see Figure 80), although the methods described in the Reducing AI_{CC} Current Requirements section can reduce the requirements on the AV_{CC} supply.

If not enough AI_{CC} current can be provided, the AV_{CC} voltage drops. Due to this AV_{CC} drop, the AI_{CC} current required for slewing increases further, causing the voltage at AV_{CC} to drop further (see Equation 3). In this case, the V_{BOOST_x} voltage and, therefore, the output voltage, may never reach their intended values. Because the AV_{CC} voltage is common to all channels, this voltage drop may also affect other channels.

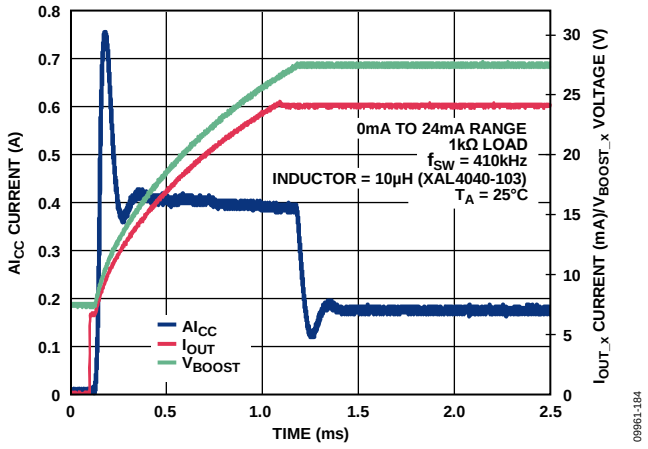


Figure 80. AI_{CC} Current vs. Time for 24 mA Step Through 1 kΩ Load with Internal Compensation Resistor

Reducing AI_{CC} Current Requirements

Two main methods can be used to reduce the AI_{CC} current requirements. One method is to add an external compensation resistor, and the other is to use slew rate control. These methods can be used together.

Adding an External Compensation Resistor

A compensation resistor can be placed at the $COMP_{DCDC\_x}$ pin in series with the 10 nF compensation capacitor. A 51 kΩ external compensation resistor is recommended. This compensation increases the slew time of the current output but reduces the AI_{CC} transient current requirements. Figure 81 shows a plot of AI_{CC} current for a 24 mA step through a 1 kΩ load when using a 51 kΩ compensation resistor. The compensation resistor reduces the current requirements through smaller loads even further, as shown in Figure 82.

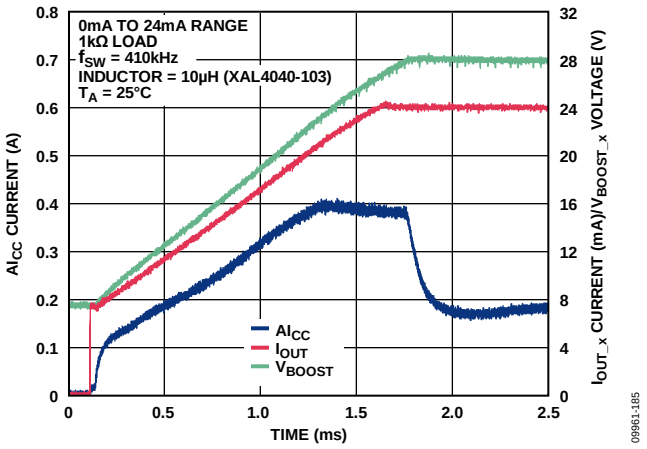


Figure 81. AI_{CC} Current vs. Time for 24 mA Step Through 1 kΩ Load with External 51 kΩ Compensation Resistor

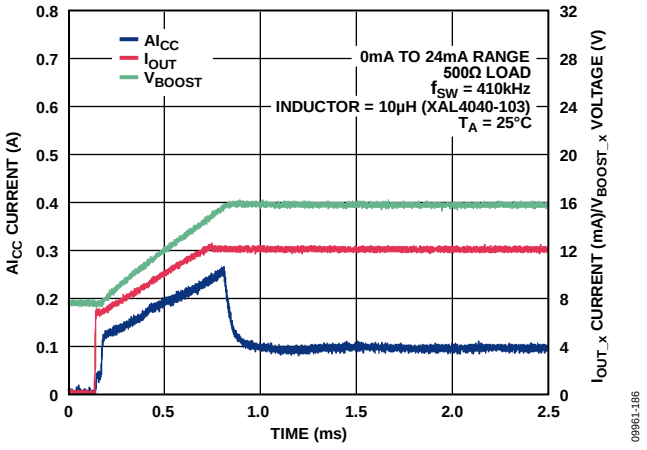


Figure 82. AI_{CC} Current vs. Time for 24 mA Step Through 500 Ω Load with External 51 kΩ Compensation Resistor

Using Slew Rate Control

Using slew rate control can greatly reduce the current requirements of the AV_{CC} supply, as shown in Figure 83.

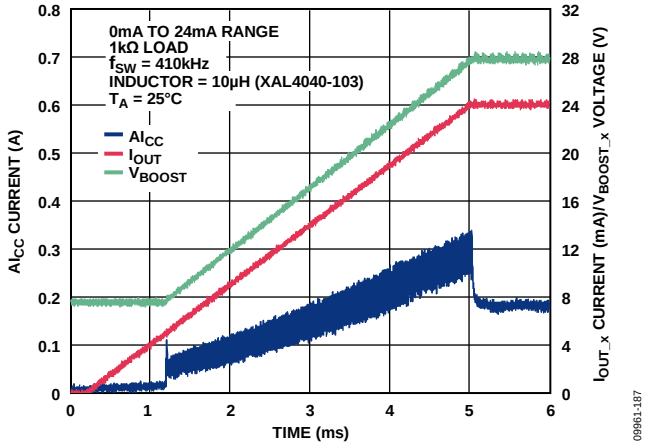


Figure 83. AI_{CC} Current vs. Time for 24 mA Step Through 1 kΩ Load with Slew Rate Control

When using slew rate control, it is important to remember that the output cannot slew faster than the dc-to-dc converter. The dc-to-dc converter slews slowest at higher currents through large loads (for example, 1 kΩ). The slew rate is also dependent on the configuration of the dc-to-dc converter. Two examples of the dc-to-dc converter output slew are shown in Figure 81 and Figure 82. (V_{BOOST} corresponds to the output voltage of the dc-to-dc converter.)

APPLICATIONS INFORMATION

VOLTAGE AND CURRENT OUTPUT PINS ON THE SAME TERMINAL

When using a channel of the AD5735, the current and voltage output pins can be connected to two separate terminals or tied together and connected to a single terminal. The two output pins can be tied together because only the voltage output or the current output can be enabled at any one time. When the current output is enabled, the voltage output is in tristate mode, and when the voltage output is enabled, the current output is in tristate mode. When the two output pins are tied together, the POC pin must be tied low and the POC bit in the main control register set to 0, or, if the POC pin is tied high, the POC bit in the main control register must be set to 1 before the current output is enabled.

As shown in the Absolute Maximum Ratings section, the output tolerances are the same for both the voltage and current output pins. The $+V_{SENSE\_x}$ and $-V_{SENSE\_x}$ connections are buffered so that current leakage into these pins is negligible when the part is operated in current output mode.

CURRENT OUTPUT MODE WITH INTERNAL R_{SET}

When using the internal R_{SET} resistor in current output mode, the output is significantly affected by how many other channels using the internal R_{SET} are enabled and by the dc crosstalk from these channels. The internal R_{SET} specifications in Table 1 are for all four channels enabled with the internal R_{SET} selected and outputting the same code.

For every channel enabled with the internal R_{SET}, the offset error decreases. For example, with one current output enabled using the internal R_{SET}, the offset error is 0.075% FSR. This value decreases proportionally as more current channels are enabled; the offset error is 0.056% FSR on each of two channels, 0.029% FSR on each of three channels, and 0.01% FSR on each of four channels.

Similarly, the dc crosstalk when using the internal R_{SET} is proportional to the number of current output channels enabled with the internal R_{SET}. For example, with the measured channel at 0x8000 and another channel going from zero to full scale, the dc crosstalk is −0.011% FSR. With two other channels going from zero to full scale, the dc crosstalk is −0.019% FSR, and with all three other channels going from zero to full scale, it is −0.025% FSR.

For the full-scale error measurement in Table 1, all channels are at 0xFFFF. This means that as any channel goes to zero scale, the full-scale error increases due to the dc crosstalk. For example, with the measured channel at 0xFFFF and three channels at zero scale, the full-scale error is 0.025% FSR. Similarly, if only one channel is enabled in current output mode with the internal R_{SET}, the full-scale error is 0.025% FSR + 0.075% FSR = 0.1% FSR.

PRECISION VOLTAGE REFERENCE SELECTION

To achieve the optimum performance from the AD5735 over its full operating temperature range, a precision voltage reference must be used. Care should be taken with the selection of the precision voltage reference. The voltage applied to the reference inputs is used to provide a buffered reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the AD5735.

Four possible sources of error must be considered when choosing a voltage reference for high accuracy applications: initial accuracy, long-term drift, temperature coefficient of the output voltage, and output voltage noise.

Initial accuracy error on the output voltage of an external reference can lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with a low initial accuracy error specification is preferred. Choosing a reference with an output trim adjustment, such as the ADR435, allows a system designer to trim out system errors by setting the reference voltage to a voltage other than the nominal. The trim adjustment can be used at any temperature to trim out any error.

Long-term drift is a measure of how much the reference output voltage drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime.

The temperature coefficient of the reference output voltage affects INL, DNL, and TUE. A reference with a tight temperature coefficient specification should be chosen to reduce the dependence of the DAC output voltage on ambient temperature.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise must be considered. Choosing a reference with as low an output noise voltage as practical for the system resolution required is important. Precision voltage references such as the ADR435 (XFET® design) produce low output noise in the 0.1 Hz to 10 Hz bandwidth. However, as the circuit bandwidth increases, filtering the output of the reference may be required to minimize the output noise.

Table 39. Recommended Precision Voltage References

Part No.	Initial Accuracy (mV Maximum)	Long-Term Drift (ppm Typical)	Temperature Coefficient (ppm/°C Maximum)	0.1 Hz to 10 Hz Noise (µV p-p Typical)
ADR445	±2	50	3	2.25
ADR02	±3	50	3	10
ADR435	±2	40	3	8
ADR395	±5	50	9	8
AD586	±2.5	15	10	4

DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads, a capacitor may be required between the I_{OUT_x} pin and the AGND pin to ensure stability. A 0.01 µF capacitor between I_{OUT_x} and AGND ensures stability of a load of 50 mH. The capacitive component of the load may cause slower settling, although this may be masked by the settling time of the AD5735. There is no maximum capacitance limit for the current output of the AD5735.

TRANSIENT VOLTAGE PROTECTION

The AD5735 contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5735 from excessively high voltage transients, external power diodes and a surge current limiting resistor (R_P) are required, as shown in Figure 84. A typical value for R_P is 10 Ω. The two protection diodes and the resistor (R_P) must have appropriate power ratings.

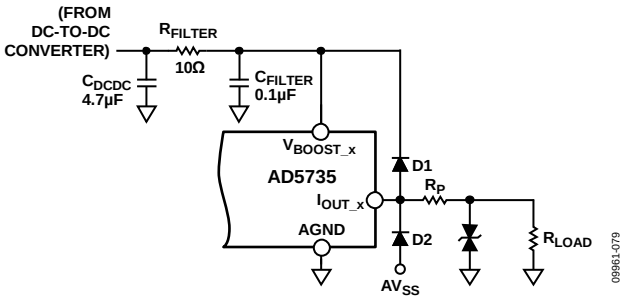


Figure 84. Output Transient Voltage Protection

Further protection can be provided using transient voltage suppressors (TVSs), also referred to as transorbs. These components are available as unidirectional suppressors, which protect against positive high voltage transients, and as bidirectional suppressors, which protect against both positive and negative high voltage transients. Transient voltage suppressors are available in a wide range of standoff and breakdown voltage ratings. The TVS should be sized with the lowest breakdown voltage possible while not conducting in the functional range of the current output.

It is recommended that all field connected nodes be protected. The voltage output node can be protected with a similar circuit, where D2 and the transorb are connected to AV_{SS}. For the voltage output node, the $+V_{SENSE\_x}$ pin should also be protected with a large value series resistance to the transorb, such as 5 kΩ. In this way, the I_{OUT_x} and V_{OUT_x} pins can also be tied together and share the same protection circuitry.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5735 is via a serial bus that uses a protocol compatible with microcontrollers and DSP processors. The communication channel is a 3-wire minimum interface consisting of a clock signal, a data signal, and a latch signal. The AD5735 requires a 24-bit data-word with data valid on the falling edge of SCLK.

The DAC output update is initiated either on the rising edge of $\overline{LDAC}$ or, if $\overline{LDAC}$ is held low, on the rising edge of $\overline{SYNC}$. The contents of the registers can be read using the readback function.

AD5735-to-ADSP-BF527 Interface

The AD5735 can be connected directly to the SPORT interface of the ADSP-BF527, an Analog Devices, Inc., Blackfin® DSP. Figure 85 shows how the SPORT interface can be connected to control the AD5735.

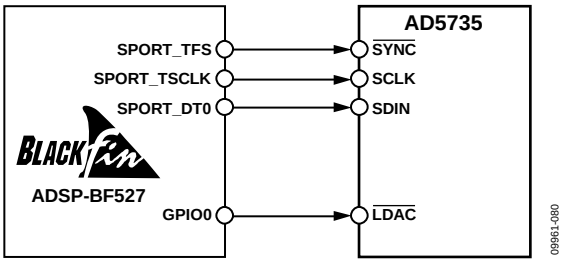


Figure 85. AD5735-to-ADSP-BF527 SPORT Interface

LAYOUT GUIDELINES

Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5735 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5735 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

The $GNDSW_x$ pin and the ground connection for the AV_{CC} supply are referred to as PGND. PGND should be confined to certain areas of the board, and the PGND-to-AGND connection should be made at one point only.

Supply Decoupling

The AD5735 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitors should have low effective series resistance (ESR) and low effective series inductance (ESL), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

Traces

The power supply lines of the AD5735 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to prevent radiating noise to other parts of the board and should never be run near the reference inputs. A ground line routed between the SDIN and SCLK traces helps reduce crosstalk between them (not required on a multilayer board that has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other to reduce the effects of feedthrough on the board. A microstrip technique is by far the best method, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, and signal traces are placed on the solder side.

DC-to-DC Converters

To achieve high efficiency, good regulation, and stability, a well-designed printed circuit board layout is required.

Follow these guidelines when designing printed circuit boards (see Figure 78):

- Keep the low ESR input capacitor, C_{IN}, close to AV_{CC} and PGND.
- Keep the high current path from C_{IN} through the inductor (L_{DCDC}) to SW_x and PGND as short as possible.
- Keep the high current path from C_{IN} through the inductor (L_{DCDC}), the diode (D_{DCDC}), and the output capacitor (C_{DCDC}) as short as possible.
- Keep high current traces as short and as wide as possible. The path from C_{IN} through the inductor (L_{DCDC}) to SW_x and PGND should be able to handle a minimum of 1 A.
- Place the compensation components as close as possible to the $COMP_{DCDC\_x}$ pin.
- Avoid routing high impedance traces near any node connected to SW_x or near the inductor to prevent radiated noise injection.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The Analog Devices *i*Coupler® products can provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5735 makes it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 86 shows a 4-channel isolated interface to the AD5735 using an ADuM1411. For more information, visit www.analog.com.

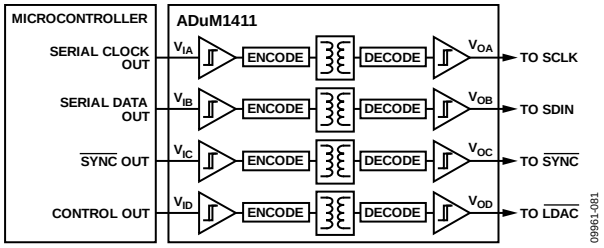
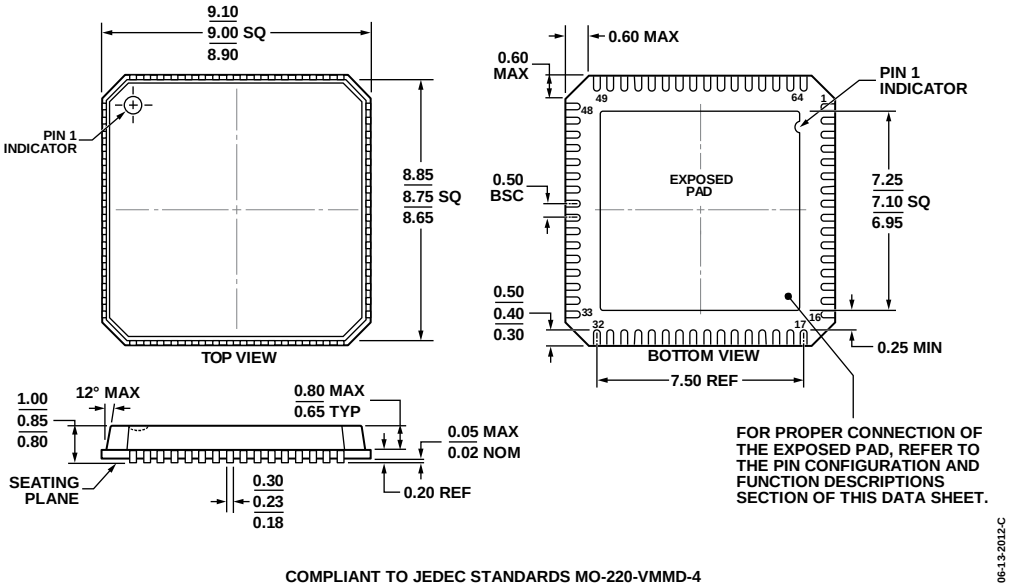


Figure 86. 4-Channel Isolated Interface to the AD5735

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 87. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution (Bits)	Temperature Range	Package Description	Package Option
AD5735ACPZ	12	−40°C to +105°C	64-Lead LFCSP_VQ	CP-64-3
AD5735ACPZ-REEL7	12	−40°C to +105°C	64-Lead LFCSP_VQ	CP-64-3

[1] Z = RoHS Compliant Part.

NOTES

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