



FEATURES

- Support for CCD and CMOS image sensors
- 4 AFE channels
- 1.8 V analog and digital core supply voltage
- Serial data output with reduced range LVDS outputs
- Differential analog inputs
- CDS or SHA configuration (CDS bypass) with
 - −3 dB, 0 dB, +3 dB, and +6 dB gain
- 6 dB to 42 dB, 10-bit variable gain amplifier (VGA)
- 14-bit, 72 MHz analog-to-digital converter (ADC)
- Black level clamp with variable level control
- Precision Timing* core with 220 ps resolution at 72 MHz

APPLICATIONS

- Digital video cameras
- Digital still cameras
- Medical Imaging
- High speed industrial cameras

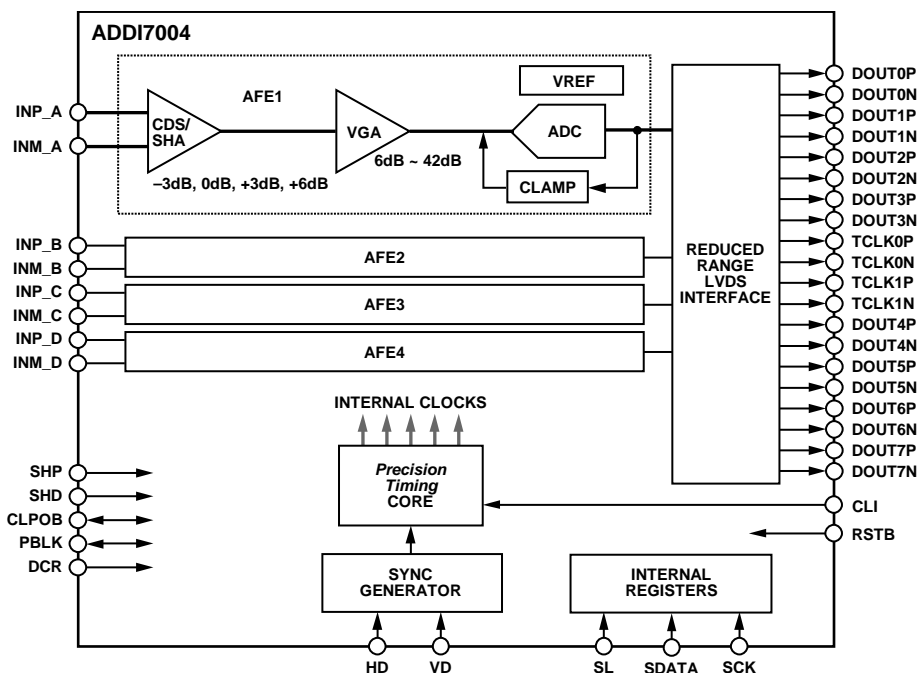
GENERAL DESCRIPTION

The [ADDI7004](#) is a highly integrated, quad-channel, HD image signal processor for high speed imaging applications. Each channel is specified at pixel rates of up to 72 MHz and consists of a complete analog front end (AFE) with ADC conversion. The *Precision Timing*™ core allows adjustment of the correlated double sampler (CDS) and sample-and-hold amplifier (SHA) clocks with 220 ps resolution at 72 MHz operation. The [ADDI7004](#) also contains a reduced range low voltage differential signaling (LVDS) interface for the dual-channel data outputs.

Each analog front end includes black level clamping, a CDS/SHA, a VGA, and a 72 MHz, 14-bit analog-to-digital converter (ADC). Operation is programmed using a 3-wire serial interface.

Packaged in a space-saving, 6 mm × 6 mm, 76-ball BGA, the [ADDI7004](#) is specified over an operating temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. THE CIRCUITRY FOR AFE1 TO AFE4 IS IDENTICAL.

Figure 1.

For more information on the [ADDI7004](#), email Analog Devices, Inc., at afe.ccd@analog.com.

Rev. SpE

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ADDI7004* Product Page Quick Links

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Comparable Parts

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Documentation

Data Sheet

- ADDI7004: Quad-Channel, HD Image Signal Processor with Precision Timing Core Data Sheet

Design Resources

- ADDI7004 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

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