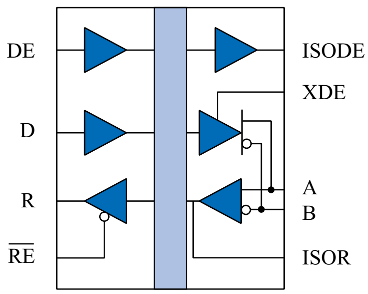
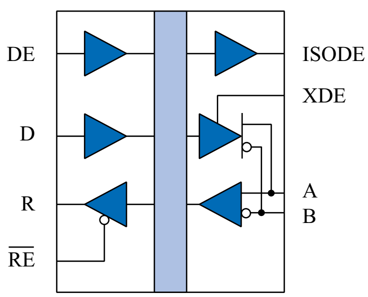
# Low-Cost Isolated RS-485 Transceivers

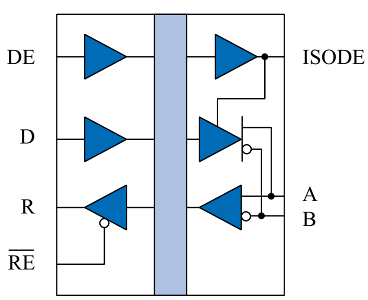
## Functional Diagrams




**IL3085-1**
(QSOP)



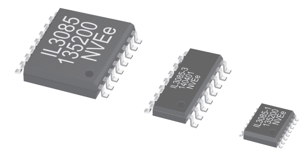

**IL3085-3**
(narrow-body)




**IL3085**
(wide-body)

| $V_{ID}$ (A-B) | DE | $\overline{RE}$ | R | D | Mode |
|---|---|---|---|---|---|
| ≥ 200 mV | L | L | H | X | Receive |
| ≤−200 mV | L | L | L | X | Receive |
| ≥ 1.5 V | H | L | H | H | Drive |
| ≤−1.5 V | H | L | L | L | Drive |
| X | X | H | Z | X | Hi-Z R |
| Open | L | L | H | X | Receive |

## Features




- 4 Mbps data rate
- Supports up to 32 nodes
- 3 V to 5 V power supplies
- 50 kV/µs typ.; 30 kV/µs min. common mode transient immunity
- Low quiescent supply current
- 600 $V_{RMS}$ working voltage per VDE V 0884-10
- 2500 $V_{RMS}$ isolation voltage per UL 1577
- 44000 year barrier life
- 7 kV bus ESD protection
- Low EMC footprint
- Thermal shutdown protection
- −40°C to +85°C temperature range
- Meets or exceeds ANSI RS-485 and ISO 8482:1987(E)
- UL 1577 recognized; IEC 60747-5-5 (VDE 0884) certified
- QSOP, 0.15" SOIC, and 0.3" True 8™ mm 16-pin SOIC packages

## Applications

- Factory automation
- Industrial control networks
- Building environmental controls
- Equipment covered under IEC 61010-1 Edition 3
- 5 $kV_{RMS}$ rated IEC 60601-1 medical applications

## Description

The IL3085 is a galvanically isolated, high-speed differential bus transceiver, designed for bidirectional data communication on balanced transmission lines. The device uses NVE's patented* IsoLoop spintronic Giant Magnetoresistance (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The wide-body version provides true 8 mm creepage. Narrow-body and QSOP packages offer unprecedented miniaturization.

The IL3085 delivers at least 1.5 V into a 27 Ω load for excellent data integrity over long cable lengths. The device is compatible with 3.3 V input supplies, allowing interface to standard microcontrollers without additional level shifting.

Current limiting and thermal shutdown features protect against output short circuits and bus contention that may cause excessive power dissipation. Receiver inputs feature a "fail-safe if open" design, ensuring a logic high R-output if A/B are floating.

IsoLoop® is a registered trademark of NVE Corporation.
*U.S. Patent number 5,831,426; 6,300,617 and others.

**REV. G**

## Absolute Maximum Ratings[11]

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | −55 | | 150 | °C | |
| Junction Temperature | $T_J$ | −55 | | 150 | °C | |
| Ambient Operating Temperature | $T_A$ | −40 | | 85 | °C | |
| Voltage Range at A or B Bus Pins | | −8 | | 12.5 | V | |
| Supply Voltage[1] | $V_{DD1}$, $V_{DD2}$ | −0.5 | | 7 | V | |
| Digital Input Voltage | | −0.5 | | $V_{DD}$ + 0.5 | V | |
| Digital Output Voltage | | −0.5 | | $V_{DD}$ + 1 | V | |
| ESD (all bus nodes) | | 7 | | | kV | HBM |

## Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD1}$<br>$V_{DD2}$ | 3.0<br>4.5 | | 5.5<br>5.5 | V | |
| Junction Temperature | $T_J$ | −40 | | 100 | °C | |
| Input Voltage at any Bus Terminal (separately or common mode) | $V_I$<br>$V_{IC}$ | | | 12<br>−7 | V | |
| High-Level Digital Input Voltage | $V_{IH}$ | 2.4<br>3.0 | | $V_{DD1}$ | V | $V_{DD1}$ = 3.3 V<br>$V_{DD1}$ = 5.0 V |
| Low-Level Digital Input Voltage | $V_{IL}$ | 0 | | 0.8 | V | |
| Differential Input Voltage[2] | $V_{ID}$ | | | +12 / −7 | V | |
| High-Level Output Current (Driver) | $I_{OH}$ | | | 60 | mA | |
| High-Level Digital Output Current (Receiver) | $I_{OH}$ | | | 8 | mA | |
| Low-Level Output Current (Driver) | $I_{OL}$ | −60 | | | mA | |
| Low-Level Digital Output Current (Receiver) | $I_{OL}$ | −8 | | | mA | |
| Ambient Operating Temperature | $T_A$ | −40 | | 85 | °C | |
| Digital Input Signal Rise and Fall Times | $t_{IR}$, $t_{IF}$ | DC Stable | | | | |

## Insulation Specifications

| Parameter | | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| Creepage Distance (external) | IL3085-1E<br>IL3085-3E<br>IL3085E | | 3.2<br>4.0<br>8.03 | <br><br>8.3 | | mm | Per IEC 60601 |
| Total Barrier Thickness (internal) | | | 0.012 | 0.013 | | mm | |
| Barrier Resistance | | $R_{IO}$ | | $>10^{14}$ | | Ω | 500 V |
| Barrier Capacitance | | $C_{IO}$ | | 7 | | pF | f = 1 MHz |
| Leakage Current | | | | 0.2 | | $\mu A_{RMS}$ | 240 $V_{RMS}$, 60 Hz |
| Comparative Tracking Index | | CTI | ≥175 | | | V | Per IEC 60112 |
| High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life) | AC<br>DC | $V_{IO}$ | 1000<br>1500 | | | $V_{RMS}$<br>$V_{DC}$ | At maximum operating temperature |
| Barrier Life | | | | 44000 | | Years | 100°C, 1000 $V_{RMS}$, 60% CL activation energy |

## Thermal Characteristics

| Parameter | | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| Junction–Ambient Thermal Resistance | QSOP<br>0.15" SOIC<br>0.3" SOIC | $\theta_{JA}$ | | 60<br>60<br>60 | | °C/W | Soldered to double-sided board; free air |
| Junction–Case (Top) Thermal Resistance | QSOP<br>0.15" SOIC<br>0.3" SOIC | $\Psi_{JT}$ | | 10<br>10<br>20 | | °C/W | |
| Power Dissipation | QSOP<br>0.15" SOIC<br>0.3" SOIC | $P_D$ | | | 675<br>700<br>800 | mW | |



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## Safety and Approvals

***VDE V 0884-10*** (VDE V 0884-11 pending; Basic Isolation; VDE File Number 5016933-4880-0001)

- Working Voltage ($V_{IORM}$) 600 $V_{RMS}$ (848 $V_{PK}$); basic insulation; pollution degree 2
- Isolation voltage ($V_{ISO}$) 2500 $V_{RMS}$
- Transient overvoltage ($V_{IOTM}$) 4000 $V_{PK}$
- Surge rating 4000 V
- Each part tested at 1590 $V_{PK}$ for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 $V_{PK}$ for 60 sec.; then 1358 $V_{PK}$ for 10 sec. with 5 pC partial discharge limit

| Safety-Limiting Values | Symbol | Value | Units |
|---|---|---|---|
| Safety rating ambient temperature | $T_S$ | 180 | °C |
| Safety rating power (180°C) | $P_S$ | 270 | mW |
| Supply current safety rating (total of supplies) | $I_S$ | 54 | mA |

***IEC 61010-1*** (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)
Reinforced Insulation; Pollution Degree II; Material Group III

| Part No. Suffix | Package | Working Voltage |
|---|---|---|
| -1 | QSOP | 150 $V_{RMS}$ |
| -3 | SOIC | 150 $V_{RMS}$ |
| None | True 8™ Wide-body SOIC | 300 $V_{RMS}$ |

***UL 1577*** (Component Recognition Program File Number E207481)
Each part tested at 3000 $V_{RMS}$ (4240 $V_{PK}$) for 1 second; each lot sample tested at 2500 $V_{RMS}$ (3530 $V_{PK}$) for 1 minute

## Soldering Profile

Per JEDEC J-STD-020C, MSL 1



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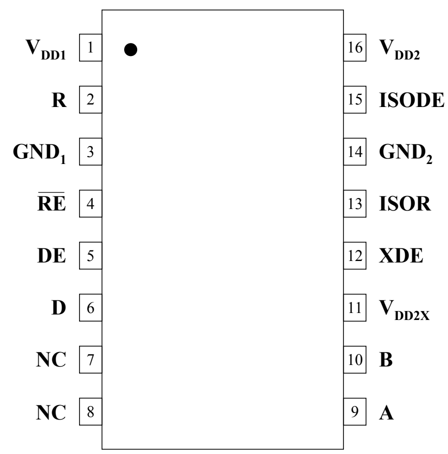
## IL3085-1 (QSOP Package) Pin Connections

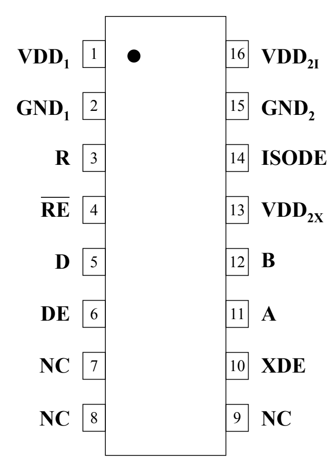
| | | |
|---|---|---|
| 1 | $V_{DD1}$ | Input power supply |
| 2 | R | Output data from bus |
| 3 | $GND_1$ | Input power supply ground return |
| 4 | $\overline{RE}$ | Read data enable<br>(if $\overline{RE}$ is high, R= high impedance) |
| 5 | DE | Drive enable |
| 6 | D | Data input to bus |
| 7, 8 | NC | No internal connection |
| 9 | A | Non-inverting bus line |
| 10 | B | Inverting bus line |
| 11 | $V_{DD2X}$ | Output transceiver power supply<br>(normally connected to pin 16) |
| 12 | XDE | Transceiver Device Enable input enables the transceiver from the bus side, or is connected to ISODE to enable the transceiver from the controller-side DE input.<br>(this input should not be left unterminated) |
| 13 | ISOR | Isolated R output<br>(for testing; no connection should be made to this pin) |
| 14 | $GND_2$ | Output power supply ground return. |
| 15 | ISODE | Isolated DE output<br>(normally connected to pin 12) |
| 16 | $V_{DD2I}$ | Output isolation power supply<br>(normally connected to pin 11) |




IL3085-1

## IL3085-3 (0.15" SOIC Package) Pin Connections

| | | |
|---|---|---|
| 1 | $V_{DD1}$ | Input power supply |
| 2 | $GND_1$ | Input power supply ground return |
| 3 | R | Output data from bus |
| 4 | $\overline{RE}$ | Read data enable<br>(if $\overline{RE}$ is high, R= high impedance) |
| 5 | D | Data input to bus |
| 6 | DE | Drive enable |
| 7, 8, 9 | NC | No internal connection |
| 10 | XDE | Transceiver Device Enable input enables the transceiver from the bus side, or is connected to ISODE to enable the transceiver from the controller-side DE input.<br>(this input should not be left unterminated) |
| 11 | A | Non-inverting bus line |
| 12 | B | Inverting bus line |
| 13 | $V_{DD2X}$ | Output transceiver power supply<br>(normally connected to pin 16) |
| 14 | ISODE | Isolated DE output<br>(normally connected to pin 10) |
| 15 | $GND_2$ | Output power supply ground return. |
| 16 | $V_{DD2I}$ | Output isolation power supply<br>(normally connected to pin 13) |

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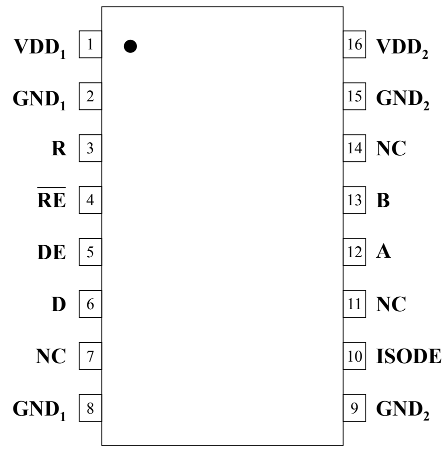
**IL3085 (0.3" SOIC Package) Pin Connections**

| | | |
|---|---|---|
| 1 | $V_{DD1}$ | Input power supply |
| 2 | $GND_1$ | Input power supply ground return (pin 2 is internally connected to pin 8) |
| 3 | R | Output data from bus |
| 4 | $\overline{RE}$ | Read data enable (if $\overline{RE}$ is high, R= high impedance) |
| 5 | DE | Drive enable |
| 6 | D | Data input to bus |
| 7 | NC | No internal connection |
| 8 | $GND_1$ | Input power supply ground return (pin 8 is internally connected to pin 2) |
| 9 | $GND_2$ | Output power supply ground return (pin 9 is internally connected to pin 15) |
| 10 | ISODE | Isolated DE output for use in PROFIBUS applications where the state of the isolated drive enable node needs to be monitored. |
| 11 | NC | No internal connection |
| 12 | A | Non-inverting bus line |
| 13 | B | Inverting bus line |
| 14 | NC | No internal connection |
| 15 | $GND_2$ | Output power supply ground return (pin 15 is internally connected to pin 9) |
| 16 | $V_{DD2}$ | Output power supply |




IL3085



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### Driver Section

| Electrical Specifications ($T_{min}$ to $T_{max}$ and $V_{DD}$ = 4.5 V to 5.5 V unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.**(5) | **Max.** | **Units** | **Test Conditions** |
| Output voltage | $V_O$ | | | $V_{DD}$ | V | $I_O = 0$ |
| Differential Output Voltage(2) | $\|V_{OD1}\|$ | | | $V_{DD}$ | V | $I_O = 0$ |
| Differential Output Voltage(2, 6) | $V_{OD3}$ | 1.5 | 2.3 | 5 | V | $R_L = 27\ \Omega$, $V_{DD} = 4.5$ V |
| Change in Magnitude of Differential Output Voltage(7) | $\Delta\|V_{OD}\|$ | | ±0.01 | ±0.2 | V | $R_L = 27\ \Omega$ or $50\ \Omega$ |
| Common Mode Output Voltage | $V_{OC}$ | | | 3 | V | $R_L = 27\ \Omega$ or $50\ \Omega$ |
| Change in Magnitude of Common Mode Output Voltage(7) | $\Delta\|V_{OC}\|$ | | ±0.01 | ±0.2 | V | $R_L = 27\ \Omega$ or $50\ \Omega$ |
| Output Current(4) | $I_O$ | | | 1<br>−0.8 | mA | Output Disabled, $V_O = 12$<br>$V_O = -7$ |
| High Level Input Current | $I_{IH}$ | | | 10 | µA | $V_I = 3.5$ V |
| Low Level Input Current | $I_{IL}$ | | | −10 | µA | $V_I = 0.4$ V |
| Absolute \|Short-circuit Output Current\| | $I_{OS}$ | | | 250 | mA | $-7\text{ V} < V_O < 12$ V |
| Supply Current $V_{DD1} = 5$ V<br>$V_{DD1} = 3.3$ V | $I_{DD1}$<br>$I_{DD1}$ | | 4<br>3 | 6<br>4 | mA | No Load<br>(Outputs Enabled) |

### **Notes** (apply to both driver and receiver sections):

1. All voltages are with respect to network ground except differential I/O bus voltages.
2. Differential input/output voltage is measured at the noninverting terminal A with respect to the inverting terminal B.
3. Skew limit is the maximum propagation delay difference between any two devices at 25°C.
4. The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
5. All typical values are at $V_{DD1}$,$V_{DD2}$ = 5 V or $V_{DD1}$= 3.3 V and $T_A$ = 25°C.
6. $-7\text{ V} < V_{CM} < 12$ V; $4.5\text{ V} < V_{DD} < 5.5$ V.
7. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of $V_{OD}$ and $V_{OC}$, respectively, that occur when the input is changed from one logic state to the other.
8. This applies for both power on and power off, refer to ANSI standard RS-485 for exact condition. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.
9. Includes 10 ns read enable time. Maximum propagation delay is 25 ns after read assertion.
10. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel.
11. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
12. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 6.
13. External magnetic field immunity is improved by this factor if the field direction is “end-to-end” rather than to “pin-to-pin” (see diagram on p. 6).



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## Receiver Section

| Electrical Specifications ($T_{min}$ to $T_{max}$ and $V_{DD}$ = 4.5 V to 5.5 V unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.**(5) | **Max.** | **Units** | **Test Conditions** |
| Positive-going Input Threshold Voltage | $V_{IT+}$ | | | 0.2 | V | $-7$ V < $V_{CM}$ < 12 V |
| Negative-going Input Threshold Voltage | $V_{IT-}$ | −0.2 | | | V | $-7$ V < $V_{CM}$ < 12 V |
| Hysteresis Voltage ($V_{IT+} - V_{IT-}$) | $V_{HYS}$ | | 70 | | mV | $V_{CM}$ = 0 V, T = 25°C |
| High Level Digital Output Voltage | $V_{OH}$ | $V_{DD}$ − 0.2 | $V_{DD}$ | | V | $V_{ID}$ = 200 mV<br>$I_{OH}$ = −20 μA |
| Low Level Digital Output Voltage | $V_{OL}$ | | | 0.2 | V | $V_{ID}$ = −200 mV<br>$I_{OH}$ = 20 μA |
| High-impedance-state output current | $I_{OZ}$ | | | ±1 | μA | $V_O$ = 0.4 to ($V_{DD2}$−0.5) V |
| Line Input Current(8) | $I_I$ | | | 1 | mA | $V_I$ = 12 V |
| | | | | −0.8 | mA | $V_I$ = −7 V |
| Input Resistance | $R_I$ | 12 | | | kΩ | |
| Supply Current | $I_{DD2}$ | | 5 | 16 | mA | No load; Outputs Enabled; $V_{DD2X}$ connected to $V_{DD2I}$ if applicable |

## Switching Characteristics

| $V_{DD1}$ = 5 V, $V_{DD2}$ = 5 V | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.**(5) | **Max.** | **Units** | **Test Conditions** |
| Data Rate | | 4 | | | Mbps | $R_L$ = 54 Ω, $C_L$ = 50 pF |
| Propagation Delay(2, 9) | $t_{PD}$ | | 48 | 150 | ns | $V_O$ = −1.5 to 1.5 V, $C_L$ = 15 pF |
| Pulse Skew(2, 10) | $t_{SK}(P)$ | | 6 | 15 | ns | $V_O$ = −1.5 to 1.5 V, $C_L$ = 15 pF |
| Output Enable Time To High Level | $t_{PZH}$ | | 33 | 50 | ns | $C_L$ = 15 pF |
| Output Enable Time To Low Level | $t_{PZL}$ | | 33 | 50 | ns | $C_L$ = 15 pF |
| Output Disable Time From High Level | $t_{PHZ}$ | | 33 | 50 | ns | $C_L$ = 15 pF |
| Output Disable Time From Low Level | $t_{PLZ}$ | | 33 | 50 | ns | $C_L$ = 15 pF |
| Common Mode Transient Immunity (Output Logic High to Logic Low) | $\|CM_H\|,\|CM_L\|$ | 30 | 50 | | kV/μs | $V_{CM}$ = 1500 $V_{DC}$<br>$t_{TRANSIENT}$ = 25 ns |
| **$V_{DD1}$ = 3.3 V, $V_{DD2}$ = 5 V** | | | | | | |
| **Parameter** | **Symbol** | **Min.** | **Typ.**(5) | **Max.** | **Units** | **Test Conditions** |
| Data Rate | | 4 | | | Mbps | $R_L$ = 54 Ω, $C_L$ = 50 pF |
| Propagation Delay(2, 9) | $t_{PD}$ | | 48 | 150 | ns | $V_O$ = −1.5 to 1.5 V, $C_L$ = 15 pF |
| Pulse Skew(2, 10) | $t_{SK}(P)$ | | 6 | 20 | ns | $V_O$ = −1.5 to 1.5 V, $C_L$ = 15 pF |
| Output Enable Time To High Level | $t_{PZH}$ | | 33 | 50 | ns | $C_L$ = 15 pF |
| Output Enable Time To Low Level | $t_{PZL}$ | | 33 | 50 | ns | $C_L$ = 15 pF |
| Output Disable Time From High Level | $t_{PHZ}$ | | 33 | 50 | ns | $C_L$ = 15 pF |
| Output Disable Time From Low Level | $t_{PLZ}$ | | 33 | 50 | ns | $C_L$ = 15 pF |
| Common Mode Transient Immunity (Output Logic High to Logic Low) | $\|CM_H\|,\|CM_L\|$ | 30 | 50 | | kV/μs | $V_{CM}$ = 1500 $V_{DC}$<br>$t_{TRANSIENT}$ = 25 ns |

**Magnetic Field Immunity**(12)

| | | | | | | |
|---|---|---|---|---|---|---|
| **$V_{DD1}$ = 5 V, $V_{DD2}$ = 5 V** | | | | | | |
| Power Frequency Magnetic Immunity | $H_{PF}$ | 2800 | 3500 | | A/m | 50Hz/60Hz |
| Pulse Magnetic Field Immunity | $H_{PM}$ | 4000 | 4500 | | A/m | $t_p$ = 8μs |
| Damped Oscillatory Magnetic Field | $H_{OSC}$ | 4000 | 4500 | | A/m | 0.1Hz – 1MHz |
| Cross-axis Immunity Multiplier(13) | $K_X$ | | 2.5 | | | |
| **$V_{DD1}$ = 3.3 V, $V_{DD2}$ = 5 V** | | | | | | |
| Power Frequency Magnetic Immunity | $H_{PF}$ | 1000 | 1500 | | A/m | 50Hz/60Hz |
| Pulse Magnetic Field Immunity | $H_{PM}$ | 1800 | 2000 | | A/m | $t_p$ = 8μs |
| Damped Oscillatory Magnetic Field | $H_{OSC}$ | 1800 | 2000 | | A/m | 0.1Hz – 1MHz |
| Cross-axis Immunity Multiplier(13) | $K_X$ | | 2.5 | | | |

## Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

## Pinout Differences Between Packages

QSOP and narrow-body version (IL3085-1E and IL3085-3E) are designed for application flexibility and minimum board area in dense PCAs. The wide-body version (IL3085E) has redundant ground pins for layout flexibility.

QSOP and narrow-body versions provide separate isolated DE output (ISODE) and Transceiver Device Enable (XDE) input. ISODE follows the Device Enable input (DE). XDE can be used to enable and disable the transceiver from the bus side, or connected to ISODE to enable and disable the transceiver from the DE controller-side input. The QSOP and narrow-body versions also provide separate bus-side power supply pins— $V_{DD2X}$ for the transceiver module and $V_{DD2I}$ for the isolation module. These should be externally connected for normal operation, but can be used separately for testing or troubleshooting. The QSOP version also has an "ISOR" output that is isolated with respect to the controller-side "R." This pin is used for testing and normally not connected, but could be used for a bus-side data output under special circumstances.

The wide-body version has internal connections between the isolated DE output and the Transceiver Device Enable input, and well as between the two $V_{DD2}$ bus-side power supply pins. The two internally-connected GND pins for each supply side provide layout flexibility. The ISODE output can be used in PROFIBUS applications where the state of the isolated drive enable node needs to be monitored, or for testing or troubleshooting.

## Dynamic Power Consumption

IsoLoop Isolators have low power consumption because data is transmitted across the isolation barrier only on edge transitions. Power consumption therefore varies with the data rate. Typical dynamic supply currents are as follows:

| Data Rate (Mbps) | $I_{DD1}$ | $I_{DD2}$ |
|---|---|---|
| 1 | 150 µA | 150 µA |
| 4 | 600 µA | 600 µA |

**Table 2. Typical Dynamic Supply Currents.**

## Power Supply Decoupling

Both $V_{DD1}$ and $V_{DD2}$ must be bypassed with 47 nF ceramic capacitors. These should be placed as close as possible to $V_{DD}$ pins for proper operation. Additionally, $V_{DD2}$ should be bypassed with a 10 µF tantalum capacitor.

## Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

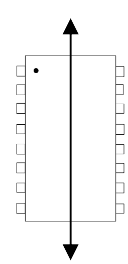
## DC Correctness

The IL3085 incorporates a patented refresh circuit to maintain the correct output state with respect to data input. At power up, the bus outputs will follow the Function Table shown on Page 1. The DE input should be held low during power-up to eliminate false drive data pulses from the bus. An external power supply monitor to minimize glitches caused by slow power-up and power-down transients is not required.

## Electromagnetic Compatibility

The IL3085 is fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. The IsoLoop Isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. NVE conducted compliance tests in the categories below:

EN50081-1
  Residential, Commercial & Light Industrial
  Methods EN55022, EN55014
EN50082-2: Industrial Environment
  Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity)
ENV50204
  Radiated Field from Digital Telephones (Immunity Test)



Immunity to external magnetic fields is even higher if the field direction is "end-to-end" (rather than to "pin-to-pin") as shown above.

## Application Information

Figures 1a, 1b, and 1c show typical connections to a bus and microcontroller for the three package versions. The schematics include typical termination and fail-safe resistors, and power supply decoupling capacitors:

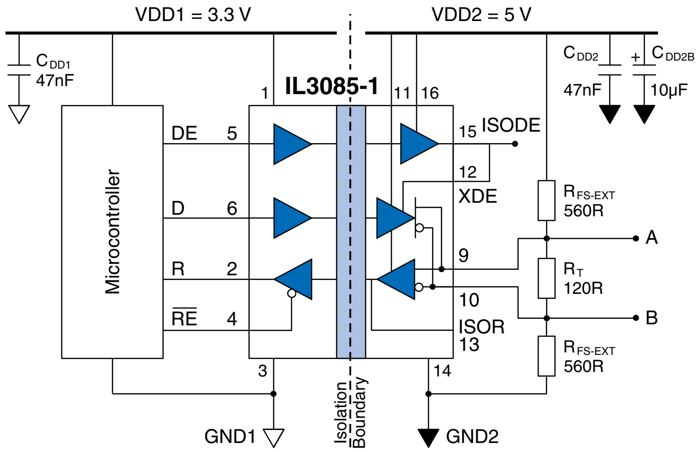



**Figure 1a. Typical QSOP transceiver connections.**

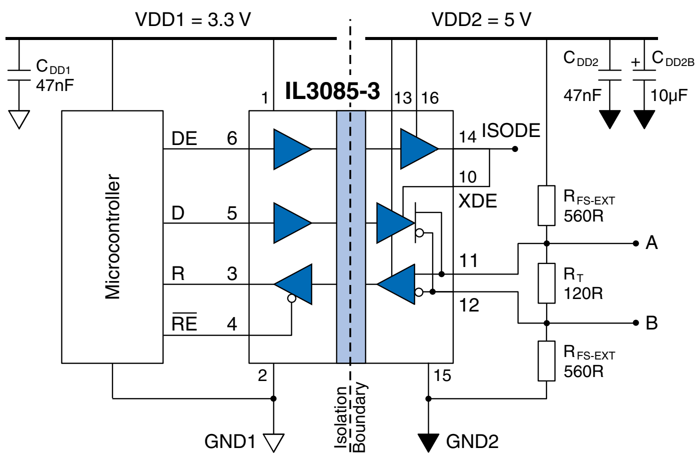



**Figure 1b. Typical narrow-body connections.**

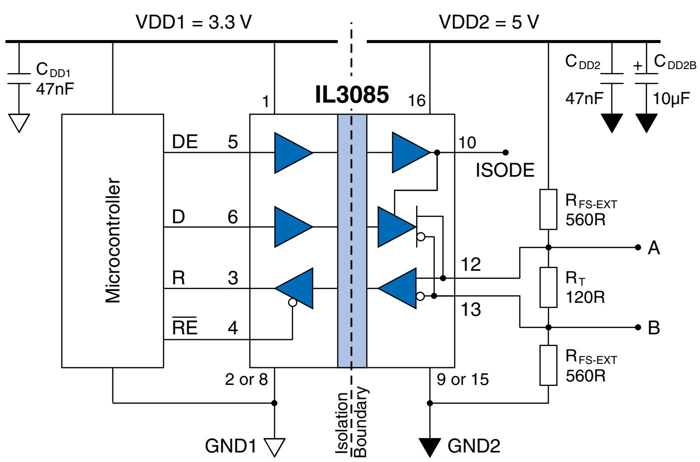



**Figure 1c. Typical wide-body connections.**



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*Receiver Features*
The receiver output "R" has tri-state capability via the active low $\overline{RE}$ input.

*Driver Features*
The RS-485 driver has a differential output and delivers at least 2.1 V across a 54 Ω load. Drivers feature low propagation delay skew to maximize bit width and minimize EMI. Drivers have tri-state capability via the active-high DE input.

*Receiver Data Rate, Cables and Terminations*
The IL3085 is intended for networks up to 4,000 feet (1,200 m), but the maximum data rate decreases as cable length increases. Twisted pair cable should be used in all networks since they tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receiver.

## Fail-Safe Operation

"Fail-safe operation" is defined here as the forcing of a logic high state on the "R" output in response to an open-circuit condition between the "A" and "B" lines of the bus, or when no drivers are active on the bus.

Proper biasing can ensure fail-safe operation, that is a known state when there are no active drivers on the bus. IL3000-Series Isolated Transceivers include internal pull-up and pull-down resistors of approximately 30 kΩ in the receiver section ($R_{FS-INT}$; see figure below). These internal resistors are designed to ensure failsafe operation but only if there are no termination resistors. The entire $V_{DD}$ will appear between inputs "A" and "B" if there is no loading and no termination resistors, and there will be more than the required 200 mV with up to four RS-485 worst-case Unit Loads of 12 kΩ. Many designs operating below 1 Mbps or less than 1,000 feet are unterminated. Termination resistors may not be necessary for very low data rates and very short cable runs because reflections have time to settle before data sampling, which occurs at the middle of the bit interval.

In busses with low-impedance termination resistors however, the differential voltage across the conductor pair will be close to zero with no active drivers. In this case the state of the bus is indeterminate, and the idle bus will be susceptible to noise. For example, with 120 Ω termination resistors ($R_T$) on each end of the cable, and four Unit Loads (12 kΩ each), without external fail-safe biasing resistors the internal pull-up and pull-down resistors will produce a voltage between inputs "A" and "B" of only about 5 mV. This is not nearly enough to ensure a known state. External fail-safe biasing resistors ($R_{FS-EXT}$) at one end of the bus can ensure fail-safe operation with a terminated bus. Resistors should be selected so that under worst-case power supply and resistor tolerances there is at least 200 mV across the conductor pair with no active drivers to meet the input sensitivity specification of the RS-485 standard.

Using the same value for pull-up and pull-down biasing resistors maintains balance for positive- and negative going transitions. Lower-value resistors increase inactive noise immunity at the expense of quiescent power consumption. Note that each Unit Load on the bus adds a worst-case loading of 12 kΩ across the conductor pair, and 32 Unit Loads add 375 Ω worst-case loading. The more loads on the bus, the lower the required values of the biasing resistors.

In the example with two 120 Ω termination resistors and four Unit Loads, 560 Ω external biasing resistors provide more than 200 mV between "A" and "B" with adequate margin for power supply variations and resistor tolerances. This ensures a known state when there are no active drivers. Other illustrative examples are shown in the following table:



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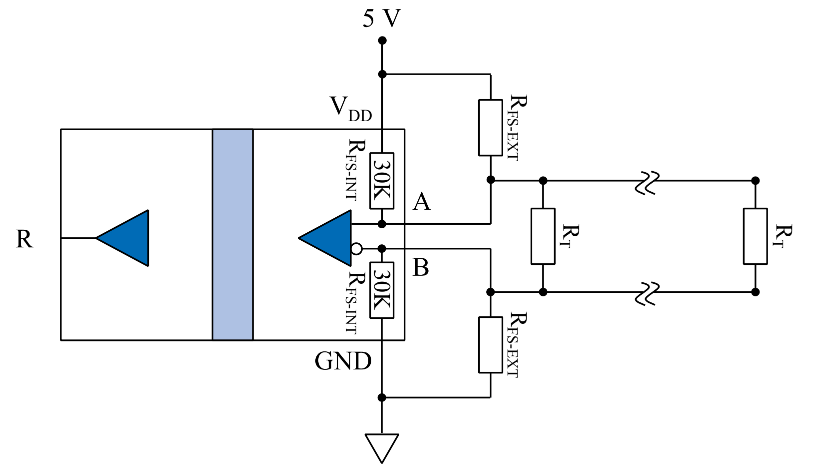
## Fail-Safe Biasing




| $R_{FS\text{-}EXT}$ | $R_T$ | Loading | Nominal $V_{A\text{-}B}$ (inactive) | Fail-Safe Operation? |
|---|---|---|---|---|
| Internal Only | None | Four unit loads (12 kΩ ea.) | 238 mV | Yes |
| Internal Only | 120 Ω | Four unit loads (12 kΩ ea.) | 5 mV | No |
| 560 Ω | 120 Ω | Four unit loads (12 kΩ ea.) | 254 mV | Yes |
| 510 Ω | 120 Ω | 32 unit loads (12 kΩ ea.) | 247 mV | Yes |



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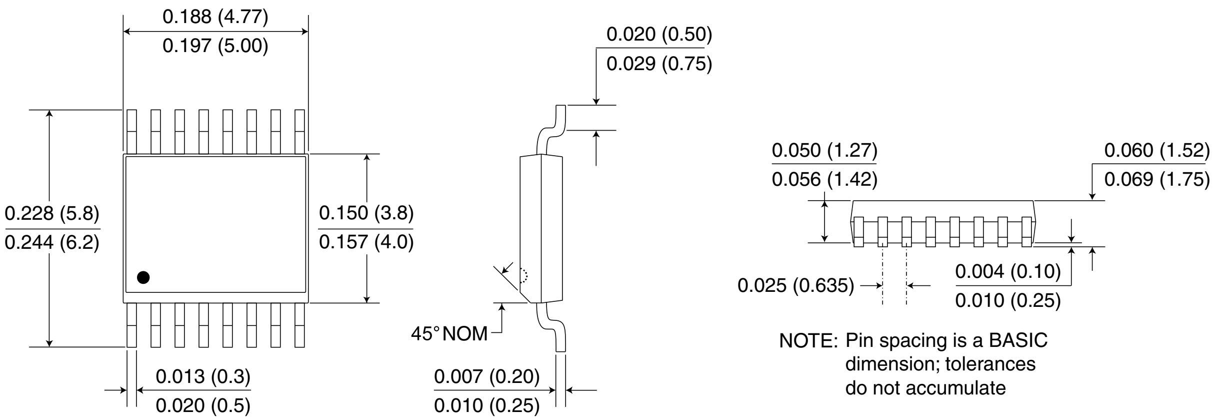
## Package Drawings

### **Ultraminiature 16-pin QSOP Package** (-1 suffix)

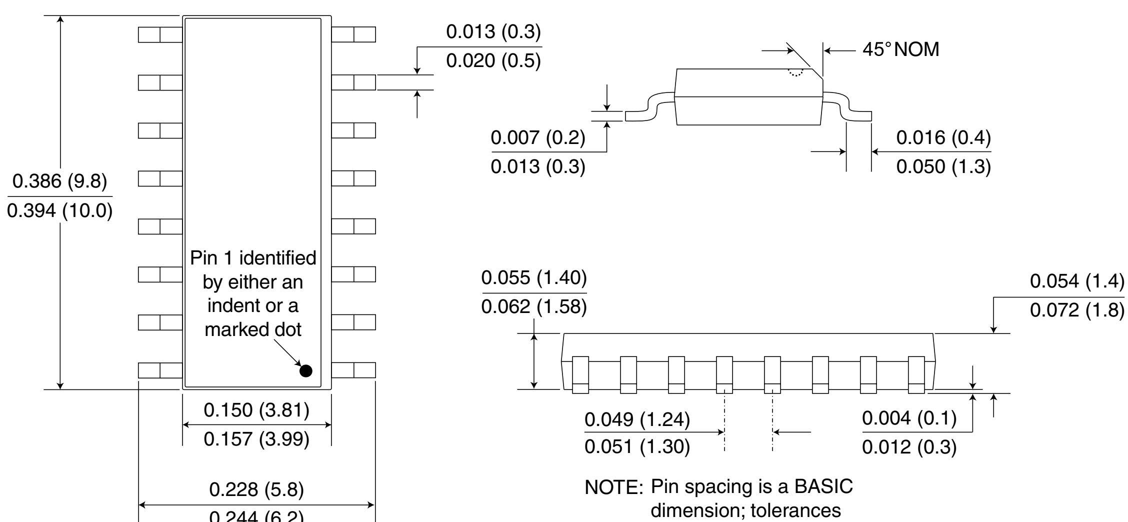
Dimensions in inches (mm); scale = approx. 5X




NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

### **0.15" 16-pin SOIC Package** (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X




NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate



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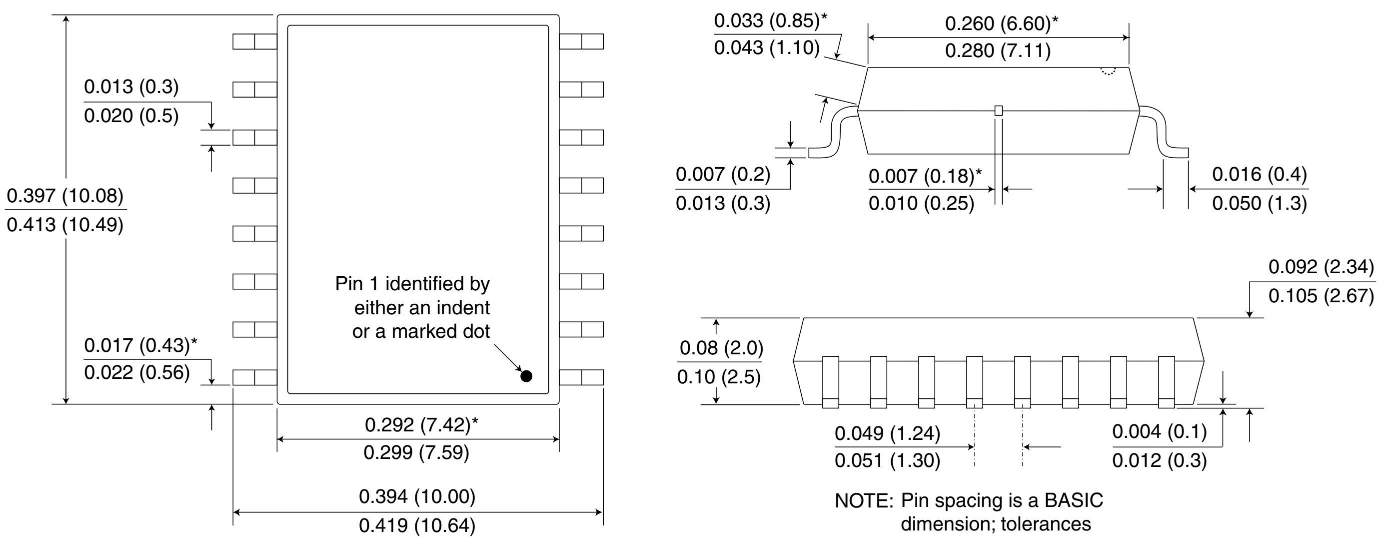
**0.3" 16-pin SOIC Package** (no suffix)

Dimensions in inches (mm); scale = approx. 5X




NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.



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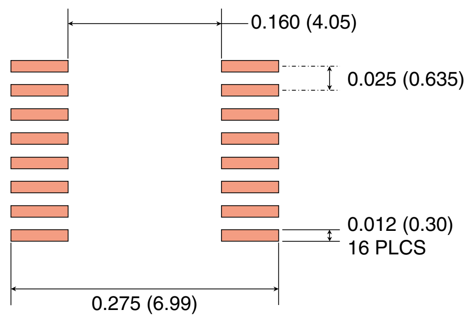
## Recommended Pad Layouts

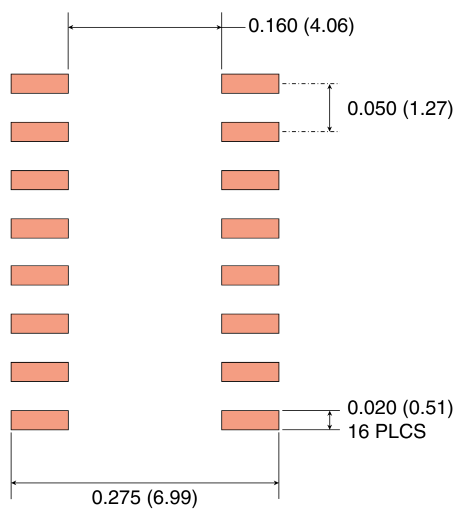
### 4 mm x 5 mm 16-pin QSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X




### 0.15" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



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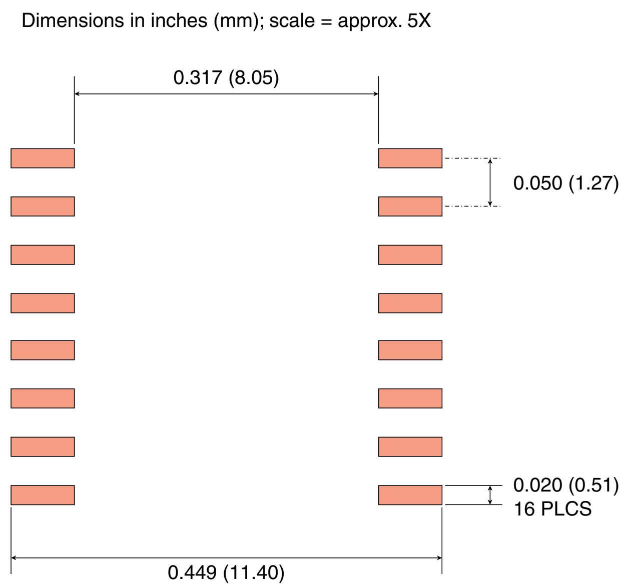
## 0.3" 16-pin SOIC Pad Layout



## Ordering Information and Valid Part Numbers

IL 30 85 -3 E TR13

**Bulk Packaging**
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

**Package**
E = RoHS Compliant

**Package Type**
Blank = 0.3" SOIC
-3 = 0.15" SOIC
-1 = 0.15" QSOP

**Channel Configuration**
85 = RS-485

**Base Part Number**
30 = Digital-In, 4 Mbps Transceiver

**Product Family**
IL = Isolators

**Valid Part Numbers**
IL3085E
IL3085E TR13
IL3085-3E
IL3085-3E TR7
IL3085-3E TR13
IL3085-1E
IL3085-1E TR7
IL3085-1E TR13

RoHS COMPLIANT



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## Revision History

| | |
|---|---|
| **ISB-DS-001-IL3085-G**<br>**November 2016** | **Change**<br>• Updated from IEC 60747-5-5 (VDE 0884) certification to VDE V 0884-10. |
| **ISB-DS-001-IL3085-F** | **Change**<br>• Increased IL3085-1E (QSOP) creepage specification from 2.75 mm to 3.2 mm (p. 2). |
| **ISB-DS-001-IL3085-E** | **Change**<br>• Added QSOP version (-1 suffix).<br>• Revised and added details to thermal characteristic specifications (p. 2).<br>• Added VDE 0884 Safety-Limiting Values (p. 3). |
| **ISB-DS-001-IL3085-D** | **Change**<br>• IEC 60747-5-5 (VDE 0884) certification.<br>• Upgraded from MSL 2 to MSL 1. |
| **ISB-DS-001-IL3085-C** | **Change**<br>• Increased transient immunity specifications based on additional data.<br>• Noted UL 1577 recognition, IEC 61010-1 approval, and VDE 0884 pending.<br>• Added transient immunity specifications.<br>• Added high voltage endurance specification.<br>• Increased magnetic immunity specifications.<br>• Updated package outline drawings and added recommended solder pad dimensions. |
| **ISB-DS-001-IL3085-B**<br>**January 2013** | **Change**<br>• Added thermal characteristics (p. 2).<br>• Finalized maximum data rate (4 Mbps).<br>• Cosmetic changes. |
| **ISB-DS-001-IL3085-A**<br>**December 2012** | **Change**<br>• Initial Release. |

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*November 2016*