

# 74LV4052

## Dual 4-channel analog multiplexer/demultiplexer

Rev. 5 — 17 March 2016

Product data sheet

### 1. General description

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The 74LV4052 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4052.

The 74LV4052 is a dual 4-channel analog multiplexer/demultiplexer with a common select logic. Each multiplexer has four independent inputs/outputs (nY0 to nY3) and a common input/output (nZ). The common channel select logics include two digital select inputs (S0 and S1) and an active LOW enable input ( $\bar{E}$ ). With  $\bar{E}$  LOW, one of the four switches is selected (low impedance ON-state) by S0 and S1. With  $\bar{E}$  HIGH, all switches are in the high impedance OFF-state, independent of S0 and S1.  $V_{CC}$  and GND are the supply voltage pins for the digital control inputs (S0, S1 and  $\bar{E}$ ). The  $V_{CC}$  to GND ranges are 1.0 V to 6.0 V. The analog inputs/outputs (nY0, to nY3, and nZ) can swing between  $V_{CC}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{CC} - V_{EE}$  may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to GND (typically ground).

### 2. Features and benefits

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- Optimized for low-voltage applications: 1.0 V to 6.0 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Low ON resistance:
  - ◆ 145  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 2.0$  V
  - ◆ 90  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 3.0$  V
  - ◆ 60  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 4.5$  V
- Logic level translation:
  - ◆ To enable 3 V logic to communicate with  $\pm 3$  V analog signals
- Typical 'break before make' built in
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and from  $-40$  °C to  $+125$  °C



### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LV4052D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4052DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV4052PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

### 4. Functional diagram

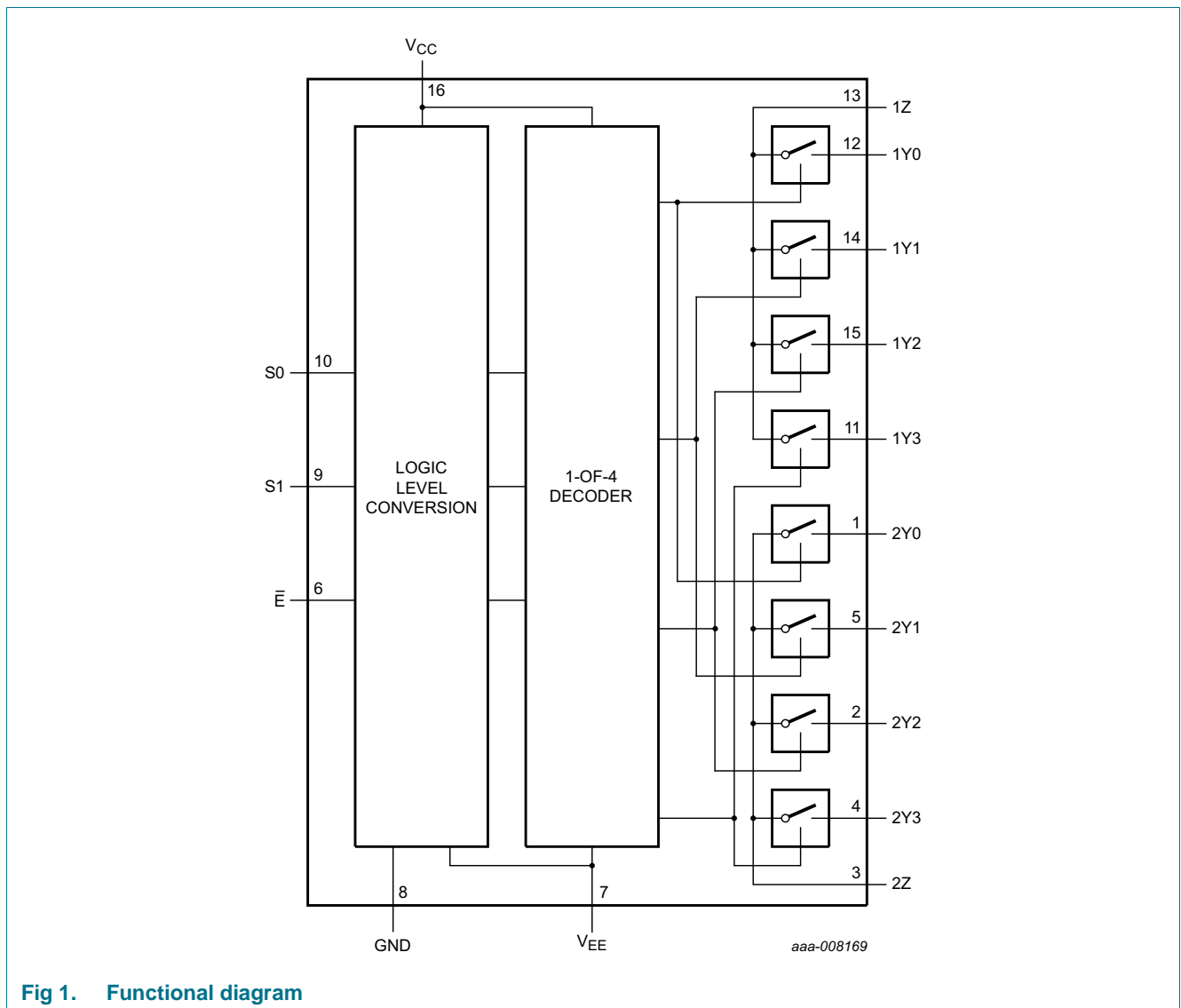


Fig 1. Functional diagram

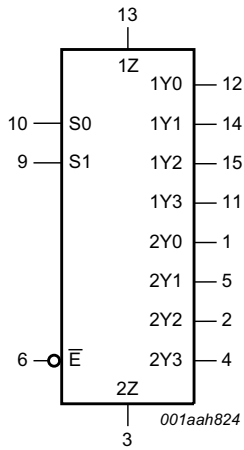


Fig 2. Logic symbol

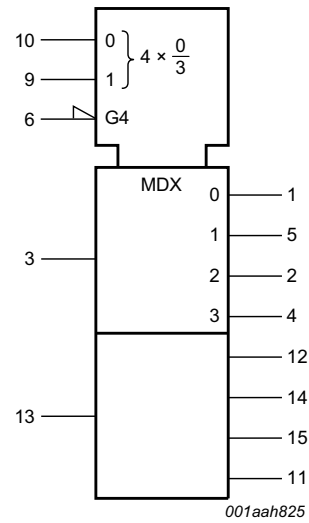


Fig 3. IEC logic symbol

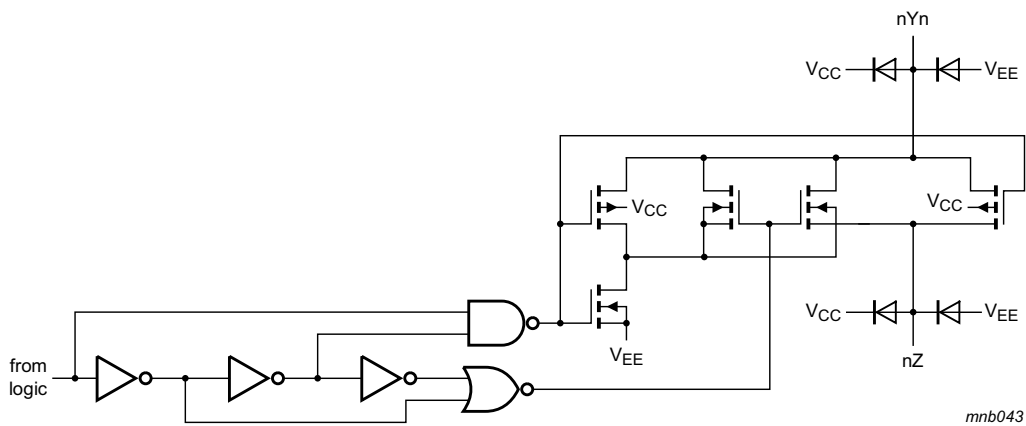


Fig 4. Schematic diagram (one switch)

## 5. Pinning information

### 5.1 Pinning

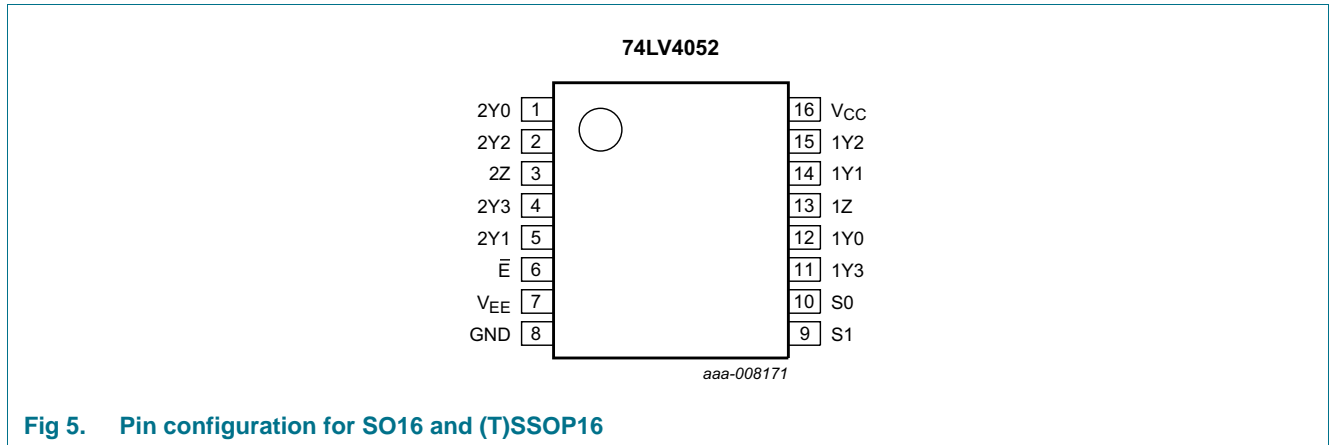


Fig 5. Pin configuration for SO16 and (T)SSOP16

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
2Y0	1	independent input or output
2Y2	2	independent input or output
2Z	3	common input or output
2Y3	4	independent input or output
2Y1	5	independent input or output
$\bar{E}$	6	enable input (active LOW)
V <sub>EE</sub>	7	negative supply voltage
GND	8	ground (0 V)
S1	9	select logic input
S0	10	select logic input
1Y3	11	independent input or output
1Y0	12	independent input or output
1Z	13	common input or output
1Y1	14	independent input or output
1Y2	15	independent input or output
V <sub>CC</sub>	16	positive supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input			Channel on
$\bar{E}$	S1	S0	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0$  V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	$\pm 20$	mA
$I_{SK}$	switch clamping current	$V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V	-	$\pm 20$	mA
$I_{SW}$	switch current	$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V; source or sink current	-	$\pm 25$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		SO16 package	-	500	mW
		SSOP16 and TSSOP16 package	-	500	mW

- [1] To avoid drawing  $V_{CC}$  current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no  $V_{CC}$  current flows out of terminals nYn. In this case, there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed  $V_{CC}$  or  $V_{EE}$ .
- [2] The minimum input voltage rating may be exceeded if the input current rating is observed.
- [3] For SO16 package: above 70 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.  
For SSOP16 and TSSOP16 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage	see <a href="#">Figure 6</a>	1	3.3	6	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_{SW}$	switch voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V to }2.0\text{ V}$	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V to }2.7\text{ V}$	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V to }6.0\text{ V}$	-	-	100	ns/V

[1] The static characteristics are guaranteed from  $V_{CC} = 1.2\text{ V to }6.0\text{ V}$ . However, LV devices are guaranteed to function down to  $V_{CC} = 1.0\text{ V}$  (with input levels GND or  $V_{CC}$ ).

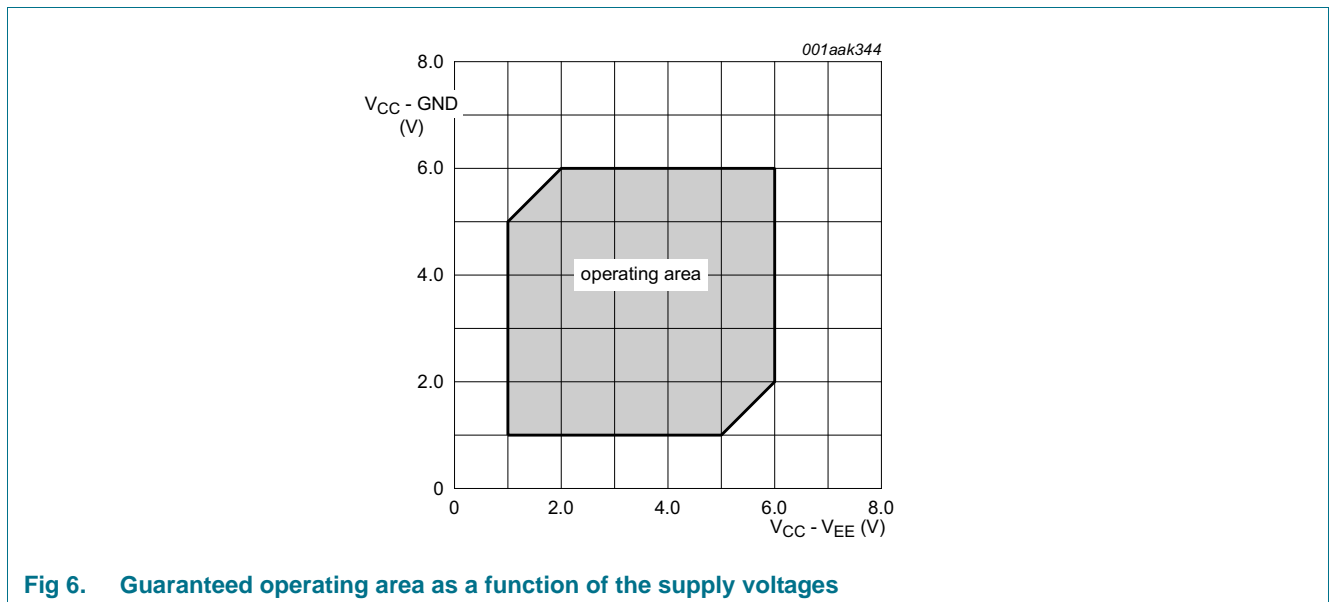


Fig 6. Guaranteed operating area as a function of the supply voltages

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	0.9	-	-	0.9	-	V
		V <sub>CC</sub> = 2.0 V	1.4	-	-	1.4	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.20	-	-	4.20	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.3	-	0.3	V
		V <sub>CC</sub> = 2.0 V	-	-	0.6	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.80	-	1.80	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND						
		V <sub>CC</sub> = 3.6 V	-	-	1.0	-	1.0	μA
		V <sub>CC</sub> = 6.0 V	-	-	2.0	-	2.0	μA
I <sub>S(OFF)</sub>	OFF-state leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 3.6 V	-	-	1.0	-	1.0	μA
		V <sub>CC</sub> = 6.0 V	-	-	2.0	-	2.0	μA
I <sub>S(ON)</sub>	ON-state leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 3.6 V	-	-	1.0	-	1.0	μA
		V <sub>CC</sub> = 6.0 V	-	-	2.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A						
		V <sub>CC</sub> = 3.6 V	-	-	20	-	40	μA
		V <sub>CC</sub> = 6.0 V	-	-	40	-	80	μA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	-	850	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF
C <sub>sw</sub>	switch capacitance	independent pins nYn	-	5	-	-	-	pF
		common pins nZ	-	12	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

9.1 Test circuits

aaa-008172

$V_I = V_{CC}$  or  $V_{EE}$  and  $V_O = V_{EE}$  or  $V_{CC}$ .

**Fig 7. Test circuit for measuring OFF-state leakage current**

aaa-008173

$V_I = V_{CC}$  or  $V_{EE}$  and  $V_O = \text{open circuit}$ .

**Fig 8. Test circuit for measuring ON-state leakage current**

9.2 ON resistance

Table 7. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see [Figure 9](#) and [Figure 10](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
R <sub>ON(peak)</sub>	ON resistance (peak)	$V_I = 0 \text{ V to } V_{CC} - V_{EE}$						
		$V_{CC} = 1.2 \text{ V}; I_{SW} = 100 \mu\text{A}$ [2]	-	-	-	-	-	$\Omega$
		$V_{CC} = 2.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	145	325	-	375	$\Omega$
		$V_{CC} = 2.7 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	90	200	-	235	$\Omega$
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	80	180	-	210	$\Omega$
		$V_{CC} = 4.5 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	60	135	-	160	$\Omega$
$\Delta R_{ON}$	ON resistance mismatch between channels	$V_I = 0 \text{ V to } V_{CC} - V_{EE}$						
		$V_{CC} = 1.2 \text{ V}; I_{SW} = 100 \mu\text{A}$ [2]	-	-	-	-	-	$\Omega$
		$V_{CC} = 2.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	5	-	-	-	$\Omega$
		$V_{CC} = 2.7 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	4	-	-	-	$\Omega$
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	4	-	-	-	$\Omega$
		$V_{CC} = 4.5 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	3	-	-	-	$\Omega$
		$V_{CC} = 6.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	2	-	-	-	$\Omega$



**Table 7. ON resistance ...continued**

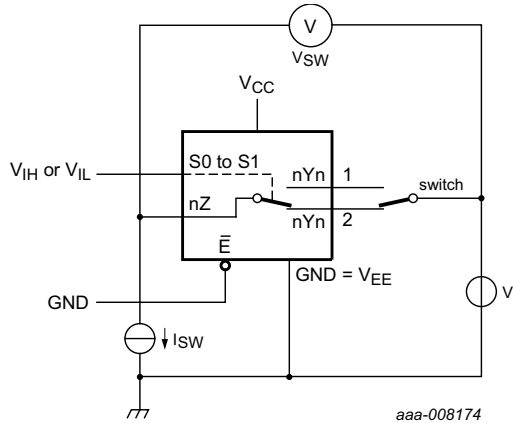
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see [Figure 9](#) and [Figure 10](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
R <sub>ON(rail)</sub>	ON resistance (rail)	V <sub>I</sub> = GND						
		V <sub>CC</sub> = 1.2 V; I <sub>SW</sub> = 100 μA <sup>[2]</sup>	-	225	-	-	-	Ω
		V <sub>CC</sub> = 2.0 V; I <sub>SW</sub> = 1000 μA	-	110	235	-	270	Ω
		V <sub>CC</sub> = 2.7 V; I <sub>SW</sub> = 1000 μA	-	70	145	-	165	Ω
		V <sub>CC</sub> = 3.0 V to 3.6 V; I <sub>SW</sub> = 1000 μA	-	60	130	-	150	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> = 1000 μA	-	45	100	-	115	Ω
		V <sub>CC</sub> = 6.0 V; I <sub>SW</sub> = 1000 μA	-	40	85	-	100	Ω
R <sub>ON(rail)</sub>	ON resistance (rail)	V <sub>I</sub> = V <sub>CC</sub> - V <sub>EE</sub>						
		V <sub>CC</sub> = 1.2 V; I <sub>SW</sub> = 100 μA <sup>[2]</sup>	-	250	-	-	-	Ω
		V <sub>CC</sub> = 2.0 V; I <sub>SW</sub> = 1000 μA	-	120	320	-	370	Ω
		V <sub>CC</sub> = 2.7 V; I <sub>SW</sub> = 1000 μA	-	75	195	-	225	Ω
		V <sub>CC</sub> = 3.0 V to 3.6 V; I <sub>SW</sub> = 1000 μA	-	70	175	-	205	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> = 1000 μA	-	50	130	-	150	Ω
		V <sub>CC</sub> = 6.0 V; I <sub>SW</sub> = 1000 μA	-	45	120	-	135	Ω

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

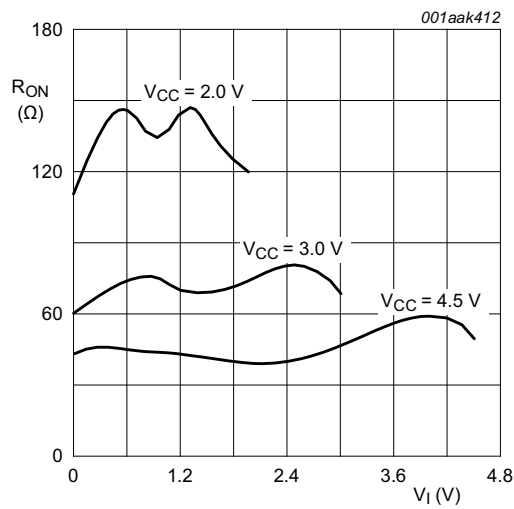
[2] When supply voltages (V<sub>CC</sub> - V<sub>EE</sub>) near 1.2 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 1.2 V, only use these devices for transmitting digital signals.

9.3 On resistance waveform and test circuit



$$R_{ON} = V_{SW} / I_{SW}$$

Fig 9. Test circuit for measuring  $R_{ON}$



$V_i = 0\text{ V to }V_{CC} - V_{EE}$

Fig 10. Typical  $R_{ON}$  as a function of input voltage

## 10. Dynamic characteristics

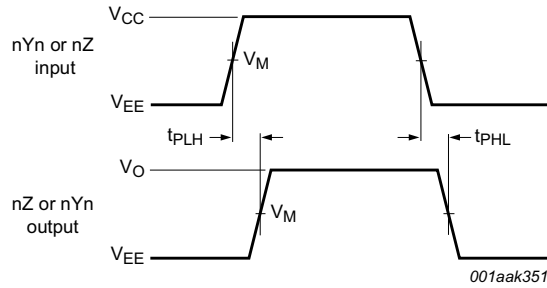
**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit, see [Figure 13](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nYn to nZ, nZ to nYn; see <a href="#">Figure 11</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	25	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	9	17	-	20	ns
		V <sub>CC</sub> = 2.7 V	-	6	13	-	15	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	5	10	-	12	ns
		V <sub>CC</sub> = 4.5 V	-	4	9	-	10	ns
		V <sub>CC</sub> = 6.0 V	-	3	7	-	8	ns
t <sub>en</sub>	enable time	$\bar{E}$ , Sn to nYn, nZ; see <a href="#">Figure 12</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	190	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	65	121	-	146	ns
		V <sub>CC</sub> = 2.7 V	-	48	89	-	108	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF <sup>[3]</sup>	-	30	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	36	71	-	86	ns
		V <sub>CC</sub> = 4.5 V	-	32	60	-	73	ns
V <sub>CC</sub> = 6.0 V	-	25	46	-	56	ns		
t <sub>dis</sub>	disable time	$\bar{E}$ , Sn to nYn, nZ; see <a href="#">Figure 12</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	125	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	43	80	-	95	ns
		V <sub>CC</sub> = 2.7 V	-	33	59	-	71	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF <sup>[3]</sup>	-	22	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	26	48	-	57	ns
		V <sub>CC</sub> = 4.5 V	-	23	41	-	49	ns
V <sub>CC</sub> = 6.0 V	-	18	32	-	38	ns		
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[4]</sup>	-	57	-	-	-	pF

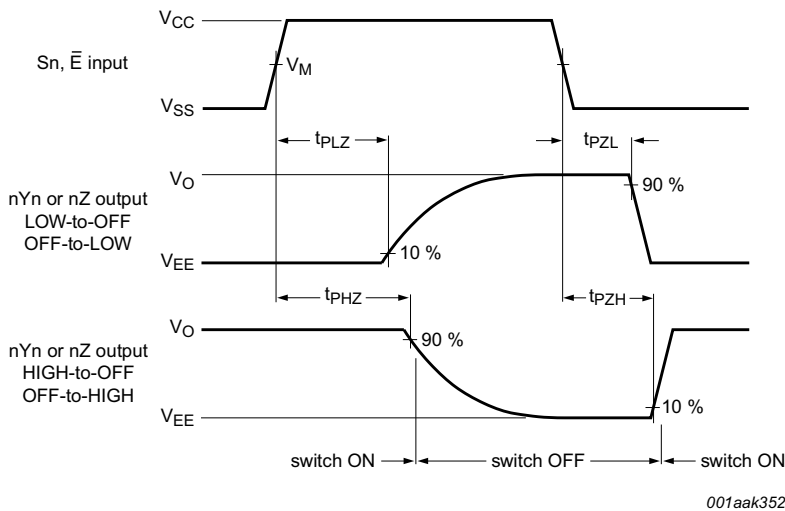
- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
t<sub>en</sub> is the same as t<sub>pZL</sub> and t<sub>pZH</sub>.  
t<sub>dis</sub> is the same as t<sub>pLZ</sub> and t<sub>pHZ</sub>.
- [3] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V).
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ((C<sub>L</sub> + C<sub>sw</sub>) × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:  
f<sub>i</sub> = input frequency in MHz, f<sub>o</sub> = output frequency in MHz  
C<sub>L</sub> = output load capacitance in pF  
C<sub>sw</sub> = maximum switch capacitance in pF;  
V<sub>CC</sub> = supply voltage in Volts  
N = number of inputs switching  
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

10.1 Waveforms



Measurement points are given in [Table 9](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig 11. nYn, nZ to nZ, nYn propagation delays

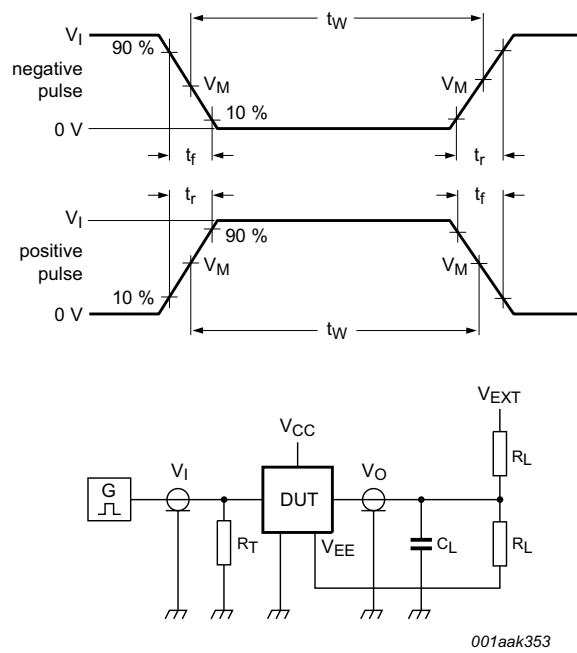


Measurement points are given in [Table 9](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig 12. Enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
> 3.6 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

Fig 13. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
< 2.7 V	$V_{CC}$	$\leq 6$ ns	50 pF	1 k $\Omega$	open	$V_{EE}$	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	$\leq 6$ ns	15 pF, 50 pF	1 k $\Omega$	open	$V_{EE}$	$2V_{CC}$
> 3.6 V	$V_{CC}$	$\leq 6$ ns	50 pF	1 k $\Omega$	open	$V_{EE}$	$2V_{CC}$

10.2 Additional dynamic parameters

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $V_I = GND$  or  $V_{CC}$  (unless otherwise specified);  $t_r = t_f \leq 6.0$  ns;  $T_{amb} = 25$  °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 1$ kHz; $C_L = 50$ pF; $R_L = 10$ k $\Omega$ ; see <a href="#">Figure 18</a>				
		$V_{CC} = 3.0$ V; $V_I = 2.75$ V (p-p)	-	0.8	-	%
		$V_{CC} = 6.0$ V; $V_I = 5.5$ V (p-p)	-	0.4	-	%
		$f_i = 10$ kHz; $C_L = 50$ pF; $R_L = 10$ k $\Omega$ ; see <a href="#">Figure 18</a>				
		$V_{CC} = 3.0$ V; $V_I = 2.75$ V (p-p)	-	2.4	-	%
		$V_{CC} = 6.0$ V; $V_I = 5.5$ V (p-p)	-	1.2	-	%
$f_{(-3dB)}$	-3 dB frequency response	$C_L = 50$ pF; $R_L = 50$ $\Omega$ ; see <a href="#">Figure 14</a> [1]				
		$V_{CC} = 3.0$ V	-	180	-	MHz
		$V_{CC} = 6.0$ V	-	200	-	MHz
$\alpha_{iso}$	isolation (OFF-state)	$f_i = 1$ MHz; $C_L = 50$ pF; $R_L = 600$ $\Omega$ ; see <a href="#">Figure 16</a> [2]				
		$V_{CC} = 3.0$ V	-	-50	-	dB
		$V_{CC} = 6.0$ V	-	-50	-	dB
$V_{ct}$	crosstalk voltage	between digital inputs and switch; $f_i = 1$ MHz; $C_L = 50$ pF; $R_L = 600$ $\Omega$ ; see <a href="#">Figure 19</a>				
		$V_{CC} = 3.0$ V	-	0.11	-	V
		$V_{CC} = 6.0$ V	-	0.12	-	V
Xtalk	crosstalk	between switches; $f_i = 1$ MHz; $C_L = 50$ pF; $R_L = 600$ $\Omega$ ; see <a href="#">Figure 20</a> [2]				
		$V_{CC} = 3.0$ V	-	-60	-	dB
		$V_{CC} = 6.0$ V	-	-60	-	dB

- [1] To obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 50  $\Omega$ ), adjust  $f_i$  voltage.
- [2] To obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 600  $\Omega$ ), adjust  $f_i$  voltage.

10.2.1 Test circuits

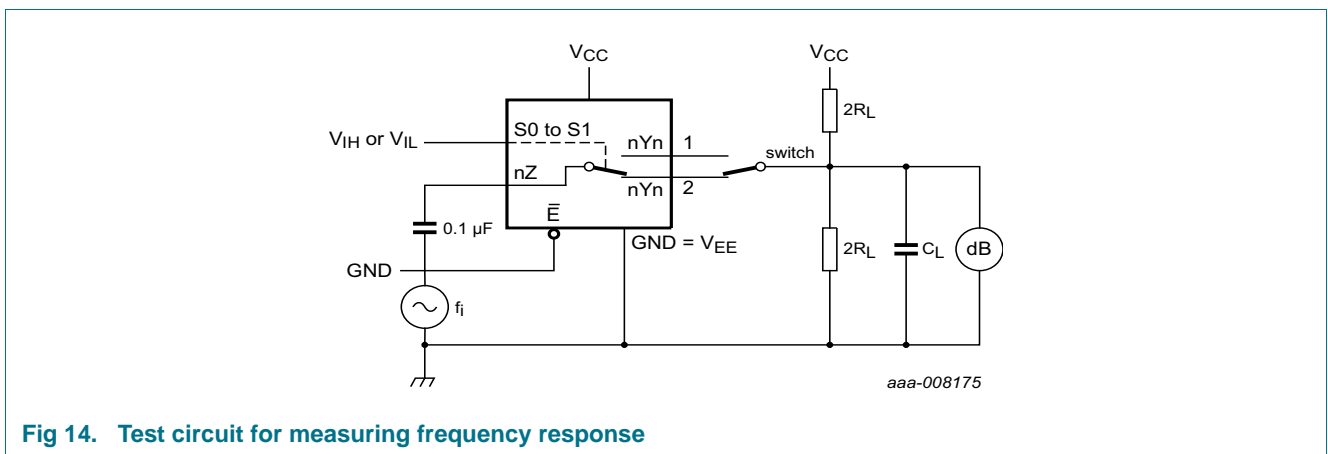
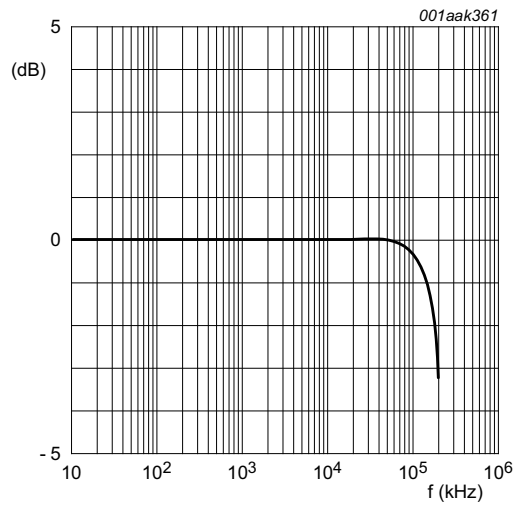


Fig 14. Test circuit for measuring frequency response



$V_{CC} = 3.0\text{ V}$ ;  $GND = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$ ;  $R_L = 50\ \Omega$ ;  $R_{SOURCE} = 1\text{ k}\Omega$ .

Fig 15. Typical frequency response

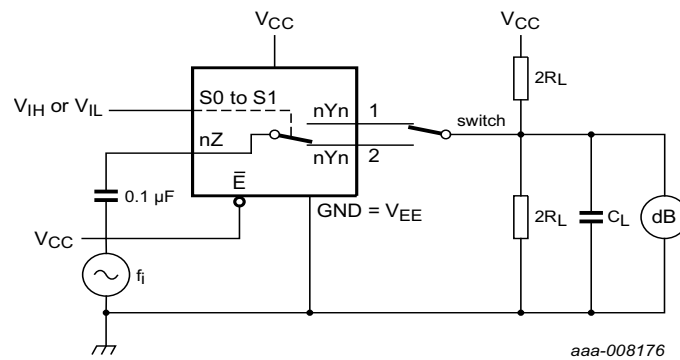
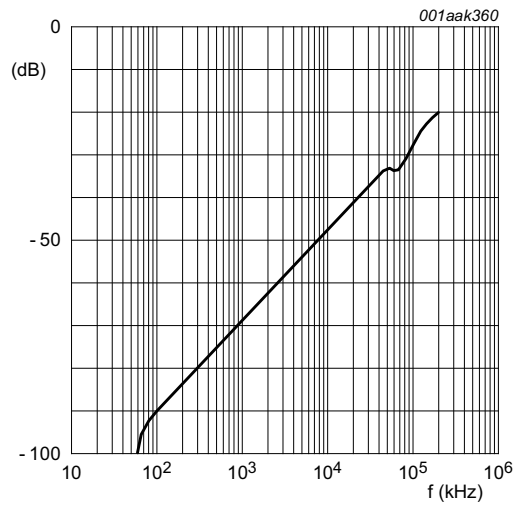


Fig 16. Test circuit for measuring isolation (OFF-state)



$V_{CC} = 3.0\text{ V}$ ;  $GND = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$ ;  $R_L = 50\ \Omega$ ;  $R_{SOURCE} = 1\text{ k}\Omega$ .

Fig 17. Typical isolation (OFF-state) as function of frequency

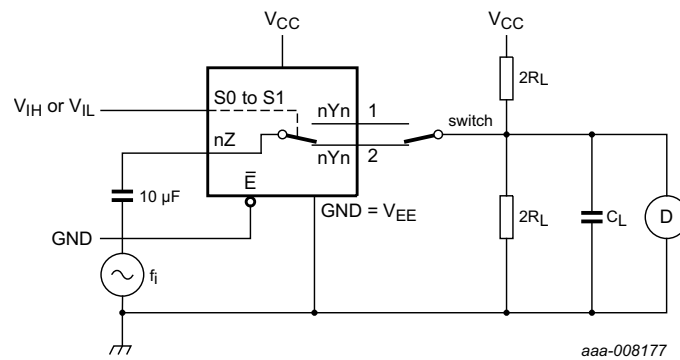
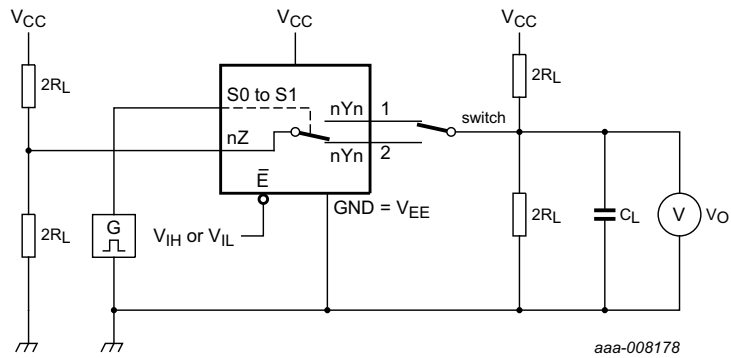
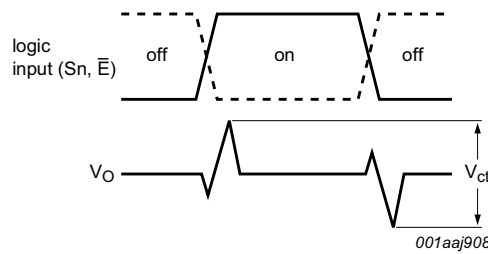


Fig 18. Test circuit for measuring total harmonic distortion





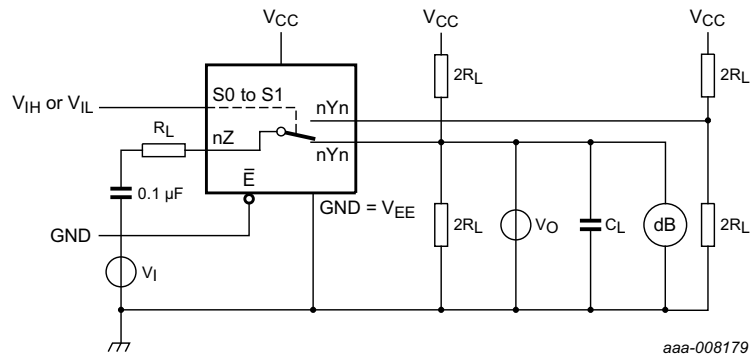
a. Test circuit



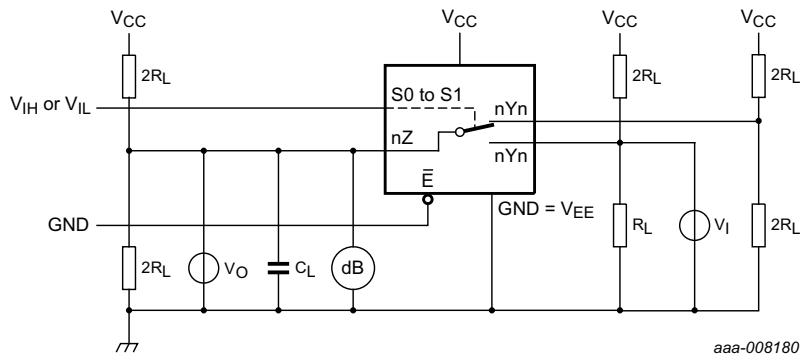
b. Input and output pulse definitions

$V_I$  may be connected to  $S_n$  or  $\bar{E}$ .

**Fig 19. Test circuit for measuring crosstalk voltage between digital inputs and switch**



a. Switch on channel.



b. Switch off channel.

**Fig 20. Test circuit for measuring crosstalk between switches**

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

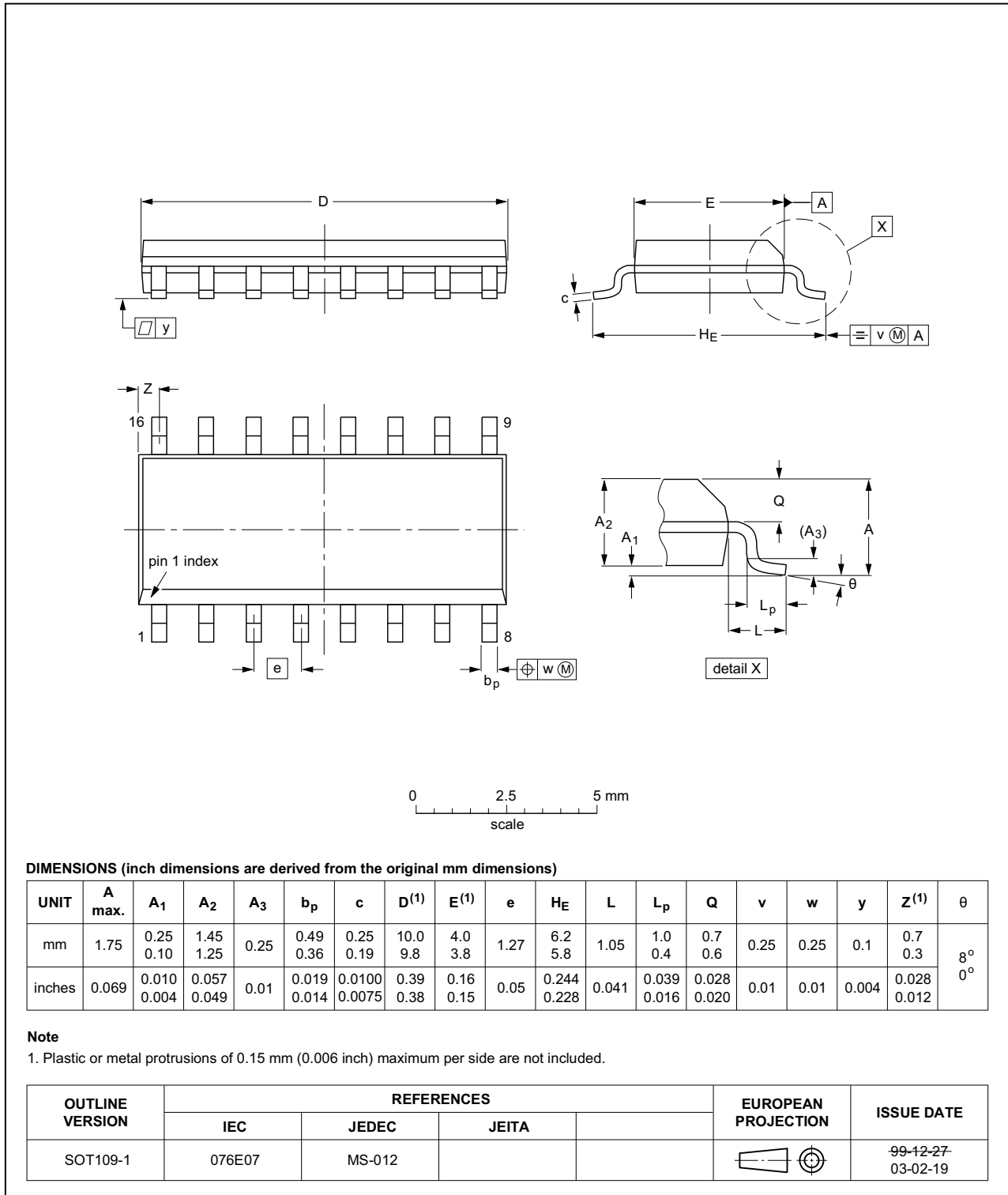


Fig 21. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



Fig 22. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

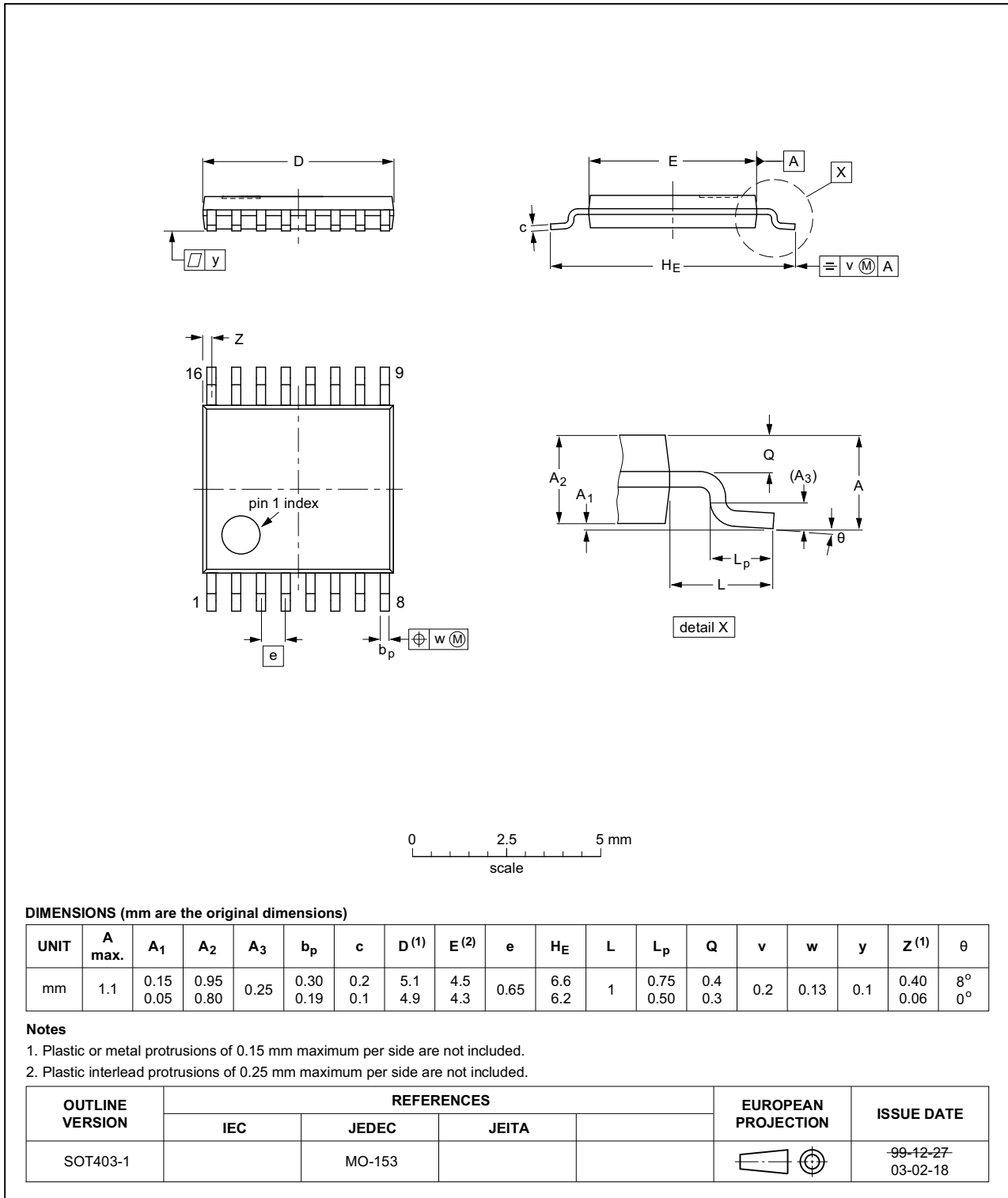


Fig 23. Package outline SOT403-1 (TSSOP16)

## 12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4052 v.5	20160317	Product data sheet	-	74LV4052 v.4
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LV4052N (SOT38-4) removed.</li> </ul>			
74LV4052 v.4	20130701	Product data sheet	-	74LV4052 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74LV4052 v.3	19980623	Product specification	-	74LV4052 v.2
74LV4052 v.2	19970715	Product specification	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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