IP4788CZ32

DVI and HDMI interface ESD and overcurrent protection, DDC/CEC buffering, hot plug detect and backdrive protection

Rev. 2 — 24 November 2014 Product data sheet

1. Product profile

1.1 General description

The IP4788CZ32 is designed to protect High-Definition Multimedia Interface (HDMI) transmitter host interfaces. It includes HDMI 5 V overcurrent / overvoltage protection, Display Data Channel (DDC) buffering and decoupling, hot plug detect, backdrive protection, Consumer Electronic Control (CEC) buffering and decoupling, and ±14 kV contact ElectroStatic Discharge (ESD) protection for all external I/Os, far exceeding the IEC 61000-4-2, level 4 standard.

The IP4788CZ32 incorporates Transmission Line Clamping (TLC) technology on the high-speed Transition Minimized Differential Signaling (TMDS) lines to simplify routing and help reducing impedance discontinuities. All TMDS lines are protected by an impedance-matched diode configuration that minimizes impedance discontinuities caused by typical shunt diodes.

The enhanced 60 mA overcurrent / overvoltage linear regulator guarantees HDMI-compliant 5 V output voltage levels with up to 6.5 V inputs.

The DDC lines use a new buffering concept which decouples the internal capacitive load from the external capacitive load for use with standard Complementary Metal Oxide Semiconductor (CMOS) or Low Voltage Transistor-Transistor Logic (LVTTL) I/O cells down to 1.8 V. This buffering also redrives the DDC and CEC signals, allowing the use of longer or cheaper HDMI cables with a higher capacitance. The internal hot plug detect module simplifies the application of the HDMI transmitter to control the hot plug signal.

All lines provide appropriate integrated pull-ups and pull-downs for HDMI compliance and backdrive protection to guarantee that HDMI interface signals are not pulled down when the system is powered down or enters Standby mode. Only a single external capacitor is required for operation.

1.2 Features and benefits

- HDMI 2.0 and all backward compatible standards are supported
- 6.0 Gbps TMDS Bit Rate (600 Mcsc TMDS Character Rate) compatible
- Supports Ultra High-Definition (UHD) 4K (2160p) 60 Hz display modes
- Impedance matched 100 Ω differential transmission line ESD protection for TMDS lines (±10 Ω). No Printed-Circuit Board (PCB) pre-compensation required
- Simplified flow-through routing utilizing less overall PCB space
- DDC capacitive decoupling between system side and HDMI connector side and buffering to drive cable with high capacitive load (> 700 pF/25 m)

- All external I/O lines with ESD protection of at least ±14 kV, exceeding the IEC 61000-4-2, level 4 standard
- Hot plug detect module
- CEC buffering and isolation, with integrated backdrive-protected 26 kΩ pull-up
- Robust ESD protection without degradation after repeated ESD strikes
- Highest integration in a small footprint, PCB level, optimized RF routing, 32-pin HVQFN leadless package

1.3 Applications

- The IP4788CZ32 can be used for a wide range of HDMI source devices, consumer and computing electronics:
  - High-Definition (HD) and Standard-Definition (SD) Blu-ray and DVD players
  - Set-top box
  - PC graphic card
  - Game console
  - HDMI picture performance quality enhancer module
  - Digital Visual Interface (DVI)

2. Pinning information

2.1 Pinning

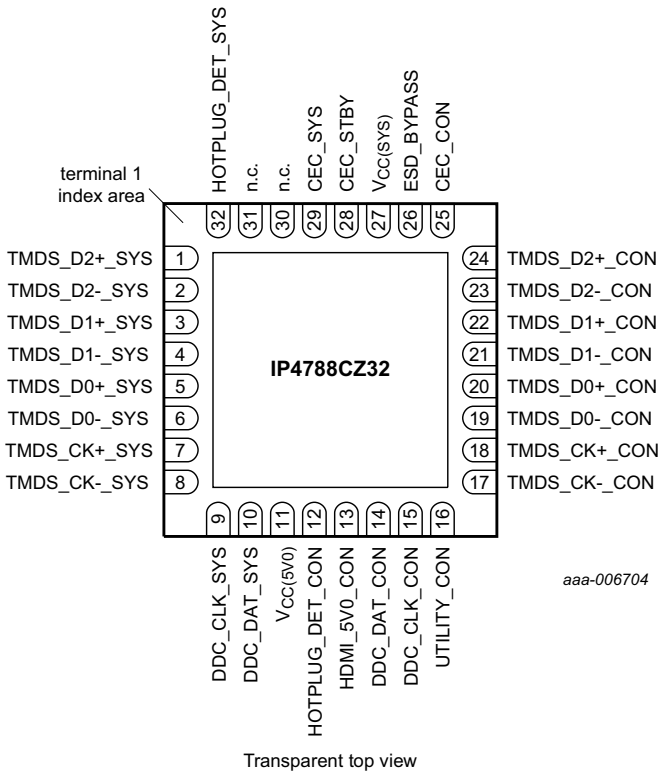

Fig 1. Pin configuration IP4788CZ32

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2.2 Pin description

Table 1. Pin description

Pin	Name	Description
1	TMDS_D2+_SYS	TMDS to ASIC inside system
2	TMDS_D2−_SYS	TMDS to ASIC inside system
3	TMDS_D1+_SYS	TMDS to ASIC inside system
4	TMDS_D1−_SYS	TMDS to ASIC inside system
5	TMDS_D0+_SYS	TMDS to ASIC inside system
6	TMDS_D0−_SYS	TMDS to ASIC inside system
7	TMDS_CK+_SYS	TMDS to ASIC inside system
8	TMDS_CK−_SYS	TMDS to ASIC inside system
9	DDC_CLK_SYS	DDC clock system side
10	DDC_DAT_SYS	DDC data system side
11	$V_{CC(5V0)}$	5 V supply input
12	HOTPLUG_DET_CON	hot plug detect connector side
13	HDMI_5V0_CON	5 V overcurrent out to connector
14	DDC_DAT_CON	DDC data connector side
15	DDC_CLK_CON	DDC clock connector side
16	UTILITY_CON	utility line ESD protection
17	TMDS_CK−_CON	TMDS ESD protection to connector
18	TMDS_CK+_CON	TMDS ESD protection to connector
19	TMDS_D0−_CON	TMDS ESD protection to connector
20	TMDS_D0+_CON	TMDS ESD protection to connector
21	TMDS_D1−_CON	TMDS ESD protection to connector
22	TMDS_D1+_CON	TMDS ESD protection to connector
23	TMDS_D2−_CON	TMDS ESD protection to connector
24	TMDS_D2+_CON	TMDS ESD protection to connector
25	CEC_CON	CEC signal connector side
26	ESD_BYPASS	ESD bias voltage
27	$V_{CC(SYS)}$	supply voltage for level shifting
28	CEC_STBY	Standby mode control (LOW for lowest power, CEC-only mode)
29	CEC_SYS	CEC I/O signal system side
30	n.c.	not connected
31	n.c.	not connected
32	HOTPLUG_DET_SYS	hot plug detect system side
ground pad	GND	ground

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3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4788CZ32	DFN5050-32 (HVQFN32)	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

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4. Functional diagram

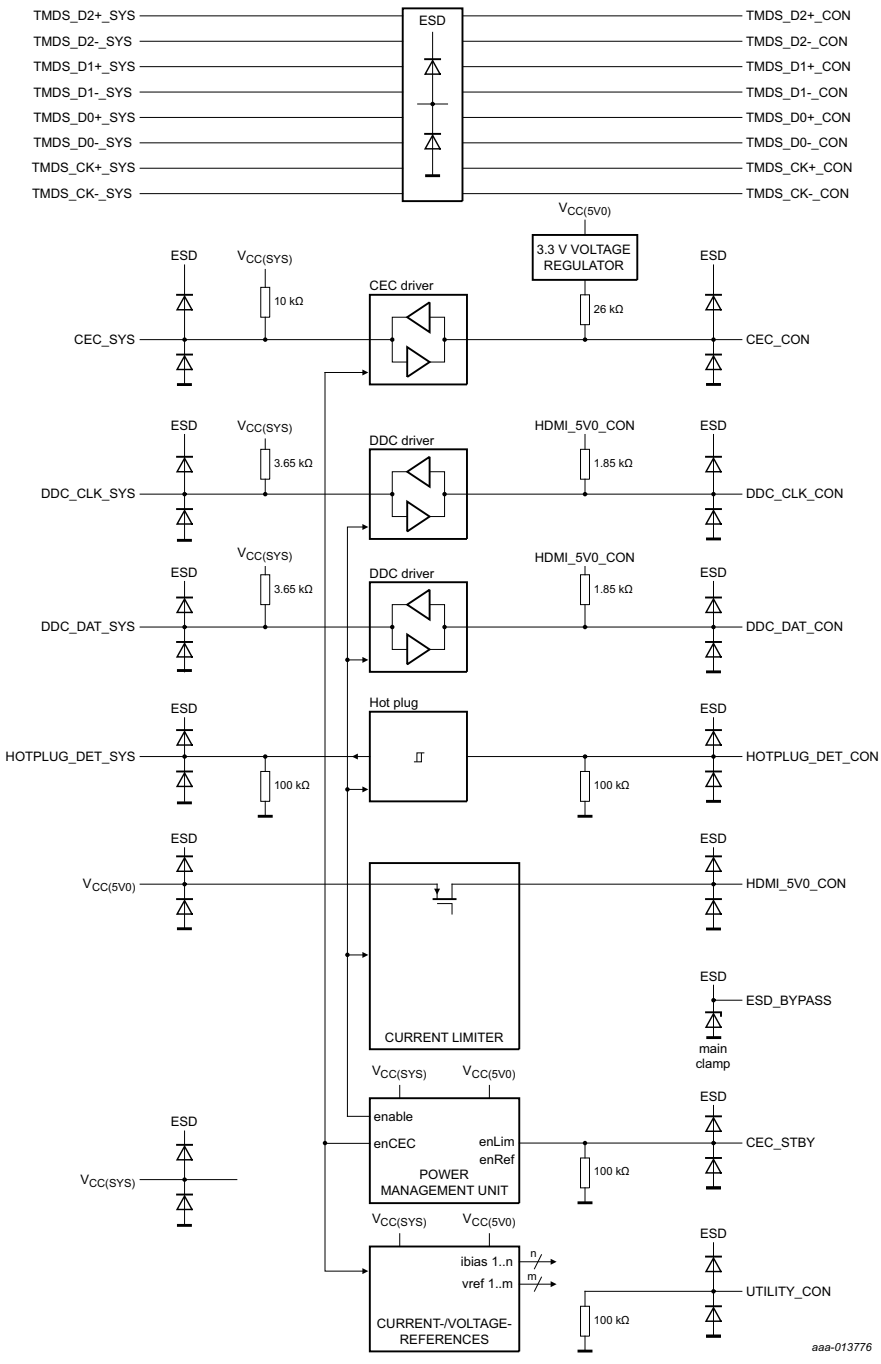

Fig 2. Functional diagram

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5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)		GND − 0.5	6.5	V
V_I	input voltage	I/O pins	GND − 0.5	5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4 (contact) [1][2]	-	±14	kV
		IEC 61000-4-2, level 1 (contact) [3]	-	±2	kV
P_{tot}	total power dissipation	DDC operating at 100 kHz; CEC operating at 1 kHz; 50 % duty cycle; CEC_STBY = HIGH; no current at HDMI_5V0_CON	-	50	mW
		DDC and CEC bus in idle mode; CEC_STBY = HIGH; no current at HDMI_5V0_CON	-	3.0	mW
		DDC and CEC bus in idle mode; CEC_STBY = LOW	-	1.0	mW
T_{amb}	ambient temperature		−25	+85	°C
T_{stg}	storage temperature		−55	+125	°C

[1] Connector-side pins (typically denoted with "_CON" suffix) to ground.

[2] Device is qualified with contact discharge pulses of ±14 kV according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

[3] System-side pins: CEC_SYS, DDC_DAT_SYS, DDC_CLK_SYS, HOTPLUG_DET_SYS, CEC_STBY, $V_{CC(SYS)}$ and $V_{CC(5V0)}$.

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6. Static characteristics

Table 4. Supplies

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)	[1]	4.5	5.0	6.5	V
$V_{CC(SYS)}$	system supply voltage		1.62	3.3	5.5	V

[1] IP4788CZ32 contains a 5 V voltage regulator function for higher input voltages. Any input voltage of 4.925 V < $V_{CC(5V0)}$ < 6.50 V provides HDMI-compliant output levels of 4.8 V to 5.3 V on HDMI_5V0_CON.

Table 5. TMDS protection circuit

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS channel						
$Z_{i(dif)}$	differential input impedance	TDR measured; t_r = 200 ps	90	100	110	Ω
C_{eff}	effective capacitance	equivalent shunt capacitance for TDR minimum; t_r = 200 ps [1][2]	-	0.6	-	pF
Protection diode						
V_{BRzd}	Zener diode breakdown voltage	I = 1.0 mA	6.0	-	9.0	V
r_{dyn}	dynamic resistance	TLP				
		positive transient [3]	-	0.5	-	Ω
		negative transient [3]	-	0.4	-	Ω
I_{bck}	back current	$V_{CC(5V0)}$ < $V_{ch(TMDS)}$ [4][5]	-	0.1	1.0	μA
I_{LR}	reverse leakage current	V_I = 3.0 V	-	1.0	-	μA
V_F	forward voltage		-	0.7	-	V
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	100 ns TLP; 50 Ω pulser at 50 ns	-	8.0	-	V

[1] This parameter is guaranteed by design.

[2] Capacitive dip at HDMI Time Domain Reflectometer (TDR) measurement conditions.

[3] ANSI-ESDSP5.5.1-2004, ESD sensitivity testing Transmission Line Pulse (TLP) component level method 50 TDR.

[4] Signal pins:
TMDS_D0+_CON, TMDS_D0−_CON, TMDS_D1+_CON, TMDS_D1−_CON, TMDS_D2+_CON, TMDS_D2−_CON, TMDS_CK+_CON, TMDS_CK−_CON,
TMDS_D0+_SYS, TMDS_D0−_SYS, TMDS_D1+_SYS, TMDS_D1−_SYS, TMDS_D2+_SYS, TMDS_D2−_SYS, TMDS_CK+_SYS and TMDS_CK−_SYS.

[5] Backdrive current from TMDS_x_SYS and TMDS_x_CON pins to local $V_{CC(5V0)}$ bias rail at power-down. Device does not block backdrive current leakage through the device to/from ASIC I/O pins connected to TMDS_x_SYS pins.

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Table 6. HDMI_5V0_CON

T_{amb} = –25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
r_{dyn}	dynamic resistance	TLP				
		positive transient [1]	-	1.0	-	Ω
		negative transient [1]	-	1.0	-	Ω
V_{CL}	clamping voltage	100 ns TLP; 50 Ω pulser at 50 ns	-	8	-	V
$I_{O(max)}$	maximum output current	$V_{(HDMI\_5V0\_CON)}$ = 4.8 V	55	-	-	mA
I_{bck}	back current	$V_{CC(5V0)} < V_{(HDMI\_5V0\_CON)}$	-	-	10	µA
$I_{O(sc)}$	short-circuit output current	$V_{(HDMI\_5V0\_CON)}$ = 0 V	-	125	175	mA
V_{do}	dropout voltage	4.5 V < $V_{CC(5V0)}$ < 4.925 V; DDC = LOW [2]				
		I_O = 10 mA	-	70	-	mV
		I_O = 55 mA	-	-	125	mV
$V_{O(LDO)}$	LDO output voltage	$I_O \leq$ 55 mA; 4.925 V < $V_{CC(5V0)}$ < 6.5 V; DDC = LOW [2]	4.8	5.05	5.3	V

[1] ANSI-ESDSP5.5.1-2004, ESD sensitivity testing TLP component level method 50 TDR.

[2] IP4788CZ32 contains a 5 V voltage regulator function for higher input voltages. Any input voltage of 4.925 V < $V_{CC(5V0)}$ < 6.50 V provides HDMI-compliant output levels of 4.8 V to 5.3 V on HDMI_5V0_CON.

Table 7. UTILITY_CON

T_{amb} = –25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies: pins $V_{CC(5V0)}$ and $V_{CC(SYS)}$						
r_{dyn}	dynamic resistance	TLP				
		positive transient [1]	-	1.0	-	Ω
		negative transient [1]	-	1.0	-	Ω
V_{CL}	clamping voltage	100 ns TLP; 50 Ω pulser at 50 ns	-	8.0	-	V
C_i	input capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz,	-	8.0	10	pF
R_{pd}	pull-down resistance		60	100	140	kΩ

[1] ANSI-ESDSP5.5.1-2004, ESD sensitivity testing TLP component level method 50 TDR.

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Table 8. Static characteristics

T_{amb} = –25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDC buffer on connector side[1]						
V_{IH}	HIGH-level input voltage		0.5 × $V_{(HDMI\_5V0\_CON)}$	-	6.5	V
V_{IL}	LOW-level input voltage		–0.5	-	0.3 × $V_{(HDMI\_5V0\_CON)}$	V
V_{OH}	HIGH-level output voltage	[2]	$V_{(HDMI\_5V0\_CON)}$ – 0.02	-	$V_{(HDMI\_5V0\_CON)}$ + 0.02	V
V_{OL}	LOW-level output voltage	internal pull-up and external sink	-	100	200	mV
V_{IK}	input clamping voltage	I_I = –18 mA	-	-	–1.0	V
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 5.0 V; $V_{CC(SYS)}$ = 3.3 V; CEC_STBY = HIGH [2][3]	-	8.0	10	pF
R_{pu}	pull-up resistance		1.6	1.8	2.0	kΩ
DDC buffer on system side[1][4]						
V_{IH}	HIGH-level input voltage	$V_{CC(SYS)}$ = 1.8 V	450	-	-	mV
		$V_{CC(SYS)}$ = 2.5 V	620	-	-	mV
		$V_{CC(SYS)}$ = 3.3 V	760	-	-	mV
		$V_{CC(SYS)}$ = 5.0 V	800	-	-	mV
V_{IL}	LOW-level input voltage	$V_{CC(SYS)}$ = 1.8 V	-	-	330	mV
		$V_{CC(SYS)}$ = 2.5 V	-	-	380	mV
		$V_{CC(SYS)}$ = 3.3 V	-	-	400	mV
		$V_{CC(SYS)}$ = 5.0 V	-	-	420	mV
V_{OH}	HIGH-level output voltage	[2]	$V_{CC(SYS)}$ – 0.02	-	$V_{CC(SYS)}$ + 0.02	V
V_{OL}	LOW-level output voltage	$V_{CC(SYS)}$ = 1.8 V	-	490	500	mV
		$V_{CC(SYS)}$ = 2.5 V	-	640	700	mV
		$V_{CC(SYS)}$ = 3.3 V	-	685	790	mV
		$V_{CC(SYS)}$ = 5.0 V	-	720	830	mV
V_{IK}	input clamping voltage	I_I = –18 mA	-	-	–1.0	V
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz [2]	-	6.0	8.0	pF
R_{pu}	pull-up resistance		3.2	3.65	4.1	kΩ

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Table 8. Static characteristics *...continued*

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CEC_CON[1]						
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.80	V
V_{OH}	HIGH-level output voltage		2.88	3.3	3.63	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.5 mA	-	100	200	mV
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz [2]	-	8.0	10	pF
R_{pu}	pull-up resistance		23.4	26.0	28.6	kΩ
$I_{L(CEC\_CON)}$	leakage current on pin CEC_CON	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; CEC_CON connected to 3.63 V via 27 kΩ	-	-	0.1	μA
CEC_SYS[1][4]						
V_{IH}	HIGH-level input voltage	$V_{CC(SYS)}$ = 1.8 V	450	-	-	mV
		$V_{CC(SYS)}$ = 2.5 V	620	-	-	mV
		$V_{CC(SYS)}$ = 3.3 V	760	-	-	mV
		$V_{CC(SYS)}$ = 5.0 V	800	-	-	mV
V_{IL}	LOW-level input voltage	$V_{CC(SYS)}$ = 1.8 V	-	-	330	mV
		$V_{CC(SYS)}$ = 2.5 V	-	-	380	mV
		$V_{CC(SYS)}$ = 3.3 V	-	-	400	mV
		$V_{CC(SYS)}$ = 5.0 V	-	-	420	mV
V_{OH}	HIGH-level output voltage	[2]	$V_{CC(SYS)}$ − 0.02	-	$V_{CC(SYS)}$ + 0.02	V
V_{OL}	LOW-level output voltage	$V_{CC(SYS)}$ = 1.8 V	-	490	500	mV
		$V_{CC(SYS)}$ = 2.5 V	-	640	690	mV
		$V_{CC(SYS)}$ = 3.3 V	-	675	770	mV
		$V_{CC(SYS)}$ = 5.0 V	-	710	800	mV
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz [2]	-	6.0	7.0	pF
R_{pu}	pull-up resistance		8.5	10	11.5	kΩ
HOTPLUG_DET_CON[1]						
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
R_{pd}	pull-down resistance		60	100	140	kΩ
C_i	input capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz [2]	-	8.0	10	pF

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Table 8. Static characteristics *...continued*

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HOTPLUG_DET_SYS[1]						
V_{OH}	HIGH-level output voltage	I_{OL} = 1 mA	0.7 × $V_{CC(SYS)}$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −1 mA	-	200	300	mV
R_{pd}	pull-down resistance		60	100	140	kΩ

[1] The device is active if the input voltage at pin CEC_STBY is above the HIGH level.

[2] This parameter is guaranteed by design.

[3] Capacitive load measured at power-on.

[4] No external pull-up resistor attached.

Table 9. CEC_STBY power management circuit

$V_{CC(SYS)}$ = 1.62 V to 5.5 V; $V_{CC(5V0)}$ = 4.5 V to 6.5 V; GND = 0 V; T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Board side: input pin CEC_STBY[1]						
V_{IH}	HIGH-level input voltage	HIGH = active [2]	1.2	-	6.5	V
V_{IL}	LOW-level input voltage	LOW = standby [3]	−0.5	-	0.8	V
R_{pd}	pull-down resistance		60	100	140	kΩ
C_i	input capacitance	V_I = 3 V or 0 V	-	6	7	pF

[1] The CEC_STBY pin should be connected permanently to $V_{CC(5V0)}$ or $V_{CC(SYS)}$ if no enable control is needed.

[2] DDC buffers, Hot Plug Detect (HPD) buffer, and HDMI_5V0_CON out enabled; CEC buffer enabled.

[3] DDC buffers, HPD buffer, and HDMI_5V0_CON out disabled; CEC buffer enabled.

7. Dynamic characteristics

Table 10. Dynamic characteristics

$V_{CC(5V0)}$ = 5.0 V; $V_{CC(SYS)}$ = 1.8 V; GND = 0 V; T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDC_DAT_SYS, DDC_CLK_SYS, DDC_DAT_CON, DDC_CLK_CON[1]						
t_{PLH}	LOW to HIGH propagation delay	system side to connector side Figure 11	-	80	-	ns
t_{PHL}	HIGH to LOW propagation delay	system side to connector side Figure 11	-	60	-	ns
t_{PLH}	LOW to HIGH propagation delay	connector side to system side Figure 12	-	120	-	ns
t_{PHL}	HIGH to LOW propagation delay	connector side to system side Figure 12	-	80	-	ns
t_{TLH}	LOW to HIGH transition time	connector side Figure 13	-	150	-	ns
t_{THL}	HIGH to LOW transition time	connector side Figure 13	-	100	-	ns
t_{TLH}	LOW to HIGH transition time	system side Figure 14	-	250	-	ns
t_{THL}	HIGH to LOW transition time	system side Figure 14	-	80	-	ns

[1] All dynamic measurements are done with a 75 pF load. Rise times are determined by internal pull-up resistors.

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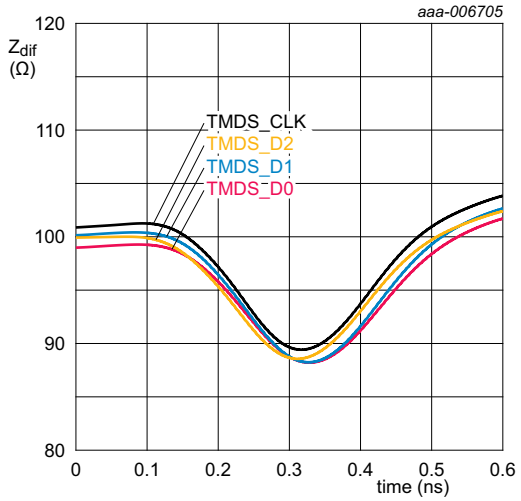
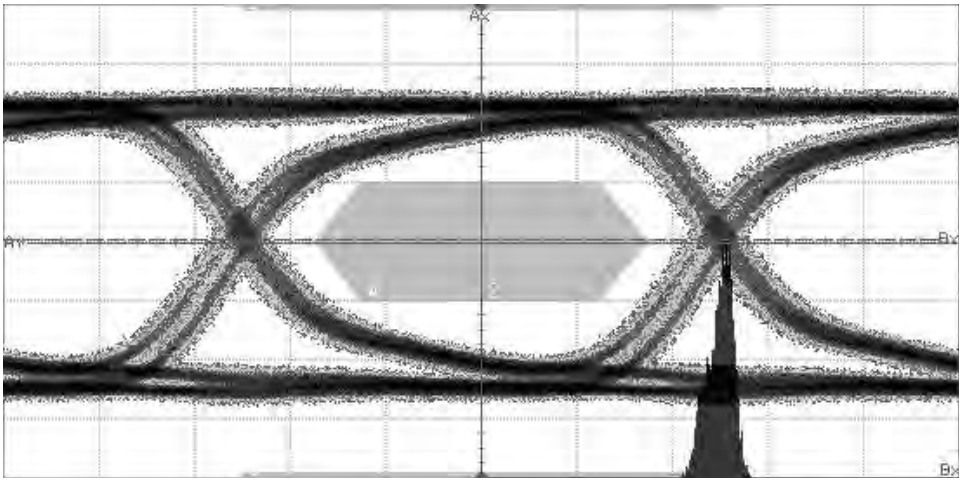


t_r = 200 ps; no filter; $V_{CC(5V0)}$ = 5 V

100 Ω differential (CH1 + CH2)

Fig 3. Differential TDR plot



227 MHz pixel clock

Horizontal scale: 90 ps/div

Vertical scale: 200 mV/div

Offset: 42.6 mV

Fig 4. Eye diagram using IP4788CZ32 (1080p, 12 bit)

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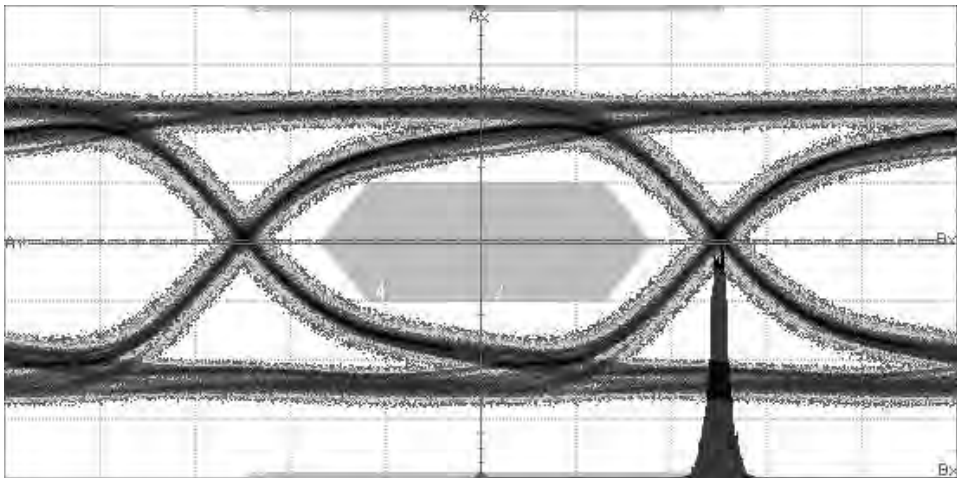
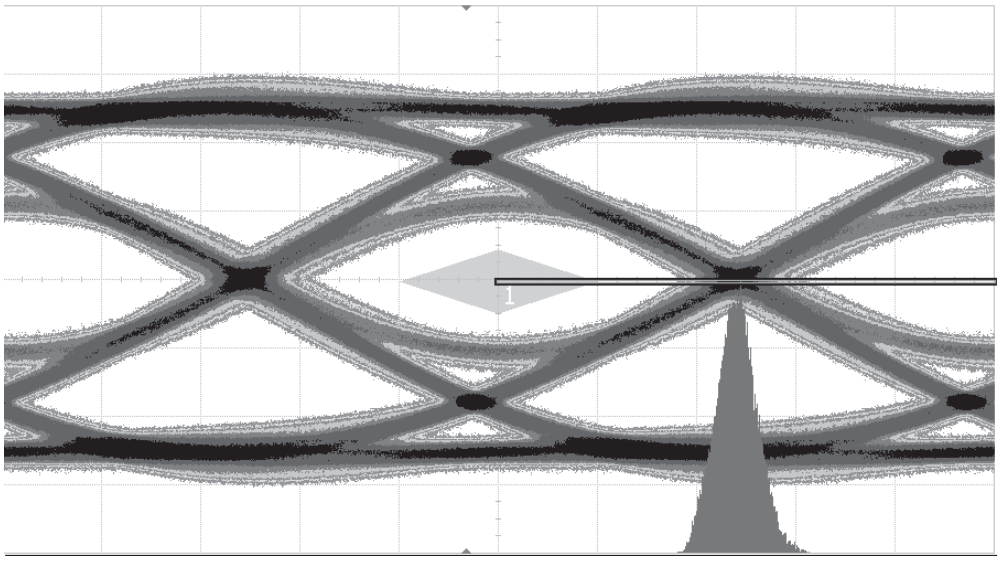


aaa-006707

297 MHz pixel clock
Horizontal scale: 67.5 ps/div
Vertical scale: 200 mV/div
Offset: 42.6 mV

Fig 5. Eye diagram using IP4788CZ32 (1080p, 16 bit)



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148 MHz test frequency
Horizontal scale: 34 ps/div
Vertical scale: 200 mV/div
Measured at TP2 with worst cable emulator, reference cable equalizer and worst case positive skew.

Fig 6. Eye diagram using IP4788CZ32 (2160p, 60 Hz)

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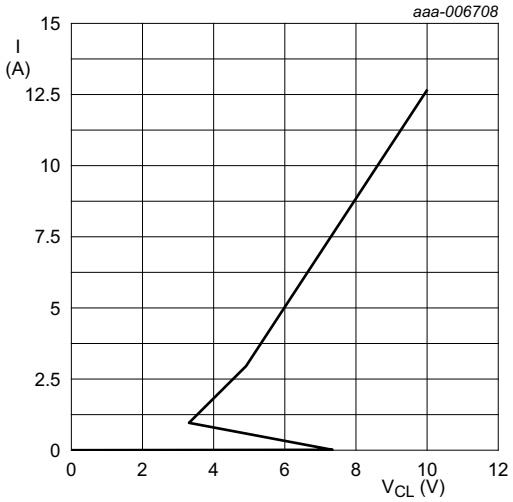
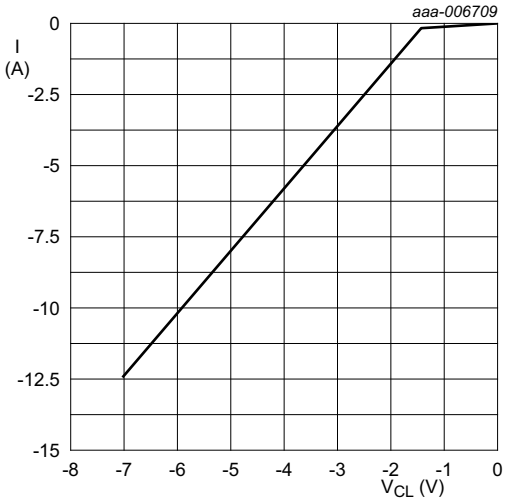


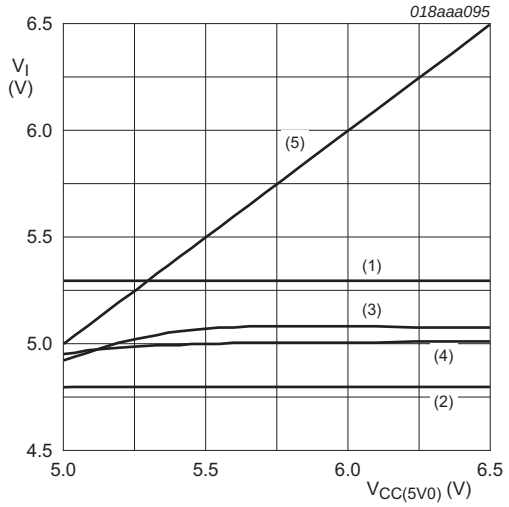
t_p = 100 ns; TLP; TMDS pins

Fig 7. Dynamic resistance with positive clamping



t_p = 100 ns; TLP; TMDS pins

Fig 8. Dynamic resistance with negative clamping



(1) 5.3 V; maximum values; HDMI CTS TID 7-11

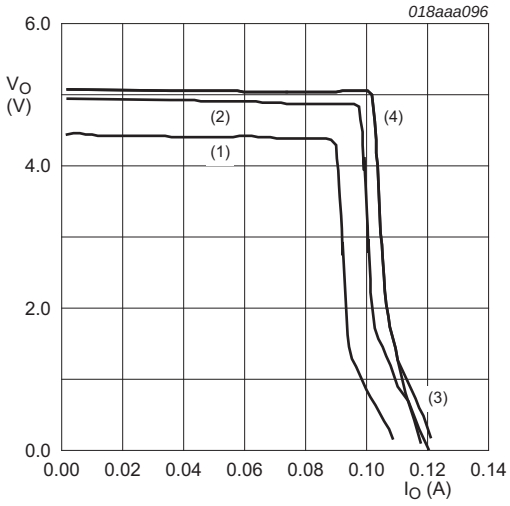
(2) 4.8 V; minimum values; HDMI CTS TID 7-11

(3) I = 0 mA

(4) I = 55 mA

(5) $V_{CC(5V0)}$ supply input; 4.925 V to 6.5 V

Fig 9. Overvoltage limiter function (HDMI_5V0_CON)



(1) $V_{CC(5V0)}$ = 4.5 V

(2) $V_{CC(5V0)}$ = 5.0 V

(3) $V_{CC(5V0)}$ = 5.5 V

(4) $V_{CC(5V0)}$ = 6.5 V

Fig 10. Overcurrent limiter function (HDMI_5V0_CON)

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8. AC waveforms

8.1 DDC propagation delay

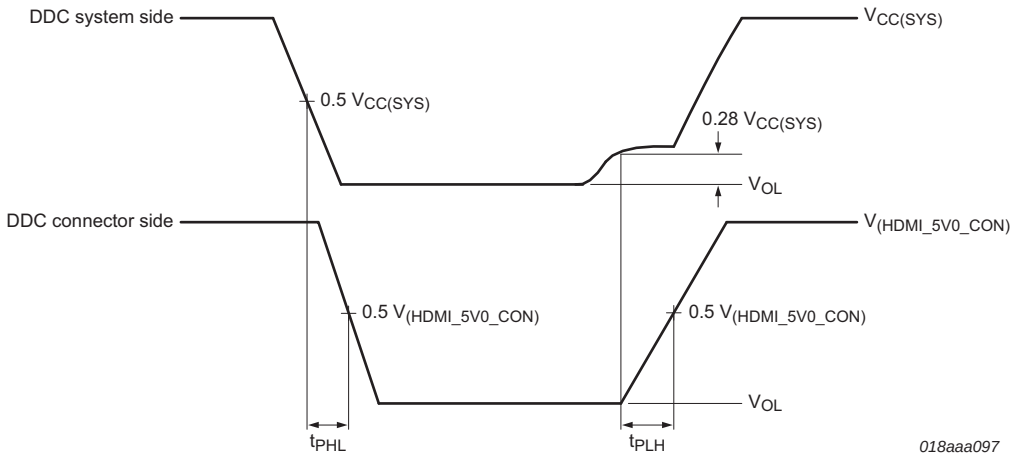

Fig 11. Propagation delay DDC, DDC system side to DDC connector side

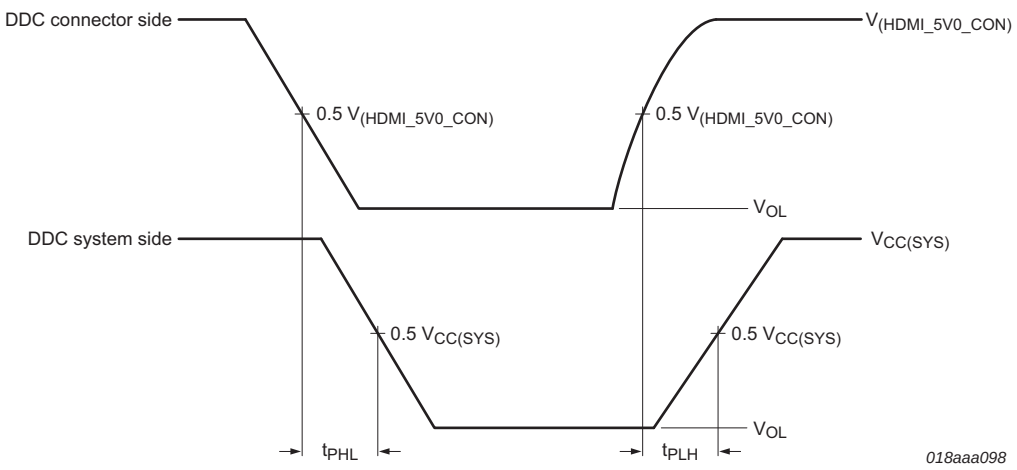

Fig 12. Propagation delay DDC, DDC connector side to DDC system side

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8.2 DDC transition time

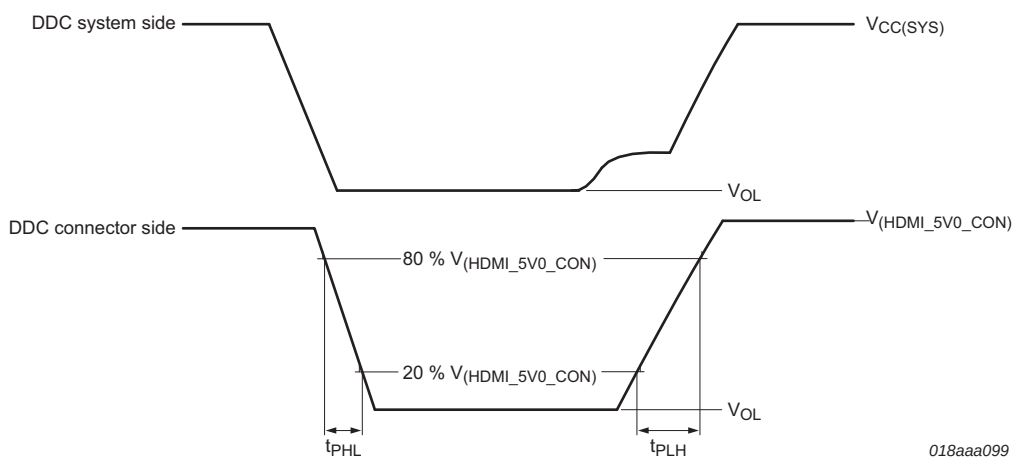

Fig 13. Transition time DDC connector side

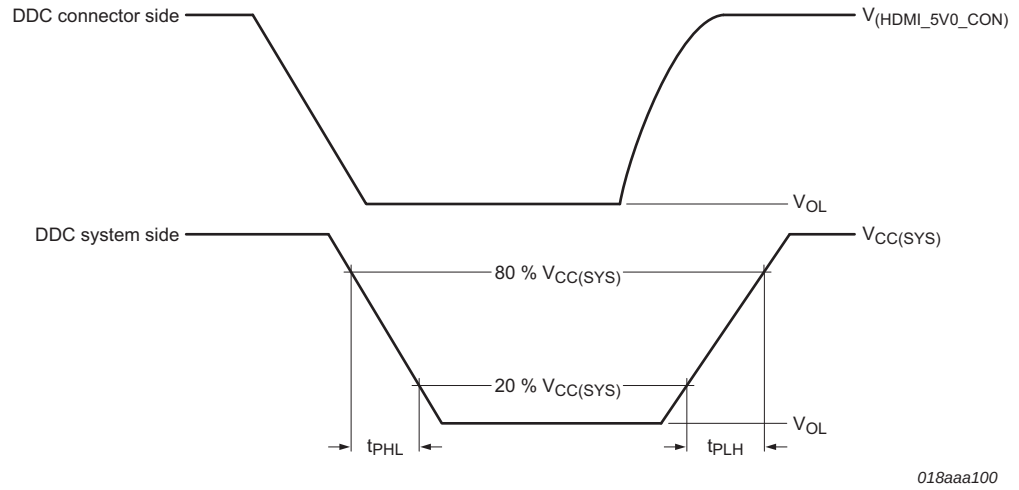

Fig 14. Transition time DDC system side

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9. Application information

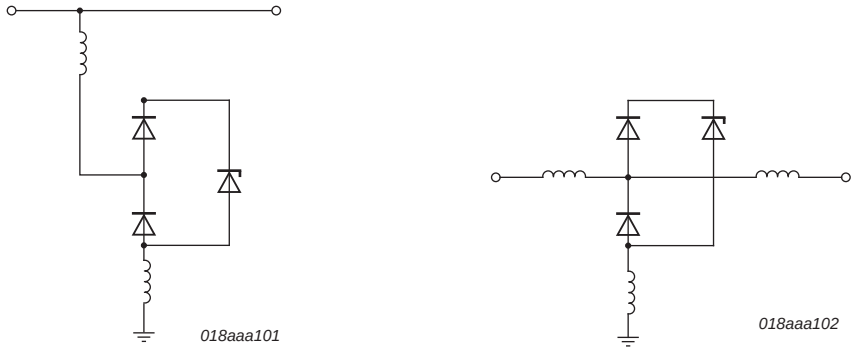
9.1 HDMI connector side ESD protection

All pins directly interfacing with the HDMI connector provide up to 14 kV contact ESD protection according to IEC 61000-4-2, exceeding level 4. In order to utilize the full scope of this protection, connect all connector side pins to the HDMI connector.

9.2 TMDS ESD

To protect the TMDS lines and also to comply with the impedance requirements of the HDMI specification, IP4788CZ32 provides ESD protection with matched TLC ESD structures. Typical Dual Rail Clamp (DRC) or rail-to-rail shunt structures are common for low-capacitance ESD protection (as shown on the left side of Figure 15) where the dominant factor for the TMDS line impedance dip is determined by the capacitive load to ground. Parasitic lead inductances of the packaging in this case work against the ESD clamping performance by including the $\Delta I/\Delta t$ reactance of the inductance into the path of the ESD shunt.

In order to present an effective capacitive load of roughly only 0.7 pF, IP4788CZ32 utilizes these inherent inductances in series with the transmission line. This TLC structure minimizes the capacitive dip, for ideal signal integrity (Figure 15; right side) without complicated PCB pre-compensation. As a beneficial side effect, this structure enhances the ESD performance of the device as well. The reactance of the series inductance attenuates the fast initial peak of the ESD pulse for a lower residual pulse delivered to the Application Specific Integrated Circuit (ASIC).



a. Classic parallel ESD shunt protection

b. Improved series shunt TLC clamping

Fig 15. TLC ESD protection of TMDS lines

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9.3 Operating and standby modes

The operating mode of IP4788CZ32 depends on the availability of the $V_{CC(5V0)}$ and $V_{CC(SYS)}$ supply voltages and on the state of the CEC_STBY input signal. Without availability of both supplies, IP4788CZ32 is in Standby mode. As soon as $V_{CC(5V0)}$ and $V_{CC(SYS)}$ are within the range specified in Section 6, the part is in an operating mode that can be controlled via the CEC_STBY input signal. In case CEC_STBY is LOW, only the CEC buffer is active and enabled to receive or send CEC commands. All other outputs are in a high-ohmic state. A HIGH input signal enables all parts of IP4788CZ32 and puts the device into full operating mode.

Table 11. Operating modes

$V_{CC(SYS)}$	$V_{CC(5V0)}$	CEC_STBY[1]	Mode	Description
< 1.1 V	< 4.5 V	X	Standby mode	all outputs high-ohmic
≥ 1.1 V	≥ 4.5 V	L	CEC Standby mode	CEC circuit active; all other outputs high-ohmic
		H	full operating mode	all functional blocks active

[1] X = Don't care (either LOW or HIGH level); L = LOW-level input; H = HIGH-level input

If no CEC Standby mode is required, or if no special Power-down modes are desired, the CEC_STBY pin can be pulled HIGH to $V_{CC(5V0)}$ or $V_{CC(SYS)}$ for continuous HDMI and CEC operation as soon as the supplies are available.

Strapping the CEC_STBY = $V_{CC(SYS)}$ = V_{DD} of ASIC guarantees that all interface signals ending with the suffix "_SYS" on the system side are disabled when $V_{CC(SYS)}$ goes LOW. This configuration protects the ASIC I/O signals from exceeding its local V_{DD}. In this mode, even if $V_{CC(5V0)}$ is powered, HDMI_5V0_CON goes active and hot plug events can be detected only when the ASIC power supply rail is on.

Strapping CEC_STBY = $V_{CC(5V0)}$ is the most basic configuration where the buffers are enabled whenever the local $V_{CC(5V0)}$ and $V_{CC(SYS)}$ supplies reach minimum operating levels.

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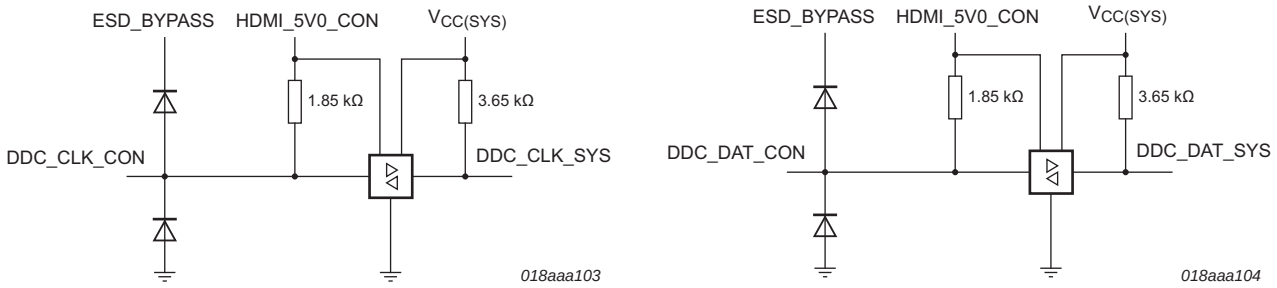
9.4 DDC circuit

The DDC bus circuit integrates all required pull-ups, and provides full capacitive decoupling between the HDMI connector and the DDC bus lines on the PCB. The capacitive decoupling ensures that the maximum capacitive load is well within the 50 pF maximum of the HDMI specification. No external pull-ups or pull-downs are required.

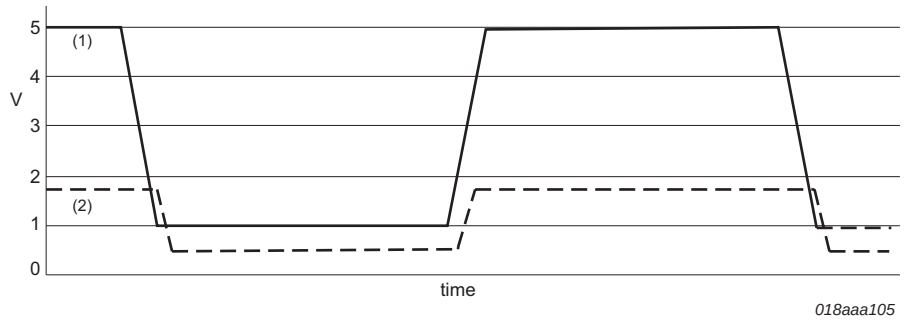
The bidirectional buffers support high-capacitive load on the HDMI cable-side. Various non-compliant but prevalent low-cost cables have been observed. They have a capacitive load of up to 6 nF on the DDC lines, far exceeding the 700 pF HDMI limit. IP4788CZ32 can easily decouple this from the weaker ASIC I/O buffers, and drive the rogue cable successfully.



a. DDC clock

b. DDC data

Fig 16. DDC circuit



(1) Valid I^2C signaling example on the cable (connector side) from 5 V (HIGH) to approximately 1 V (LOW).

(2) Valid logic-level signaling example to the ASIC (system side) from 1.8 V (HIGH) to approximately 0.5 V (LOW).

Fig 17. DDC level shifting waveform example

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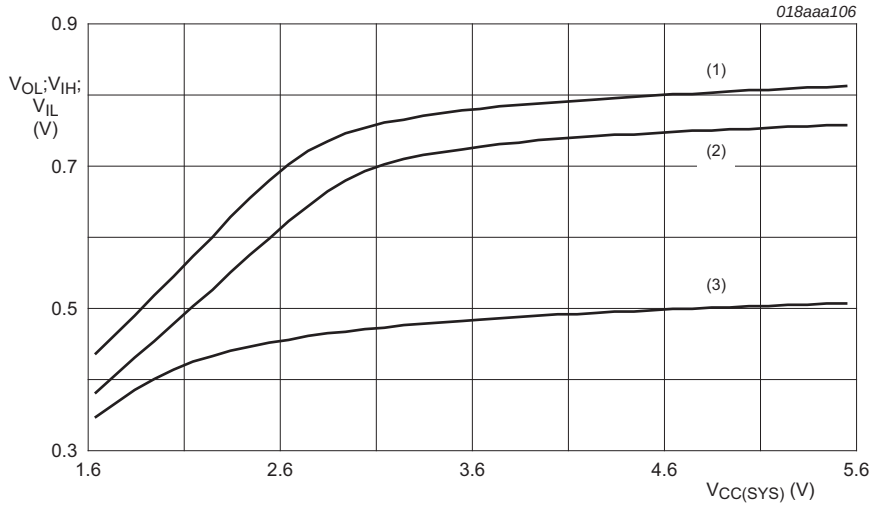
9.5 Logic low I²C voltage shifter

The DDC buffers provide an additional feature commonly required for high-integration HDMI ASICs. In order to be compatible with the 5 V I²C standard used for DDC communication, I/O buffer cells of many HDMI modern transmitter chips require level shifting. As FET-based level shifting just limits the high level of the signal, the low level remains unchanged. As a result, the low-level voltages on the DDC bus often exceed the 0.3 V_{DD} LOW-level input voltage (V_{IL}) limit of low-voltage I/O buffers.

To enable proper operation that is independent of the system side I/O voltage, the DDC buffers inside IP4788CZ32 shift both the high and the low levels by the required amount. This ensures that low levels on the system side DDC bus match the low-level input voltage requirements down to I/O voltages of 1.8 V.

Besides the DDC buffers, this feature is also included in the CEC buffer, allowing standard I/O buffer cells to be used in HDMI ASICs and microcontrollers.



(1) $V_{OL(max)}$ driven to system (ASIC) side when I²C logic low (less than 0.3 × HDMI_5V0_CON)

(2) $V_{IH(min)}$ threshold on system (ASIC) side to drive I²C logic low

(3) $V_{IL(max)}$ threshold on system (ASIC) side to drive I²C logic low

Fig 18. Logic voltage thresholds as a function of supply voltage; on connector (HDMI) side

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9.6 Hot plug detect circuit and HEAC support

IP4788CZ32 includes a hot plug detect circuit which simplifies the hot plug application. The circuit generates a standard logic level from the hot plug signal.

The hot plug detect circuit is pulling down the signal to avoid any floating signal. The comparator guarantees a save detection of the 2 V hot plug signal without any glitches or oscillation at the hot plug output.

IP4788CZ32 also provides an additional ESD pin to protect the reserved / HEAC pin along with hot plug detect to 14 kV IEC 61000-4-2.

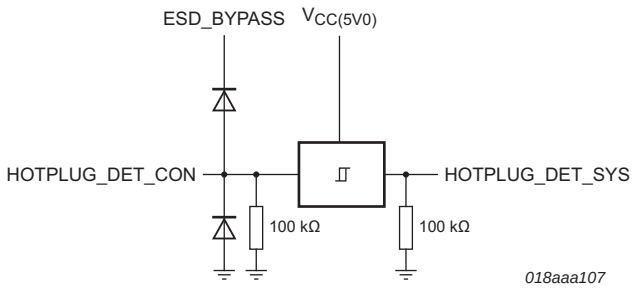

Fig 19. Hot plug detect circuit

9.7 CEC

The logical multidrop topology of the CEC bus can include complex physical stubs, loading cables, and interconnects which may deteriorate signal quality.
The IP4788CZ32 includes a full bidirectional buffer to drive the CEC bus and isolate the CEC microcontroller or ASIC General-Purpose Input/Output (GPIO).

The CEC buffer derives power from an on-board 3.3 V regulator from the $V_{CC(5V0)}$ domain (see Figure 20). This deviation allows extensive system power management configurations and guarantees an HDMI-compliant $V_{(CEC\_CON)}$ on the connector. It also allows a backdrive-protected 125 μA nominal CEC pull-up which does not degrade the bus when powered down.

By placing the CEC microcontroller and $V_{CC(5V0)}$ input on a 5 V rail as shown in Figure 23, the CEC microcontroller can communicate over CEC for power commands. It can then enable the HDMI port via the CEC_STBY pin, as well as the rest of the system as needed.

The CEC buffer is always active as soon as both supply voltages are present. For details on the operating and Standby modes of IP4788CZ32, see Section 9.3.

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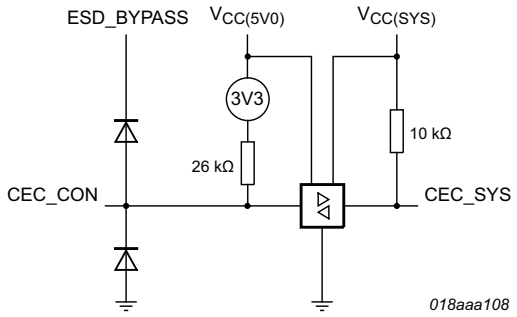

Fig 20. CEC module

9.8 Backdrive protection

The HDMI connector contains various signals which can partly supply current into an HDMI device which is powered down.

Typically, the DDC lines and the CEC signals can force significant current back into the powered-down rails as shown in Figure 21, causing power-on reset problems with the system, and possible damage. The IP4788CZ32 prevents this backdrive condition whenever the I/O voltage is greater than the local supply.

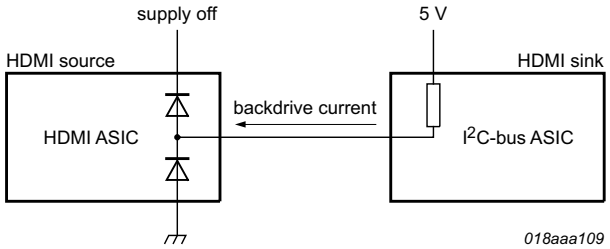

Fig 21. Generalized backdrive protection

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9.9 55 mA overcurrent / overvoltage LDO function

To isolate faults from the source power supply while still meeting HDMI output specifications, IP4788CZ32 integrates a complete linear output overcurrent protection.

The Low DropOut (LDO) design provides a low-cost solution requiring just a single output capacitor (1 μF or higher, Equivalent Series Resistance (ESR) < 1 Ω), eliminating start-up and ripple concerns (see Figure 22).

A typical 100 mV V_{do} overcurrent-only solution would require a 5.1 V ± 3 % input supply to guarantee 4.8 V to 5.3 V over 0 mA to 55 mA at the HDMI connector.
The overcurrent / overvoltage feature of IP4788CZ32 allows the use of wider tolerance input supplies up to 6.5 V while still meeting the 4.8 V-to-5.3 V output limit required by HDMI. So, for example, a cost-reduced 5.2 V ± 5 % or even a 5.5 V ± 10 % supply can be used with the IP4788CZ32.

As with all the I/O pins, this block is ESD-protected and also provides backdrive protection when a rogue HDMI sink powers the HDMI cable unexpectedly.

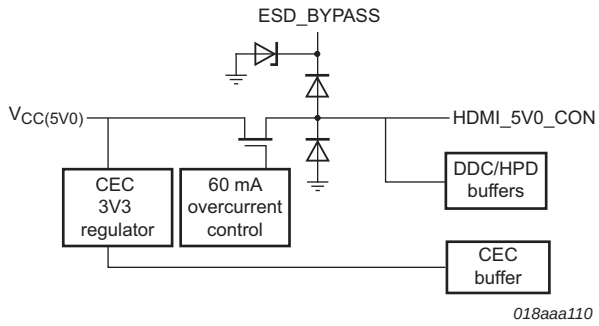

Fig 22. 5 V LDO with overcurrent / overvoltage protection

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9.10 Schematic view of application

Only a single external component (C_O = 1 µF) is required to protect and interface the ASIC to a complete and compliant HDMI port. The 100 nF ESD bypass capacitor is optional.

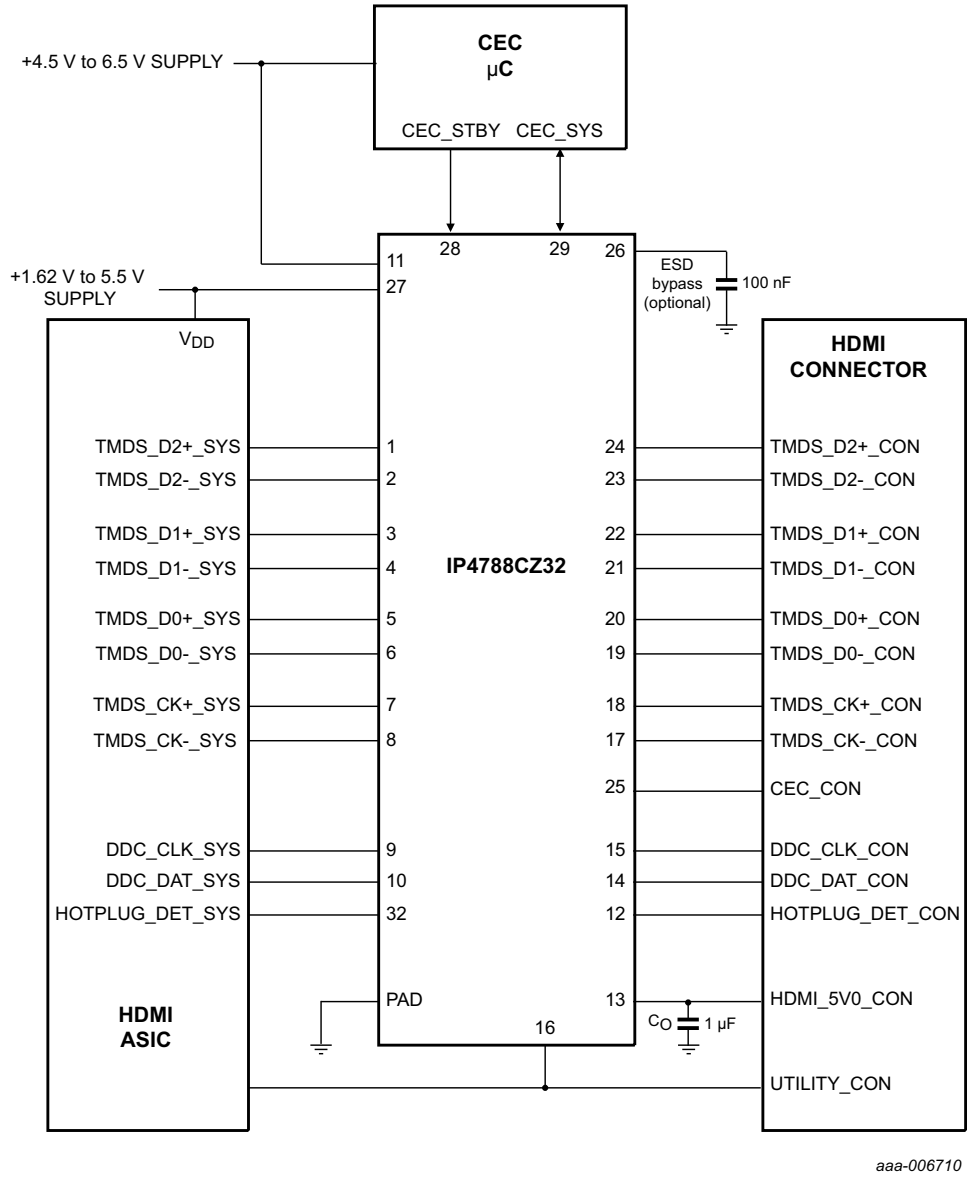

Fig 23. Schematic view of IP4788CZ32 application

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9.11 Typical application

The IP4788CZ32 is designed to simplify routing to the HDMI connector and to ease the incorporation of high-level ESD protection into delicately balanced high-speed TMDS lines. These lines rely on tightly controlled microstrip or stripline transmission lines with minimal impedance discontinuities. They can deteriorate return loss, increase deterministic jitter and generally erode overall link signal integrity.

Normally when designing the PCB with standard shunt ESD clamps, careful consideration must be given to manual pre-compensation of the additional load of the added ESD component. With the IP4788CZ32 TLCs, the ESD suppressor is designed to maintain the characteristic impedance of the PCB microstrip or stripline. Therefore the designer needs only to be concerned with the standard-controlled impedance of the unloaded PCB lines. This feature simplifies the task of the PCB designer, and minimizes the tuning cycles, which are sometimes required when pre-compensation misses the mark. A basic application diagram for the ESD protection of an HDMI interface is shown in Figure 24 for a type-A HDMI connector.

The optimized DFN5050-32 pinning simplifies the PCB design to keep the ESD protection close to the connector where it can minimize the coupling of the ESD pulse onto other lines in the system during a strike.

Due to the integrated pull-up and pull-down resistors, only two external capacitors are required to implement a fully compliant HDMI port.

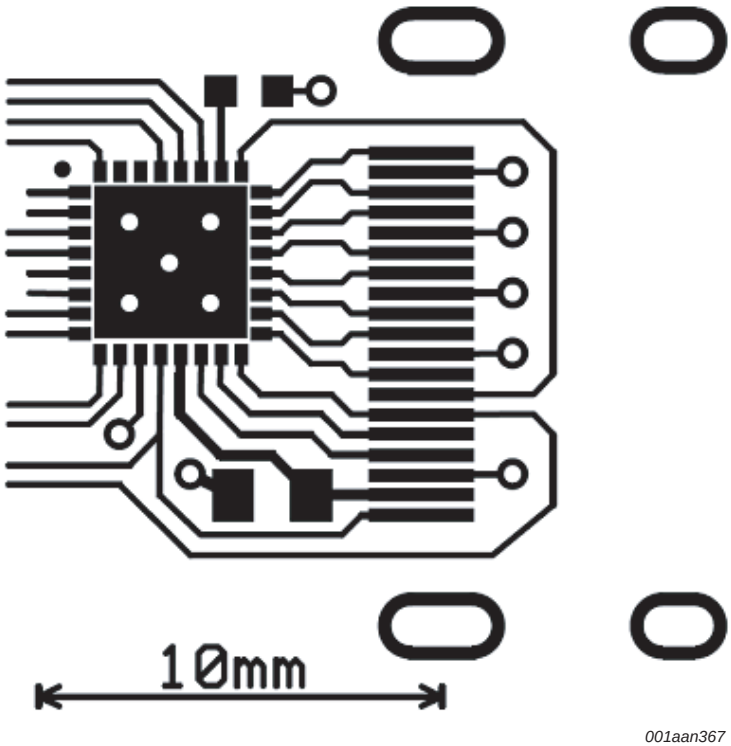

Fig 24. Application of the IP4788CZ32 showing optimized single-layer HDMI type-A connector routing

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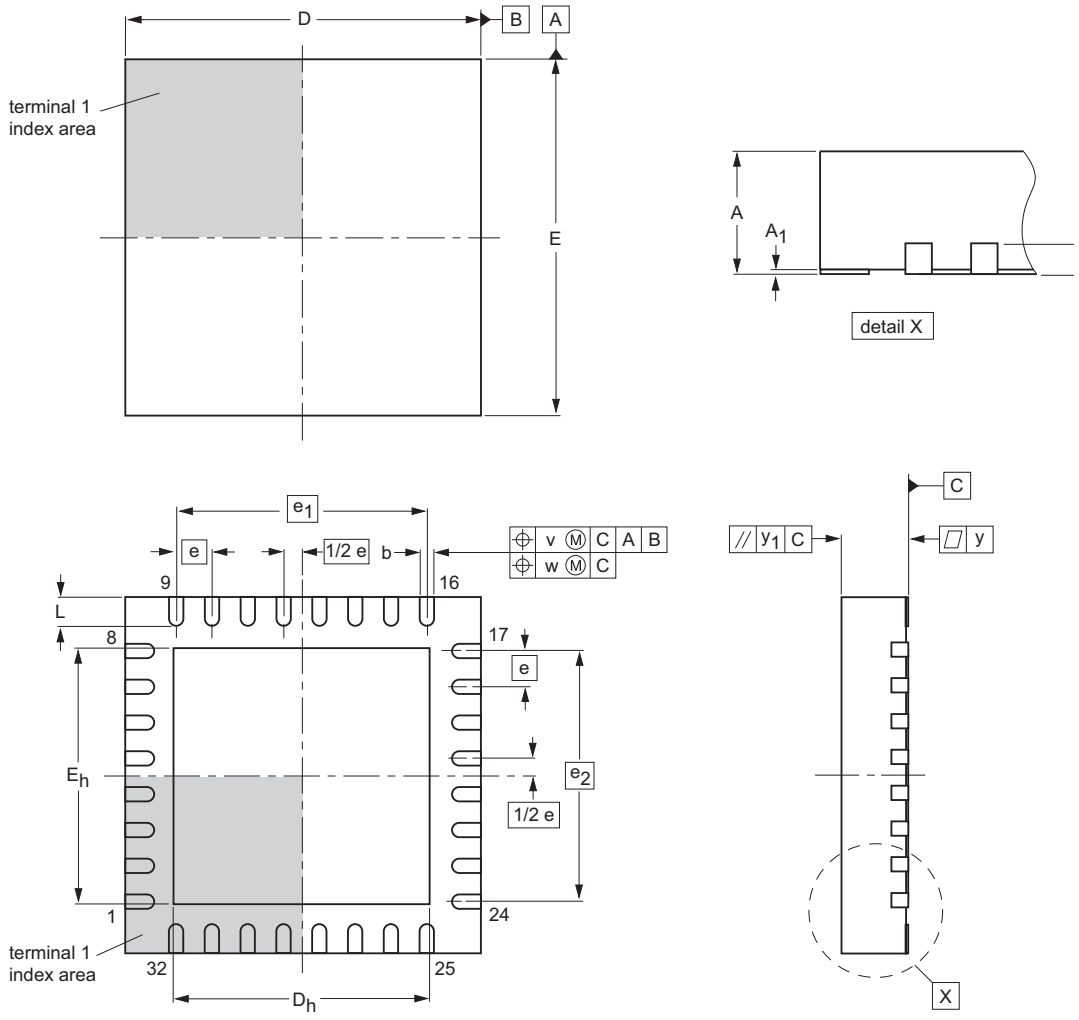
10. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



Dimensions

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-3		MO-220				~~11-06-14~~ 11-06-21

Fig 25. Package outline DFN5050-32 (SOT617-3/HVQFN32)

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11. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

11.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

11.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

11.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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11.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 26) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

Table 12. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 26.

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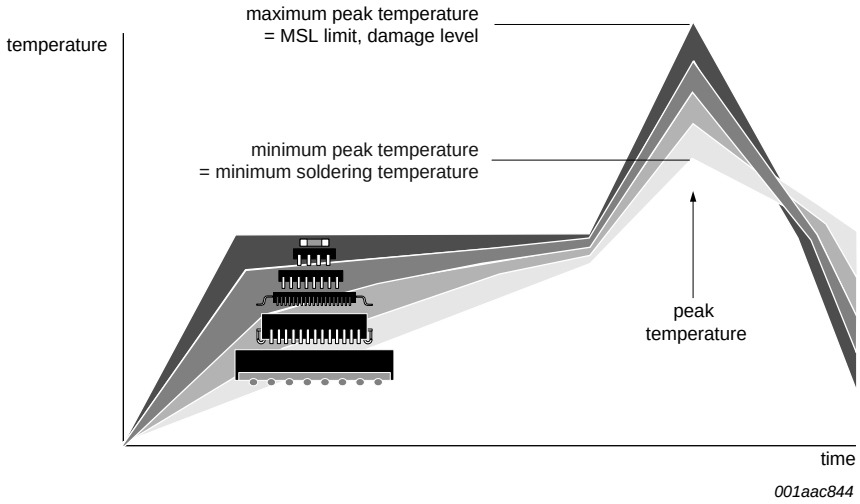

MSL: Moisture Sensitivity Level

Fig 26. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

12. Glossary

HDMI sink — Device which receives HDMI signals for example, a TV set.

HDMI source — Device which transmits HDMI signal for example, DVD player.

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13. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4788CZ32 v.2	20141124	Product data sheet	-	IP4788CZ32 v.1
Modifications:	• Editorial updates • Section 1 “Product profile”: updated • Figure 2 “Functional diagram”: updated • Table 3 “Limiting values”: V_{ESD} value corrected • Table 8 “Static characteristics”: added parameter leakage current on pin CEC_CON • Figure 6: added • Section 14 “Legal information”: updated			
IP4788CZ32 v.1	20130308	Product data sheet	-	-

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14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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