

## N-channel 500 V, 0.45 $\Omega$ typ, 8 A, MDmesh II Plus™ low $Q_g$ Power MOSFETs in DPAK and TO-220FP packages

Datasheet - preliminary data

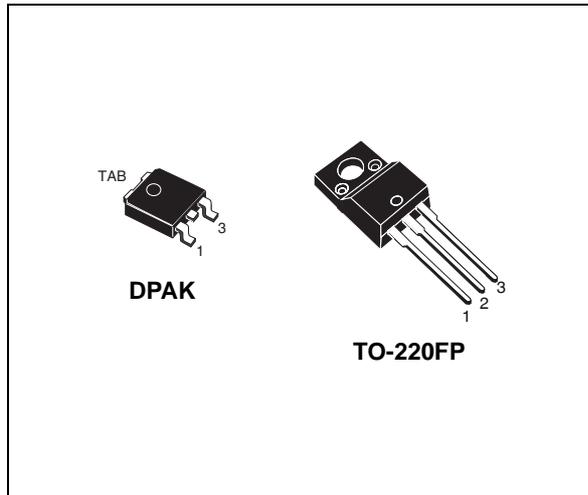
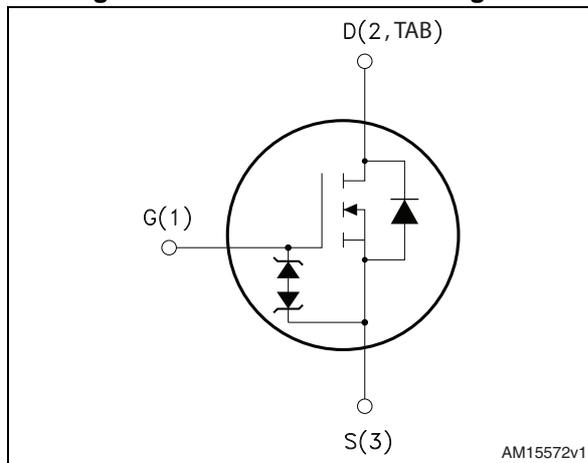


Figure 1. Internal schematic diagram



### Features

Order codes	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	$I_D$
STD11N50M2	550 V	0.53 $\Omega$	8 A
STF11N50M2			

- Extremely low gate charge
- Lower  $R_{DS(on)}$  x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

These devices are N-channel Power MOSFETs developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low  $Q_g$ . These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD11N50M2	11N50M2	DPAK	Tape and reel
STF11N50M2		TO-220FP	Tube

# Contents

- 1      Electrical ratings ..... 3**
- 2      Electrical characteristics ..... 4**
  - 2.1    Electrical characteristics (curves) ..... 6
- 3      Test circuits ..... 9**
- 4      Package mechanical data ..... 10**
  - 4.1    DPAK, STD11N50M2 .....11
  - 4.2    TO-220FP, STF11N50M2 ..... 14
- 5      Packaging mechanical data ..... 16**
- 6      Revision history ..... 18**



# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
$V_{GS}$	Gate-source voltage	± 25		V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	8		A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	5		A
$I_{DM}^{(1)}$	Drain current (pulsed)	32		A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	85	25	W
$dv/dt^{(1)}$	Peak diode recovery voltage slope	15		V/ns
$dv/dt^{(2)}$	MOSFET $dv/dt$ ruggedness	50		
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}$ ; $T_C = 25\text{ °C}$ )	2500		
$T_{stg}$	Storage temperature	- 55 to 150		°C
$T_j$	Max. operating junction temperature			

- $I_{SD} \leq 8\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\ peak} < V_{(BR)DSS}$ ,  $V_{DD}=400\text{ V}$
- $V_{DS} \leq 400\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.47	5	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max <sup>(1)</sup>	50		°C/W
$R_{thj-amb}$	Thermal al resistance junction-ambient max	62.5		°C/W

- When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	2		A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25\text{ °C}$ , $I_D= I_{AR}$ ; $V_{DD}=50$ )	190		mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	500			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 500\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 500\text{ V}, T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 4\text{ A}$		0.45	0.53	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	395	-	pF
$C_{oss}$	Output capacitance		-	26	-	pF
$C_{riss}$	Reverse transfer capacitance		-	1	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }400\text{ V}$	-	108	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0$	-	6.3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}, I_D = 8\text{ A}, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> )	-	12	-	nC
$Q_{gs}$	Gate-source charge		-	2	-	nC
$Q_{gd}$	Gate-drain charge		-	6.4	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}, I_D = 4\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> and <a href="#">Figure 21</a> )	-	11	-	ns
$t_r$	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	8	-	ns
$t_f$	Fall time		-	28.5	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0, I_{SD} = 8 \text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 18</a> )	-	258		ns
$Q_{rr}$	Reverse recovery charge		-	1.84		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	14.3		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 18</a> )	-	370		ns
$Q_{rr}$	Reverse recovery charge		-	2.87		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	15.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK

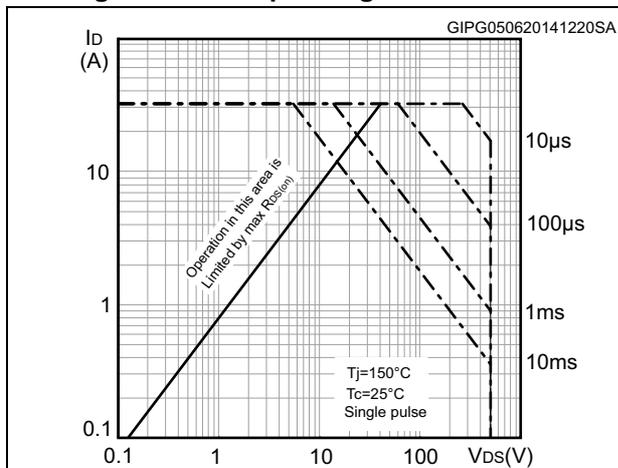


Figure 3. Thermal impedance for DPAK

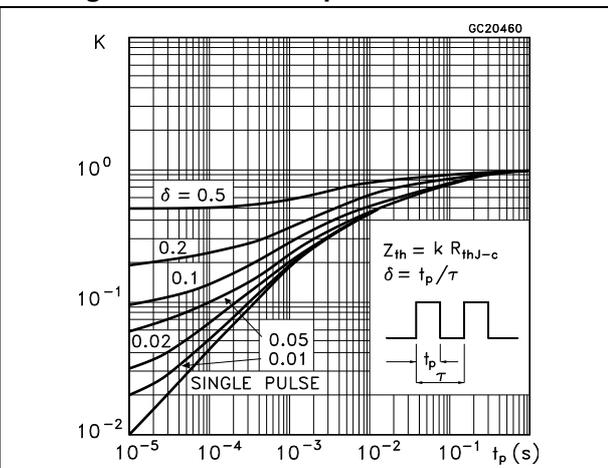


Figure 4. Safe operating area for TO-220FP

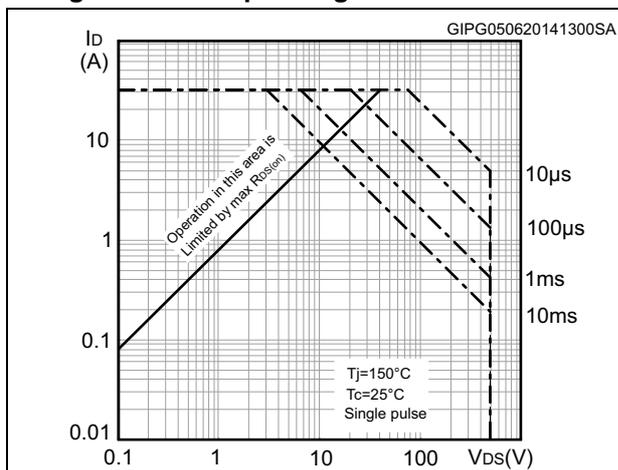


Figure 5. Thermal impedance for TO-220FP

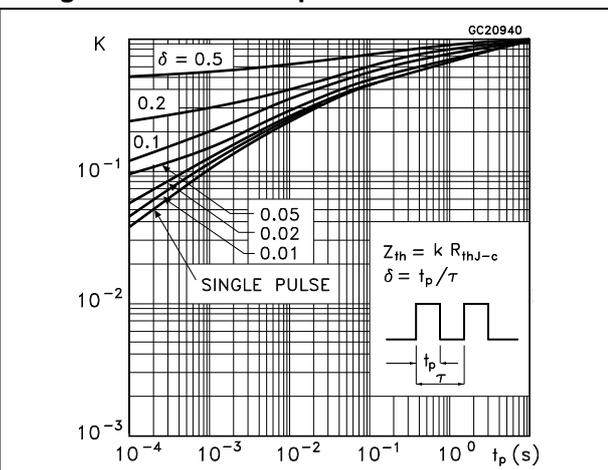


Figure 6. Output characteristics

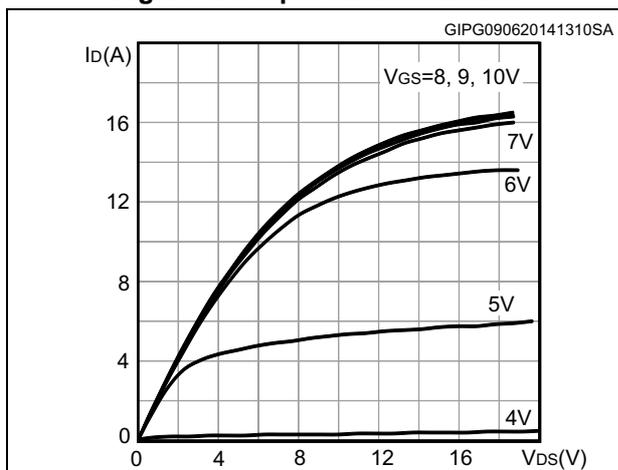


Figure 7. Transfer characteristics

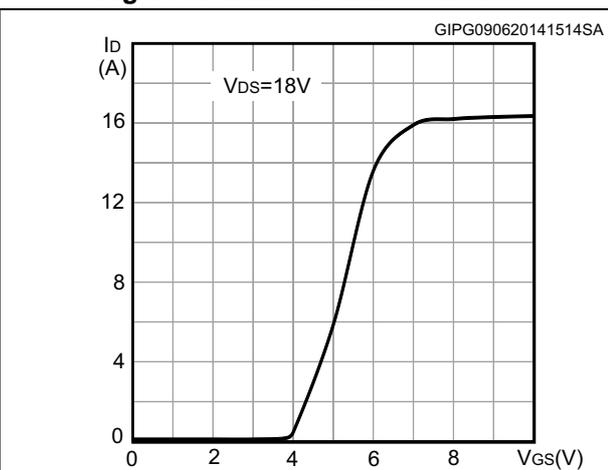


Figure 8. Gate charge vs gate-source voltage

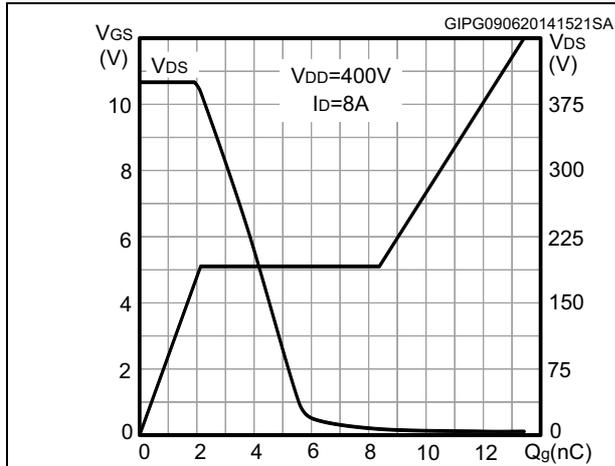


Figure 9. Static drain-source on-resistance

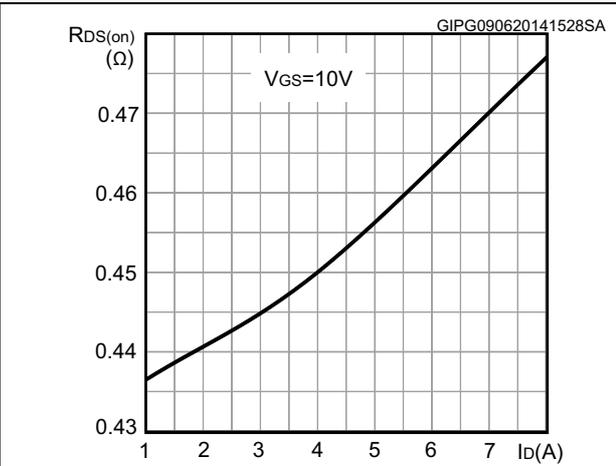


Figure 10. Capacitance variations

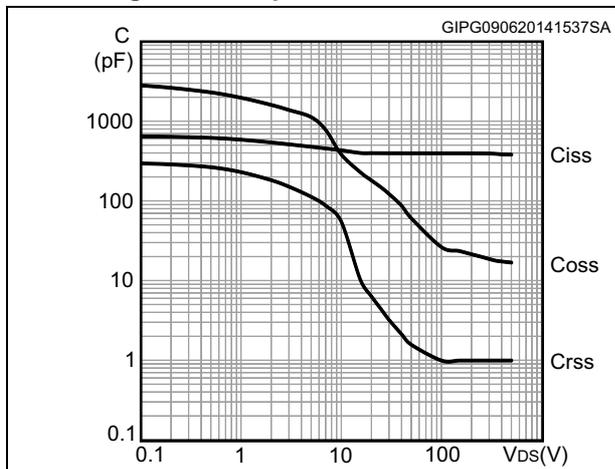


Figure 11. Output capacitance stored energy

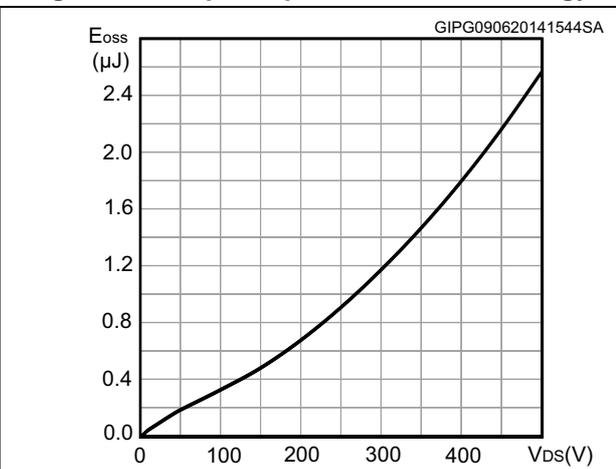


Figure 12. Normalized gate threshold voltage vs temperature

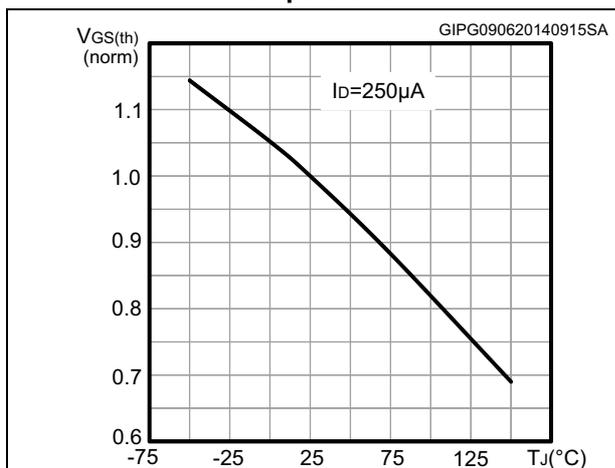


Figure 13. Normalized on-resistance vs temperature

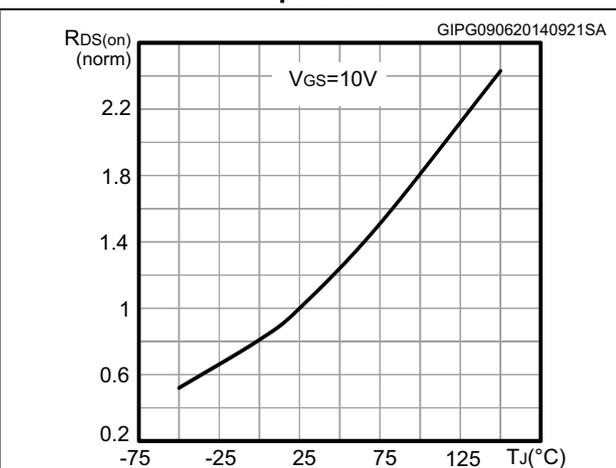


Figure 14. Normalized  $V_{(BR)DSS}$  vs temperature

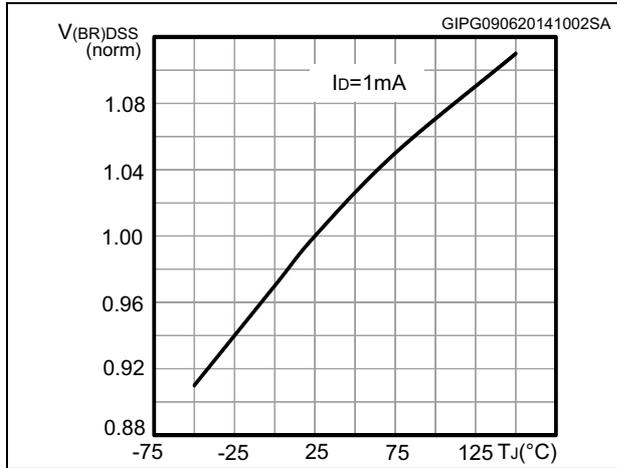
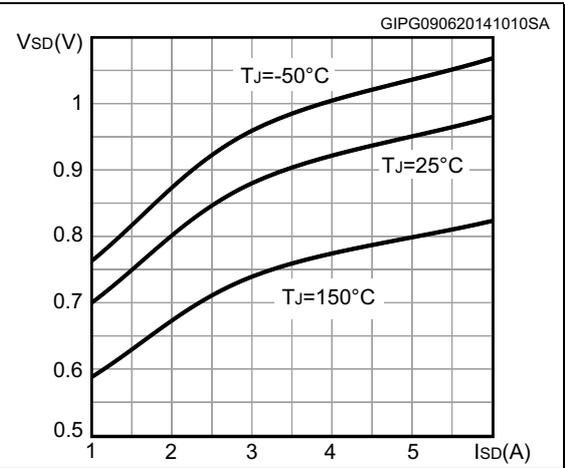
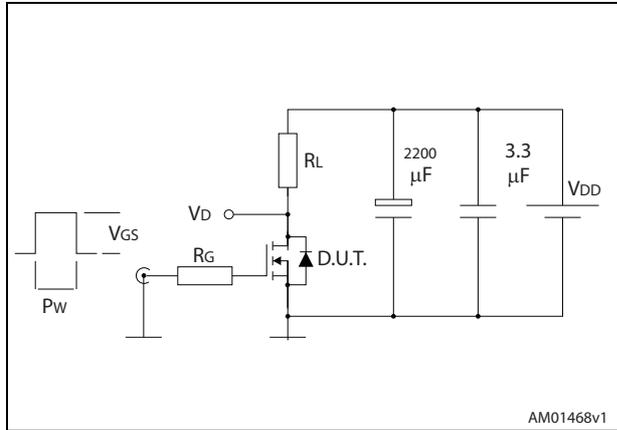


Figure 15. Source-drain diode forward characteristics



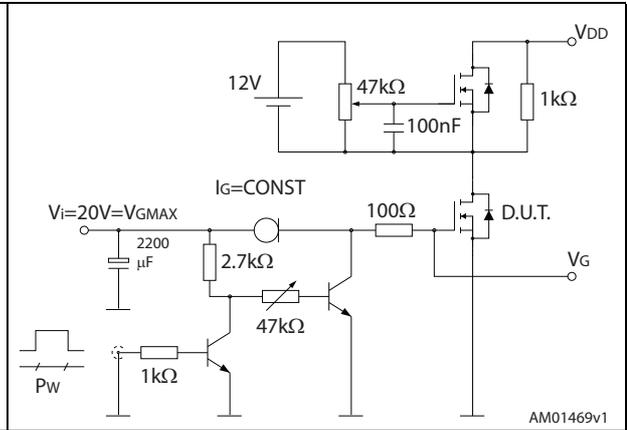
### 3 Test circuits

Figure 16. Switching times test circuit for resistive load



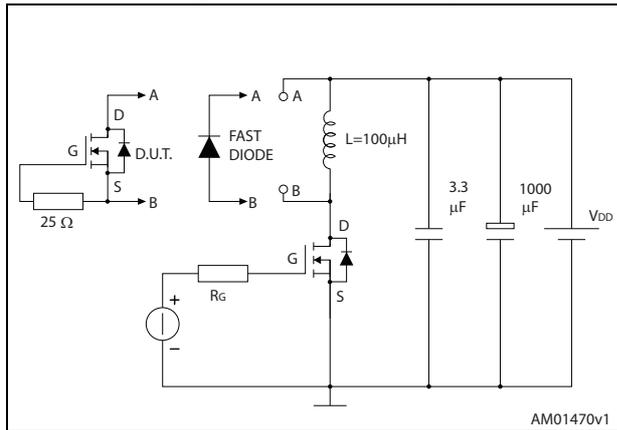
AM01468v1

Figure 17. Gate charge test circuit



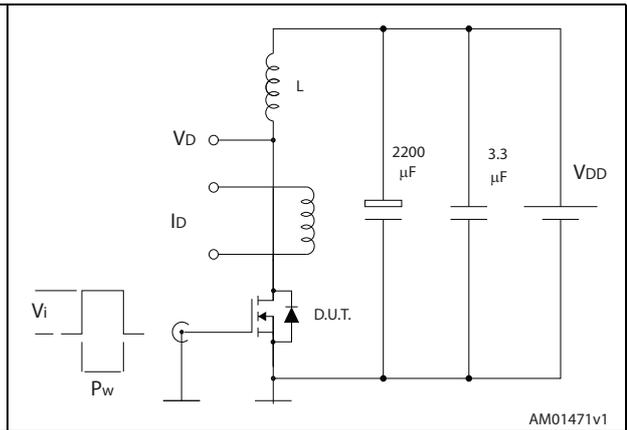
AM01469v1

Figure 18. Test circuit for inductive load switching and diode recovery times



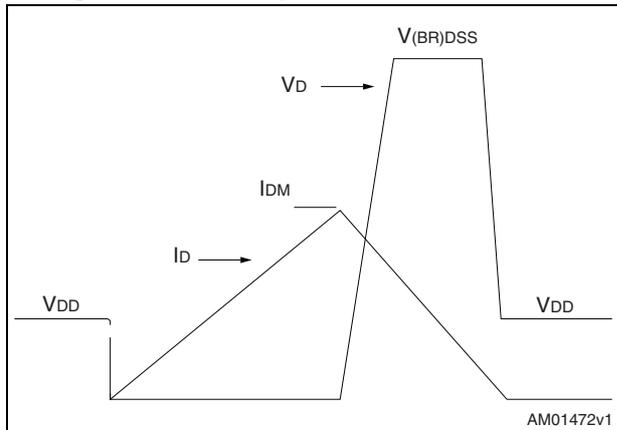
AM01470v1

Figure 19. Unclamped inductive load test circuit



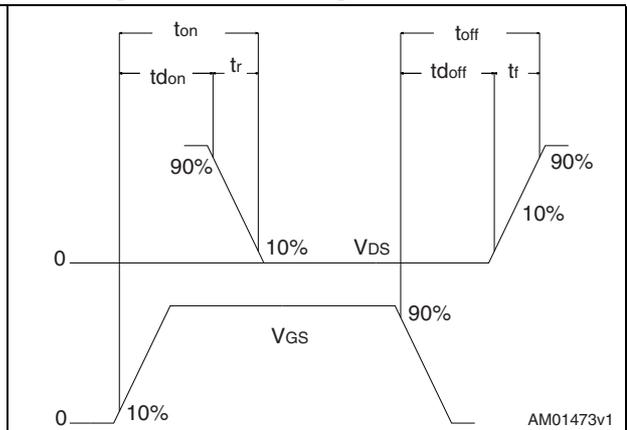
AM01471v1

Figure 20. Unclamped inductive waveform



AM01472v1

Figure 21. Switching time waveform



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

4.1 DPAK, STD11N50M2

Figure 22. DPAK (TO-252) type A drawing

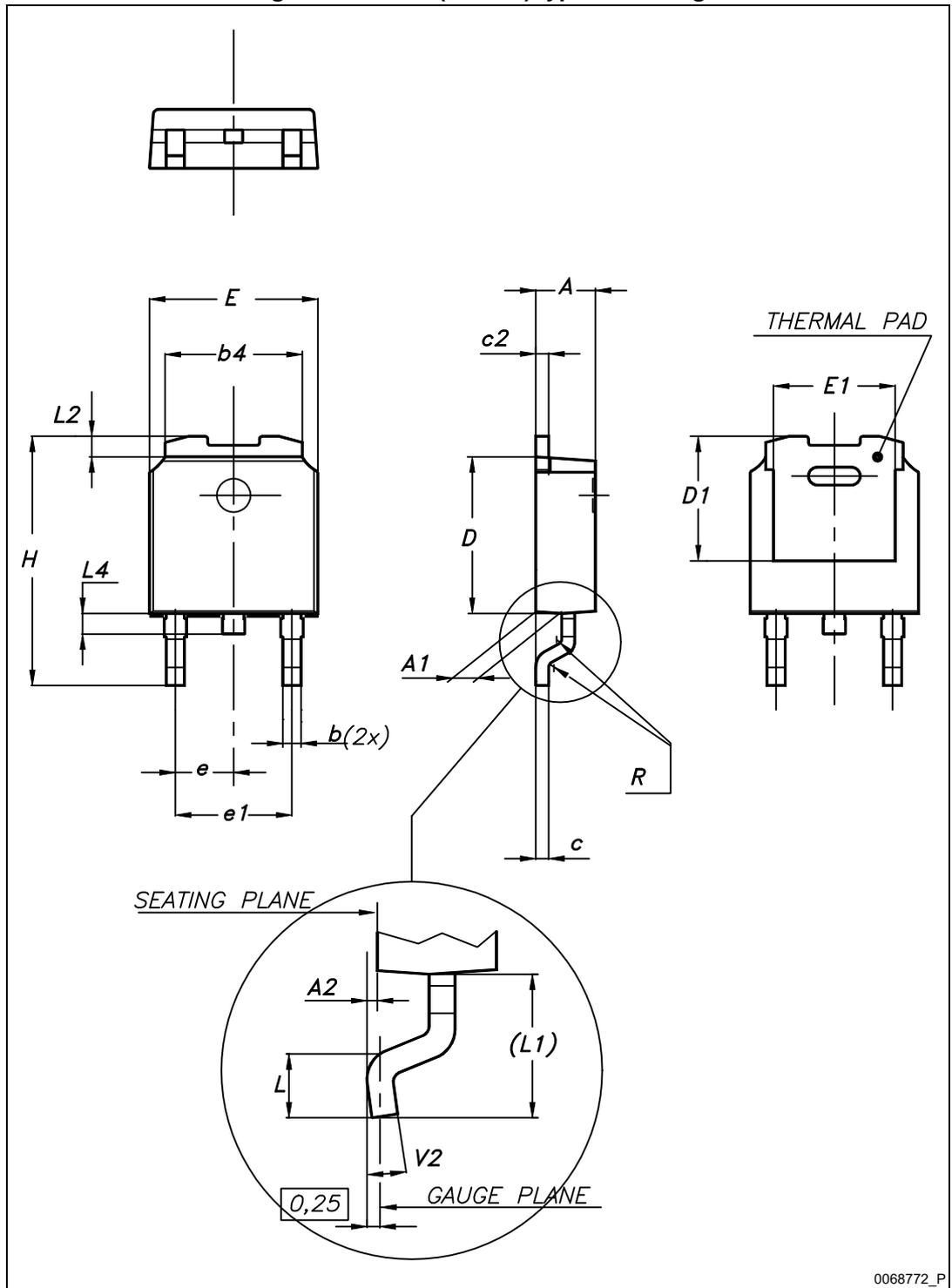
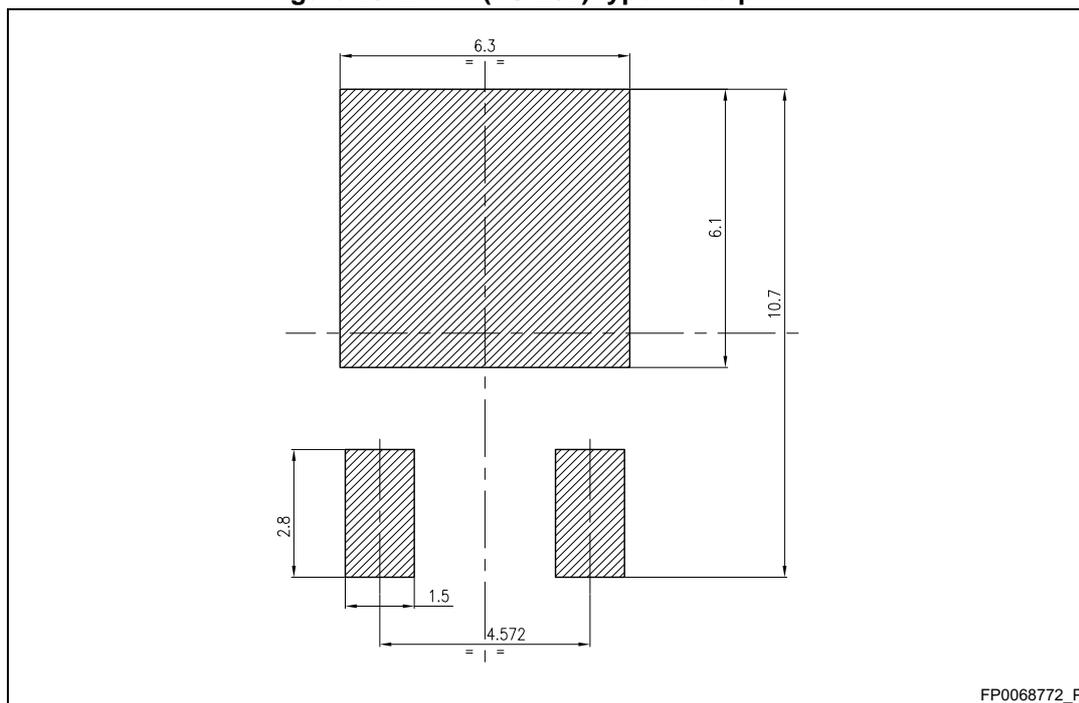


Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

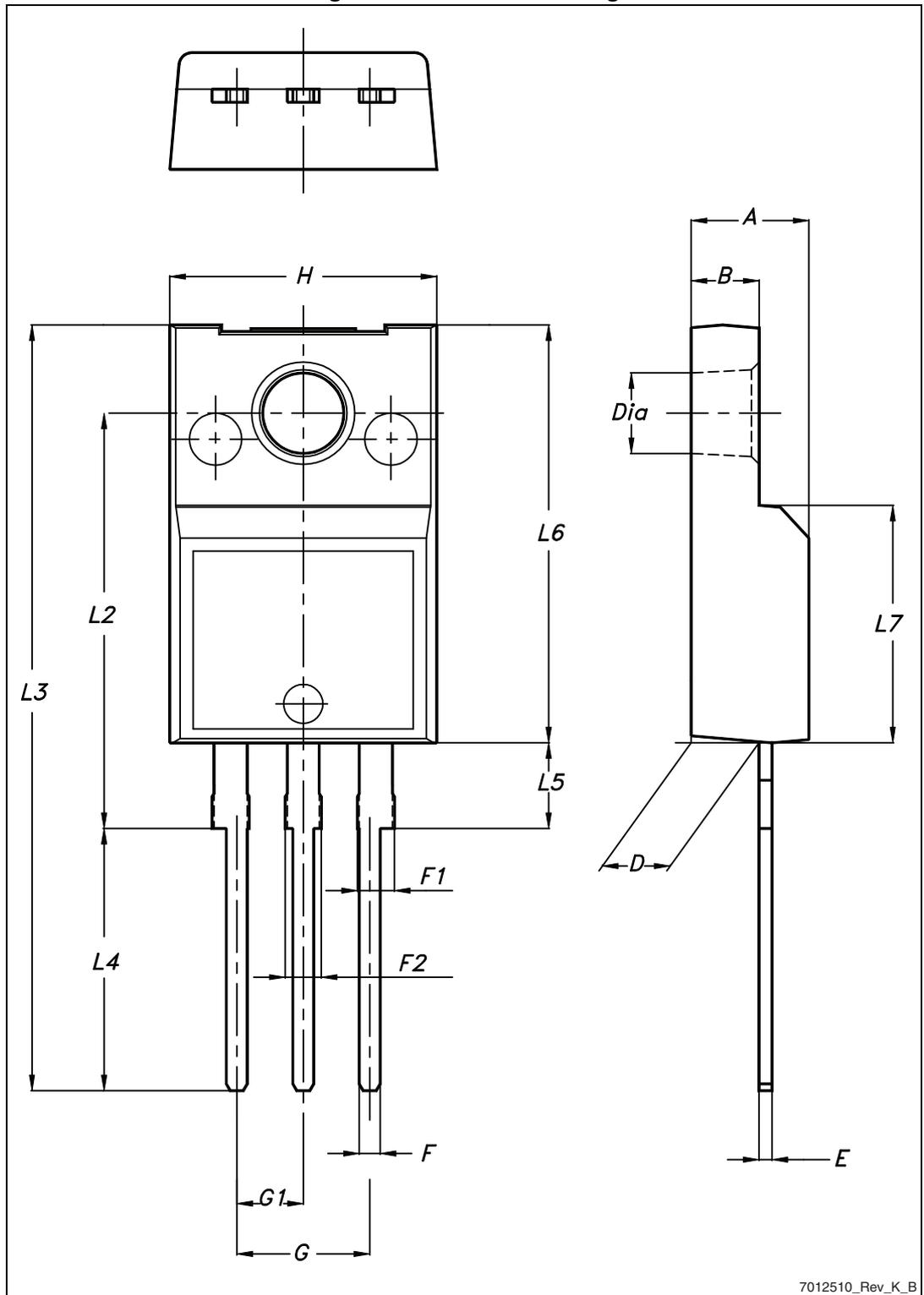
Figure 23. DPAK (TO-252) type A footprint (a)



a. All dimensions are in millimeters

### 4.2 TO-220FP, STF11N50M2

Figure 24. TO-220FP drawing



7012510\_Rev\_K\_B

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Ø	3		3.2

# 5 Packaging mechanical data

Figure 25. Tape for DPAK (TO-252)

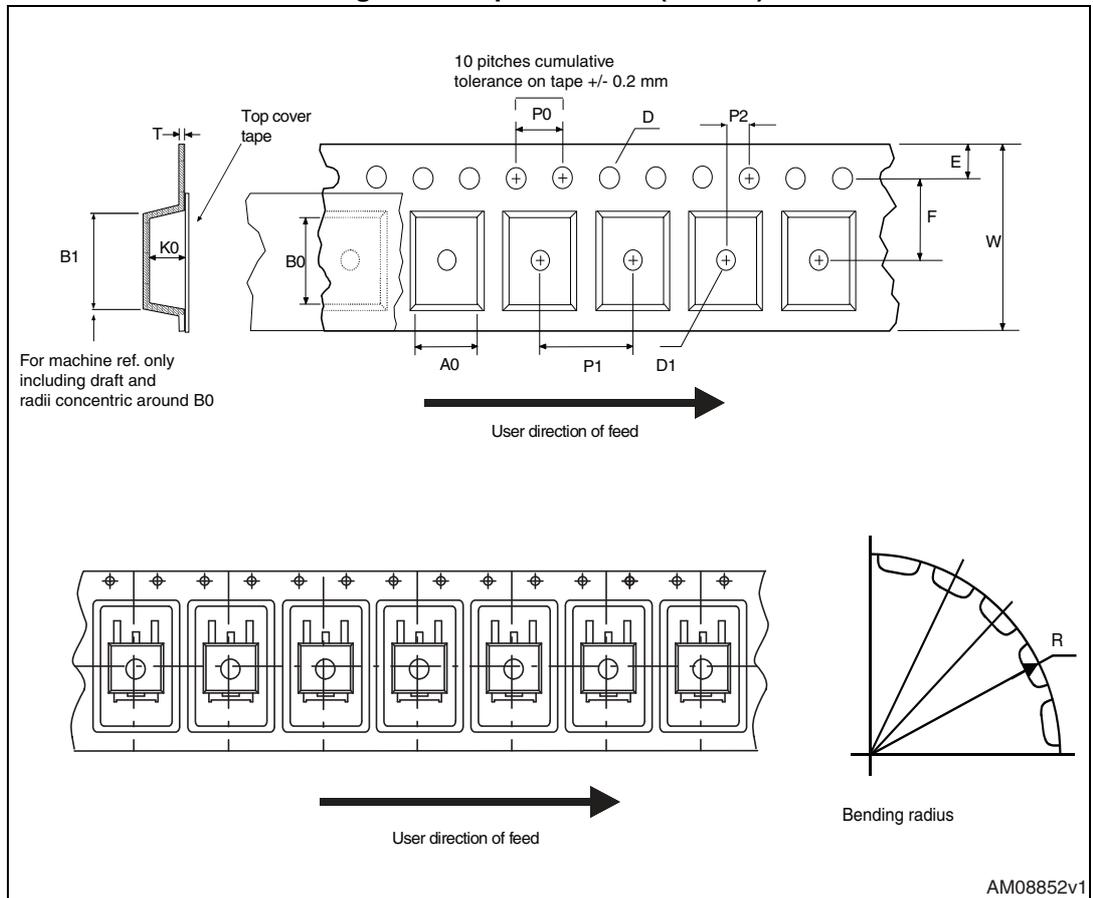
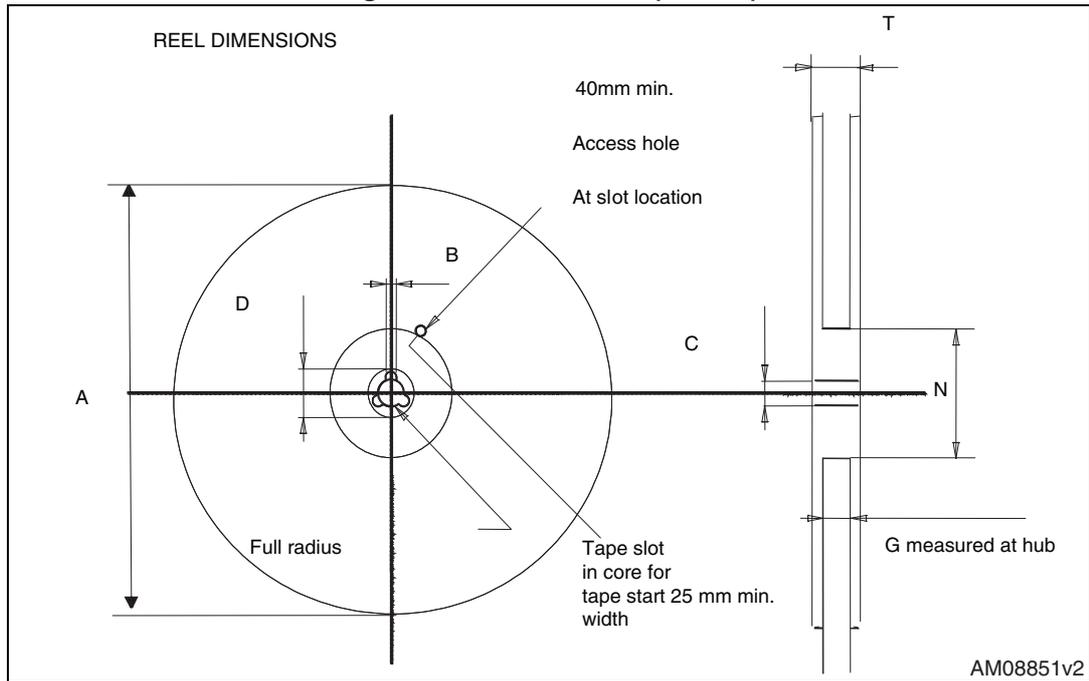


Figure 26. Reel or DPAK (TO-252)



AM08851v2

Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 6 Revision history

Table 12. Document revision history

Date	Revision	Changes
12-Feb-2014	1	First release.
17-Jun-2014	2	<ul style="list-style-type: none"><li>– Modified: title</li><li>– Modified: dv/dt values in <a href="#">Table 2</a></li><li>– Modified: values in <a href="#">Table 4</a></li><li>– Modified: <math>R_{DS(on)}</math> value in <a href="#">Table 5</a></li><li>– Modified: the entire typical values in <a href="#">Table 6, 7</a> and <a href="#">8</a></li><li>– Added: <a href="#">Section 2.1: Electrical characteristics (curves)</a></li><li>– Updated: <a href="#">Section 4: Package mechanical data</a></li><li>– Minor text changes</li></ul>

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

