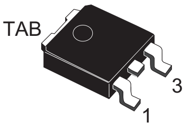
STD47N10F7AG

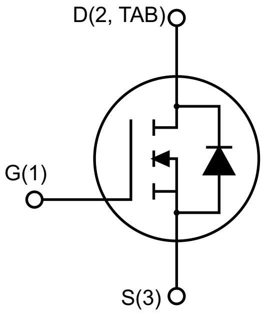
Automotive-grade N-channel 100 V, 0.0125 Ω typ., 45 A, STripFET™ F7 Power MOSFET in a DPAK package

Datasheet - production data



DPAK

Figure 1. Internal schematic diagram



AM01475v1

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD47N10F7AG	100 V	0.018Ω	22 A	60 W

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packaging
STD47N10F7AG	47N10F7	DPAK	Tape and reel

This is information on a product in full production.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	±10	V
I_D	Drain current (continuous) at T_C = 25 °C	45	A
I_D	Drain current (continuous) at T_C = 100 °C	32	A
I_{DM}(1)	Drain current (pulsed)	180	A
P_{TOT}	Total dissipation at T_c = 25 °C	60	W
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		°C

1. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.2	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 1 mA	100		-	V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 100 V			10	µA
		V_{DS} = 100 V; T_C = 125 °C			100	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 22.5 A		0.0125	0.018	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f =1 MHz, V_{GS} = 0	-	1640	-	pF
C_{oss}	Output capacitance		-	360	-	pF
C_{rss}	Reverse transfer capacitance		-	25	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 45 A V_{GS} = 10 V *Figure 14*	-	25	-	nC
Q_{gs}	Gate-source charge		-	5.1	-	nC
Q_{gd}	Gate-drain charge		-	12.2	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 22.5 A, R_G = 4.7 Ω, V_{GS} = 10 V *Figure 13*	-	15	-	ns
t_r	Rise time		-	17	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		45	A
I_{SDM}(1)	Source-drain current (pulsed)		-		180	A
V_{SD}(2)	Forward on voltage	I_{SD} = 45 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 45 A, di/dt = 100 A/µs, V_{DD} = 80 V, T_j = 150 °C	-	53		ns
Q_{rr}	Reverse recovery charge		-	67		nC
I_{RRM}	Reverse recovery current		-	2.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

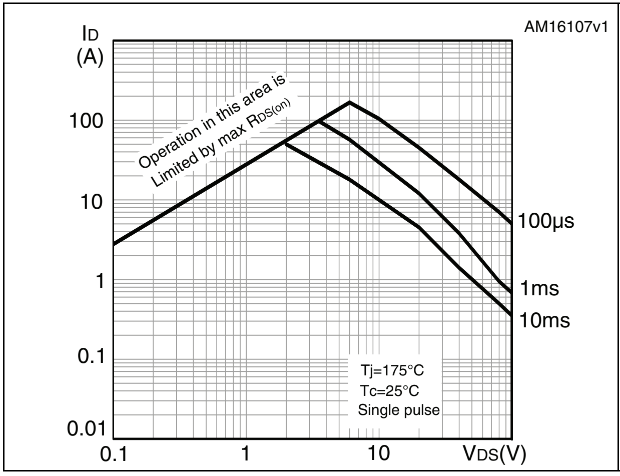


Figure 3. Thermal impedance

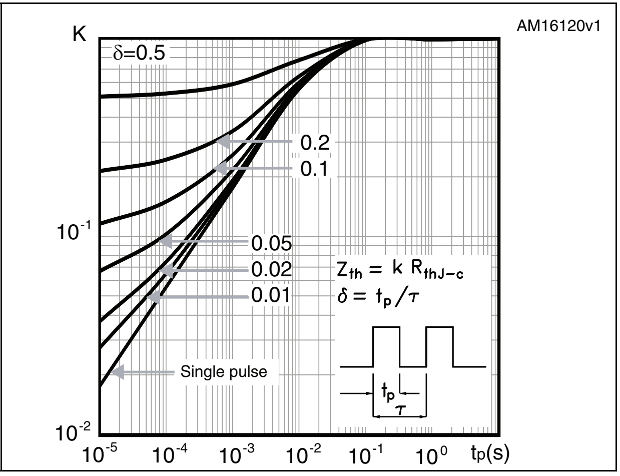


Figure 4. Output characteristics

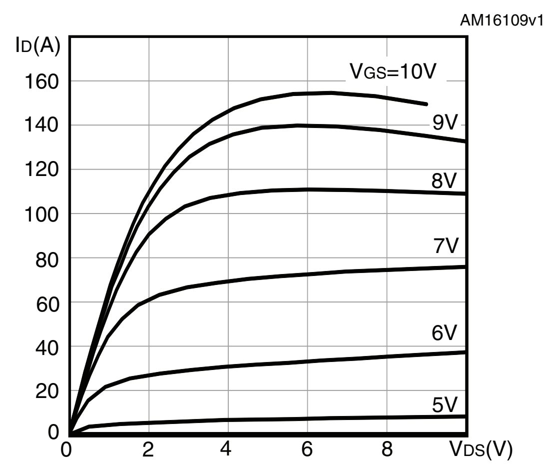


Figure 5. Transfer characteristics

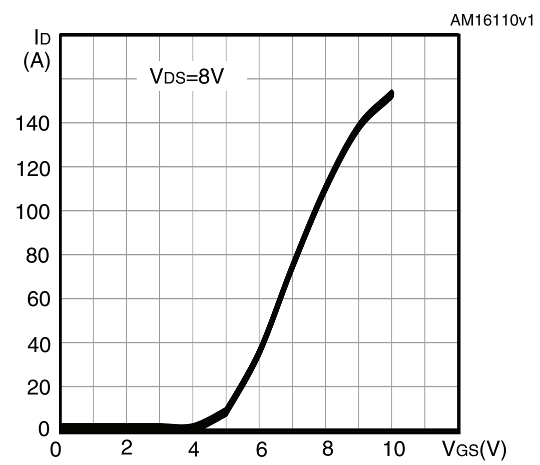


Figure 6. Gate charge vs gate-source voltage

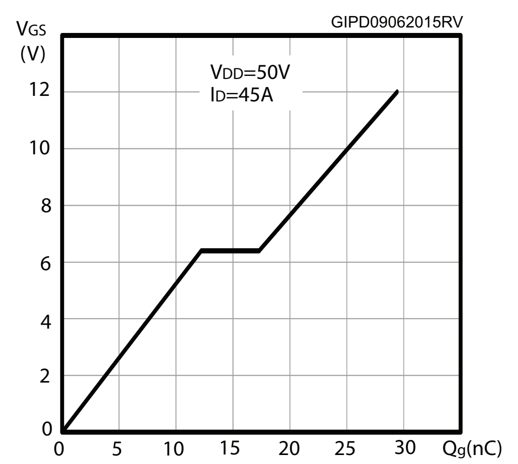


Figure 7. Static drain-source on-resistance

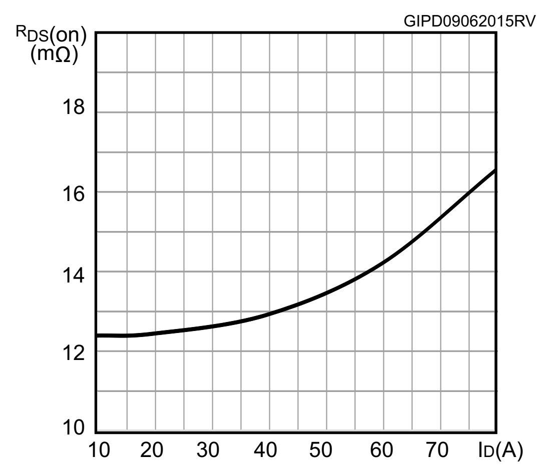


Figure 8. Capacitance variations

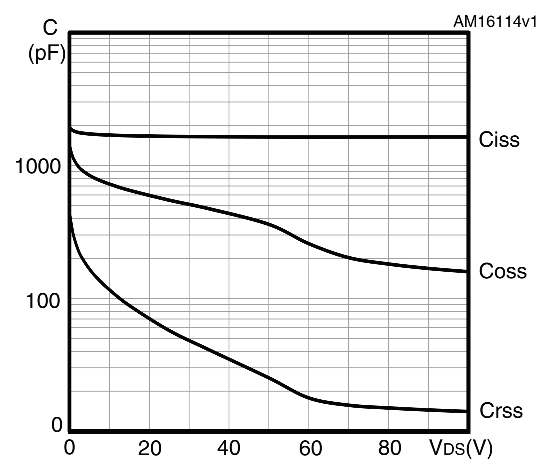


Figure 9. Normalized gate threshold voltage vs temperature

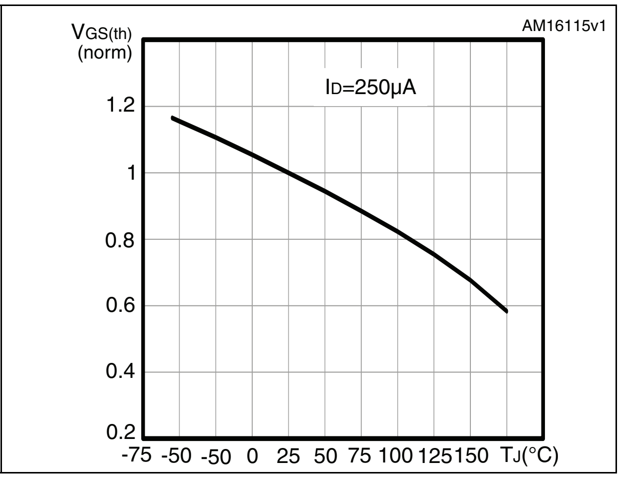


Figure 10. Normalized on-resistance vs temperature

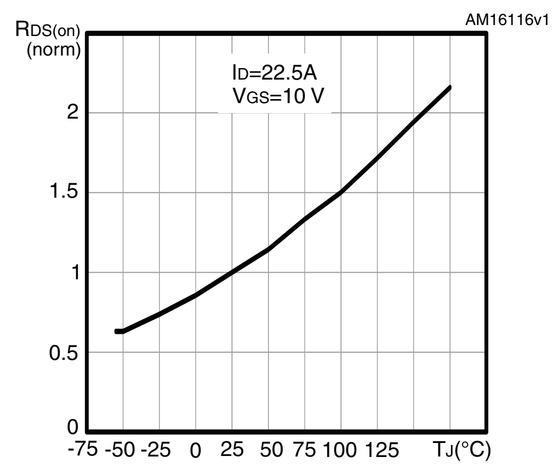


Figure 11. Source-drain diode forward characteristics

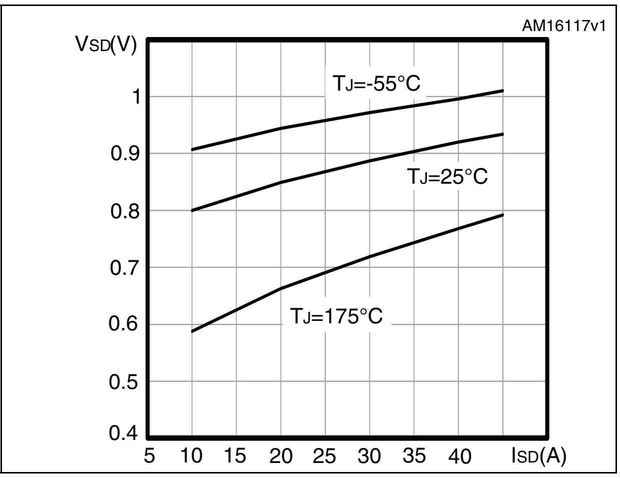
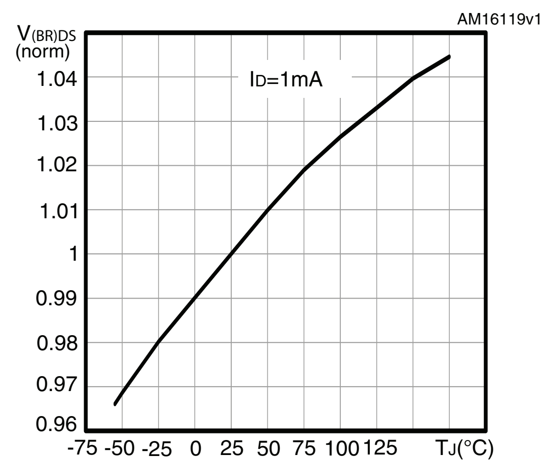


Figure 12. Normalized $V_{(BR)DS}$ vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

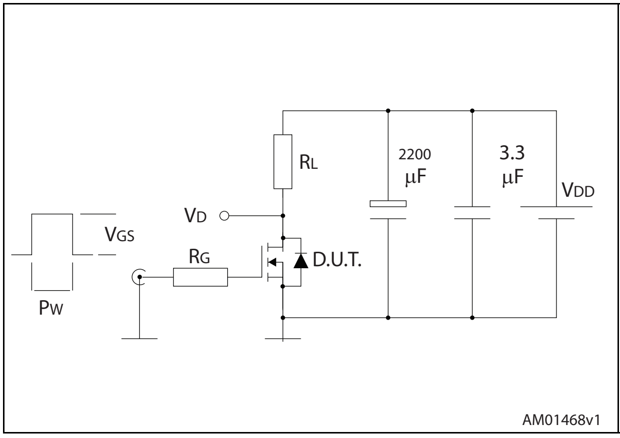


Figure 14. Gate charge test circuit

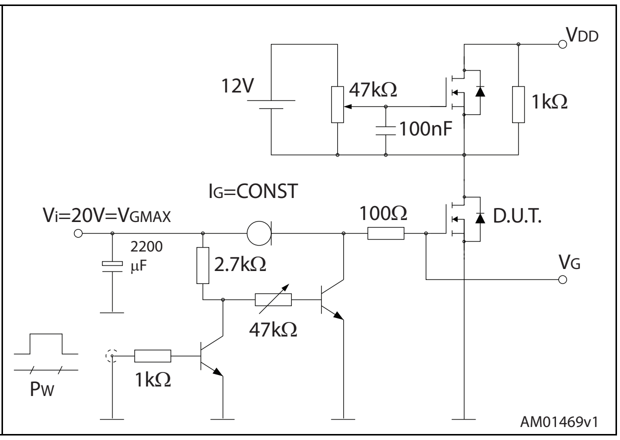


Figure 15. Test circuit for inductive load switching and diode recovery times

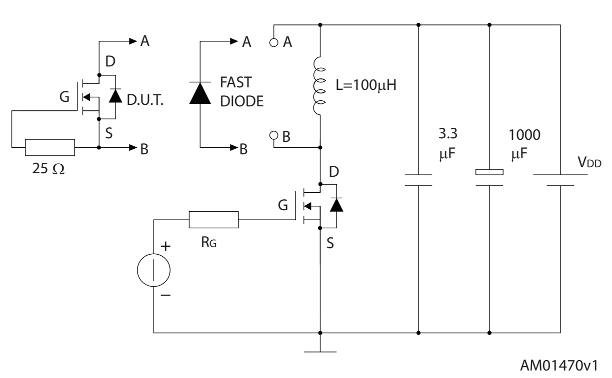


Figure 16. Unclamped inductive load test circuit

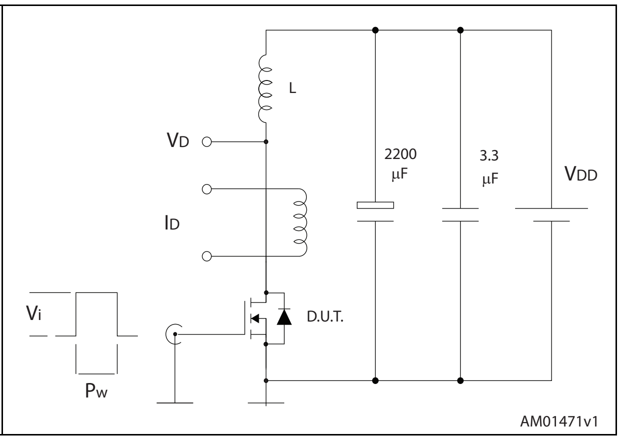


Figure 17. Unclamped inductive waveform

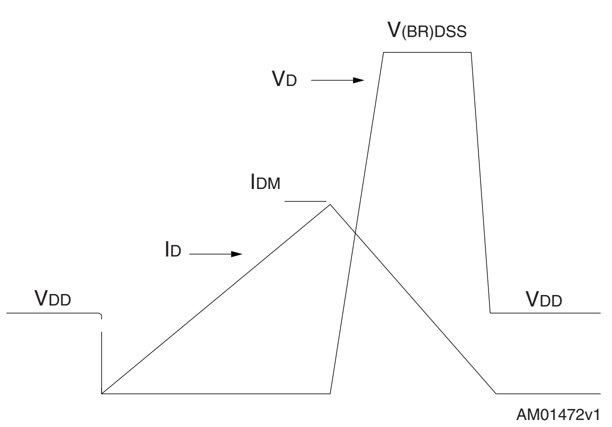
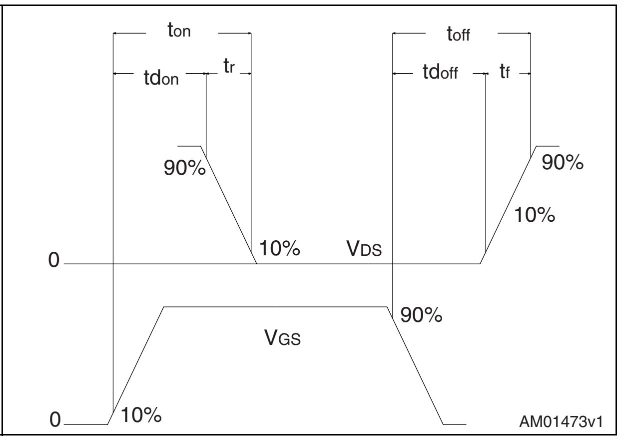


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 19. DPAK (TO-252) type A2 drawing

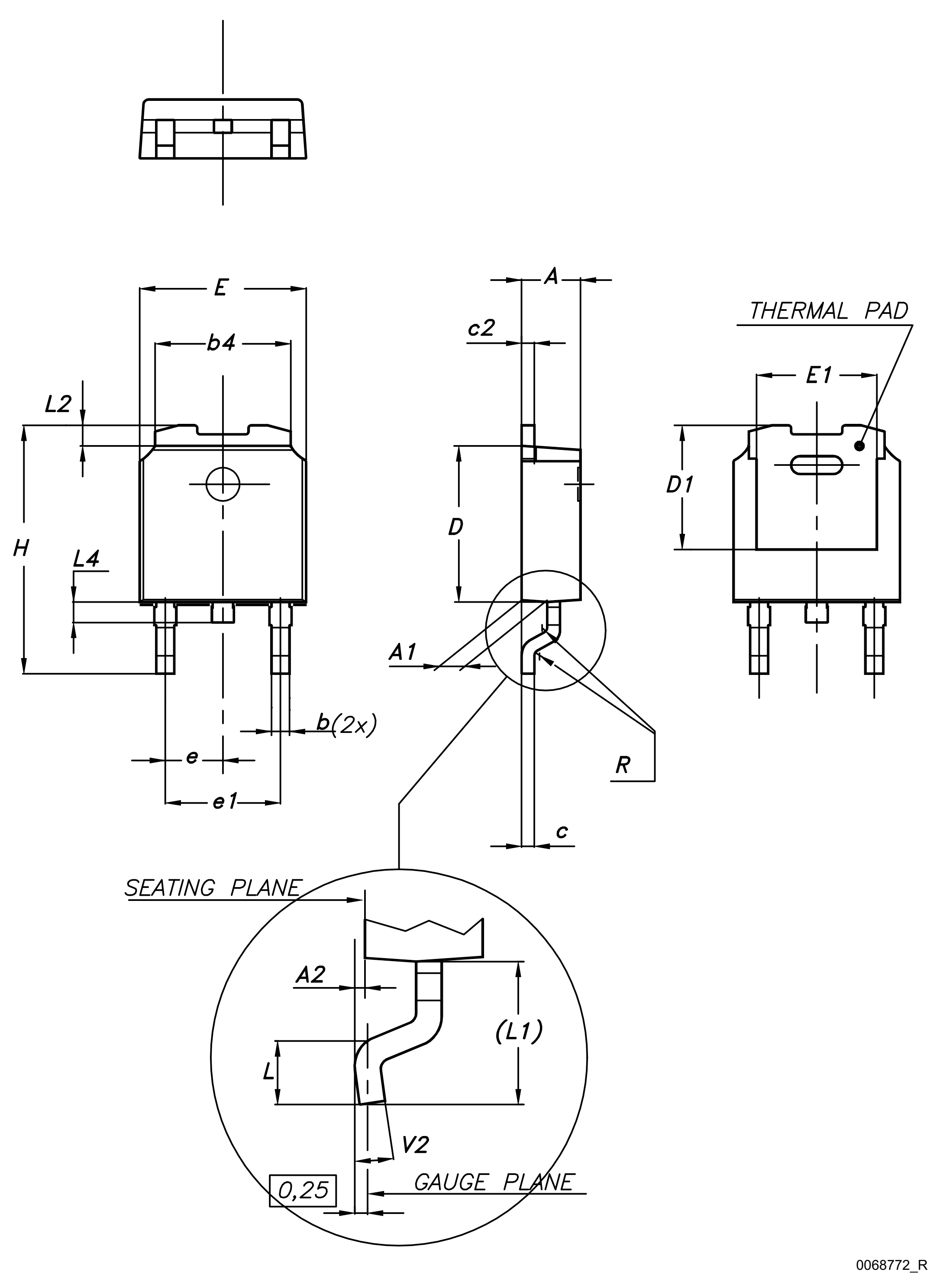
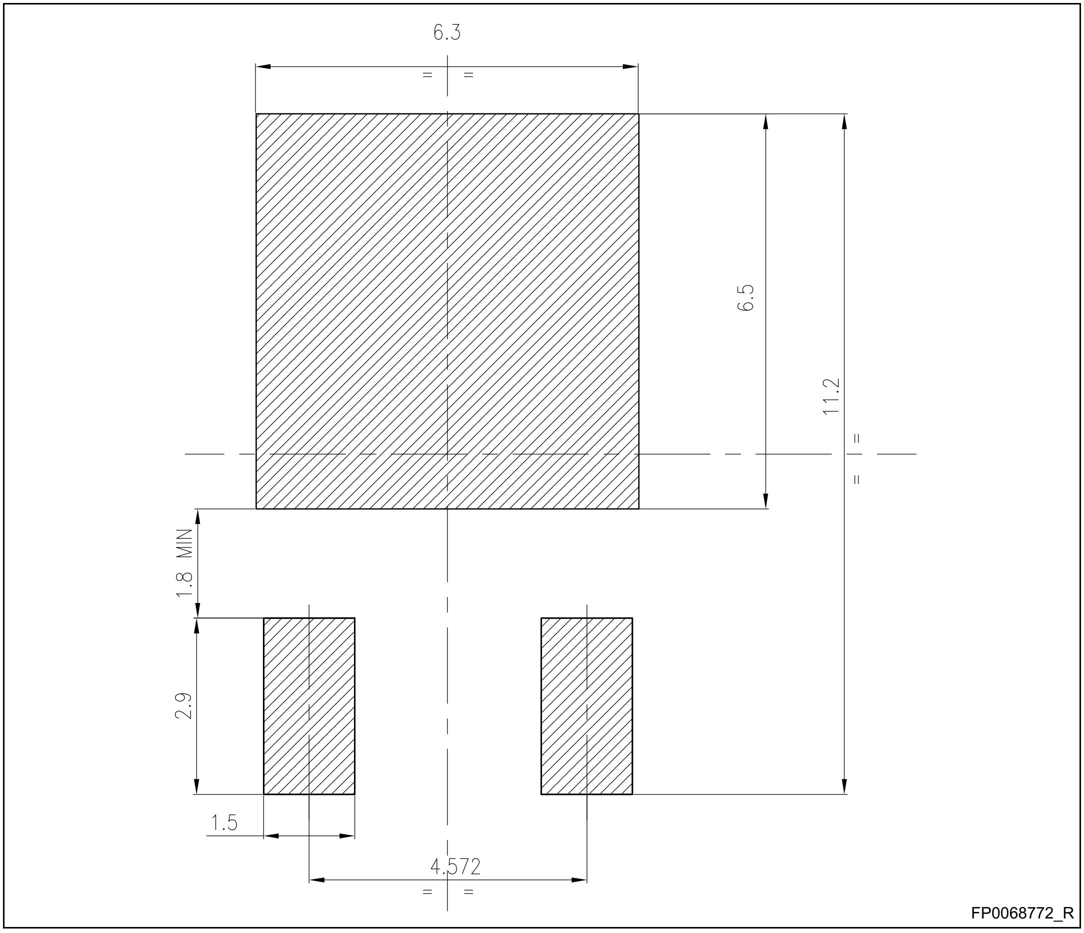


Table 8. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		5.20	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20. DPAK footprint [a]



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[a] All dimensions are in millimeters

5 Packaging mechanical data

Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	**mm**		**Dim.**	**mm**	
	Min.	**Max.**		**Min.**	**Max.**
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 21. Tape

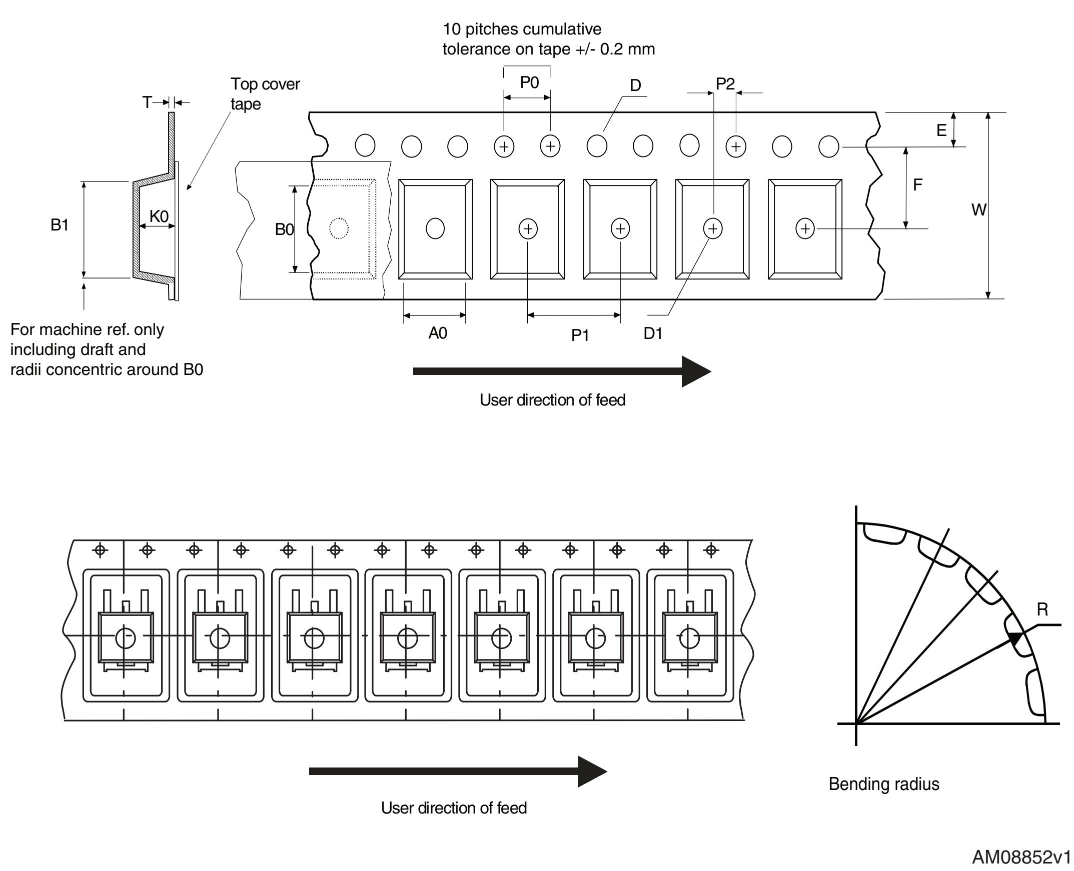
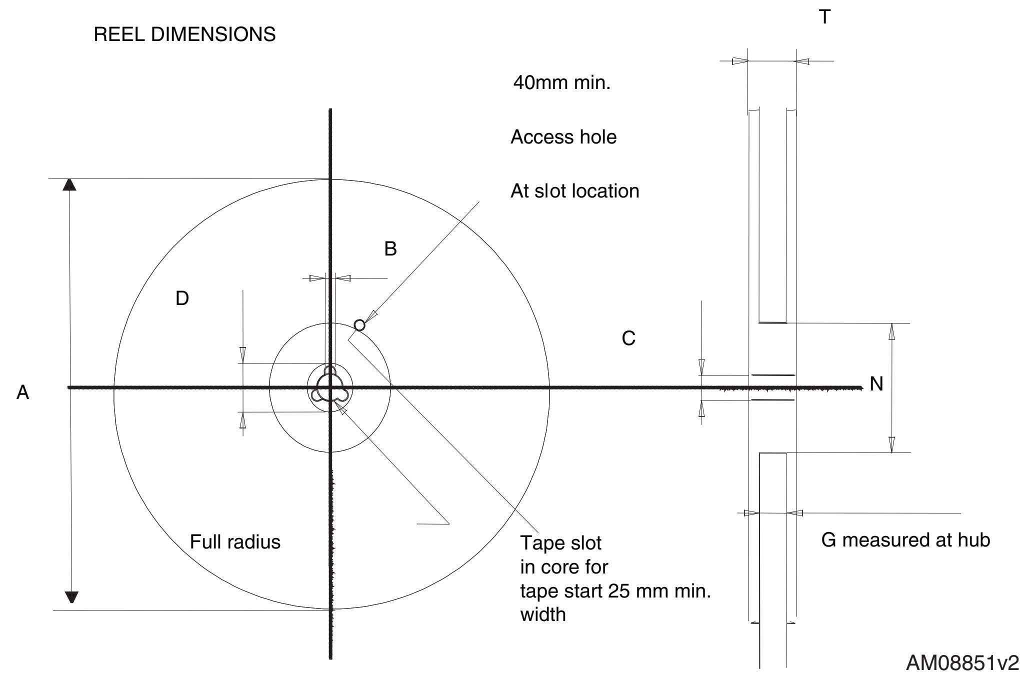


Figure 22. Reel



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
23-Feb-2015	1	First release.
17-Jun-2015	2	Updated *4: Package mechanical data* Minor text changes.