CC3100 SimpleLink™ Wi-Fi® Network Processor, Internet-of-Things Solution for MCU Applications

1 Device Overview

1.1 Features

- CC3100 SimpleLink Wi-Fi Consists of Wi-Fi Network Processor and Power-Management Subsystems
- Wi-Fi CERTIFIED™ Chip
- Wi-Fi Network Processor Subsystem
  - Featuring Wi-Fi Internet-On-a-Chip™
  - Dedicated ARM MCU

    Completely Offloads Wi-Fi and Internet Protocols from the External Microcontroller
  - Wi-Fi Driver and Multiple Internet Protocols in ROM
  - 802.11 b/g/n Radio, Baseband, and Medium Access Control (MAC), Wi-Fi Driver, and Supplicant
  - TCP/IP Stack
    - Industry-Standard BSD Socket Application Programming Interfaces (APIs)
    - 8 Simultaneous TCP or UDP Sockets
    - 2 Simultaneous TLS and SSL Sockets
  - Powerful Crypto Engine for Fast, Secure Wi-Fi and Internet Connections with 256-Bit AES Encryption for TLS and SSL Connections
  - Station, AP, and Wi-Fi Direct® Modes
  - WPA2 Personal and Enterprise Security
  - SimpleLink Connection Manager for Autonomous and Fast Wi-Fi Connections
  - SmartConfig™ Technology, AP Mode, and WPS2 for Easy and Flexible Wi-Fi Provisioning
  - TX Power
    - 18.0 dBm @ 1 DSSS
    - 14.5 dBm @ 54 OFDM
  - RX Sensitivity
    - –95.7 dBm @ 1 DSSS
    - –74.0 dBm @ 54 OFDM
  - Application Throughput
    - UDP: 16 Mbps
    - TCP: 13 Mbps
- Host Interface
  - Interfaces with 8-, 16-, and 32-Bit MCU or ASICs Over SPI or UART Interface
  - Low External Host Driver Footprint: Less Than 7KB of Code Memory and 700 B of RAM Memory Required for TCP Client Application
- Power-Management Subsystem
  - Integrated DC-DC Supports a Wide Range of Supply Voltage:
    - V_{BAT} Wide-Voltage Mode: 2.1 to 3.6 V
    - Preregulated 1.85-V Mode
  - Advanced Low-Power Modes
    - Hibernate with RTC: 4 µA
    - Low-Power Deep Sleep (LPDS): 115 µA
    - RX Traffic (MCU Active): 53 mA @ 54 OFDM
    - TX Traffic (MCU Active): 223 mA @ 54 OFDM, Maximum Power
    - Idle Connected: 690 µA @ DTIM = 1
- Clock Source
  - 40.0-MHz Crystal with Internal Oscillator
  - 32.768-kHz Crystal or External RTC Clock
- Package and Operating Temperature
  - 0.5-mm Pitch, 64-Pin, 9-mm × 9-mm QFN
  - Ambient Temperature Range: –40°C to 85°C

1.2 Applications

- For Internet-of-Things applications, such as:
  - Cloud Connectivity
  - Home Automation
  - Home Appliances
  - Access Control
  - Security Systems
  - Smart Energy
  - Internet Gateway
  - Industrial Control
  - Smart Plug and Metering
  - Wireless Audio
  - IP Network Sensor Nodes

1.3 Description

Connect any low-cost, low-power microcontroller (MCU) to the Internet of Things (IoT). The CC3100 device is the industry's first Wi-Fi CERTIFIED chip used in the wireless networking solution. The CC3100 device is part of the new SimpleLink Wi-Fi family that dramatically simplifies the implementation of Internet connectivity. The CC3100 device integrates all protocols for Wi-Fi and Internet, which greatly minimizes host MCU software requirements. With built-in security protocols, the CC3100 solution provides a robust and simple security experience. Additionally, the CC3100 device is a complete platform solution including various tools and software, sample applications, user and programming guides, reference designs and the TI E2E™ support community. The CC3100 device is available in an easy-to-layout QFN package.

The Wi-Fi network processor subsystem features a Wi-Fi Internet-on-a-Chip and contains an additional dedicated ARM MCU that completely offloads the host MCU. This subsystem includes an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for fast, secure Internet connections with 256-bit encryption. The CC3100 device supports Station, Access Point, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security and WPS 2.0. This subsystem includes embedded TCP/IP and TLS/SSL stacks, HTTP server, and multiple Internet protocols.

The power-management subsystem includes integrated DC-DC converters supporting a wide range of supply voltages. This subsystem enables low-power consumption modes, such as the hibernate with RTC mode requiringabout 4 µA of current.

The CC3100 device can connect to any 8, 16, or 32-bit MCU over the SPI or UART Interface. The device driver minimizes the host memory footprint requirements requiring less than 7KB of code memory and 700 B of RAM memory for a TCP client application.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
CC3100R11MRGCR/T	QFN (64)	9.0 mm x 9.0 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

1.4 Functional Block Diagram

Figure 1-1 shows the CC3100 hardware overview.

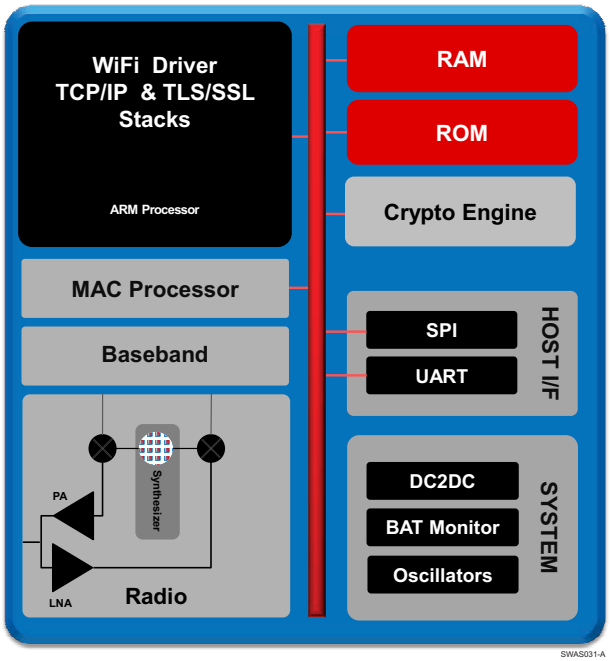

Figure 1-1. CC3100 Hardware Overview

Figure 1-2 shows an overview of the CC3100 embedded software.

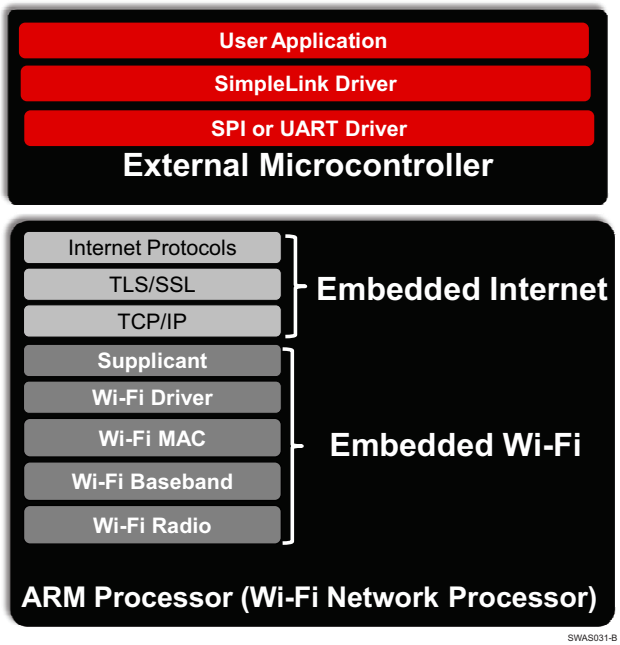

Figure 1-2. CC3100 Software Overview

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2014) to Revision D	Page
• Added Wi-Fi CERTIFIED	1
• Changed TCP value from 12 Mbps in Section 1.1, *Features*	1
• Changed part number in Device Information table from CC3100	2
• Changed pin 19 from NC and pin 18 from reserved in Figure 3-1	5
• Changed pin 19 from NC in Table 3-1	6
• Added to pin 2 (nHIB) description in Table 3-1	6
• Changed pins 8 and 14 to active low	6
• Changed pin 15 to active high	6
• Added note in Section 4.4, *Recommended Operating Conditions*, on avoiding the PA auto-protect feature	8
• Added Section 4.5, *Brown-Out and Black-Out*	9
• Added Table 4-1	9
• Added VIL (nRESET pin) and corresponding note in Section 4.6, *Electrical Characteristics (3.3 V, 25°C)*	10
• Added note on RX current measurement in Section 4.9 *Current Consumption*.	11
• Changed T_{hib_min} description from "minimum pulse width of nHIB = 0" in Table 4-4	16
• Added footnote in Table 4-4 to ensure that the nHIB pulse width is kept above the minimum requirement.	16
• Changed frequency accuracy from ±20 ppm in Table 4-5	18
• Added 4.11.3.6, *WLAN Filter Requirements*	19
• Added note on asserting nCS (active low signal) in Table 4-10	20
• Changed HOST_SPI_CS to HOST_SPI_nCS in Table 4-13	23
• Changed H_IRQ to HOST_INTR(IRQ) in Figure 4-17	24
• Changed TCP of item 17 from 12 Mbps in Table 5-1	28
• Changed part number of item 13 from XCC3100RTD in Table 6-1	32
• Added note following Table 6-1	32
• Changed part number of item 13 from XCC3100RTD in Table 6-2	34
• Added note following Table 6-2	34

3 Terminal Configuration and Functions

Figure 3-1 shows pin assignments for the 64-pin QFN package.

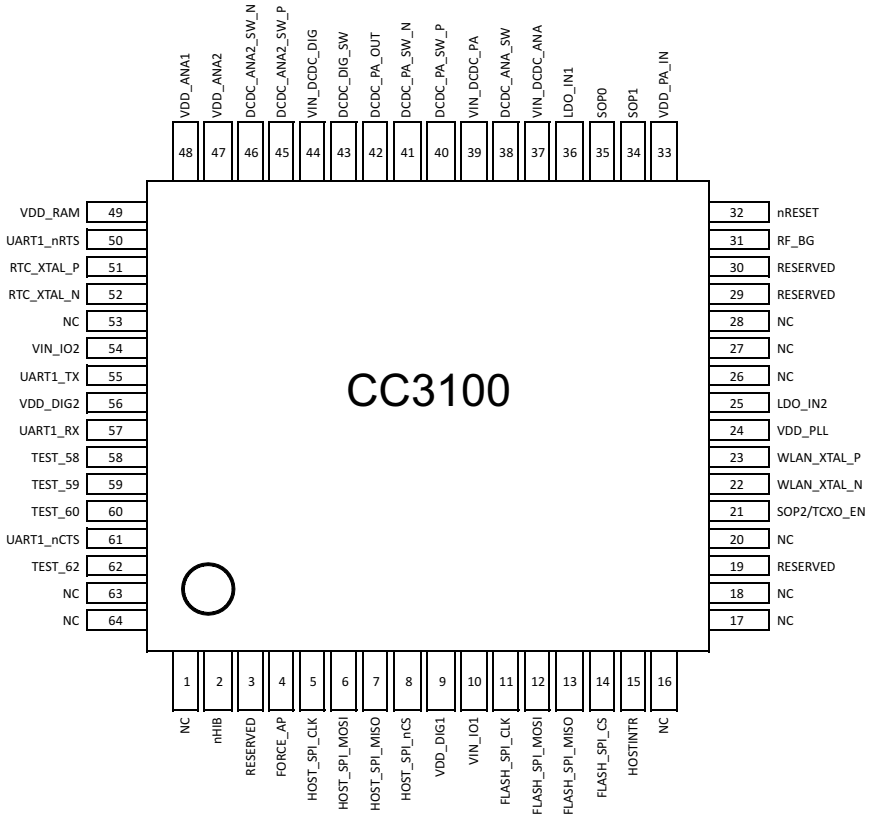


Figure 3-1. QFN 64-Pin Assignments (Top View)

3.1 Pin Attributes

Table 3-1 describes the CC3100 pins.

NOTE

If an external device drives a positive voltage to signal pads when the CC3100 device is not powered, DC current is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3100 device can occur. To prevent current draw, TI recommends one of the following:

- All devices interfaced to the CC3100 device must be powered from the same power rail as the CC3100 device.
- Use level-shifters between the CC3100 device and any external devices fed from other independent rails.
- The nRESET pin of the CC3100 device must be held low until the VBAT supply to the device is driven and stable.

Table 3-1. Pin Attributes

PIN	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE	DESCRIPTION
1	NC	Hi-Z	N/A	Unused; leave unconnected.
2	nHIB	Hi-Z	I	Hibernate signal input to the NWP (active low). This is connected to the MCU GPIO. If the GPIO from the MCU can float while the MCU enters low power, consider adding a pull-up resistor on the board to avoid floating.
3	Reserved	Hi-Z	NA	Reserved for future use
4	FORCE_AP	Hi-Z	I	For forced AP mode, pull to high on the board using 100k resistor. Otherwise, pull down to ground using 100k resistor.(1)
5	HOST_SPI_CLK	Hi-Z	I	Host interface SPI clock
6	HOST_SPI_MOSI	Hi-Z	I	Host interface SPI data input
7	HOST_SPI_MISO	Hi-Z	O	Host interface SPI data output
8	HOST_SPI_nCS	Hi-Z	I	Host interface SPI chip select (active low)
9	VDD_DIG1	Hi-Z	Power	Digital core supply (1.2 V)
10	VIN_IO1	Hi-Z	Power	I/O supply
11	FLASH_SPI_CLK	Hi-Z	O	Serial flash interface: SPI clock
12	FLASH_SPI_MOSI	Hi-Z	O	Serial flash interface: SPI data out
13	FLASH _SPI_MISO (active high)	Hi-Z	I	Serial flash interface: SPI data in
14	FLASH _SPI_nCS	Hi-Z	O	Serial flash interface: SPI chip select (active low)
15	HOST_INTR	Hi-Z	O	Interrupt output (active high)
16	NC	Hi-Z	N/A	Unused; leave unconnected.
17	NC	Hi-Z	N/A	Unused; leave unconnected.
18	NC	Hi-Z	N/A	Unused; leave unconnected.
19	Reserved	Hi-Z	N/A	Connect 100K pull-down to ground.
20	NC	Hi-Z	N/A	Unused; leave unconnected.
21	SOP2/TCXO_EN	Hi-Z	O	Enable signal for external TCXO. Add 10k pulldown to ground.
22	WLAN_XTAL_N	Hi-Z	Analog	Connect the WLAN 40-MHz XTAL here.
23	WLAN_XTAL_P	Hi-Z	Analog	Connect the WLAN 40-MHz XTAL here.
24	VDD_PLL	Hi-Z	Power	Internal PLL power supply (1.4 V nominal)
25	LDO_IN2	Hi-Z	Power	Input to internal LDO
26	NC	Hi-Z	N/A	Unused; leave unconnected.
27	NC	Hi-Z	N/A	Unused; leave unconnected.
28	NC	Hi-Z	N/A	Unused; leave unconnected.
29	Reserved	Hi-Z	O	Reserved for future use
30	Reserved	Hi-Z	O	Reserved for future use
31	RF_BG	Hi-Z	RF	2.4-GHz RF TX/RX
32	nRESET	Hi-Z	I	RESET input for the device. Active low input. Use RC circuit (100k || 0.1 µF) for power on reset.
33	VDD_PA_IN	Hi-Z	Power	Power supply for the RF power amplifier (PA)
34	SOP1	Hi-Z	N/A	Add 100K pulldown to ground.
35	SOP0	Hi-Z	N/A	Add 100K pulldown to ground.
36	LDO_IN1	Hi-Z	Power	Input to internal LDO
37	VIN_DCDC_ANA	Hi-Z	Power	Power supply for the DC-DC converter for analog section

(1) Using a configuration file stored on flash, the vendor can optionally block any possibility of bringing up AP using the FORCE_AP pin.

Table 3-1. Pin Attributes (continued)

PIN	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE	DESCRIPTION
38	DCDC_ANA_SW	Hi-Z	Power	Analog DC-DC converter switch output
39	VIN_DCDC_PA	Hi-Z	Power	PA DC-DC converter input supply
40	DCDC_PA_SW_P	Hi-Z	Power	PA DC-DC converter switch output +ve
41	DCDC_PA_SW_N	Hi-Z	Power	PA DC-DC converter switch output –ve
42	DCDC_PA_OUT	Hi-Z	Power	PA DC-DC converter output. Connect the output capacitor for DC-DC here.
43	DCDC_DIG_SW	Hi-Z	Power	Digital DC-DC converter switch output
44	VIN_DCDC_DIG	Hi-Z	Power	Power supply input for the digital DC-DC converter
45	DCDC_ANA2_SW_P	Hi-Z	Power	Analog2 DC-DC converter switch output +ve
46	DCDC_ANA2_SW_N	Hi-Z	Power	Analog2 DC-DC converter switch output –ve
47	VDD_ANA2	Hi-Z	Power	Analog2 power supply input
48	VDD_ANA1	Hi-Z	Power	Analog1 power supply input
49	VDD_RAM	Hi-Z	Power	Power supply for the internal RAM
50	UART1_nRTS	Hi-Z	O	UART host interface
51	RTC_XTAL_P	Hi-Z	Analog	32.768 kHz XTAL_P/external CMOS level clock input
52	RTC_XTAL_N	Hi-Z	Analog	32.768 kHz XTAL_N/100k external pullup for external clock
53	NC	Hi-Z	N/A	Unused. Leave unconnected.
54	VIN_IO2	Hi-Z	Power	I/O power supply. Same as battery voltage.
55	UART1_TX	Hi-Z	O	UART host interface. Connect to test point on prototype for flash programming.
56	VDD_DIG2	Hi-Z	Power	Digital power supply (1.2 V)
57	UART1_RX	Hi-Z	I	UART host interface. Connect to test point on prototype for flash programming.
58	TEST_58		N/A	Test signal. Connect to an external test point.
59	TEST_59		N/A	Test signal. Connect to an external test point.
60	TEST_60	Hi-Z	O	Test signal. Connect to an external test point.
61	UART1_nCTS	Hi-Z	I	UART host interface
62	TEST_62	Hi-Z	O	Test signal. Connect to an external test point.
63	NC	Hi-Z	I/O	Leave unconnected
64	NC	Hi-Z	I/O	Leave unconnected
65	GND		Power	Ground tab used as thermal and electrical ground

4 Specifications

All measurements are referenced at the device pins, unless otherwise indicated. All specifications are over process and voltage, unless otherwise indicated.

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETERS	PINS	MIN	MAX	UNIT
V_{BAT} and V_{IO}	37, 39, 44	–0.5	3.8	V
V_{IO}-V_{BAT} (differential)	10, 54		0.0	V
Digital inputs		–0.5	V_{IO} + 0.5	V
RF pins		–0.5	2.1	V
Analog pins (XTAL)		–0.5	2.1	V
Operating temperature range (T_A)		–40	+85	°C

4.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	+125	°C
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	+2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	+500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Power-On Hours

CONDITIONS	POH
$T_{Ambient}$ up to 85°C, assuming 20% active mode and 80% sleep mode	17,500(1)

(1) The CC3100 device can be operated reliably for 10 years.

4.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)(2)

PARAMETERS	PINS	CONDITIONS(3) (4)	MIN	TYP	MAX	UNIT
V_{BAT}, V_{IO} (shorted to V_{BAT})	10, 37, 39, 44, 54	Direct battery connection	2.1	3.3	3.6	V
V_{BAT}, V_{IO} (shorted to V_{BAT})	10, 37, 39, 44, 54	Preregulated 1.85 V	1.76	1.85	1.9	V
Ambient thermal slew			–20		20	°C/minute

(1) Operating temperature is limited by crystal frequency variation.
(2) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.

(3) To ensure WLAN performance, ripple on the 2.1- to 3.3-V supply must be less than ±300 mV.
(4) To ensure WLAN performance, ripple on the 1.85-V supply must be less than 2% (±40 mV).

4.5 Brown-Out and Black-Out

The device enters a brown-out condition whenever the input voltage dips below V_{BROWN} (see Figure 4-1 and Figure 4-2). This condition must be considered during design of the power supply routing, especially if operating from a battery. High-current operations (such as a TX packet) cause a dip in the supply voltage, potentially triggering a brown-out. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (4 contacts for a 2 x AA battery) and the wiring and PCB routing resistance.

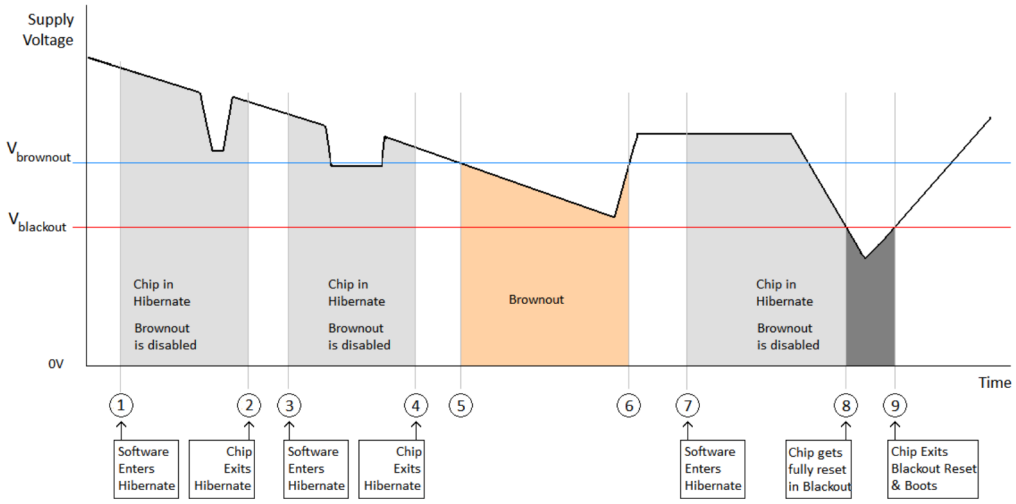


Figure 4-1. Brown-Out and Black-Out Levels (1 of 2)

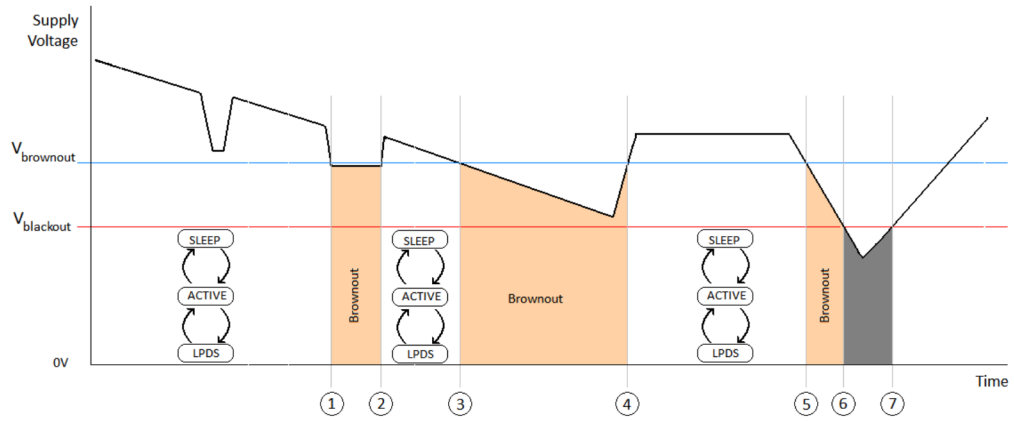


Figure 4-2. Brown-Out and Black-Out Levels (2 of 2)

In the brown-out condition, all sections of the device shut down except for the Hibernate module (including the 32-kHz RTC clock), which remains on. The current in this state can reach approximately 400 µA.

The black-out condition is equivalent to a hardware reset event in which all states within the device are lost. Table 4-1 lists the brown-out and black-out voltage levels.

Table 4-1. Brown-Out and Black-out Voltage Levels

CONDITION	VOLTAGE LEVEL	UNIT
$V_{brownout}$	2.1	V
$V_{blackout}$	1.67	V

4.6 Electrical Characteristics (3.3 V, 25°C)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{IN}	Pin capacitance			4		pF
V_{IH}	High-level input voltage		0.65 × VDD		VDD + 0.5 V	V
V_{IL}	Low-level input voltage		–0.5		0.35 × VDD	V
I_{IH}	High-level input current			5		nA
I_{IL}	Low-level input current			5		nA
V_{OH}	High-level output voltage (VDD = 3.0 V)		2.4			V
V_{OL}	Low-level output voltage (VDD = 3.0 V)				0.4	V
I_{OH}	High-level source current, VOH = 2.4		6			mA
I_{OL}	Low-level sink current, VOH = 0.4		6			mA
Pin Internal Pullup and Pulldown (25°C)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**NOM**	**MAX**	**UNIT**
I_{OH}	Pull-Up current, V_{OH} = 2.4 (VDD = 3.0 V)		5		10	µA
I_{OL}	Pull-Down current, V_{OL} = 0.4 (VDD = 3.0 V)		5			µA
V_{IL}	nRESET(1)			0.6		V

(1) The nRESET pin must be held below 0.6 V for the device to register a reset.

4.7 WLAN Receiver Characteristics

T_A = +25°C, V_{BAT} = 2.1 to 3.6 V. Parameters measured at SoC pin on channel 7 (2442 MHz)

Parameter	Condition (Mbps)	Min	Typ	Max	Units
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)(10% PER)(1)	1 DSSS		–95.7		dBm
	2 DSSS		–93.6		
	11 CCK		–88.0		
	6 OFDM		–90.0		
	9 OFDM		–89.0		
	18 OFDM		–86.0		
	36 OFDM		–80.5		
	54 OFDM		–74.0		
	MCS0 (GF)(2)		–89.0		
	MCS7 (GF)(2)		–71.0		
Maximum input level (10% PER)	802.11b		–4.0		
	802.11g		–10.0		

(1) Sensitivity is 1-dB worse on channel 13 (2472 MHz).
(2) Sensitivity for mixed mode is 1-dB worse.

4.8 WLAN Transmitter Characteristics

T_A = +25°C, V_{BAT} = 2.1 to 3.6 V. Parameters measured at SoC pin on channel 7 (2442 MHz).(1)

Parameter	Condition(2)	Min	Typ	Max	Units
Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM	1 DSSS		18.0		dBm
	2 DSSS		18.0		
	11 CCK		18.3		
	6 OFDM		17.3		
	9 OFDM		17.3		
	18 OFDM		17.0		
	36 OFDM		16.0		
	54 OFDM		14.5		
	MCS7 (MM)		13.0		
Transmit center frequency accuracy		–25		25	ppm

(1) Channel-to-channel variation is up to 2 dB. The edge channels (2412 and 2472 MHz) have reduced TX power to meet FCC emission limits.
(2) In preregulated 1.85-V mode, maximum TX power is 0.25 to 0.75 dB lower for modulations higher than 18 OFDM.

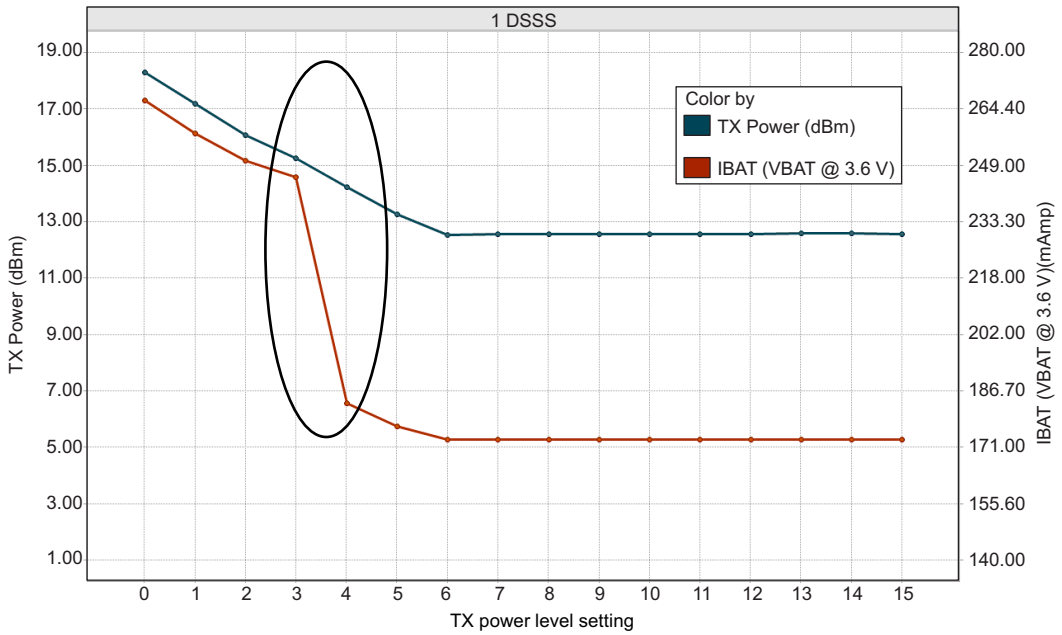
4.9 Current Consumption

T_A = +25°C, V_{BAT} = 3.6 V

PARAMETER	TEST CONDITIONS(1) (2)		MIN	TYP(3)	MAX	UNIT
TX	1 DSSS	TX power level = 0		272		mA
		TX power level = 4		188		
	6 OFDM	TX power level = 0		248		
		TX power level = 4		179		
	54 OFDM	TX power level = 0		223		
		TX power level = 4		160		
RX(4)	1 DSSS			53		
	54 OFDM			53		
Idle connected(5)				0.690		
LPDS				0.115		
Hibernate(6)				4		µA
Peak calibration current (7)(4)	V_{BAT} = 3.3 V			450		mA
	V_{BAT} = 2.1 V			670		
	V_{BAT} = 1.85 V			700		

(1) TX power level = 0 implies maximum power (see Figure 4-3 through Figure 4-5). TX power level = 4 implies output power backed off approximately 4 dB.
(2) The CC3100 system is a constant power-source system. The active current numbers scale based on the V_{BAT} voltage supplied.
(3) External serial-flash-current consumption is not included.
(4) The RX current is measured with a 1-Mbps throughput rate.

(5) DTIM = 1
(6) For the 1.85-V mode, the Hibernate current is higher by 50 µA across all operating modes because of leakage into the PA and analog power inputs.
(7) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms . Calibration is performed sparingly, typically when coming out of Hibernate and only if temperature has changed by more than 20°C or the time elapsed from prior calibration is greater than 24 hours.



Note: The area enclosed in the circle represents a significant reduction in current when transitioning from TX power level 3 to 4. In the case of lower range requirements (14 dbm output power), TI recommends using TX power level 4 to reduce the current.

Figure 4-3. TX Power and IBAT vs TX Power Level Settings (1 DSSS)

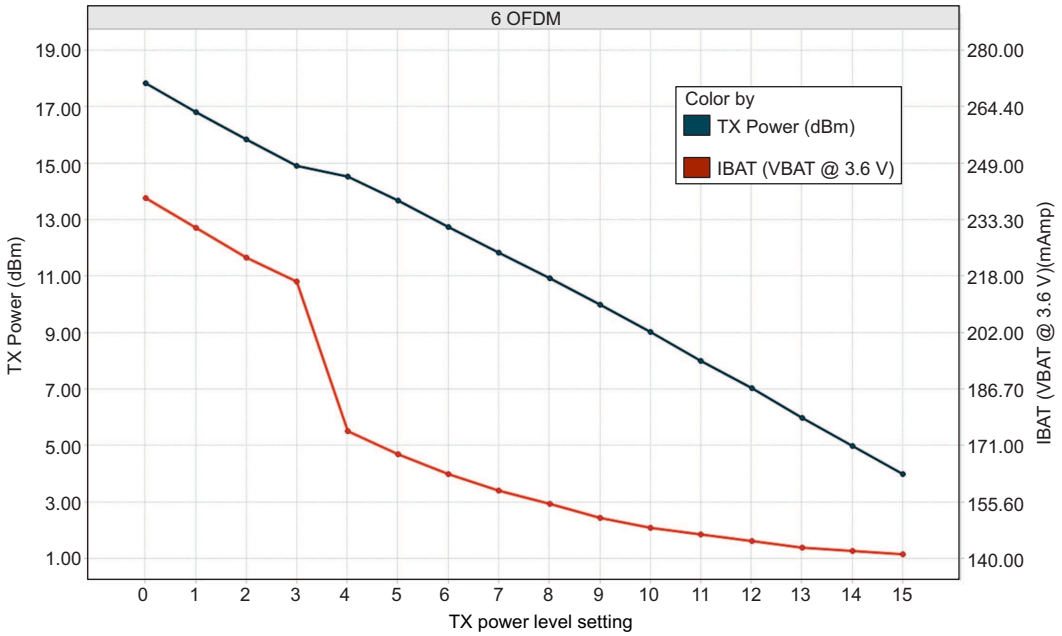


Figure 4-4. TX Power and IBAT vs TX Power Level Settings (6 OFDM)

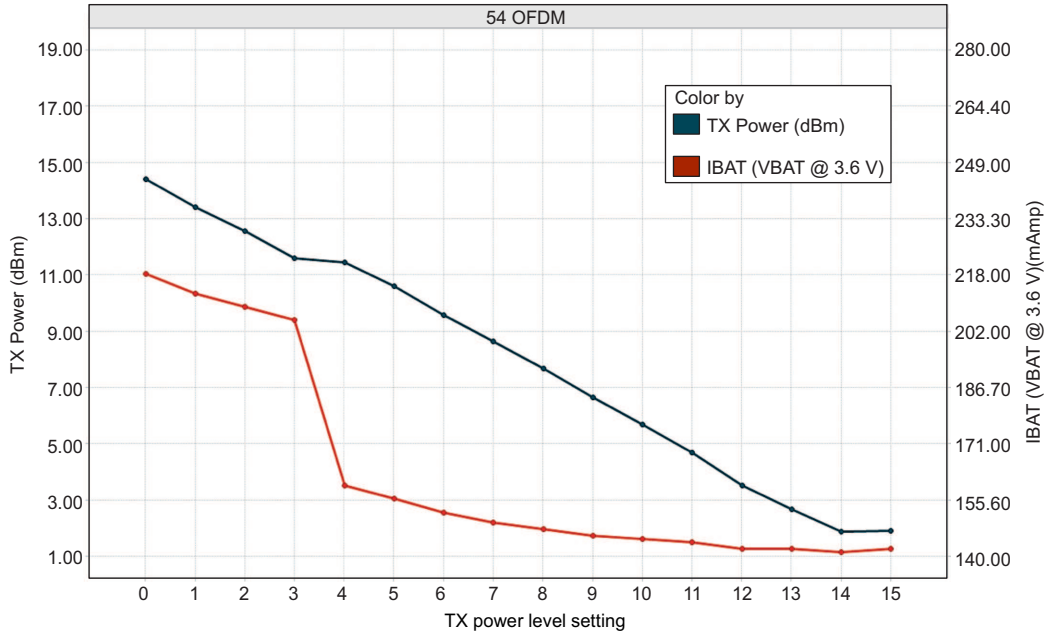


Figure 4-5. TX Power and IBAT vs TX Power Level Settings (54 OFDM)

4.10 Thermal Characteristics for RGC Package

AIR FLOW				
PARAMETER	**0 lfm (C/W)**	**150 lfm (C/W)**	**250 lfm (C/W)**	**500 lfm (C/W)**
θ_{ja}	23	14.6	12.4	10.8
Ψ_{jt}	0.2	0.2	0.3	0.1
Ψ_{jb}	2.3	2.3	2.2	2.4
θ_{jc}	6.3			
θ_{jb}	2.4			

4.11 Timing and Switching Characteristics

4.11.1 Power Supply Sequencing

For proper operation of the CC3100 device, perform the recommended power-up sequencing as follows:

1. Tie V_{BAT} (pins 37, 39, 44) and V_{IO} (pins 54 and 10) together on the board.
2. Hold the RESET pin low while the supplies are ramping up. TI recommends using a simple RC circuit (100K || 0.1 µF, RC = 10 ms).
3. For an external RTC clock, ensure that the clock is stable before RESET is deasserted (high).

For timing diagrams, see Section 4.11.2, *Reset Timing*.

4.11.2 Reset Timing

4.11.2.1 nRESET (32K XTAL)

Figure 4-6 shows the reset timing diagram for the 32K XTAL first-time power-up and reset removal.

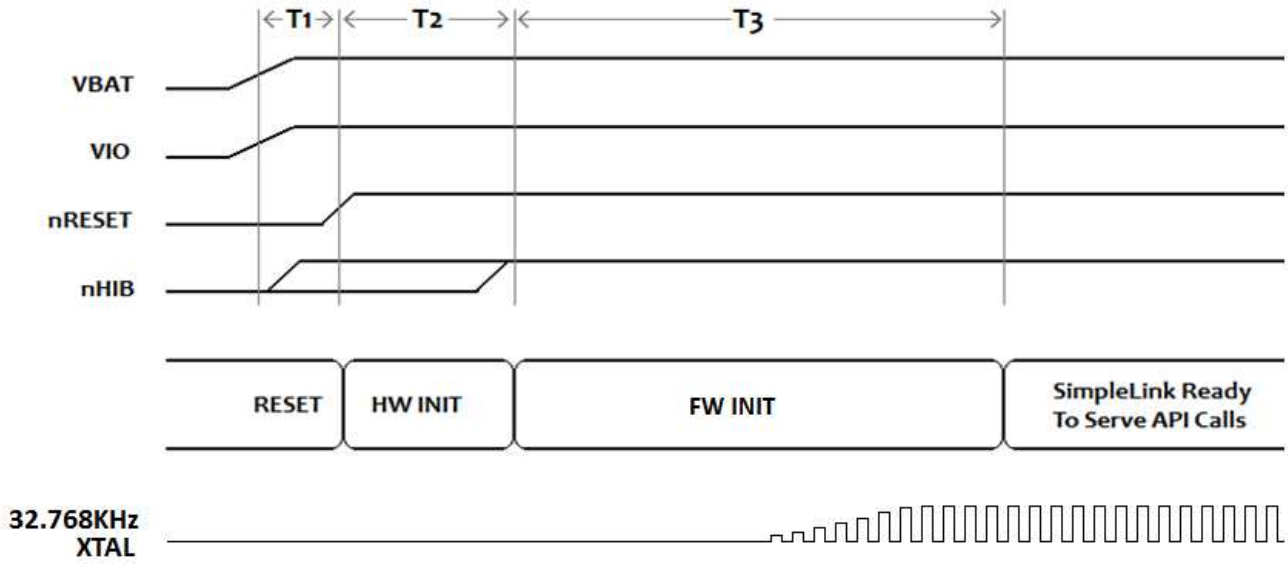


Figure 4-6. First-Time Power-Up and Reset Removal Timing Diagram (32K XTAL)

Table 4-2 describes the timing requirements for the 32K XTAL first-time power-up and reset removal.

Table 4-2. First-Time Power-Up and Reset Removal Timing Requirements (32K XTAL)

Item	Name	Description	Min	Typ	Max
T1	Supply settling time	Depends on application board power supply, decap, and so on		3 ms	
T2	Hardware wakeup time			25 ms	
T3	Initialization time	32-kHz XTAL settling + firmware initialization time + radio calibration		1.35 s	

4.11.2.2 nRESET (External 32K)

Figure 4-7 shows the reset timing diagram for the external 32K first-time power-up and reset removal.

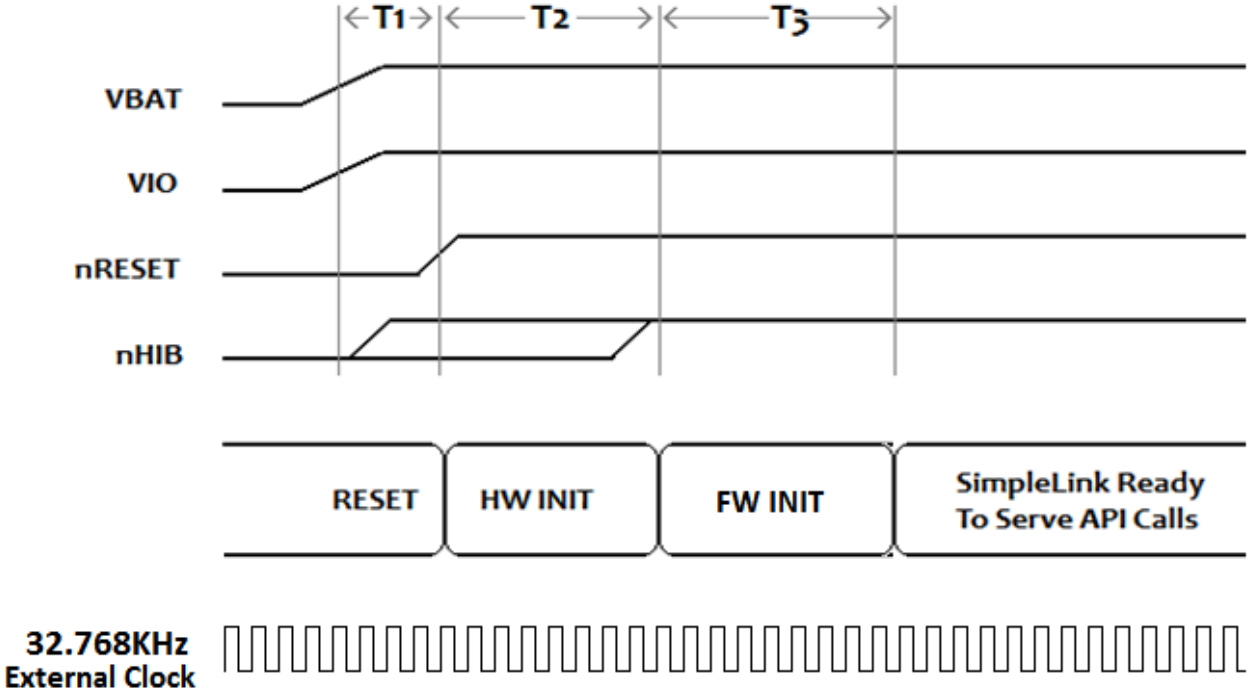


Figure 4-7. First-Time Power-Up and Reset Removal Timing Diagram (External 32K)

Table 4-3 describes the timing requirements for the external 32K first-time power-up and reset removal.

Table 4-3. First-Time Power-Up and Reset Removal Timing Requirements (External 32K)

Item	Name	Description	Min	Typ	Max
T1	Supply settling time	Depends on application board power supply, decap, and so on		3 ms	
T2	Hardware wakeup time			25 ms	
T3	Initialization time	Firmware initialization time + radio calibration		250 ms	

4.11.2.3 Wakeup from Hibernate

Figure 4-8 shows the timing diagram for wakeup from the hibernate state.

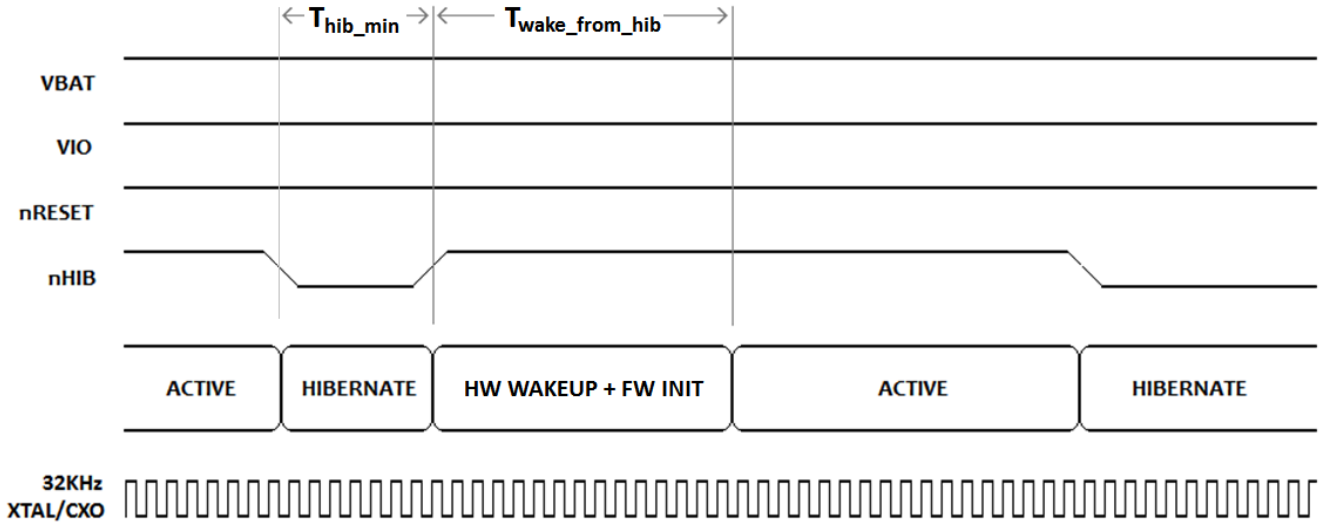


Figure 4-8. nHIB Timing Diagram

NOTE

The 32.768-kHz XTAL is kept enabled by default when the chip goes to hibernate in response to nHIB being pulled low.

Table 4-4 describes the timing requirements for nHIB.

Table 4-4. nHIB Timing Requirements

Item	Name	Description	Min	Typ	Max
T_{hib_min}	Minimum hibernate time	Minimum pulse width of nHIB being low(1)	10 ms		
$T_{wake\_from\_hib}$	Hardware wakeup time plus firmware initialization time	See (2).		50 ms	

(1) Ensure that the nHIB pulse width is kept above the minimum requirement under all conditions (such as power up, MCU reset, and so on).

(2) If temperature changes by more than 20°C, initialization time from HIB can increase by 200 ms due to radio calibration.

4.11.3 Clock Specifications

The CC3100 device requires two separate clocks for its operation:

- A slow clock running at 32.768 kHz is used for the RTC.
- A fast clock running at 40 MHz is used by the device for the internal processor and the WLAN subsystem.

The device features internal oscillators that enable the use of cheaper crystals rather than dedicated TCXOs for these clocks. The RTC can also be fed externally to provide reuse of an existing clock on the system and reduce overall cost.

4.11.3.1 Slow Clock Using Internal Oscillator

The RTC crystal connected on the device supplies the free-running slow clock. The accuracy of the slow clock frequency must be 32.768 kHz ±150 ppm. In this mode of operation, the crystal is tied between RTC_XTAL_P (pin 51) and RTC_XTAL_N (pin 52) with a suitable load capacitance.

Figure 4-9 shows the crystal connections for the slow clock.

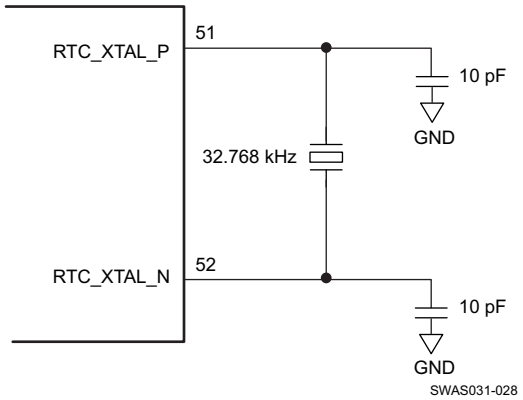


Figure 4-9. RTC Crystal Connections

4.11.3.2 Slow Clock Using an External Clock

When an RTC clock oscillator is present in the system, the CC3100 device can accept this clock directly as an input. The clock is fed on the RTC_XTAL_P line and the RTC_XTAL_N line is held to VIO. The clock must be a CMOS-level clock compatible with VIO fed to the device.

Figure 4-10 shows the external RTC clock input connection.

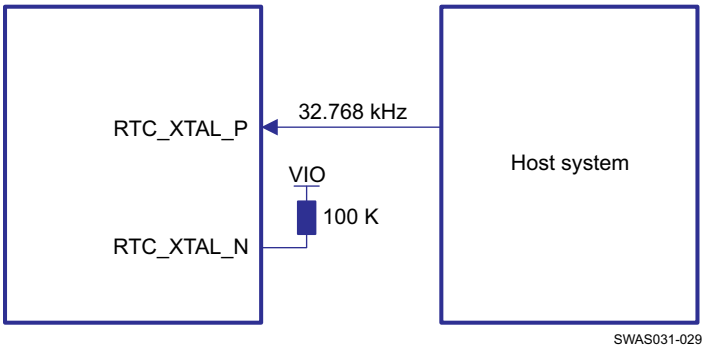


Figure 4-10. External RTC Clock Input

4.11.3.3 Fast Clock (F_{ref}) Using an External Crystal

The CC3100 device also incorporates an internal crystal oscillator to support a crystal-based fast clock. The XTAL is fed directly between WLAN_XTAL_P (pin 23) and WLAN_XTAL_N (pin 22) with suitable loading capacitors.

Figure 4-11 shows the crystal connections for the fast clock.

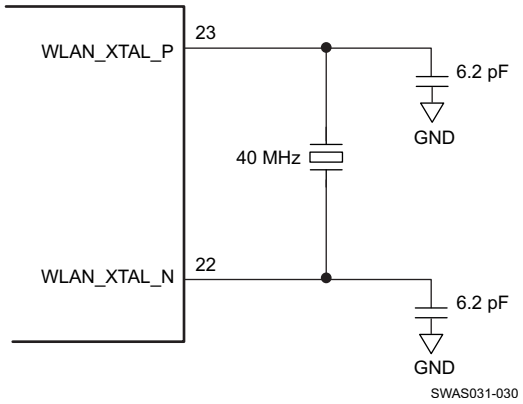


Figure 4-11. Fast Clock Crystal Connections

4.11.3.4 Fast Clock (F_{ref}) Using an External Oscillator

The CC3100 device can accept an external TCXO/XO for the 40-MHz clock. In this mode of operation, the clock is connected to WLAN_XTAL_P (pin 23). WLAN_XTAL_N (pin 22) is connected to GND. The external TCXO/XO can be enabled by TCXO_EN (pin 21) from the device to optimize the power consumption of the system.

If the TCXO does not have an enable input, an external LDO with an enable function can be used. Using the LDO improves noise on the TCXO power supply.

Figure 4-12 shows the connection.

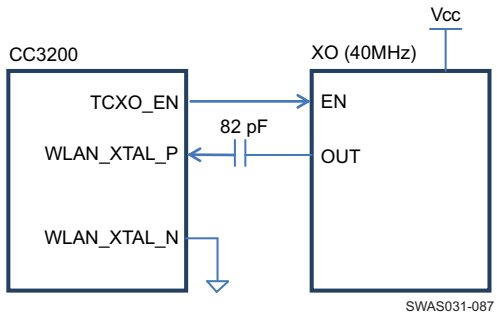


Figure 4-12. External TCXO Input

Table 4-5 lists the external F_{ref} clock requirements.

Table 4-5. External F_{ref} Clock Requirements (–40°C to +85°C)

Characteristics		Condition	Sym	Min	Typ	Max	Unit
Frequency					40.00		MHz
Frequency accuracy (Initial + temp + aging)						±25	ppm
Frequency input duty cycle				45	50	55	%
Clock voltage limits		Sine or clipped sine wave, AC coupled	Vpp	0.7		1.2	Vpp
Phase noise @ 40 MHz		@ 1 kHz				–125	dBc/Hz
		@ 10 kHz				–138.5	dBc/Hz
		@ 100 kHz				–143	dBc/Hz
Input impedance	Resistance			12			KΩ
	Capacitance					7	pF

4.11.3.5 Input Clocks/Oscillators

Table 4-6 lists the RTC crystal requirements.

Table 4-6. RTC Crystal Requirements

CHARACTERISTICS	CONDITION	SYM	MIN	TYP	MAX	UNIT
Frequency				32.768		kHz
Frequency accuracy	Initial + temp + aging				±150	ppm
Crystal ESR	32.768 kHz, C1 = C2 = 10 pF				70	kΩ

Table 4-7 lists the external RTC digital clock requirements.

Table 4-7. External RTC Digital Clock Requirements

CHARACTERISTICS	CONDITION	SYM	MIN	TYP	MAX	UNIT
Frequency				32768		Hz
Frequency accuracy (Initial + temp + aging)					±150	ppm
Input transition time t_r/t_f (10% to 90%)		t_r/t_f			100	ns
Frequency input duty cycle			20	50	80	%
Slow clock input voltage limits	Square wave, DC coupled	V_{ih}	0.65 × V_{IO}		V_{IO}	V
		V_{il}	0		0.35 × V_{IO}	V peak
Input impedance			1			MΩ
					5	pF

Table 4-8 lists the WLAN fast-clock crystal requirements.

Table 4-8. WLAN Fast-Clock Crystal Requirements

CHARACTERISTICS	CONDITION	SYM	MIN	TYP	MAX	UNIT
Frequency				40		MHz
Frequency accuracy	Initial + temp + aging				±25	ppm
Crystal ESR	40 MHz, C1 = C2 = 6.2 pF		40	50	60	Ohm

4.11.3.6 WLAN Filter Requirements

The device requires an external bandpass filter to meet the various emission standards, including FCC. Table 4-9 presents the attenuation requirements for the bandpass filter. TI recommends using the same filter used in the reference design to ease the process of certification.

Table 4-9. WLAN Filter Requirements

Parameter	Frequency (MHz)	Requirements			
		Min	Typ	Max	Units
Return loss	2412 to 2484	10			dB
Insertion loss(1)	2412 to 2484		1	1.5	dB

(1) Insertion loss directly impacts output power and sensitivity. At customer discretion, insertion loss can be relaxed to meet attenuation requirements.

Table 4-9. WLAN Filter Requirements (continued)

Parameter	Frequency (MHz)	Requirements			
		Min	Typ	Max	Units
Attenuation	800 to 830	30	45		dB
	1600 to 1670	20	25		
	3200 to 3300	30	48		
	4000 to 4150	45	50		
	4800 to 5000	20	25		
	5600 to 5800	20	25		
	6400 to 6600	20	35		
	7200 to 7500	35	45		
	7500 to 10000	20	25		
Reference Impendence	2412 to 2484		50		Ω
Filter type	Bandpass				

4.11.4 Interfaces

This section describes the interfaces that are supported by the CC3100 device:

- Host SPI
- Flash SPI
- Host UART

4.11.4.1 Host SPI Interface Timing

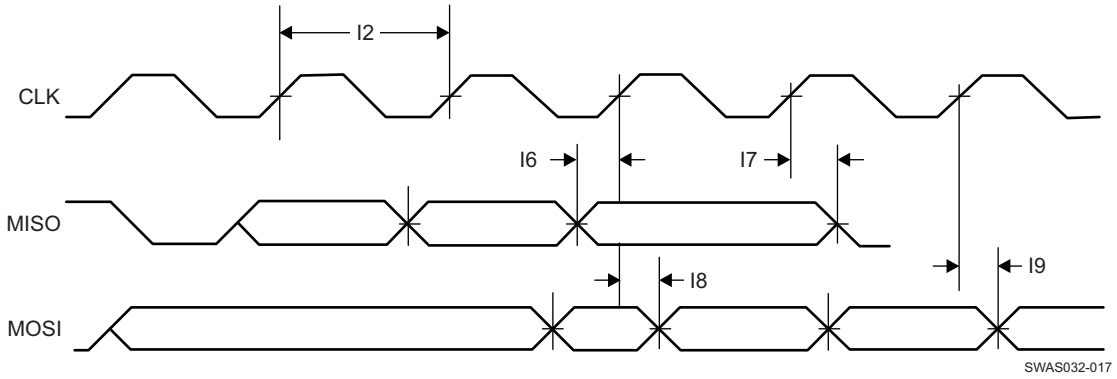


Figure 4-13. Host SPI Interface Timing

Table 4-10. Host SPI Interface Timing Parameters

Parameter Number	Parameter[1]	Parameter Name	Min	Max	Unit
I1	F	Clock frequency @ V_{BAT} = 3.3 V		20	MHz
		Clock frequency @ V_{BAT} ≤ 2.1 V		12	
I2	t_{clk}[2]	Clock period	50		ns
I3	t_{LP}	Clock low period		25	ns
I4	t_{HT}	Clock high period		25	ns
I5	D	Duty cycle	45	55	%
I6	t_{IS}	RX data setup time	4		ns
I7	t_{IH}	RX data hold time	4		ns
I8	t_{OD}	TX data output delay		20	

(1) The timing parameter has a maximum load of 20 pf at 3.3 V.
(2) Ensure that nCS (active-low signa)l is asserted 10 ns before the clock is toggled. nCS can be deasserted 10 ns after the clock edge.

Table 4-10. Host SPI Interface Timing Parameters (continued)

Parameter Number	Parameter[1]	Parameter Name	Min	Max	Unit
I9	t_{OH}	TX data hold time		24	ns

4.11.4.2 Flash SPI Interface Timing

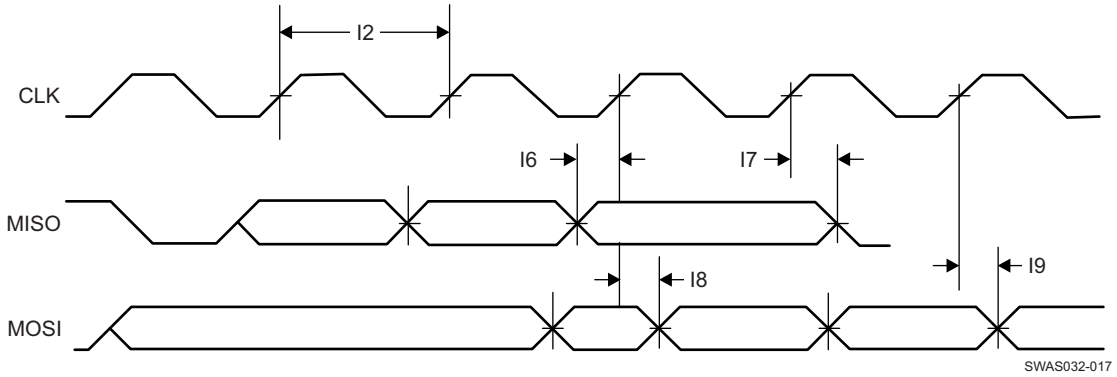


Figure 4-14. Flash SPI Interface Timing

Table 4-11. Flash SPI Interface Timing Parameters

Parameter Number	Parameter	Parameter Name	Min	Max	Unit
I1	F	Clock frequency		20	MHz
I2	t_{clk}	Clock period	50		ns
I3	t_{LP}	Clock low period		25	ns
I4	t_{HT}	Clock high period		25	ns
I5	D	Duty cycle	45	55	%
I6	t_{IS}	RX data setup time	1		ns
I7	t_{IH}	RX data hold time	2		ns
I8	t_{OD}	TX data output delay		8.5	ns
I9	t_{OH}	TX data hold time		8	ns

4.12 External Interfaces

4.12.1 SPI Flash Interface

The external serial flash stores the user profiles and firmware patch updates. The CC3100 device acts as a master in this case; the SPI serial flash acts as the slave device. This interface can work up to a speed of 20 MHz.

Figure 4-15 shows the SPI flash interface.

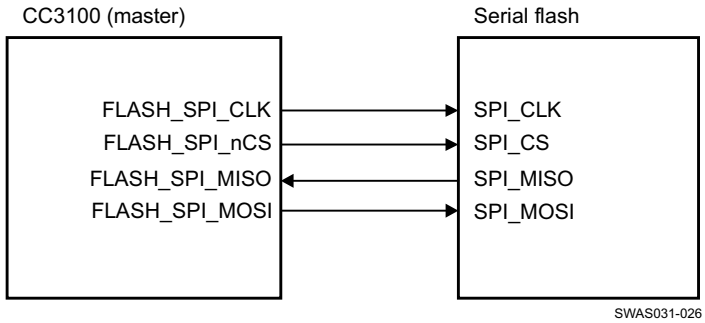


Figure 4-15. SPI Flash Interface

Table 4-12 lists the SPI flash interface pins.

Table 4-12. SPI Flash Interface

Pin Name	Description
FLASH_SPI_CLK	Clock (up to 20 MHz) CC3100 device to serial flash
FLASH_SPI_CS	CS (active low) signal from CC3100 device to serial flash
FLASH_SPI_MISO	Data from serial flash to CC3100 device
FLASH_SPI_MOSI	Data from CC3100 device to serial flash

4.12.2 SPI Host Interface

The device interfaces to an external host using the SPI interface. The CC3100 device can interrupt the host using the HOST_INTR line to initiate the data transfer over the interface. The SPI host interface can work up to a speed of 20 MHz.

Figure 4-16 shows the SPI host interface.

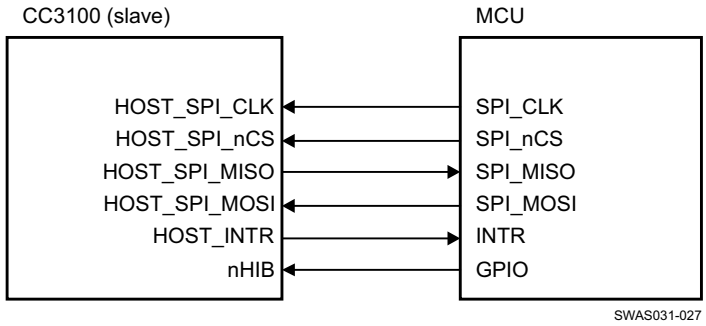


Figure 4-16. SPI Host Interface

Table 4-13 lists the SPI host interface pins.

Table 4-13. SPI Host Interface

Pin Name	Description
HOST_SPI_CLK	Clock (up to 20 MHz) from MCU host to CC3100 device
HOST_SPI_nCS	CS (active low) signal from MCU host to CC3100 device
HOST_SPI_MOSI	Data from MCU host to CC3100 device
HOST_INTR	Interrupt from CC3100 device to MCU host
HOST_SPI_MISO	Data from CC3100 device to MCU host
nHIB	Active-low signal that commands the CC3100 device to enter hibernate mode (lowest power state)

4.13 Host UART

The SimpleLink device requires the UART configuration described in Table 4-14.

Table 4-14. SimpleLink UART Configuration

Property	Supported CC3100 Configuration
Baud rate	115200 bps, no auto-baud rate detection, can be changed by the host up to 3 Mbps using a special command
Data bits	8 bits
Flow control	CTS/RTS
Parity	None
Stop bits	1
Bit order	LSBit first
Host interrupt polarity	Active high
Host interrupt mode	Rising edge or level 1
Endianness	Little-endian only(1)

(1) The SimpleLink device does not support automatic detection of the host length while using the UART interface.

4.13.1 5-Wire UART Topology

Figure 4-17 shows the typical 5-wire UART topology comprised of 4 standard UART lines plus one IRQ line from the device to the host controller to allow efficient low power mode.

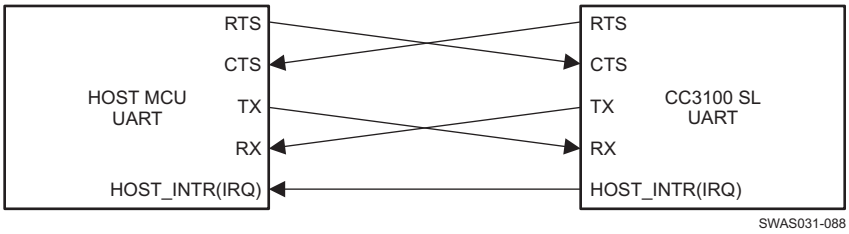


Figure 4-17. Typical 5-Wire UART Topology

This is the typical and recommended UART topology because it offers the maximum communication reliability and flexibility between the host and the SimpleLink device.

4.13.2 4-Wire UART Topology

The 4-wire UART topology eliminates the host IRQ line (see Figure 4-18). Using this topology requires one of the following conditions to be met:

- Host is always awake or active.
- Host goes to sleep but the UART module has receiver start-edge detection for auto wakeup and does not lose data.

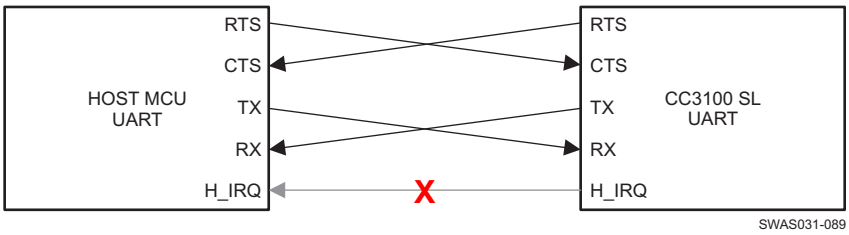


Figure 4-18. 4-Wire UART Configuration

4.13.3 3-Wire UART Topology

The 3-wire UART topology requires only the following lines (see Figure 4-19):

- RX
- TX
- CTS

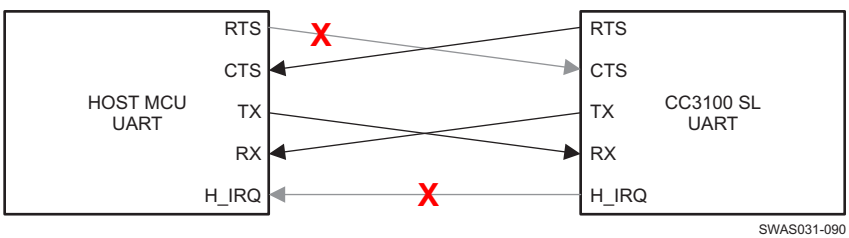


Figure 4-19. 3-Wire UART Topology

Using this topology requires one of the following conditions to be met:

- Host always stays awake or active.

- Host goes to sleep but the UART module has receiver start-edge detection for auto wakeup and does not lose data.
- Host can always receive any amount of data transmitted by the SimpleLink device because there is no flow control in this direction.

Because there is no full flow control, the host cannot stop the SimpleLink device to send its data; thus, the following parameters must be carefully considered:

- Max baud rate
- RX character interrupt latency and low-level driver jitter buffer
- Time consumed by the user's application

5 Detailed Description

5.1 Overview

5.1.1 Device Features

5.1.1.1 WLAN

- 802.11b/g/n integrated radio, modem, and MAC supporting WLAN communication as a BSS station with CCK and OFDM rates in the 2.4-GHz ISM band
- Auto-calibrated radio with a single-ended 50-Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with multiple user-configurable profiles stored in an NVMEM allows automatic fast connection to an access point without user or host intervention.
- Supports all common Wi-Fi security modes for personal and enterprise networks with on-chip security accelerators
- SmartConfig technology: A 1-step, 1-time process to connect a CC3100-enabled device to the home wireless network, removing dependency on the I/O capabilities of the host MCU; thus, it is usable by deeply embedded applications.
- 802.11 transceiver mode: Allows transmitting and receiving of proprietary data through a socket without adding MAC or PHY headers. This mode provides the option to select the working channel, rate, and transmitted power. The receiver mode works together with the filtering options.

5.1.1.2 Network Stack

- Integrated IPv4 TCP/IP stack with BSD socket APIs for simple Internet connectivity with any MCU, microprocessor, or ASIC
- Support of eight simultaneous TCP, UDP, or RAW sockets
- Built-in network protocols: ARP, ICMP, DHCP client, and DNS client for easy connection to the local network and the Internet
- Service discovery: Multicast DNS service discovery lets a client advertise its service without a centralized server. After connecting to the access point, the CC3100 device provides critical information, such as device name, IP, vendor, and port number.

5.1.1.3 Host Interface and Driver

- Interfaces over a 4-wire serial peripheral interface (SPI) with any MCU or a processor at a clock speed of 20 MHz.
- Interfaces over UART with any MCU with a baud rate up to 3 Mbps. A low footprint driver is provided for TI MCUs and is easily ported to any processor or ASIC.
- Simple APIs enable easy integration with any single-threaded or multithreaded application.

5.1.1.4 System

- Works from a single preregulated power supply or connects directly to a battery
- Ultra-low leakage when disabled (hibernate mode) with a current of less than 4 µA with the RTC running
- Integrated clock sources

5.2 Functional Block Diagram

Figure 5-1 shows the functional block diagram of the CC3100 SimpleLink Wi-Fi solution.

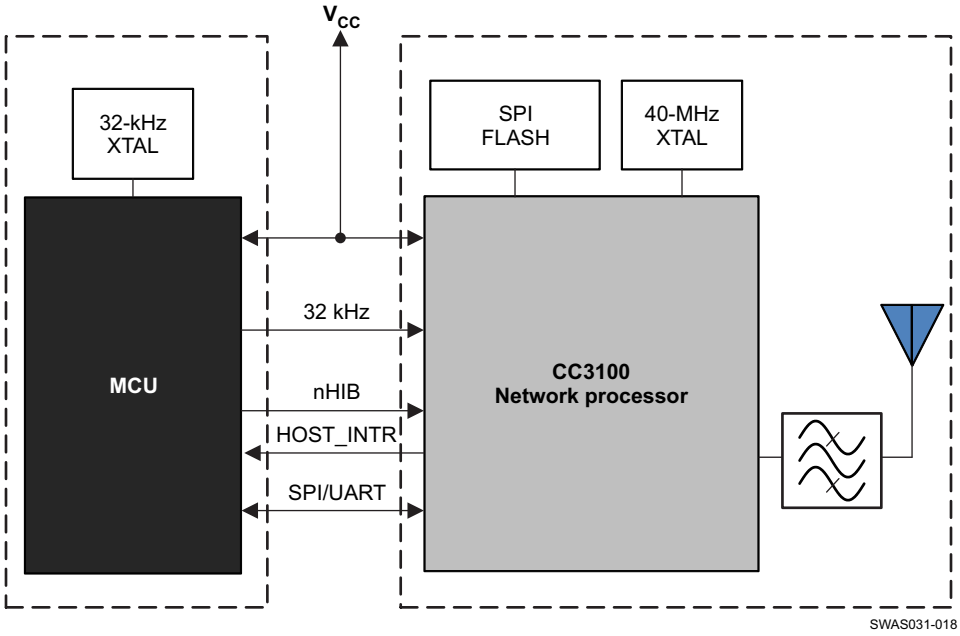


Figure 5-1. Functional Block Diagram

5.3 Wi-Fi Network Processor Subsystem

The Wi-Fi network processor subsystem includes a dedicated ARM MCU to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The CC3100 device supports station, AP, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security and WPS 2.0. The Wi-Fi network processor includes an embedded IPv4 TCP/IP stack.

Table 5-1 summarizes the NWP features.

Table 5-1. Summary of Features Supported by the NWP Subsystem

Item	Domain	Category	Feature	Details
1	TCP/IP	Network Stack	IPv4	Baseline IPv4 stack
2	TCP/IP	Network Stack	TCP/UDP	Base protocols
3	TCP/IP	Protocols	DHCP	Client and server mode
4	TCP/IP	Protocols	ARP	Support ARP protocol
5	TCP/IP	Protocols	DNS/mDNS	DNS Address resolution and local server
6	TCP/IP	Protocols	IGMP	Up to IGMPv3 for multicast management
7	TCP/IP	Applications	mDNS	Support multicast DNS for service publishing over IP
8	TCP/IP	Applications	mDNS-SD	Service discovery protocol over IP in local network
9	TCP/IP	Applications	Web Sever/HTTP Server	URL static and dynamic response with template.
10	TCP/IP	Security	TLS/SSL	TLS v1.2 (client/server)/SSL v3.0
11	TCP/IP	Security	TLS/SSL	For the supported Cipher Suite, go to SimpleLink Wi-Fi CC3100 SDK.
12	TCP/IP	Sockets	RAW Sockets	User-defined encapsulation at WLAN MAC/PHY or IP layers
13	WLAN	Connection	Policies	Allows management of connection and reconnection policy
14	WLAN	MAC	Promiscuous mode	Filter-based Promiscuous mode frame receiver

Table 5-1. Summary of Features Supported by the NWP Subsystem (continued)

Item	Domain	Category	Feature	Details
15	WLAN	Performance	Initialization time	From enable to first connection to open AP less than 50 ms
16	WLAN	Performance	Throughput	UDP = 16 Mbps
17	WLAN	Performance	Throughput	TCP = 13 Mbps
18	WLAN	Provisioning	WPS2	Enrollee using push button or PIN method.
19	WLAN	Provisioning	AP Config	AP mode for initial product configuration (with configurable Web page and beacon Info element)
20	WLAN	Provisioning	SmartConfig	Alternate method for initial product configuration
21	WLAN	Role	Station	802.11bgn Station with legacy 802.11 power save
22	WLAN	Role	Soft AP	802.11 bg single station with legacy 802.11 power save
23	WLAN	Role	P2P	P2P operation as GO
24	WLAN	Role	P2P	P2P operation as CLIENT
25	WLAN	Security	STA-Personal	WPA2 personal security
26	WLAN	Security	STA-Enterprise	WPA2 enterprise security
27	WLAN	Security	STA-Enterprise	EAP-TLS
28	WLAN	Security	STA-Enterprise	EAP-PEAPv0/TLS
29	WLAN	Security	STA-Enterprise	EAP-PEAPv1/TLS
30	WLAN	Security	STA-Enterprise	EAP-PEAPv0/MSCHAPv2
31	WLAN	Security	STA-Enterprise	EAP-PEAPv1/MSCHAPv2
32	WLAN	Security	STA-Enterprise	EAP-TTLS/EAP-TLS
33	WLAN	Security	STA-Enterprise	EAP-TTLS/MSCHAPv2
34	WLAN	Security	AP-Personal	WPA2 personal security

5.4 Power-Management Subsystem

The CC3100 power-management subsystem contains DC-DC converters to accommodate the differing voltage or current requirements of the system.

- Digital DC-DC
  - Input: VBAT wide voltage (2.1 to 3.6 V) or preregulated 1.85 V
- ANA1 DC-DC
  - Input: VBAT wide voltage (2.1 to 3.6 V)
  - In preregulated 1.85-V mode, the ANA1 DC-DC converter is bypassed.
- PA DC-DC
  - Input: VBAT wide voltage (2.1 to 3.6 V)
  - In preregulated 1.85-V mode, the PA DC-DC converter is bypassed.

In preregulated 1.85-V mode, the ANA1 DC-DC and PA DC-DC converters are bypassed. The CC3100 device is a single-chip WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC-DC converters and LDOs, generates all of the voltages required for the device to operate from a wide variety of input sources. For maximum flexibility, the device can operate in the modes described in the following sections.

5.4.1 VBAT Wide-Voltage Connection

In the wide-voltage battery connection, the device is powered directly by the battery. All other voltages required to operate the device are generated internally by the DC-DC converters. This scheme is the most common mode for the device as it supports wide-voltage operation from 2.1 to 3.6 V (for electrical connections, see Section 6.1.1, *Typical Application – CC3100 Wide-Voltage Mode*).

5.4.2 Preregulated 1.85 V

The preregulated 1.85-V mode of operation applies an external regulated 1.85 V directly at the pins 10, 25, 33, 36, 37, 39, 44, 48, and 54 of the device. The VBAT and the VIO are also connected to the 1.85-V supply. This mode provides the lowest BOM count version in which inductors used for PA DC-DC and ANA1 DC-DC (2.2 and 1 µH) and a capacitor (22 µF) can be avoided. For electrical connections, see Section 6.1.2, *Typical Application – CC3100 Preregulated 1.85-V Mode*.

In the preregulated 1.85-V mode, the regulator providing the 1.85 V must have the following characteristics:

- Load current capacity ≥900 mA.
- Line and load regulation with <2% ripple with 500 mA step current and settling time of <4 µs with the load step.
- The regulator must be placed very close to the CC3100 device so that the IR drop to the device is very low.

5.5 Low-Power Operating Modes

This section describes the low-power modes supported by the device to optimize battery life.

5.5.1 Low-Power Deep Sleep

The low-power deep-sleep (LPDS) mode is an energy-efficient and transparent sleep mode that is entered automatically during periods of inactivity based on internal power optimization algorithms. The device can wake up in less than 3 ms from the internal timer or from any incoming host command. Typical battery drain in this mode is 115 µA. During LPDS mode, the device retains the software state and certain configuration information. The operation is transparent to the external host; thus, no additional handshake is required to enter or exit this sleep mode.

5.5.2 Hibernate

The hibernate mode is the lowest power mode in which all of the digital logic is power-gated. Only a small section of the logic powered directly by the main input supply is retained. The real-time clock (RTC) is kept running and the device wakes up once the nHIB line is asserted by the host driver. The wake-up time is longer than LPDS mode at about 50 ms.

NOTE

Wake-up time can be extended to 75 ms if a patch is loaded from the serial flash.

5.6 Memory

5.6.1 External Memory Requirements

The CC3100 device maintains a proprietary file system on the SFLASH. The CC3100 file system stores the service pack file, system files, configuration files, certificate files, web page files, and user files. By using a format command through the API, users can provide the total size allocated for the file system. The starting address of the file system cannot be set and is always located at the beginning of the SFLASH. The applications microcontroller must access the SFLASH memory area allocated to the file system directly through the CC3100 file system. The applications microcontroller must not access the SFLASH memory area directly.

The file system manages the allocation of SFLASH blocks for stored files according to download order, which means that the location of a specific file is not fixed in all systems. Files are stored on SFLASH using human-readable file names rather than file IDs. The file system API works using plain text, and file encryption and decryption is invisible to the user. Encrypted files can be accessed only through the file system.

All file types can have a maximum of 128 supported files in the file system. All files are stored in blocks of 4KB and thus use a minimum of 4KB of flash space. Encrypted files with fail-safe support and optional security are twice the original size and use a minimum of 8KB. Encrypted files are counted as fail safe in terms of space. The maximum file size is 16MB.

Table 5-2 lists the SFLASH size recommendations.

Table 5-2. CC3100 SFLASH Size Recommendations

Item	Typical Fail-Safe	Typical NonFail-Safe
File system	20KB	20KB
Service pack	224KB	112KB
System and configuration files	216KB	108KB
Total	4Mb	2Mb
Recommended	8Mb	4Mb

The CC3100 device supports JEDEC specification SFDP (serial flash device parameters). The following SFLASH devices are verified for functionality with the CC3100 device in addition to the ones in the reference design:

- Micron (N25Q128-A13BSE40): 128Mb
- Spansion (S25FL208K): 8Mb
- Winbond (W25Q16V): 16Mb
- Adesto (AT25DF081A): 8Mb
- Macronix (MX25L12835F-M2): 128Mb

For compatibility with the CC3100 device, the SFLASH device must support the following commands:

- Command 0x9F (read the device ID [JEDEC]). Procedure: SEND 0x9F, READ 3 bytes.
- Command 0x05 (read the status of the SFLASH). Procedure: SEND 0x05, READ 1 byte. Assume bit 0 is busy and bit 1 is write enable.
- Command 0x06 (set write enable). Procedure: SEND 0x06, read status until write-enable bit is set.
- Command 0xC7 (chip erase). Procedure: SEND 0xC7, read status until busy bit is cleared.
- Command 0x03 (read data). Procedure: SEND 0x03, SEND 24-bit address, read *n* bytes.
- Command 0x02 (write page). Procedure: SEND 0x02, SEND 24-bit address, write *n* bytes ($0<n<256$).
- Command 0x20 (sector erase). Procedure: SEND 0x20, SEND 24-bit address, read status until busy bit is cleared. Sector size is assumed to be always 4K.

6 Applications and Implementation

6.1 Application Information

6.1.1 Typical Application – CC3100 Wide-Voltage Mode

Figure 6-1 shows the schematics for an application using the CC3100 wide-voltage mode.

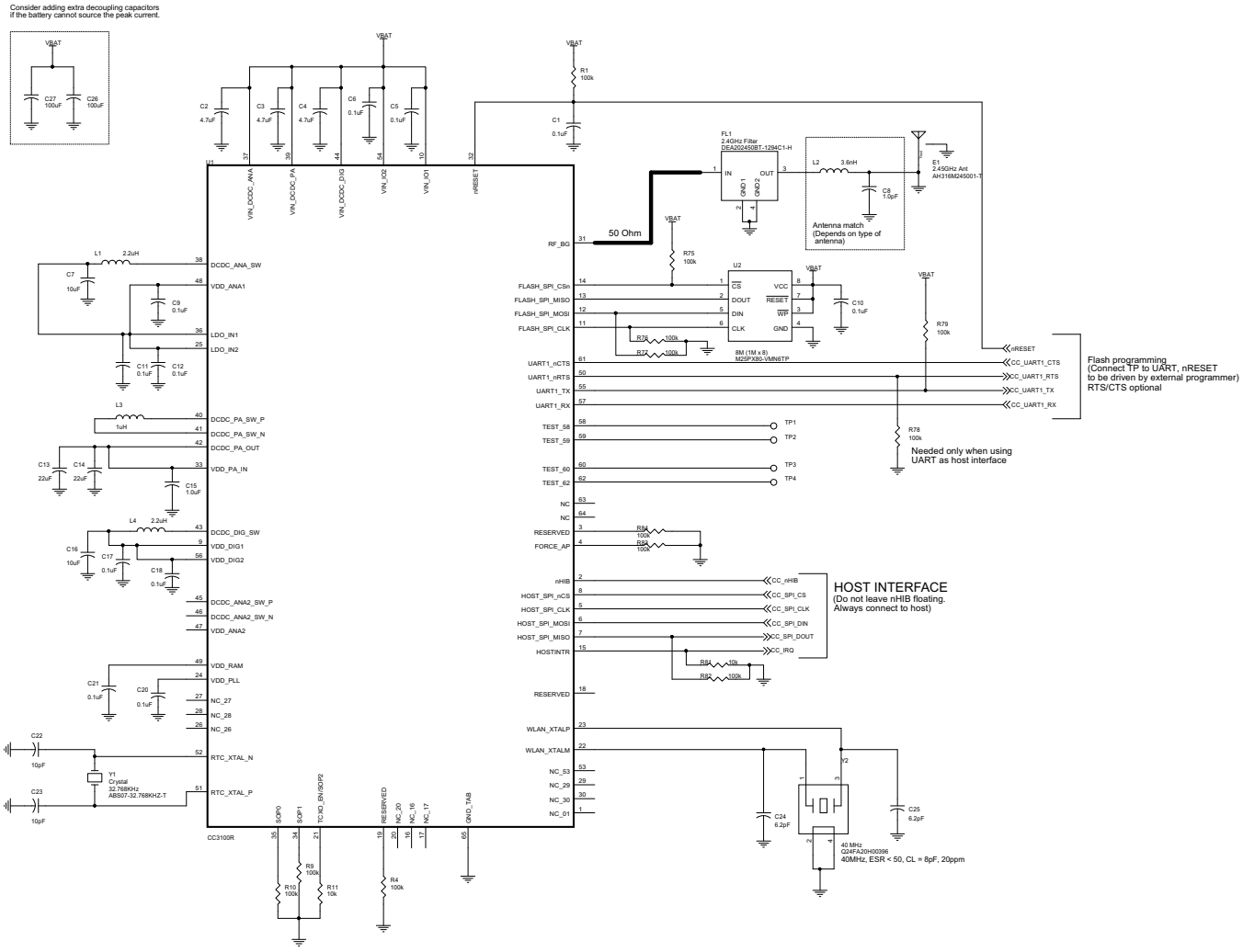


Figure 6-1. Schematics for CC3100 Wide-Voltage Mode Application

Table 6-1 lists the bill of materials for an application using the CC3100 wide-voltage mode.

Table 6-1. Bill of Materials for CC3100 Wide Voltage Mode ApplicationTable 6-1

Item	Qty	Reference	Value	Manufacturer	Part Number	Description
1	12	C1 C5 C6 C9 C10 C11 C12 C17 C18 C20 C21 C28	0.1 µF	Taiyo Yuden	LMK105BJ104KV-F	CAP CER 0.1 µF 10 V 10% X5R 0402
2	3	C2 C3 C4	4.7 µF	Samsung Electro-Mechanics America, Inc	CL05A475MQ5NRNC	CAP CER 4.7 µF 6.3 V 20% X5R 0402
3	1	C8	1.0 pF	Murata Electronics North America	GJM1555C1H1R0BB01D	CAP CER 1 pF 50 V NP0 0402
4	1	C13	22 µF	Taiyo Yuden	AMK107BBJ226MAHT	CAP CER 22 µF 4 V 20% X5R 0603
5	1	C16	10 µF	Murata Electronics North America	GRM188R60J106ME47D	CAP CER 10 µF 6.3 V 20% X5R 0603
6	2	C22 C23	10 pF	Murata Electronics North America	GRM1555C1H100FA01D	CAP CER 10 pF 50 V 1% NP0 0402
7	2	C24 C25	6.2 pF	Kemet	CBR04C609B1GAC	CAP CER 6 pF 100 V NP0 0402
8	2	C26 C27	100 µF	TDK Corportation	C3216X5R0J107M160AB	CAP CER 100 µF 6.3 V 20% X5R 1206
9	1	E1	2.45G Hz Ant	Taiyo Yuden	AH316M245001-T	ANT BLUETOOTH WLAN ZIGBEE WIMAX
10	1	FL1	2.4G Hz Filter	TDK-Epcos	DEA202450BT-1294C1-H	FILTER BANDPASS 2.45 GHZ WLAN SMD
11	1	L2	3.6 nH	Murata Electronics North America	LQP15MN3N6B02D	INDUCTOR 3.6 nH 0.1 nH 0402
12	1	L4	2.2 µH	Murata Electronics North America	LQM2HPN2R2MG0L	INDUCTOR 2.2 µH 20% 1300 mA 1008
13	1	U1	CC3100	Texas Instruments	CC3100R1	802.11bg Wi-Fi Processor
14	1	U2	8M (1M x 8)	Winbond	W25Q80BWZPIG	IC FLASH 8 Mb 75 MHZ 8WSON
15	1	Y1	Crystal	Abracon Corporation	ABS07-32.768KHZ-T	CRYSTAL 32.768 KHZ 12.5 pF SMD
16	1	Y2	Crystal	Epson	Q24FA20H00396	CRYSTAL 40 MHZ 8 pF SMD

NOTE

Use any 5% tolerance resistor 0402 or higher package.

6.1.2 Typical Application – CC3100 Preregulated 1.85-V Mode

Figure 6-2 shows the schematics for an application using the CC3100 preregulated 1.85-V mode.

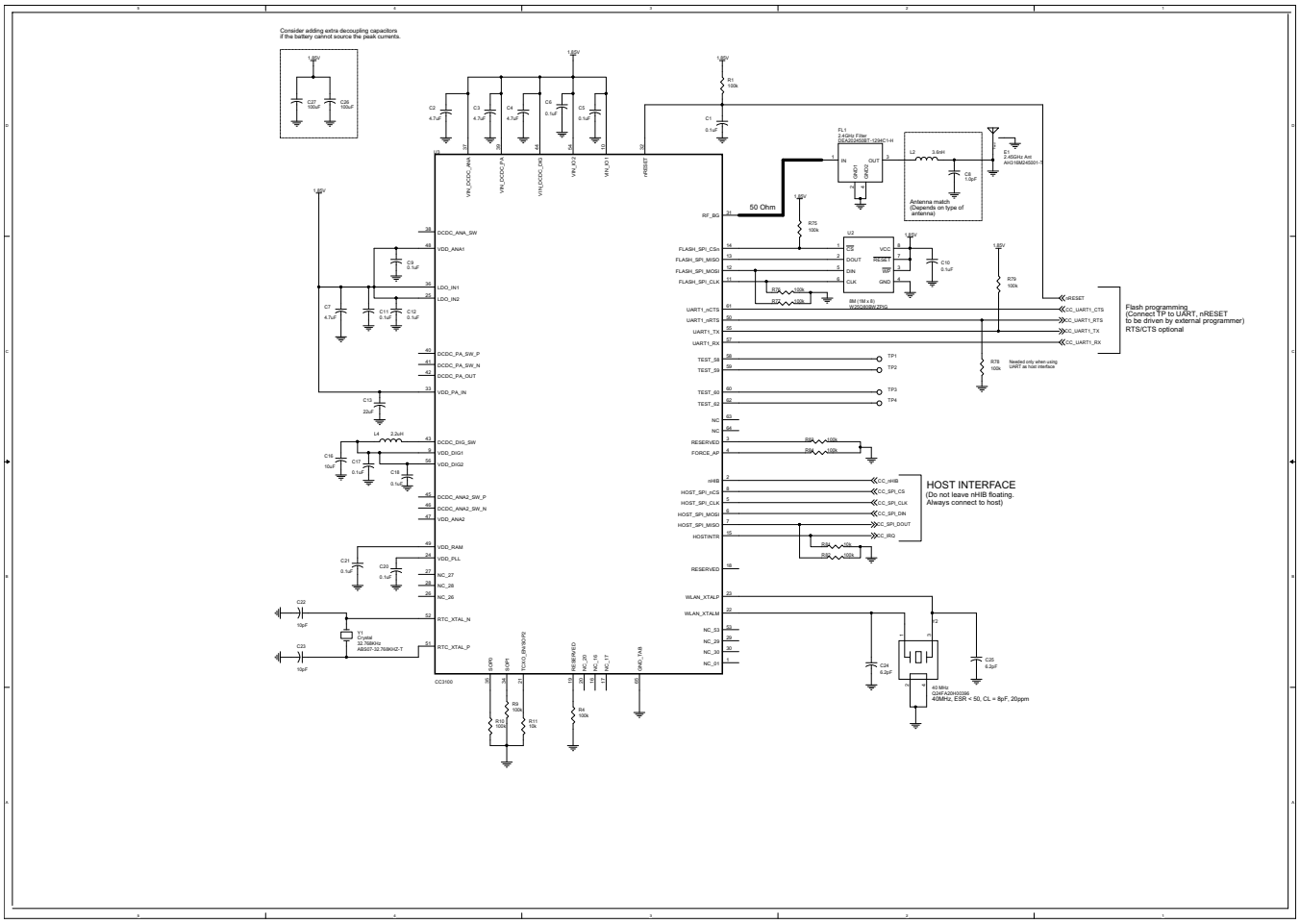


Figure 6-2. Schematics for CC3100 Preregulated 1.85-V Mode Application

Table 6-1 lists the bill of materials for an application using the CC3100 preregulated 1.85-V mode.

Table 6-2. Bill of Materials for CC3100 Preregulated 1.85-V Mode Application

Item	Qty	Reference	Value	Manufacturer	Part Number	Description
1	12	C1 C5 C6 C9 C10 C11 C12 C17 C18 C20 C21 C28	0.1 µF	Taiyo Yuden	LMK105BJ104KV-F	Capacitor, Ceramic: 0.1 µF 10 V 10% X5R 0402
2	4	C2 C3 C4 C7	4.7 µF	Samsung Electro-Mechanics America, Inc	CL05A475MQ5NRNC	Capacitor, Ceramic: 4.7 µF 6.3 V 20% X5R 0402
3	1	C8	1.0 pF	Murata Electronics North America	GJM1555C1H1R0BB01D	Capacitor, Ceramic: 1 pF 50 V NP0 0402
4	1	C13	22 µF	Taiyo Yuden	AMK107BBJ226MAHT	Capacitor, Ceramic: 22 µF 4 V 20% X5R 0603
5	1	C16	10 µF	Murata Electronics North America	GRM188R60J106ME47D	Capacitor, Ceramic: 10 µF 6.3 V 20% X5R 0603
6	2	C22 C23	10 pF	Murata Electronics North America	GRM1555C1H100FA01D	Capacitor, Ceramic: 10 pF 50 V 1% NP0 0402
7	2	C24 C25	6.2 pF	Kemet	CBR04C609B1GAC	Capacitor, Ceramic: 6 pF 100 V NP0 0402
8	2	C26 C27	100 µF	TDK Corportation	C3216X5R0J107M160AB	Capacitor, Ceramic: 100 µF 6.3 V 20% X5R 1206
9	1	E1	2.45-GHz Ant	Taiyo Yuden	AH316M245001-T	Antenna, Bluetooth: WLAN ZigBee WIMAX
10	1	FL1	2.4-GHz Filter	TDK-Epcos	DEA202450BT-1294C1-H	Filter, Bandpass: 2.45 GHz WLAN SMD
11	1	L2	3.6 nH	Murata Electronics North America	LQP15MN3N6B02D	Inductor: 3.6 nH 0.1 nH 0402
12	1	L4	2.2 µH	Murata Electronics North America	LQM2HPN2R2MG0L	Inductor: 2.2 µH 20% 1300 mA 1008
13	1	U1	CC3100	Texas Instruments	CC3100R1	802.11bg Wi-Fi Processor
14	1	U2	8M (1M x 8)	Winbond	W25Q80BWZPIG	IC Flash 8 Mb 75 MHz 8WSON
15	1	Y1	Crystal	Abracon Corporation	ABS07-32.768KHZ-T	Crystal 32.768 kHz 12.5 pF SMD
16	1	Y2	Crystal	Epson	Q24FA20H00396	Crystal 40 MHZ 8 pF SMD

NOTE

Use any 5% tolerance resistor 0402 or higher package.

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

The CC3100 evaluation board includes a set of tools and documentation to help the user during the development phase.

7.1.1.1 Radio Tool

The SimpleLink radio tool is a utility for operating and testing the CC3100 chipset RF performance characteristics during development of the application board. The CC3100 device has an auto-calibrated radio that enables easy connection to the antenna without requiring expertise in radio circuit design.

7.1.1.2 Uniflash Flash Programmer

The Uniflash flash programmer utility allows end users to communicate with the SimpleLink device to update the serial flash. The easy GUI interface enables flashing of files (including read-back verification option), storage format (secured and nonsecured formatting), version reading for boot loader and chip ID, and so on.

7.1.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of the CC3100 device and support tools (see Figure 7-1).

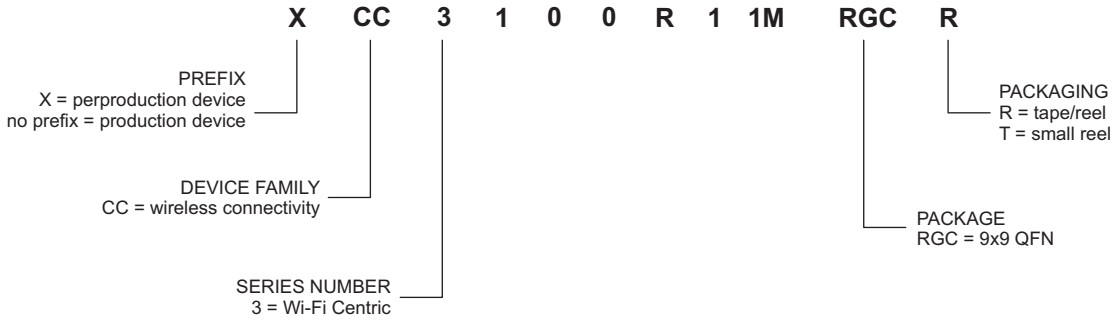


Figure 7-1. CC3100 Device Nomenclature

7.2 Documentation Support

The following documents provide support for the CC3100 device.

SWRU370	*CC3100 and CC3200 SimpleLink Wi-Fi and IoT Solution Layout Guidelines*
SWRU375	*CC3100 SimpleLink Wi-Fi and IoT Solution Getting Started Guide*
SWRU368	*CC3100 SimpleLink Wi-Fi and IoT Solution Programmer's Guide*
SWRU371	*CC3100 SimpleLink Wi-Fi and IoT Solution BoosterPack Hardware User Guide*
SWRC288	*CC3100 SimpleLink Wi-Fi and IoT Solution Booster Pack Design Files*

7.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.4 Trademarks

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical Packaging and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC3100R11MRGC	ACTIVE	VQFN	RGC	64	260	Green (RoHS & no Sb/Br)	CU	Level-3-260C-168 HR	-40 to 85	CC3100R1	Samples
CC3100R11MRGCR	ACTIVE	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	CU	Level-3-260C-168 HR	-40 to 85	CC3100R1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

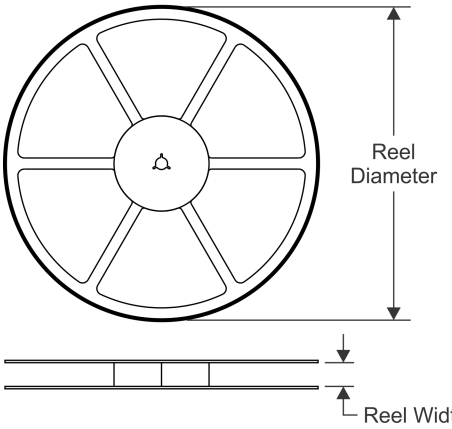
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

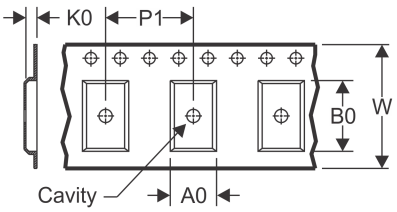
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

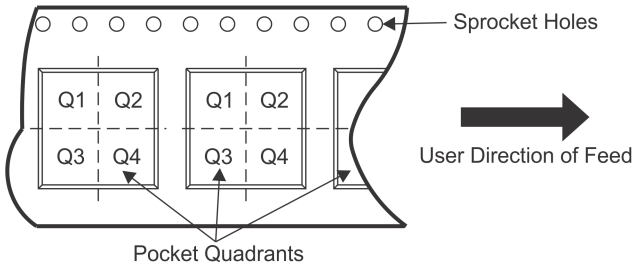


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

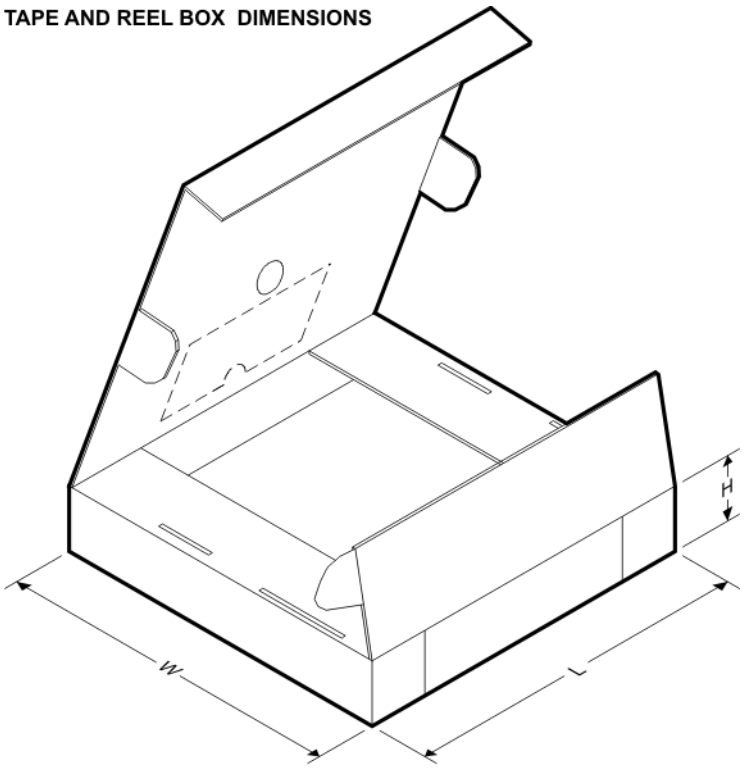
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC3100R11MRGCR	VQFN	RGC	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

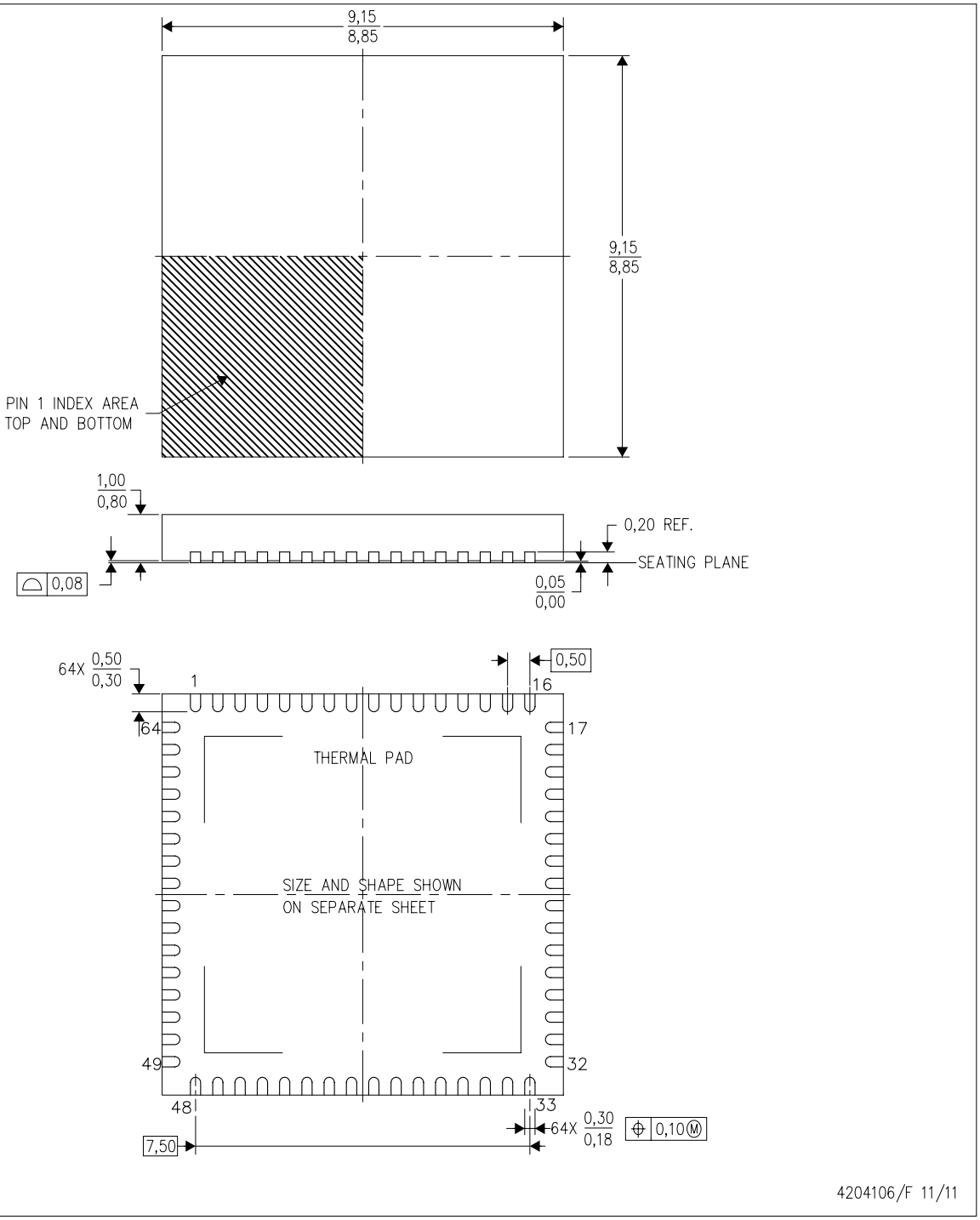
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC3100R11MRGCR	VQFN	RGC	64	2500	367.0	367.0	38.0

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

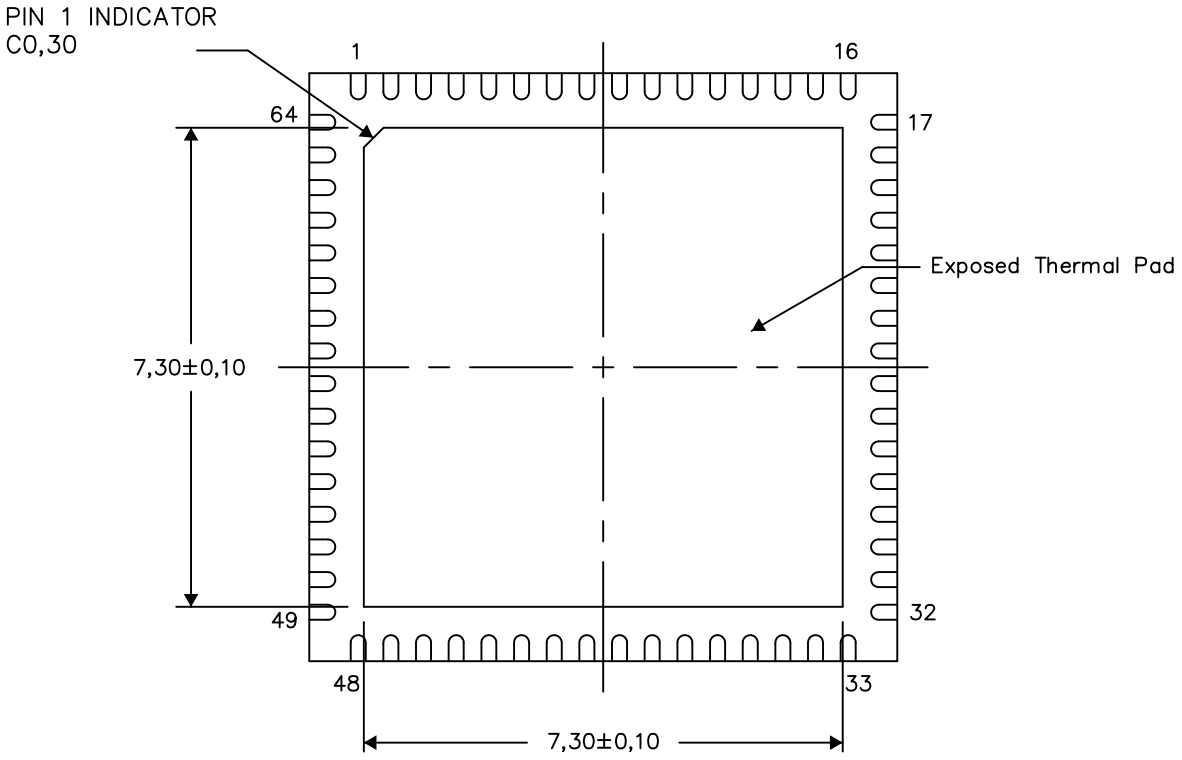
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206192–14/AE 03/15

NOTE: A. All linear dimensions are in millimeters

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