

CY74FCT2244T

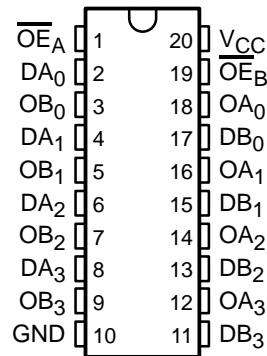
8-BIT BUFFER/LINE DRIVER

WITH 3-STATE OUTPUTS

SCCS074 – OCTOBER 2001

- Function and Pinout Compatible With FCT and F Logic
- 25-Ω Output Series Resistors Reduce Transmission-Line Reflection Noise
- TTL-Output-Level Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- 12-mA Output Sink Current
15-mA Output Source Current
- 3-State Outputs

Q OR SO PACKAGE
(TOP VIEW)



description

The CY74FCT2244T is an octal buffer and line driver that includes on-chip 25-Ω terminating resistors at each of the outputs to minimize noise resulting from reflections or standing waves in high-performance applications. The on-chip resistors reduce overall board space and component count. Designed to be employed as a memory address driver, clock driver, and bus-oriented transmitter/receiver, this device provides speed and drive capabilities commensurate with its fastest bipolar logic counterparts, while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices, without the need for external components.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

| T _A | PACKAGE† | | SPEED (ns) | ORDERABLE PART NUMBER | TOP-SIDE MARKING | |
|----------------|---------------|---------------|---------------|-----------------------|------------------|----------|
| –40°C to 85°C | QSOP – Q | Tape and reel | 4.3 | CY74FCT2244CTQCT | FCT2244C | |
| | | Tube | 4.3 | CY74FCT2244CTSOC | FCT2244C | |
| | SOIC – SO | Tape and reel | 4.3 | CY74FCT2244CTSOCT | | |
| | | QSOP – Q | Tape and reel | 4.6 | CY74FCT2244ATQCT | FCT2244A |
| | SOIC – SO | | Tube | 4.6 | CY74FCT2244ATSOC | FCT2244A |
| | | Tape and reel | 4.6 | CY74FCT2244ATSOCT | | |
| | –40°C to 85°C | QSOP – Q | Tape and reel | 6.5 | CY74FCT2244TQCT | FCT2244 |
| | | | Tube | 6.5 | CY74FCT2244TSOC | FCT2244 |
| | | SOIC – SO | Tape and reel | 6.5 | CY74FCT2244TSOCT | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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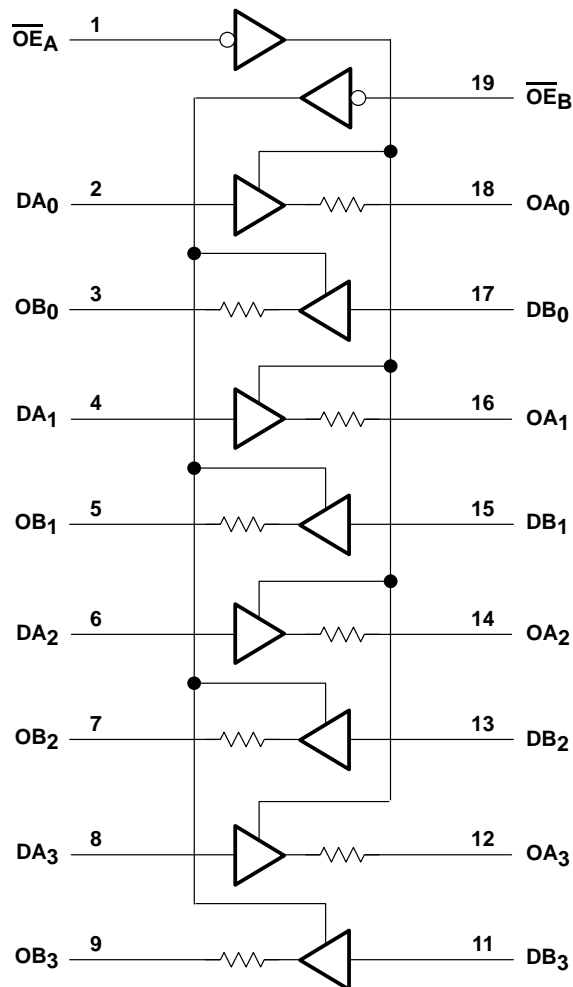
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FUNCTION TABLE

| INPUTS | | | OUTPUT |
|-------------------|-------------------|---|--------|
| \overline{OE}_A | \overline{OE}_B | D | O |
| L | L | L | L |
| L | L | H | H |
| H | H | X | Z |

H = High logic level, L = Low logic level,
 X = Don't care, Z = High-impedance (off)
 state

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|-----------------|
| Supply voltage range to ground potential | –0.5 V to 7 V |
| DC input voltage range | –0.5 V to 7 V |
| DC output voltage range | –0.5 V to 7 V |
| DC output current (maximum sink current/pin) | 120 mA |
| Package thermal impedance, θ_{JA} (see Note 1): Q package | 68°C/W |
| SO package | 58°C/W |
| Ambient temperature range with power applied, T_A | –65°C to +135°C |
| Storage temperature range, T_{stg} | –65°C to +150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

| | MIN | NOM | MAX | UNIT |
|--------------------------------------|------|-----|------|------|
| V_{CC} Supply voltage | 4.75 | 5 | 5.25 | V |
| V_{IH} High-level input voltage | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.8 | V |
| I_{OH} High-level output current | | | –15 | mA |
| I_{OL} Low-level output current | | | 12 | mA |
| T_A Operating free-air temperature | –40 | | 85 | °C |

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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8-BIT BUFFER/LINE DRIVER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---------------------|--|--|--|------|---------|---------------|
| V_{IK} | $V_{CC} = 4.75\text{ V}$, | $I_{IN} = -18\text{ mA}$ | | -0.7 | -1.2 | V |
| V_{OH} | $V_{CC} = 4.75\text{ V}$, | $I_{OH} = -15\text{ mA}$ | 2.4 | 3.3 | | V |
| V_{OL} | $V_{CC} = 4.75\text{ V}$, | $I_{OL} = 12\text{ mA}$ | | 0.3 | 0.55 | V |
| R_{OUT} | $V_{CC} = 4.75\text{ V}$, | $I_{OL} = 12\text{ mA}$ | 20 | 25 | 40 | Ω |
| V_{hys} | All inputs | | | 0.2 | | V |
| I_I | $V_{CC} = 5.25\text{ V}$, | $V_{IN} = V_{CC}$ | | | 5 | μA |
| I_{IH} | $V_{CC} = 5.25\text{ V}$, | $V_{IN} = 2.7\text{ V}$ | | | ± 1 | μA |
| I_{IL} | $V_{CC} = 5.25\text{ V}$, | $V_{IN} = 0.5\text{ V}$ | | | ± 1 | μA |
| I_{OZH} | $V_{CC} = 5.25\text{ V}$, | $V_{OUT} = 2.7\text{ V}$ | | | 10 | μA |
| I_{OZL} | $V_{CC} = 5.25\text{ V}$, | $V_{OUT} = 0.5\text{ V}$ | | | -10 | μA |
| I_{OS}^\ddagger | $V_{CC} = 5.25\text{ V}$, | $V_{OUT} = 0\text{ V}$ | -60 | -120 | -225 | mA |
| I_{off} | $V_{CC} = 0\text{ V}$, | $V_{OUT} = 4.5\text{ V}$ | | | ± 1 | μA |
| I_{CC} | $V_{CC} = 5.25\text{ V}$, | $V_{IN} \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ | | 0.1 | 0.2 | mA |
| ΔI_{CC} | $V_{CC} = 5.25\text{ V}$, $V_{IN} = 3.4\text{ V}^\S$, $f_1 = 0$, Outputs open | | | 0.5 | 2 | mA |
| I_{CCD}^\parallel | $V_{CC} = 5.25\text{ V}$, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$, $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$ | | | 0.06 | 0.12 | mA/MHz |
| $I_C^\#$ | $V_{CC} = 5.25\text{ V}$, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$ | One bit switching at $f_1 = 10\text{ MHz}$ at 50% duty cycle | $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$ | 0.7 | 1.4 | mA |
| | | | $V_{IN} = 3.4\text{ V}$ or GND | 1 | 2.4 | |
| | | Eight bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle | $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$ | 1.3 | 2.6 | |
| | | | $V_{IN} = 3.4\text{ V}$ or GND | 3.3 | 10.6 | |
| C_i | | | | 5 | 10 | pF |
| C_o | | | | 9 | 12 | pF |

† Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input ($V_{IN} = 3.4\text{ V}$); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

$$\# I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4\text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_C formula.



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switching characteristics over operating free-air temperature range (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CY74FCT2244T | | CY74FCT2244AT | | CY74FCT2244CT | | UNIT |
|------------------|-----------------|----------------|--------------|-----|---------------|-----|---------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | D | O | 1.5 | 6.5 | 1.5 | 4.6 | 1.5 | 4.1 | ns |
| t _{PHL} | | | 1.5 | 6.5 | 1.5 | 4.6 | 1.5 | 4.1 | |
| t _{PZH} | \overline{OE} | O | 1.5 | 8 | 1.5 | 6.2 | 1.5 | 5.8 | ns |
| t _{PZL} | | | 1.5 | 8 | 1.5 | 6.2 | 1.5 | 5.8 | |
| t _{PHZ} | \overline{OE} | O | 1.5 | 7 | 1.5 | 5.6 | 1.5 | 5.2 | ns |
| t _{PLZ} | | | 1.5 | 7 | 1.5 | 5.6 | 1.5 | 5.2 | |



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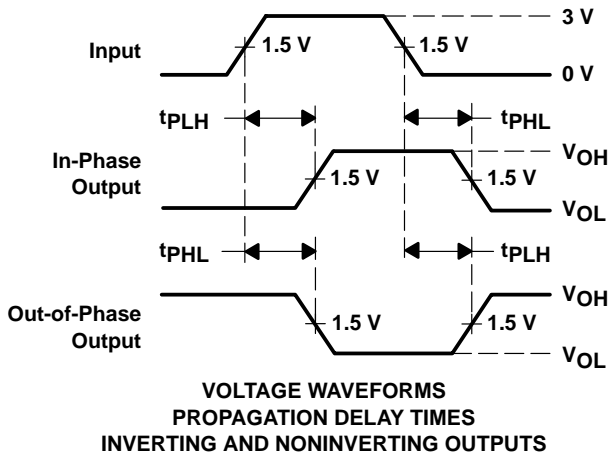
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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CY74FCT2244ATQCT | ACTIVE | SSOP | DBQ | 20 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT2244A | Samples |
| CY74FCT2244ATQCTE4 | ACTIVE | SSOP | DBQ | 20 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT2244A | Samples |
| CY74FCT2244ATSOC | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2244A | Samples |
| CY74FCT2244CTQCT | ACTIVE | SSOP | DBQ | 20 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT2244C | Samples |
| CY74FCT2244CTSOC | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2244C | Samples |
| CY74FCT2244CTSOCG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2244C | Samples |
| CY74FCT2244TQCT | ACTIVE | SSOP | DBQ | 20 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT2244 | Samples |
| CY74FCT2244TSOC | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2244 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CY74FCT2244ATQCT | SSOP | DBQ | 20 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CY74FCT2244CTQCT | SSOP | DBQ | 20 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CY74FCT2244TQCT | SSOP | DBQ | 20 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CY74FCT2244ATQCT | SSOP | DBQ | 20 | 2500 | 367.0 | 367.0 | 38.0 |
| CY74FCT2244CTQCT | SSOP | DBQ | 20 | 2500 | 367.0 | 367.0 | 38.0 |
| CY74FCT2244TQCT | SSOP | DBQ | 20 | 2500 | 367.0 | 367.0 | 38.0 |

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

DBQ (R-PDSO-G20)

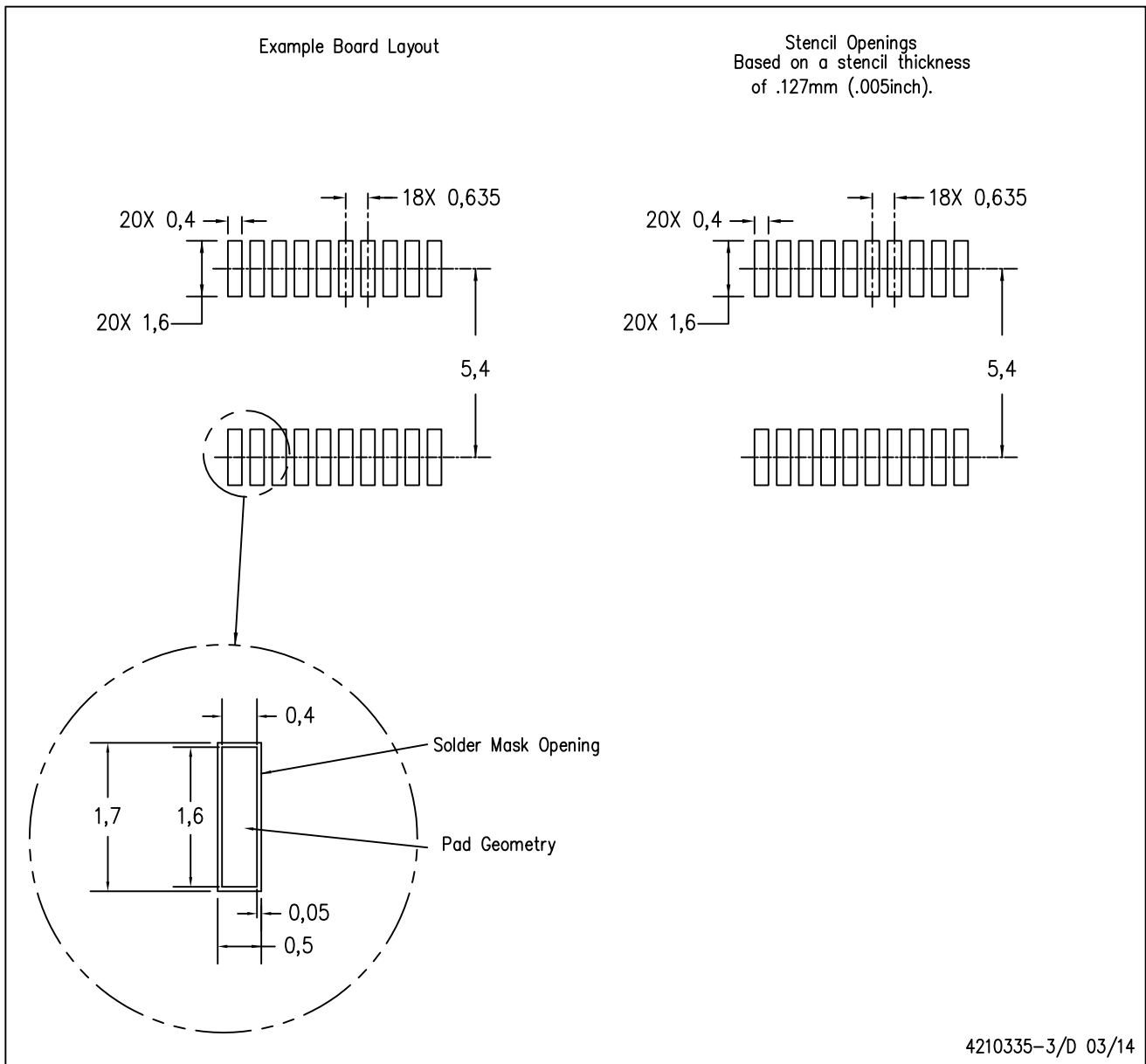
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AD.

DBQ (R-PDSO-G20)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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