# DS25CP102 3.125 Gbps 2X2 LVDS Crosspoint Switch with Transmit Pre-Emphasis and Receive Equalization

**Check for Samples: DS25CP102**

## FEATURES

- **DC - 3.125 Gbps Low Jitter, Low Skew, Low Power Operation**
- **Pin Configurable, Fully Differential, Non-Blocking Architecture**
- **Pin Selectable Transmit Pre-Emphasis and Receive Equalization Eliminate Data Dependant Jitter**
- **Wide Input Common Mode Voltage Range Allows DC-Coupled Interface to CML and LVPECL Drivers**
- **On-Chip 100Ω Input and Output Termination Minimizes Insertion and Return Losses, Reduces Component Count, Minimizes Board Space**
- **8 kV ESD on LVDS I/O Pins Protects Adjoining Components**
- **Small 4 mm x 4 mm WQFN-16 Space Saving Package**

## APPLICATIONS

- **High-Speed Channel Select Applications**
- **Clock and Data Buffering and Muxing**
- **OC-48 / STM-16**
- **SD/HD/3GHD SDI Routers**

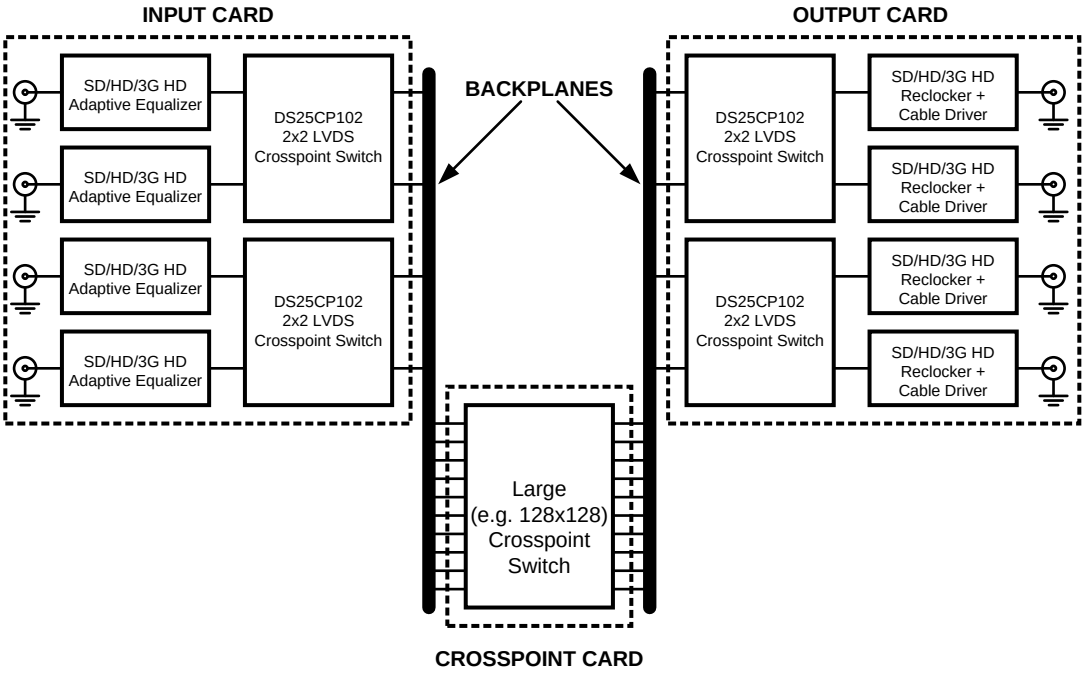
## DESCRIPTION

The DS25CP102 is a 3.125 Gbps 2x2 LVDS crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output or outputs.

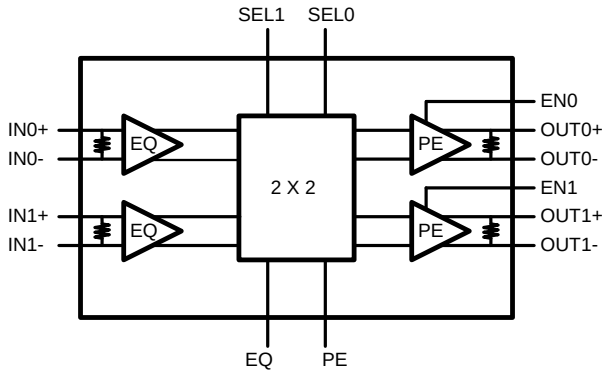
The DS25CP102 features two levels (Off and On) of transmit pre-emphasis (PE) and two levels (Off and On) of receive equalization (EQ).

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. Each differential input and output is internally terminated with a 100Ω resistor to lower device insertion and return losses, reduce component count and further minimize board space.

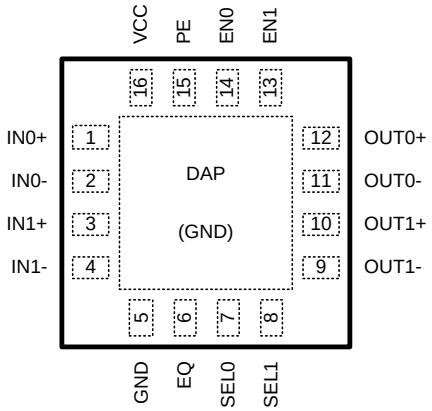
## Typical Application




## Block Diagram




## Connection Diagram



## PIN DESCRIPTIONS

| Pin Name | Pin Number | I/O, Type | Pin Description |
|---|---|---|---|
| IN0+, IN0- , IN1+, IN1- | 1, 2, 3, 4 | I, LVDS | Inverting and non-inverting high speed LVDS input pins. |
| OUT0+, OUT0-, OUT1+, OUT1- | 12, 11, 10, 9 | O, LVDS | Inverting and non-inverting high speed LVDS output pins. |
| SEL0, SEL1 | 7, 8 | I, LVCMOS | Switch configuration pins. There is a 20k pulldown resistor on this pin. |
| EN0, EN1 | 14, 13 | I, LVCMOS | Output enable pins. There is a 20k pulldown resistor on this pin. |
| PE | 15 | I, LVCMOS | Transmit Pre-Emphasis select pin. There is a 20k pulldown resistor on this pin. |
| EQ | 6 | I, LVCMOS | Receive Equalization select pin. There is a 20k pulldown resistor on this pin. |
| VDD | 16 | Power | Power supply pin. |
| GND | 5, DAP | Power | Ground pin and Device Attach Pad (DAP) ground. |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings[1][2]

| | |
|---|---|
| Supply Voltage | −0.3V to +4V |
| LVCMOS Input Voltage | −0.3V to ($V_{CC}$ + 0.3V) |
| LVDS Input Voltage | −0.3V to +4V |
| Differential Input Voltage \|VID\| | 1.0V |
| LVDS Output Voltage | −0.3V to ($V_{CC}$ + 0.3V) |
| LVDS Differential Output Voltage | 0V to 1.0V |
| LVDS Output Short Circuit Current Duration | 5 ms |
| Junction Temperature | +150°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature Range | |
| Soldering (4 sec.) | +260°C |
| Maximum Package Power Dissipation at 25°C | |
| RGH0016A Package | 2.99W |
| Derate RGH0016A Package | 23.9 mW/°C above +25°C |
| Package Thermal Resistance | |
| $\theta_{JA}$ | +41.8°C/W |
| $\theta_{JC}$ | +6.9°C/W |
| ESD Susceptibility | |
| HBM [3] | ≥8 kV |
| MM [4] | ≥250V |
| CDM [5] | ≥1250V |

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

## Recommended Operating Conditions

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 3.0 | 3.3 | 3.6 | V |
| Receiver Differential Input Voltage ($V_{ID}$) | 0 | | 1 | V |
| Operating Free Air Temperature ($T_A$) | −40 | +25 | +85 | °C |

## DC Electrical Characteristics(1)(2)(3)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **LVCMOS DC SPECIFICATIONS** | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Low Level Input Voltage | | GND | | 0.8 | V |
| $I_{IH}$ | High Level Input Current | $V_{IN}$ = 3.6V<br>$V_{CC}$ = 3.6V | 40 | 175 | 250 | µA |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = GND<br>$V_{CC}$ = 3.6V | | 0 | ±10 | µA |
| $V_{CL}$ | Input Clamp Voltage | $I_{CL}$ = −18 mA, $V_{CC}$ = 0V | | −0.9 | −1.5 | V |
| **LVDS INPUT DC SPECIFICATIONS** | | | | | | |
| $V_{ID}$ | Input Differential Voltage | | 0 | | 1 | V |
| $V_{TH}$ | Differential Input High Threshold | $V_{CM}$ = +0.05V or $V_{CC}$-0.05V | | 0 | +100 | mV |
| $V_{TL}$ | Differential Input Low Threshold | | −100 | 0 | | mV |
| $V_{CMR}$ | Common Mode Voltage Range | $V_{ID}$ = 100 mV | 0.05 | | $V_{CC}$ - 0.05 | V |
| $I_{IN}$ | Input Current | $V_{IN}$ = +3.6V or 0V<br>$V_{CC}$ = 3.6V or 0V | | ±1 | ±10 | µA |
| $C_{IN}$ | Input Capacitance | Any LVDS Input Pin to GND | | 1.7 | | pF |
| $R_{IN}$ | Input Termination Resistor | Between IN+ and IN- | | 100 | | Ω |
| **LVDS OUTPUT DC SPECIFICATIONS** | | | | | | |
| $V_{OD}$ | Differential Output Voltage | $R_L$ = 100Ω | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in Magnitude of $V_{OD}$ for Complimentary Output States | | -35 | | 35 | mV |
| $V_{OS}$ | Offset Voltage | $R_L$ = 100Ω | 1.05 | 1.2 | 1.375 | V |
| $\Delta V_{OS}$ | Change in Magnitude of $V_{OS}$ for Complimentary Output States | | -35 | | 35 | mV |
| $I_{OS}$ | Output Short Circuit Current (4) | OUT to GND | | -35 | -55 | mA |
| | | OUT to $V_{CC}$ | | 7 | 55 | mA |
| $C_{OUT}$ | Output Capacitance | Any LVDS Output Pin to GND | | 1.2 | | pF |
| $R_{OUT}$ | Output Termination Resistor | Between OUT+ and OUT- | | 100 | | Ω |
| **SUPPLY CURRENT** | | | | | | |
| $I_{CC}$ | Supply Current | PE = OFF, EQ = OFF | | 77 | 90 | mA |
| $I_{CCZ}$ | Supply Current with Outputs Disabled | EN0 = EN1 = 0 | | 23 | 29 | mA |

(1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except $V_{OD}$ and $\Delta V_{OD}$.
(3) Typical values represent most likely parametric norms for $V_{CC}$ = +3.3V and $T_A$ = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
(4) Output short circuit current ($I_{OS}$) is specified as magnitude only, minus sign indicates direction only.

## AC Electrical Characteristics (1)

Over recommended operating supply and temperature ranges unless otherwise specified. (2) (3)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **LVDS OUTPUT AC SPECIFICATIONS** | | | | | | | |
| $t_{PLHD}$ | Differential Propagation Delay Low to High | $R_L$ = 100Ω | | | 365 | 500 | ps |
| $t_{PHLD}$ | Differential Propagation Delay High to Low | | | | 345 | 500 | ps |
| $t_{SKD1}$ | Pulse Skew $\|t_{PLHD} - t_{PHLD}\|$ (4) | | | | 20 | 55 | ps |
| $t_{SKD2}$ | Channel to Channel Skew (5) | | | | 12 | 25 | ps |
| $t_{SKD3}$ | Part to Part Skew , (6) | | | | 50 | 150 | ps |
| $t_{LHT}$ | Rise Time | $R_L$ = 100Ω | | | 65 | 120 | ps |
| $t_{HLT}$ | Fall Time | | | | 65 | 120 | ps |
| $t_{ON}$ | Output Enable Time | ENn = LH to output active | | | 7 | 20 | µs |
| $t_{OFF}$ | Output Disable Time | ENn = HL to output inactive | | | 5 | 12 | ns |
| $t_{SEL}$ | Select Time | SELn LH or HL to output | | | 3.5 | 12 | ns |
| **JITTER PERFORMANCE WITH EQ = Off, PE = Off (Figure 5)** | | | | | | | |
| $t_{RJ1}$ | Random Jitter (RMS Value) No Test Channels (7) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V Clock (RZ) | 2.5 Gbps | | 0.5 | 1 | ps |
| $t_{RJ2}$ | | | 3.125 Gbps | | 0.5 | 1 | ps |
| $t_{DJ1}$ | Deterministic Jitter (Peak to Peak) No Test Channels (8) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V K28.5 (NRZ) | 2.5 Gbps | | 6 | 22 | ps |
| $t_{DJ2}$ | | | 3.125 Gbps | | 6 | 22 | ps |
| $t_{TJ1}$ | Total Jitter (Peak to Peak) No Test Channels (9) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V PRBS-23 (NRZ) | 2.5 Gbps | | 0.03 | 0.08 | $UI_{P-P}$ |
| $t_{TJ2}$ | | | 3.125 Gbps | | 0.05 | 0.11 | $UI_{P-P}$ |
| **JITTER PERFORMANCE WITH EQ = Off, PE = On (Figure 6, Figure 9)** | | | | | | | |
| $t_{RJ1B}$ | Random Jitter (RMS Value) Test Channel B (7) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V Clock (RZ) | 2.5 Gbps | | 0.5 | 1 | ps |
| $t_{RJ2B}$ | | | 3.125 Gbps | | 0.5 | 1 | ps |
| $t_{DJ1B}$ | Deterministic Jitter (Peak to Peak) Test Channel B (8) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V K28.5 (NRZ) | 2.5 Gbps | | 3 | 12 | ps |
| $t_{DJ2B}$ | | | 3.125 Gbps | | 3 | 12 | ps |
| $t_{TJ1B}$ | Total Jitter (Peak to Peak) Test Channel B (9) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V PRBS-23 (NRZ) | 2.5 Gbps | | 0.03 | 0.06 | $UI_{P-P}$ |
| $t_{TJ2B}$ | | | 3.125 Gbps | | 0.04 | 0.09 | $UI_{P-P}$ |
| **JITTER PERFORMANCE WITH EQ = On, PE = Off (Figure 7, Figure 9)** | | | | | | | |
| $t_{RJ1D}$ | Random Jitter (RMS Value) Test Channel D (7) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V Clock (RZ) | 2.5 Gbps | | 0.5 | 1 | ps |
| $t_{RJ2D}$ | | | 3.125 Gbps | | 0.5 | 1 | ps |
| $t_{DJ1D}$ | Deterministic Jitter (Peak to Peak) Test Channel D (8) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V K28.5 (NRZ) | 2.5 Gbps | | 16 | 24 | ps |
| $t_{DJ2D}$ | | | 3.125 Gbps | | 12 | 24 | ps |

(1) Specification is guaranteed by characterization and is not tested in production.
(2) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
(3) Typical values represent most likely parametric norms for $V_{CC}$ = +3.3V and $T_A$ = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
(4) $t_{SKD1}$, $|t_{PLHD} - t_{PHLD}|$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) $t_{SKD2}$, Channel to Channel Skew, is the difference in propagation delay ($t_{PLHD}$ or $t_{PHLD}$) among all output channels in Broadcast mode (any one input to all outputs).
(6) $t_{SKD3}$, Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same $V_{CC}$ and within 5°C of each other within the operating temperature range.
(7) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
(8) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
(9) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

## AC Electrical Characteristics (1) (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (2) (3)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{TJ1D}$ | Total Jitter (Peak to Peak) Test Channel D (9) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V PRBS-23 (NRZ) | 2.5 Gbps | | 0.07 | 0.11 | $UI_{P-P}$ |
| $t_{TJ2D}$ | | | 3.125 Gbps | | 0.07 | 0.11 | $UI_{P-P}$ |
| **JITTER PERFORMANCE WITH EQ = On, PE = On (Figure 8, Figure 9)** | | | | | | | |
| $t_{RJ1BD}$ | Random Jitter (RMS Value) Input Test Channel D Output Test Channel B (7) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V Clock (RZ) | 2.5 Gbps | | 0.5 | 1 | ps |
| $t_{RJ2BD}$ | | | 3.125 Gbps | | 0.5 | 1 | ps |
| $t_{DJ1BD}$ | Deterministic Jitter (Peak to Peak) Input Test Channel D Output Test Channel B (8) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V K28.5 (NRZ) | 2.5 Gbps | | 14 | 31 | ps |
| $t_{DJ2BD}$ | | | 3.125 Gbps | | 6 | 21 | ps |
| $t_{TJ1BD}$ | Total Jitter (Peak to Peak) Input Test Channel D Output Test Channel B (9) | $V_{ID}$ = 350 mV $V_{CM}$ = 1.2V PRBS-23 (NRZ) | 2.5 Gbps | | 0.08 | 0.15 | $UI_{P-P}$ |
| $t_{TJ2BD}$ | | | 3.125 Gbps | | 0.10 | 0.16 | $UI_{P-P}$ |

## DC TEST CIRCUITS

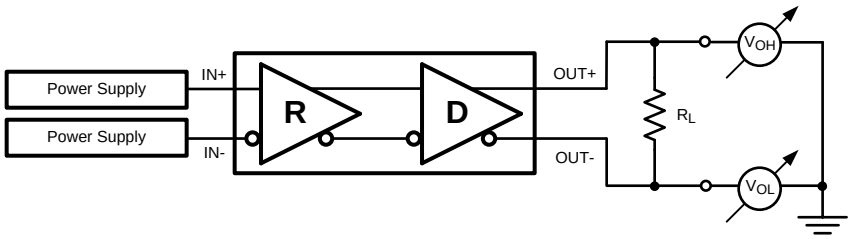



**Figure 1. Differential Driver DC Test Circuit**

## AC Test Circuits and Timing Diagrams

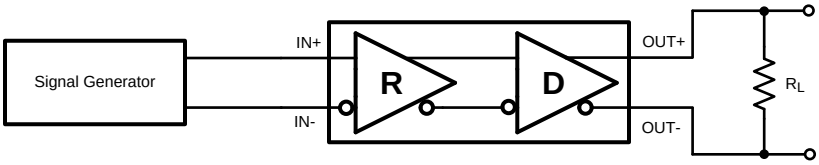



**Figure 2. Differential Driver AC Test Circuit**

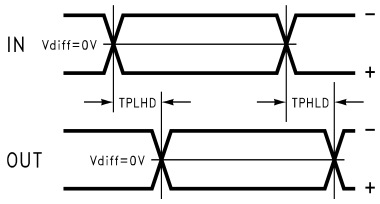



**Figure 3. Propagation Delay Timing Diagram**

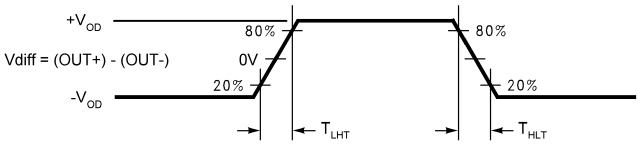



**Figure 4. LVDS Output Transition Times**

## Pre-Emphasis and Equalization Test Circuits

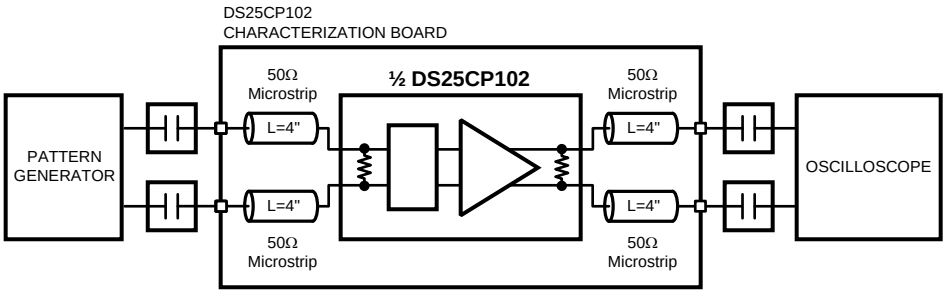



**Figure 5. Jitter Performance Test Circuit**

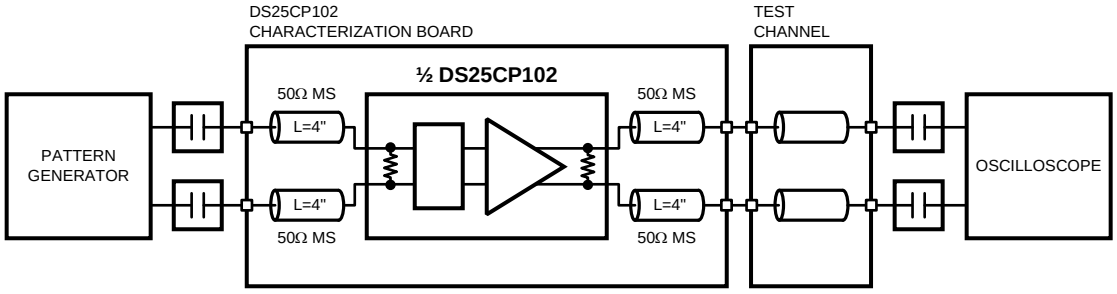



**Figure 6. Pre-Emphasis Performance Test Circuit**

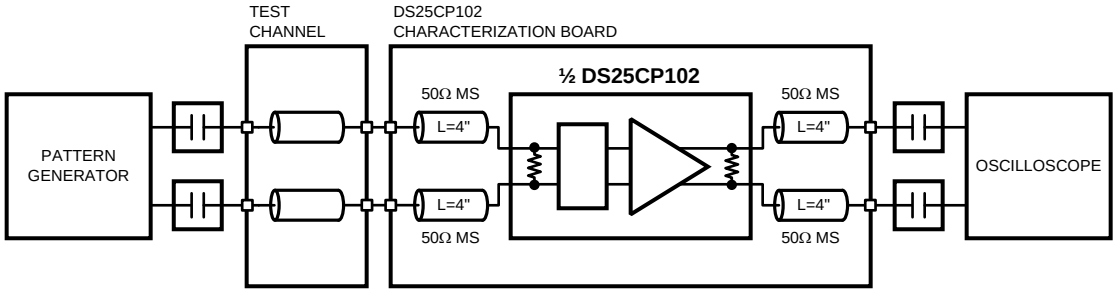



**Figure 7. Equalization Performance Test Circuit**

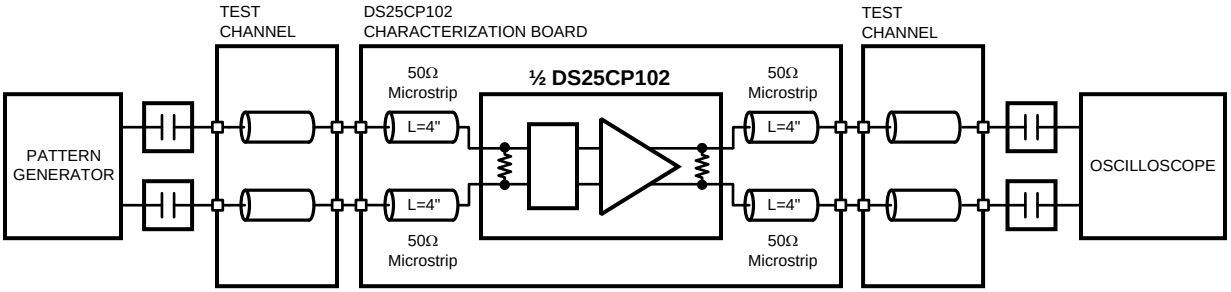



**Figure 8. Pre-Emphasis and Equalization Performance Test Circuit**

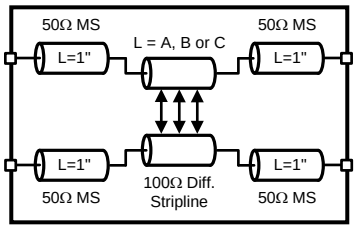



**Figure 9. Test Channel Block Diagram**

## Test Channel Loss Characteristics

The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

| Test Channel | Length (inches) | Insertion Loss (dB) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 500 MHz | 750 MHz | 1000 MHz | 1250 MHz | 1500 MHz | 1560 MHz |
| A | 10 | -1.2 | -1.7 | -2.0 | -2.4 | -2.7 | -2.8 |
| B | 20 | -2.6 | -3.5 | -4.1 | -4.8 | -5.5 | -5.6 |
| C | 30 | -4.3 | -5.7 | -7.0 | -8.2 | -9.4 | -9.7 |
| D | 15 | -1.6 | -2.2 | -2.7 | -3.2 | -3.7 | -3.8 |
| E | 30 | -3.4 | -4.5 | -5.6 | -6.6 | -7.7 | -7.9 |
| F | 60 | -7.8 | -10.3 | -12.4 | -14.5 | -16.6 | -17.0 |

## Functional Description

The DS25CP102 is a 3.125 Gbps 2x2 LVDS digital crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables.

**Table 1. Switch Configuration Truth Table**

| SEL1 | SEL0 | OUT1 | OUT0 |
|---|---|---|---|
| 0 | 0 | IN0 | IN0 |
| 0 | 1 | IN0 | IN1 |
| 1 | 0 | IN1 | IN0 |
| 1 | 1 | IN1 | IN1 |

**Table 2. Output Enable Truth Table**

| EN1 | EN0 | OUT1 | OUT0 |
|---|---|---|---|
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | Disabled | Enabled |
| 1 | 0 | Enabled | Disabled |
| 1 | 1 | Enabled | Enabled |

In addition, the DS25CP102 has a pre-emphasis control pin for switching the transmit pre-emphasis to ON and OFF setting and an equalization control pin for switching the receive equalization to ON and OFF setting. The following are the transmit pre-emphasis and receive equalization truth tables.

**Table 3. Transmit Pre-Emphasis Truth Table(1)**

| OUTPUTS OUT0 and OUT1 | |
|---|---|
| **CONTROL Pin (PE) State** | **Pre-Emphasis Level** |
| 0 | OFF |
| 1 | ON |

(1) Transmit Pre-Emphasis Level Selection

**Table 4. Receive Equalization Truth Table(1)**

| INPUTS IN0 and IN1 | |
|---|---|
| **CONTROL Pin (EQ) State** | **Equalization Level** |
| 0 | OFF |
| 1 | ON |

(1) Receive Equalization Level Selection

## Input Interfacing

The DS25CP102 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25CP102 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25CP102 inputs are internally terminated with a 100Ω resistor.

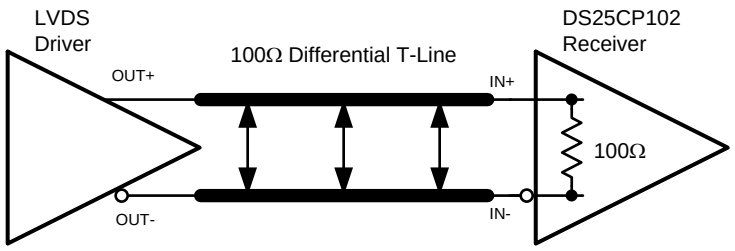



**Figure 10. Typical LVDS Driver DC-Coupled Interface to DS25CP102 Input**

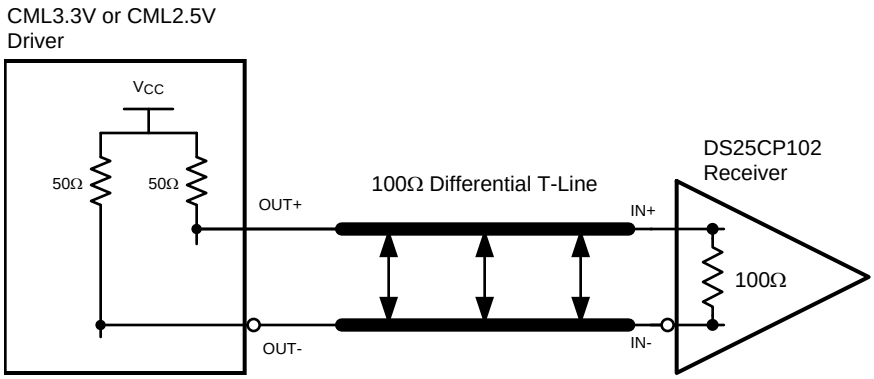



**Figure 11. Typical CML Driver DC-Coupled Interface to DS25CP102 Input**

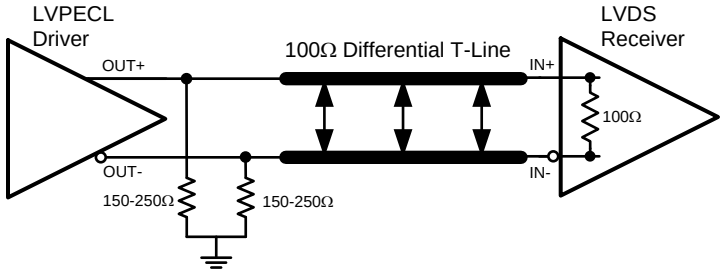



**Figure 12. Typical LVPECL Driver DC-Coupled Interface to DS25CP102 Input**

## Output Interfacing

The DS25CP102 outputs signals that are compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

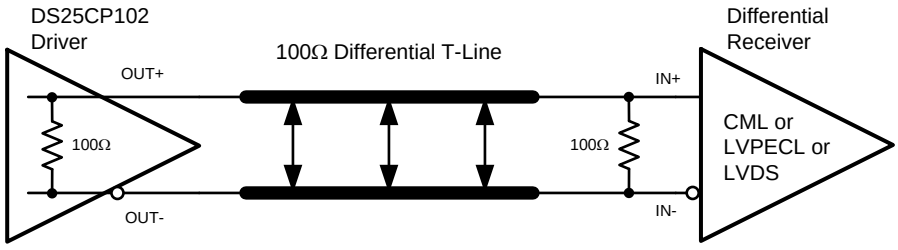



**Figure 13. Typical DS25CP102 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver**

## Typical Performance Characteristics

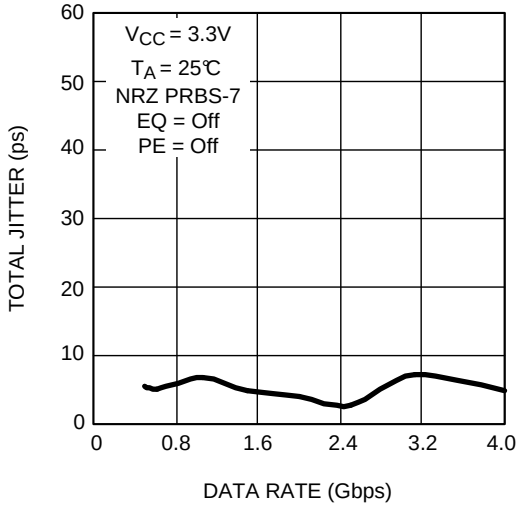



**Figure 14. Total Jitter as a Function of Data Rate**

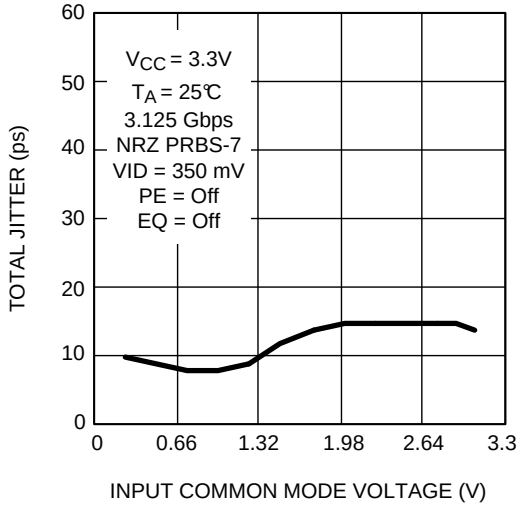



**Figure 15. Total Jitter as a Function of Input Common Mode Voltage**

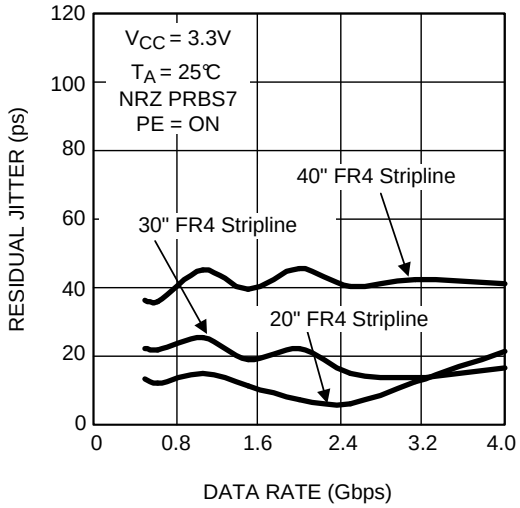



**Figure 16. Residual Jitter as a Function of Data Rate, FR4 Stripline Length and PE Level**

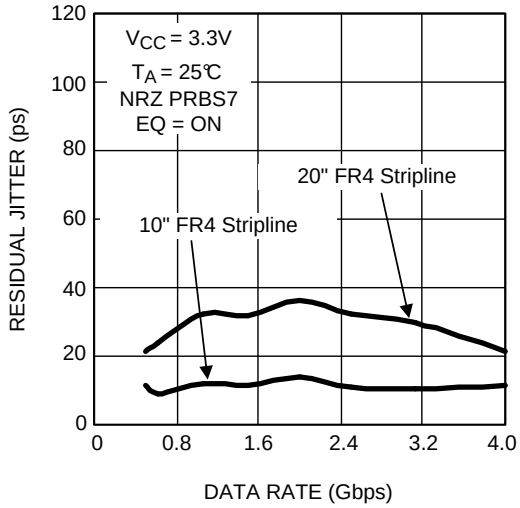



**Figure 17. Residual Jitter as a Function of Data Rate, FR4 Stripline Length and EQ Level**

## Typical Performance Characteristics (continued)

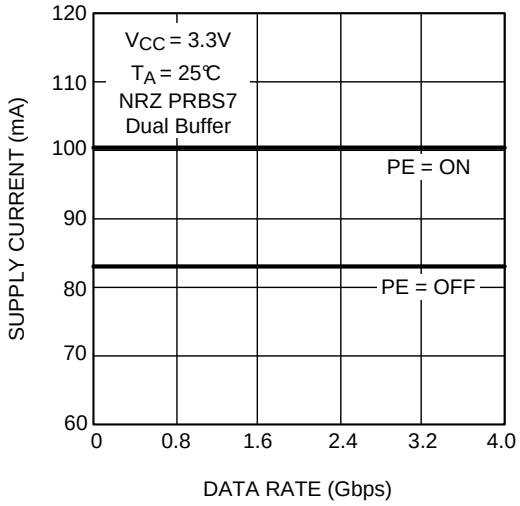



**Figure 18. Supply Current as a Function of Data Rate and PE Level**

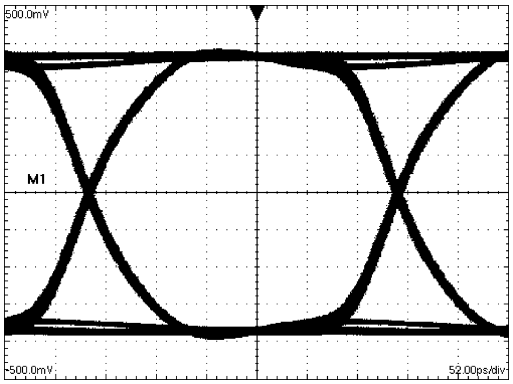



**Figure 19. A 3.125 Gbps NRZ PRBS-7 without PE or EQ After 2" Differential FR-4 Stripline H: 50 ps / DIV, V: 100 mV / DIV**

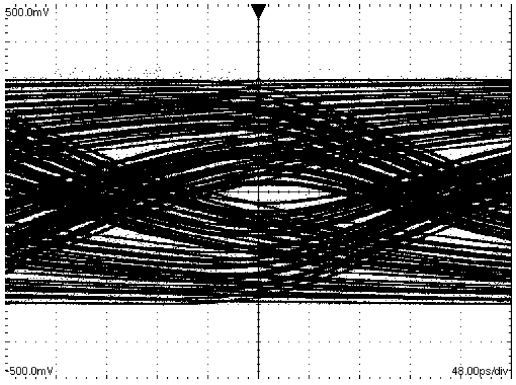



**Figure 20. A 3.125 Gbps NRZ PRBS-7 without PE or EQ After 40" Differential FR-4 Stripline H: 50 ps / DIV, V: 100 mV / DIV**

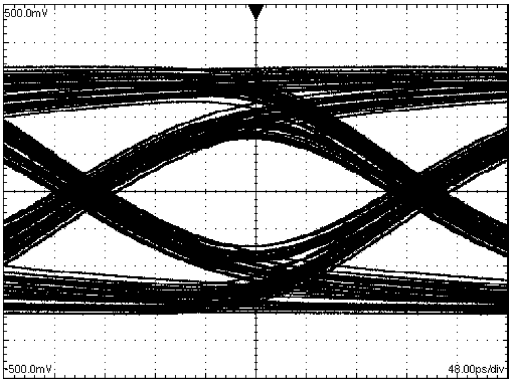



**Figure 21. A 3.125 Gbps NRZ PRBS-7 with PE After 40" Differential FR-4 Stripline H: 50 ps / DIV, V: 100 mV / DIV**

## REVISION HISTORY

| Changes from Revision D (March 2013) to Revision E | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 12 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DS25CP102TSQ/NOPB | ACTIVE | WQFN | RGH | 16 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | 2C102SQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

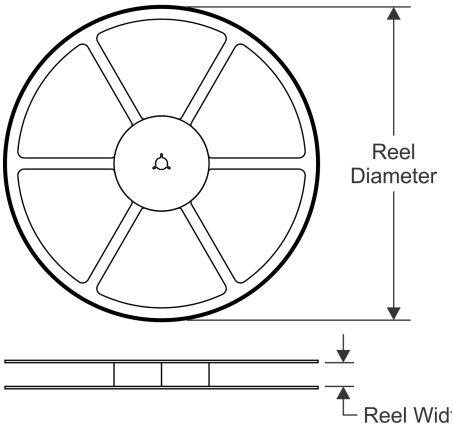
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

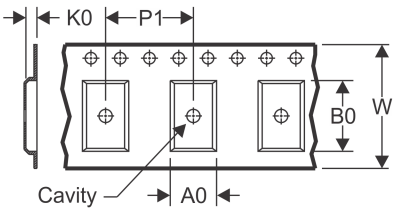
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

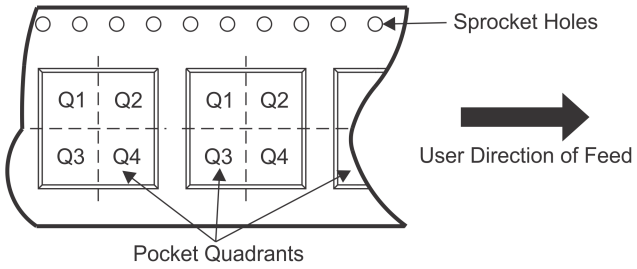



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

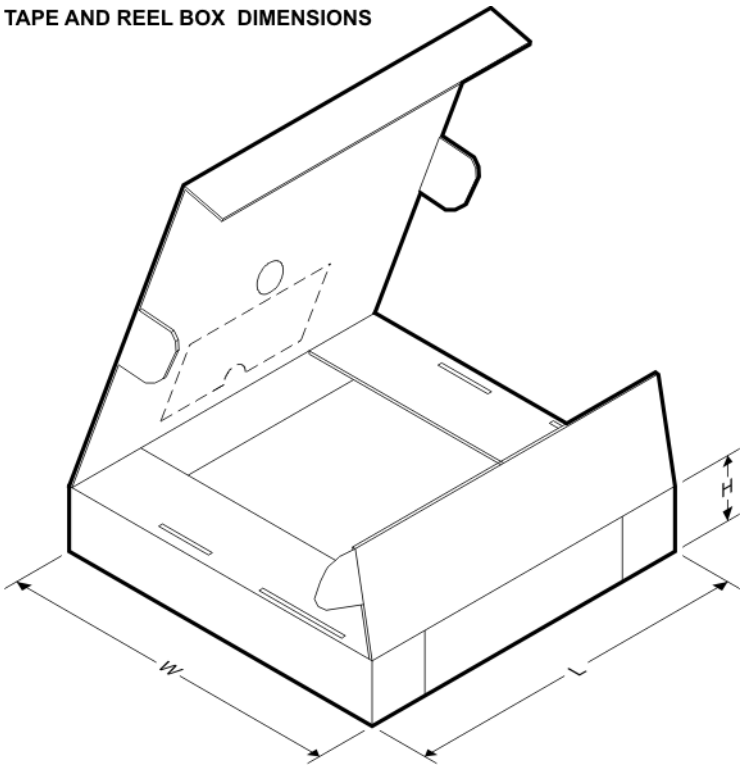
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

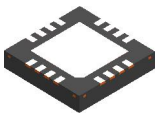
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS25CP102TSQ/NOPB | WQFN | RGH | 16 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

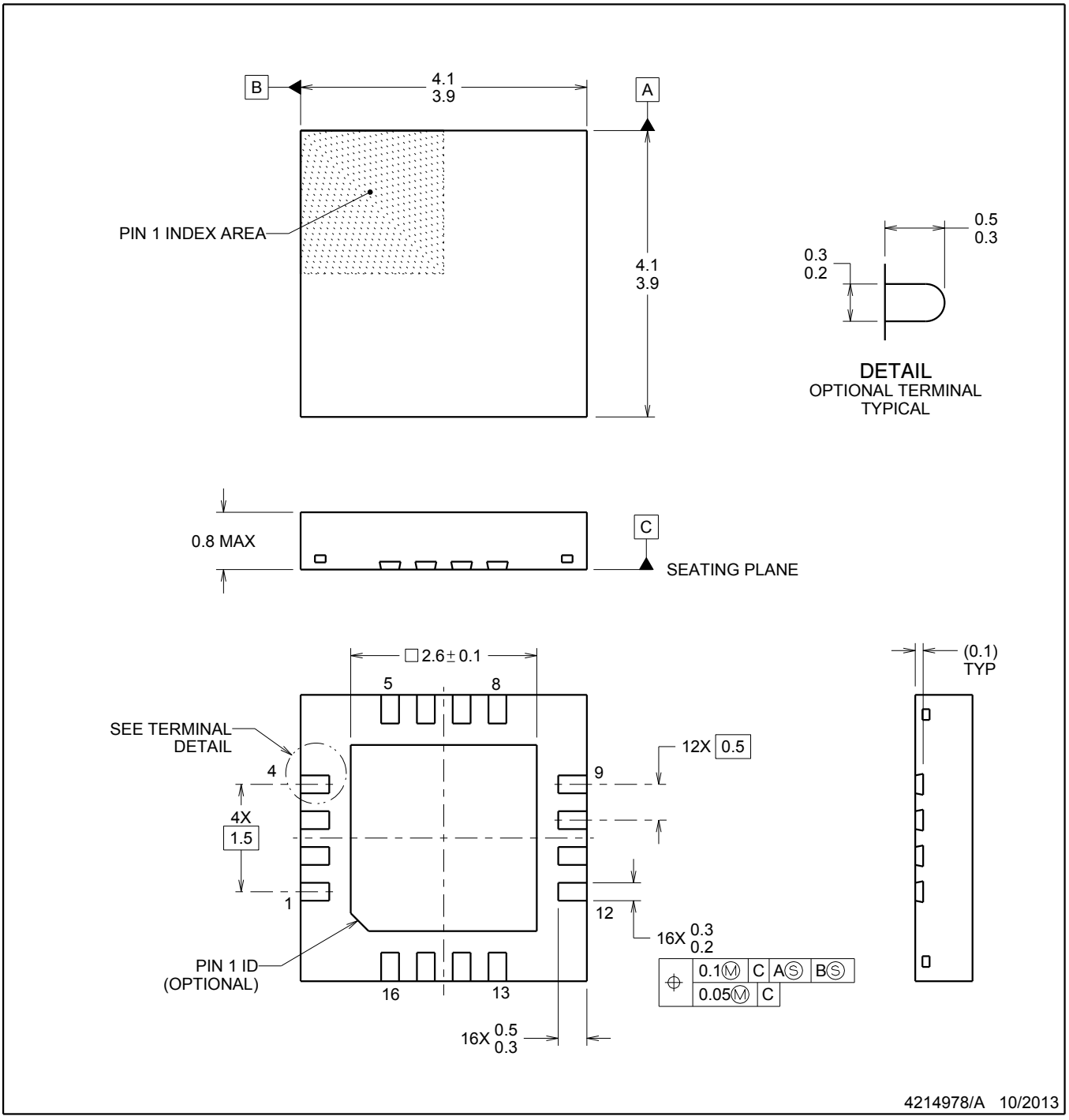
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DS25CP102TSQ/NOPB | WQFN | RGH | 16 | 1000 | 210.0 | 185.0 | 35.0 |



# RGH0016A

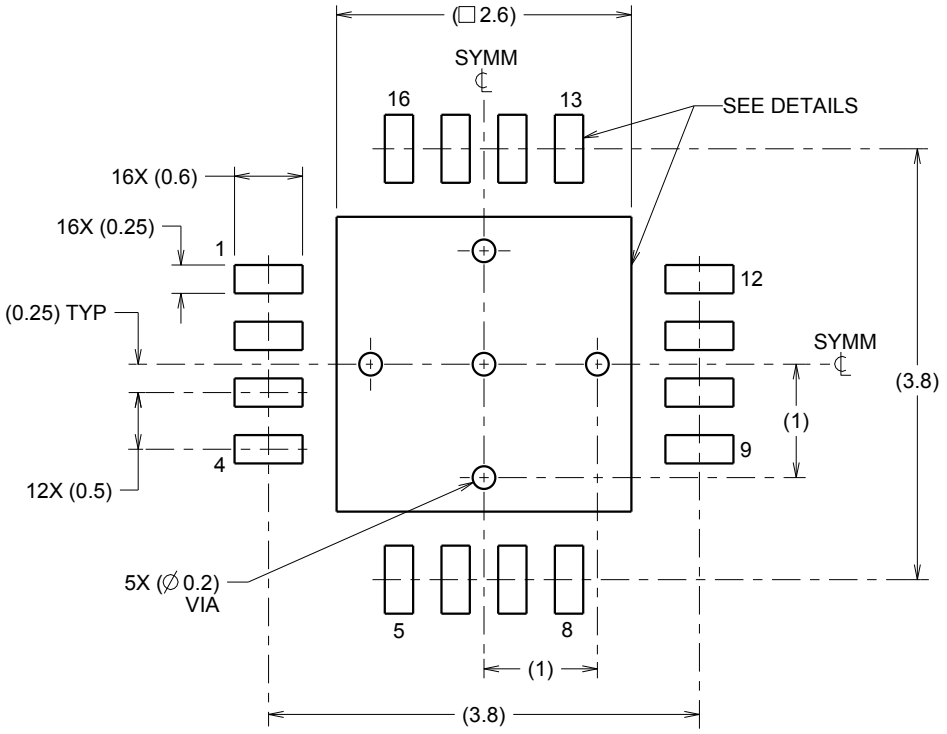
## WQFN - 0.8 mm max height

WQFN

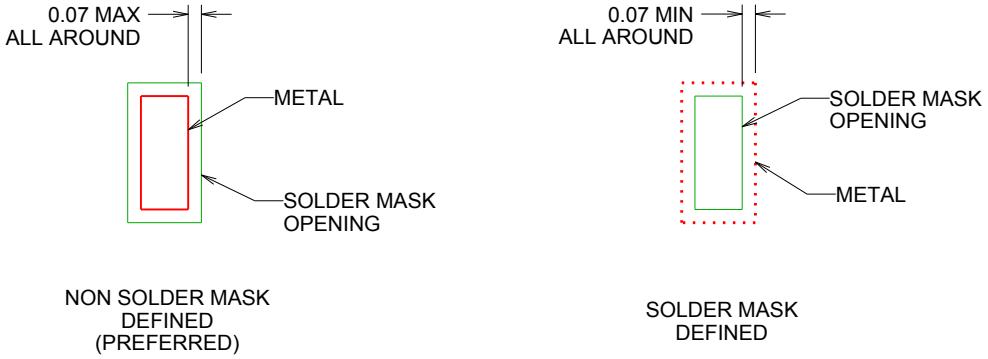



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:15X

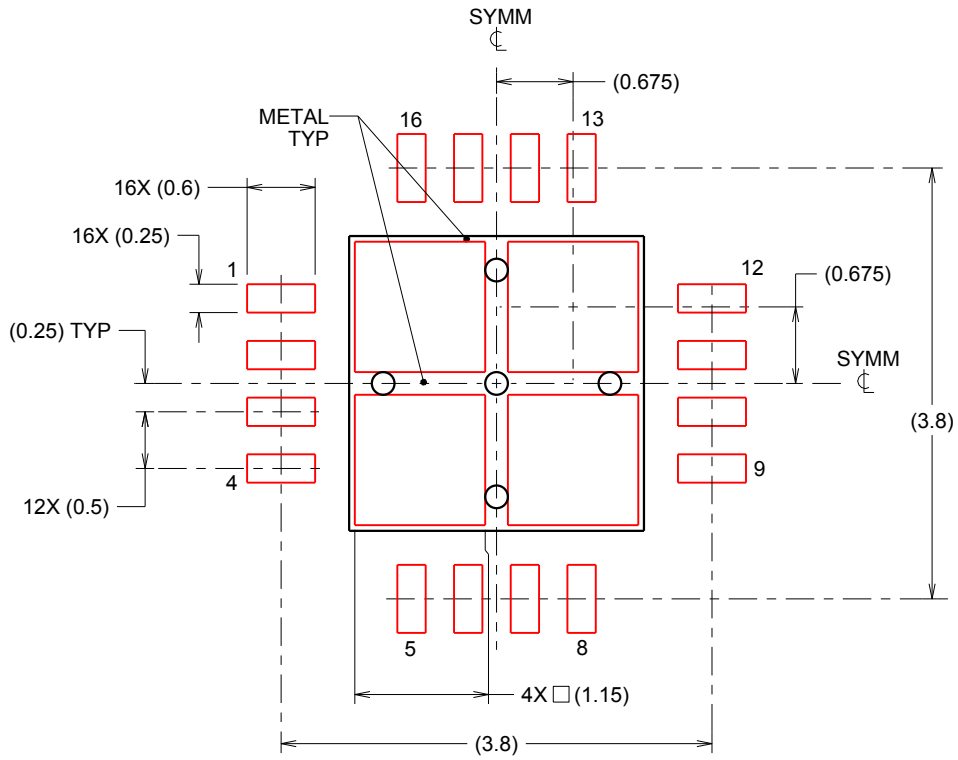



SOLDER MASK DETAILS

4214978/A 10/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4214978/A 10/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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