LM3280 Adjustable Step-Down DC-DC Converter and 3 LDOs for RF Power Management

Check for Samples: LM3280

FEATURES

- **2MHz (typ.) PWM Switching Frequency**
- **Operates from a Single Li-Ion Cell (2.7V to 5.5V)**
- **Adjustable Output Voltage (0.8V to 3.6V) DC-DC**
- **High-Efficiency Synchronous Buck Converter**
- **300mA Maximum Load Capability (PWM Mode)**
- **500mA Maximum Load Capability (Bypass mode)**
- **PWM, Forced and Automatic Bypass Mode**
- **3 Low-Dropout and Fast Transient Response LDOs**
- **16-pin DSBGA Package**
- **Current Overload Protection**
- **Thermal Overload Protection**

APPLICATIONS

- **Cellular Phones**
- **Hand-Held Radios**
- **Battery Powered RF Devices**

DESCRIPTION

The LM3280 is a multi-functional Power Management Unit, optimized for low-power handheld applications such as Cellular Phones.

The LM3280 incorporates three low-dropout LDO voltage regulators and one step down PWM DC-DC converter with an internal Bypass FET. The step down converter's output voltage can be set using an analog input (V_{CON}) for optimizing efficiency of the RF PA at various power levels. The LDO operates a nominal output voltage of 2.85V and maximum load current capability of 20mA for a reference voltage required by linear RF power amplifiers. The LM3280 additionally features a separate enable pin for each output.

The LM3280 is available in a 16-pin lead free DSBGA package.

Typical Application

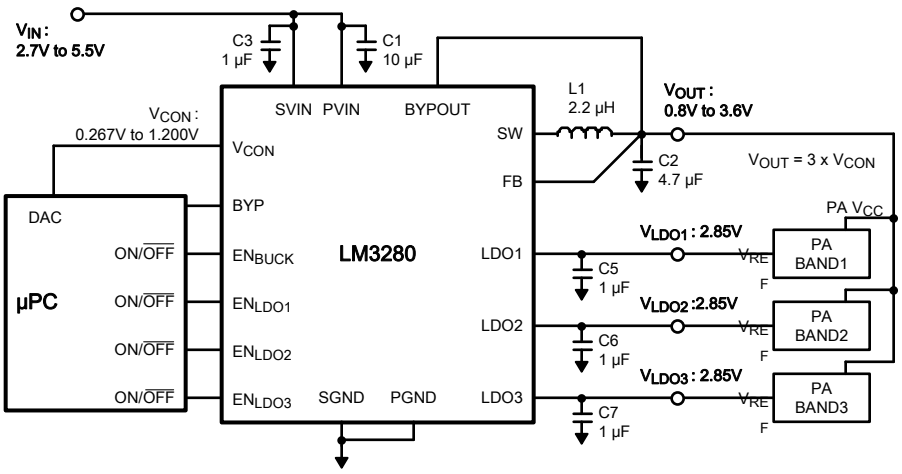
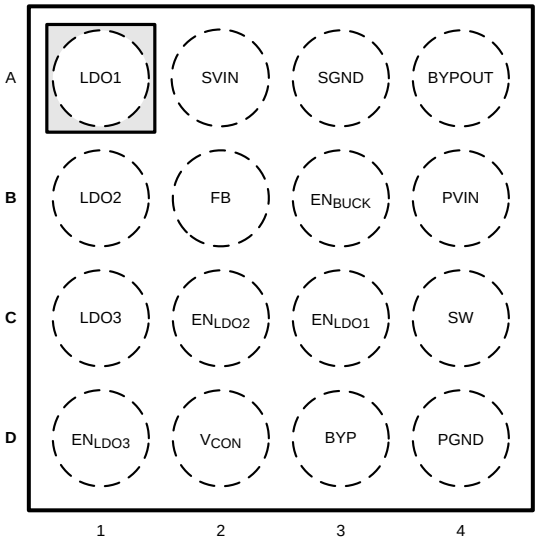


Figure 1. LM3280 Typical Application

Connection Diagrams



Top View

Figure 2. 16–Bump DSBGA Package, Large Bump
See Package Number YZR0016QQA

Pin Descriptions

Pin #	Name	Description
A1	LDO1	LDO1 Output.
B1	LDO2	LDO2 Output.
C1	LDO3	LDO3 Output.
D1	EN_{LDO3}	LDO3 Enable Input. Set this digital input high to turn on LDO3. (EN_{BUCK} pin must be also set high.) For turning LDO3 off, set low.
A2	SVIN	Analog, Signal, and LDO Supply Input.
B2	FB	Buck Converter Feedback Analog Input. Connect to the output at the output filter capacitor.
C2	EN_{LDO2}	LDO2 Enable Input. Set this digital input high to turn on LDO2. (EN_{BUCK} pin must be also set high.) For turning LDO2 off, set low.
D2	V_{CON}	Buck Converter Voltage Control Analog Input. This pin controls V_{OUT} in PWM mode. Set: V_{OUT} = 3 x $V_{CON.}$ Do not leave floating.
A3	SGND	Analog, Signal, and LDO Ground.
B3	EN_{BUCK}	Buck Converter Enable Input. Set this digital input high after Vin >2.7V for normal operation. For shutdown, set low.
C3	EN_{LDO1}	LDO1 Enable Input. Set this digital input high to turn on LDO1. (EN_{BUCK} pin must be also set high.) For turning LDO1 off, set low.
D3	BYP	Forced Bypass Input. Use this digital input to command operation in Bypass mode. Set BYP low (<0.4V) for normal operation.
A4	BYPOUT	Bypass FET Drain. Connect to the output capacitor. Do not leave floating.
B4	PVIN	Buck Converter Power Supply Voltage Input to the internal PFET switch and Bypass FET.
C4	SW	Buck Converter Switch Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit of the PWM Buck Converter.
D4	PGND	Buck Converter Power Ground.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

SVIN, PVIN to SGND	−0.2V to +6.0V
PGND to SGND	−0.2V to +0.2V
ENs, FB, BYP, V_{CON}	(SGND −0.2V) to (SVIN +0.2V) w/6.0V max
SW, BYPOUT	(PGND −0.2V) to (PVIN +0.2V) w/6.0V max
PVIN to SVIN	−0.2V to +0.2V
Continuous Power Dissipation (3)	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec.)	+260°C
ESD Rating (4) Human Body Model Machine Model	 2k V 200 V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 125°C (typ.).
(4) The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200pF capacitor discharged directly into each pin. National Semiconductor recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper ESD handling techniques can result in damage.

Operating Ratings (1) (2)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	
PWM Mode:	0mA to 300mA
Bypass Mode:	0mA to 500mA
LDO:	0mA to 20mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range (3)	−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) Shutdown current includes leakage current of PFET and Bypass FET.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), DSBGA Package (1)	48 °C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from thermal measurements, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. A 1" x 1", 4 layer, 1.5oz. Cu board was used for the measurements. The θ_{JA}, which is performed under the 4 layer cellphone board condition, is 86°C/W.

General Electrical Characteristics(1)(2)(3)

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +85°C$). Unless otherwise noted, specifications apply to the LM3280 with: V_{IN} = (SVIN = PVIN =) 3.6V, EN_{BUCK} = 3.6V, $EN_{LDO1} = EN_{LDO2} = EN_{LDO3}$ = BYP = 0V, FB = 2V, V_{CON} = 0.267V.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_Q	Shutdown Supply Current	EN_{BUCK} = 0V, FB = SW = V_{CON} = 0V, BYPOUT = 0V		0.1	**3**	µA
	No Load Supply Current	EN_{BUCK} = 3.6V, BYPOUT = 0V		720	**800**	µA
		EN_{BUCK} = 3.6V, BYPOUT = 0V, EN_{LDO1} = 3.6V		920	**1300**	µA
		EN_{BUCK} = BYP = 3.6V		720	**800**	µA
		EN_{BUCK} = BYP = 3.6V, EN_{LDO1} = 3.6V		920	**1300**	µA
V_{IH}	Logic High Input Threshold Voltage for ENx, BYP	FB = 0V	**1.2**			V
V_{IL}	Logic Low Input Threshold Voltage for ENx, BYP	FB = 0V			**0.4**	V
I_{PDWN}	Logic Input Pull Down Current for ENx, BYP	ENx, BYP = 3.6V		5	**10**	µA
THSD	Thermal Shutdown Temperature	(2)		150		°C
	Hysteresis Temperature	(2)		25		°C

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(3) The LM3280 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.

Buck Electrical Characteristics(1)(2)(3)

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +85°C$). Unless otherwise noted, specifications apply to the LM3280 with: V_{IN} = (SVIN = PVIN =) 3.6V, EN_{BUCK} = 3.6V, $EN_{LDO1} = EN_{LDO2} = EN_{LDO3}$ = BYP = 0V, FB = 2V, V_{CON} = 0.267V.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{FB_MIN}	Feedback Voltage at Minimum Setting	V_{CON} = 0.267V	**0.75**	0.800	**0.85**	V
V_{FB_MAX}	Feedback Voltage at Maximum Setting	V_{CON} = 1.20V, V_{IN} = 4.2V	**3.528**	3.600	**3.672**	V
OVP	Over-Voltage Protection Threshold	(4)		330	400	mV
$V_{BYPASS-}$	Auto Bypass Detection Negative Threshold	(5)	160	250	320	mV
$V_{BYPASS+}$	Auto Bypass Detection Positive Threshold	(5)	350	450	540	mV
$R_{DSON\ (P)}$	Pin-Pin Resistance for PFET	I_{SW} = 500mA, FB = 0V		320	**450**	mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for N-FET	I_{SW} = - 200mA		310	**450**	mΩ
$R_{DSON\ (BYP)}$	Pin-Pin Resistance for Bypass FET	I_{BYPOUT} = 500mA		85	**120**	mΩ

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(3) Shutdown current includes leakage current of PFET and Bypass FET.
(4) Over-Voltage protection (OVP) threshold is the voltage above the nominal V_{OUT} where the OVP comparator turns off the PFET switch while in PWM mode.
(5) SVIN is compared to the programmed output voltage (V_{OUT}). When SVIN – V_{OUT} falls below $V_{BYPASS-}$ for longer than T_{BYP} the Bypass FET turns on and the switching FETs turn off. This is called the Bypass mode. The device comes out of Bypass mode when SVIN – V_{OUT} exceeds V_{BYPASS}^+ for longer than T_{BYP}, and PWM mode returns. The hysteresis for the bypass detection threshold V_{BYPASS}^+ – $V_{BYPASS-}$ will always be positive and will be approximately 200mV (typ.).

Buck Electrical Characteristics[1][2][3] (continued)

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +85°C$). Unless otherwise noted, specifications apply to the LM3280 with: V_{IN} = (SVIN = PVIN =) 3.6V, EN_{BUCK} = 3.6V, $EN_{LDO1} = EN_{LDO2} = EN_{LDO3}$ = BYP = 0V, FB = 2V, V_{CON} = 0.267V.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
$I_{LIM-PWM}$	Switch Current Limit	FB = 0V [6]	**700**	820	**940**	mA
$I_{LIM-BYP}$	Bypass FET Current Limit	[7]	**800**	1000	**1200**	mA
F_{OSC}	Internal Oscillator Frequency		**1.8**	2	**2.2**	MHz
Gain	V_{CON} to V_{OUT} Gain	$0.267V \le V_{CON} \le 1.20V$, V_{IN} = 4.2V		3		V/V
I_{CON}	V_{CON} Input Leakage Current	V_{CON} = 1.2V		10		nA

(6) Electrical Characteristic table reflects open loop data (FB = 0V and current drawn from SW pin ramped up until cycle by cycle current limit is activated). Refer to datasheet curves for closed loop data and its variation with regards to supply voltage and temperature. Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.
(7) The current is defined as the load current at which the BYPOUT voltage is 1V lower than PVIN.

Buck System Characteristics[1][2]

The following spec table entries are guaranteed by design if the component values in the typical application circuit are used. **These parameters are not guaranteed by production testing.**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{RESPONSE}$	Time for V_{OUT} to Rise from 0.8V to 3.4V in PWM Mode	V_{IN} = 4.2V, C_{OUT} = 4.7µF, R_{LOAD} = 15Ω, L = 2.2 µH (I_{SAT} > 0.94A)		25		µs
$T_{STARTUP}$	Time for V_{OUT} to rise to 3.4V in PWM Mode [3]	V_{IN} = 4.2V, C_{OUT} = 4.7µF, R_{LOAD} = 15Ω, L = 2.2µH (I_{SAT} = 0.94A), EN = Low to High		36		µs
C_{CON}	V_{CON} Input Capacitance	V_{IN} = 3.6V, V_{CON} = 1V, Test Freq. = 100kHz			15	pF
T_{ON_BYP}	Bypass FET Turn On Time In Bypass Mode	V_{IN} = 3.6V, V_{CON} = 0.267V, C_{OUT} = 4.7µF, R_{LOAD} = 15Ω, BYP = Low to High			30	µs
T_{BYP}	Auto Bypass Detect Delay Time	[4]	10	15	20	µs

(1) All voltages are with respect to the potential at the GND pins.
(2) Shutdown current includes leakage current of PFET and Bypass FET.
(3) The startup time is the time to reach 90% of 3.4V nominal output voltage from the EN_{BUCK} being low to high.
(4) SVIN is compared to the programmed output voltage (V_{OUT}). When SVIN – V_{OUT} falls below $V_{BYPASS-}$ for longer than T_{BYP} the Bypass FET turns on and the switching FETs turn off. This is called the Bypass mode. The device comes out of Bypass mode when SVIN – V_{OUT} exceeds V_{BYPASS}^+ for longer than T_{BYP}, and PWM mode returns. The hysteresis for the bypass detection threshold $V_{BYPASS}^+ - V_{BYPASS}-$ will always be positive and will be approximately 200mV (typ.).

LDO1, 2, and 3 Electrical Characteristics[1][2]

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +85°C$). Unless otherwise noted, specifications apply to the LM3280 with: V_{IN} = 3.6V, EN_{BUCK} = 3.6V, BYP = 0V, FB = 2V, V_{CON} = 0.267V, EN_{LDOx} = 3.6V [3].

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{LDO}	LDO Output Voltage Accuracy	V_{LDO} = 2.85V, I_{OUT} = 1mA	-1 **-2**		+1 **+2**	% %
ΔV_{LDO}	Line Regulation	$V_{IN} = V_{LDO(nom)}$ + 0.5V to 5.5V, I_{OUT} = 1mA		0.1		%/V
	Load Regulation	I_{OUT} = 1mA to 20mA		0.01	**0.04**	%/mA

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(3) The EN_{LDOx} means that the one of EN_{LDO1}, EN_{LDO2}, and EN_{LDO3} is set high (> 1.2V) and the others are set 0V.

LDO1, 2, and 3 Electrical Characteristics(1)(2) (continued)

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +85°C$). Unless otherwise noted, specifications apply to the LM3280 with: V_{IN} = 3.6V, EN_{BUCK} = 3.6V, BYP = 0V, FB = 2V, V_{CON} = 0.267V, EN_{LDOx} = 3.6V (3).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LIM_LDO}	LDO Current Limit	(4)	**30**	40	**55**	mA
I_{PU}	Pull-Up Current	(4)	**40**	60	**80**	mA
R_{PD}	Pull-Down Resistance	I_{OUT} = -50mA, EN_{BUCK} = all EN_{LDO} = 0V	**10**	13.5	**17**	Ω
V_{DROP}	Dropout Voltage	I_{OUT} = 20mA (5)		70	**115**	mV

(4) The current is defined as the load current at which the LDOx voltage is 1.0V lower than the nominal output voltage.
(5) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100mV below the nominal voltage.

LDO1, 2, and 3 System Characteristics(1)

The following spec table entries are guaranteed by design if the component values in the typical application circuit are used. Unless otherwise noted, specifications apply to the LM3280 with: V_{IN} = 3.6V. **These parameters are not guaranteed by production testing.**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PSRR	Power Supply Ripple Rejection Ratio	Test Freq. = 1KHz, V_{RIPPLE} = 0.5Vpp C_{OUT} = 1µF, I_{OUT} = 1mA, BYP = V_{IN}		55		dB
T_{LDO_ON}	Time to reach 90% of $V_{LDO(nom)}$ after EN_{LDO} signal goes high.	V_{IN} = EN_{BUCK} = 3V, C_{OUT} = 1µF, EN_{LDOx} = Low to High, R_{LOAD} = 270Ω		50	100	µs
		V_{IN} = 3V, C_{OUT} = 1µF, EN_{BUCK} = EN_{LDOx} = Low to High, R_{LOAD} = 270Ω		80	130	µs
T_{LDO_OFF}	Time to reach 0.1V of V_{LDO} after EN_{LDO} signal goes low.	V_{IN} = 3V, C_{OUT} = 1µF, EN_{LDOx} = High to Low, I_{OUT} = 0mA		50	200	µs

(1) All voltages are with respect to the potential at the GND pins.

Typical Performance Characteristics

(V_{IN} = EN_{BUCK} = 3.6V, EN_{LDOx} = BYP = 0V, T_A = 25°C, unless otherwise noted)

Quiescent Current vs Supply Voltage (V_{CON} = 0.267V, FB = 2V, No Switching, LDO Disabled)

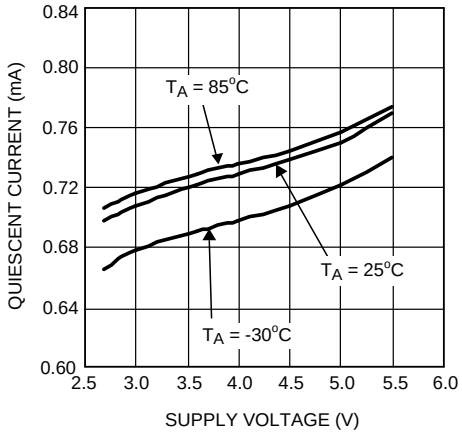


Figure 3.

Quiescent Current vs Supply Voltage (V_{CON} = 0.267V, FB = 2V, No Switching, LDO Enabled)

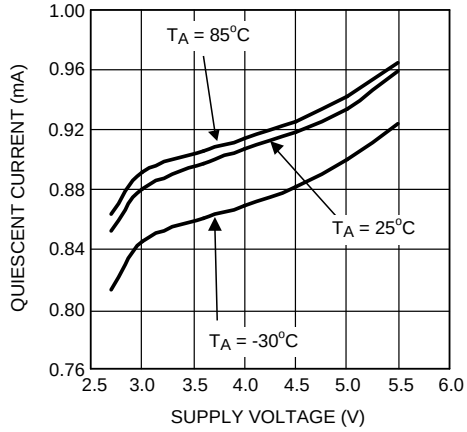


Figure 4.

Shutdown Current vs Temperature (all EN = BYPOUT = V_{CON} = SW = FB = 0V)

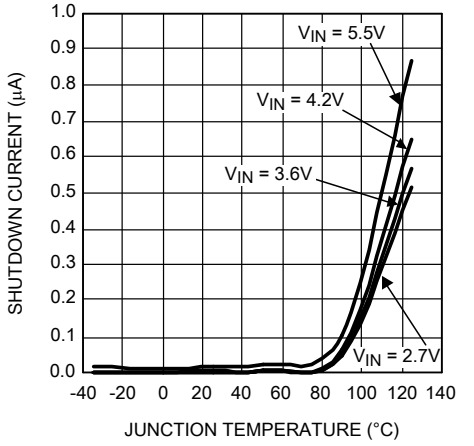


Figure 5.

LDO Line Transient Response (R_{LOAD} = 270Ω, C_{OUT} = 1µF)

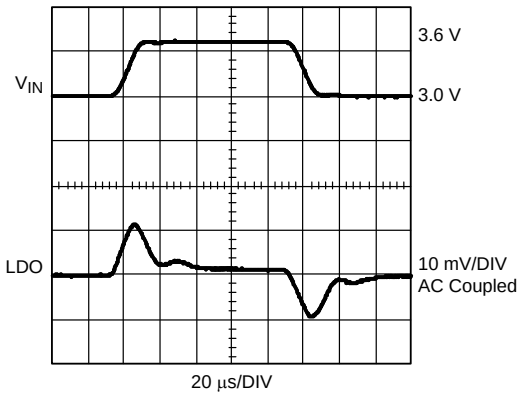


Figure 6.

LDO Turn ON (EN_{LDO} = Low to High)

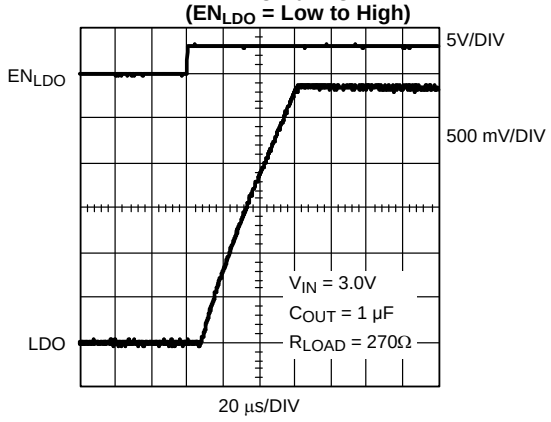


Figure 7.

LDO Turn ON (EN_{BUCK} = EN_{LDO} = Low to High)

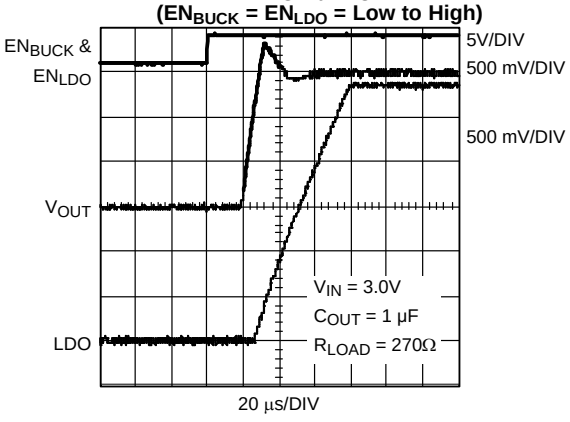


Figure 8.

Typical Performance Characteristics (continued)

(V_{IN} = EN_{BUCK} = 3.6V, EN_{LDOx} = BYP = 0V, T_A = 25°C, unless otherwise noted)

LDO Turn OFF (EN_{LDO} = High to Low)

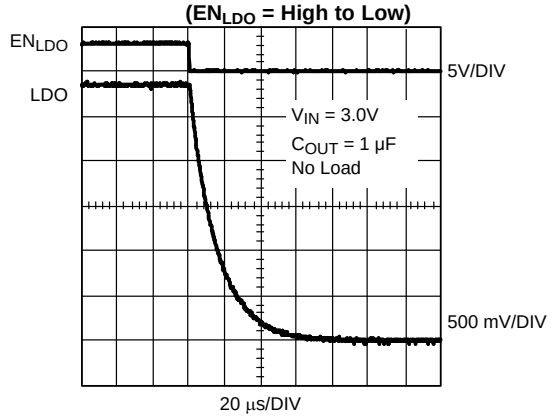


Figure 9.

LDO Load Transient Response (C_{OUT} = 1µF)

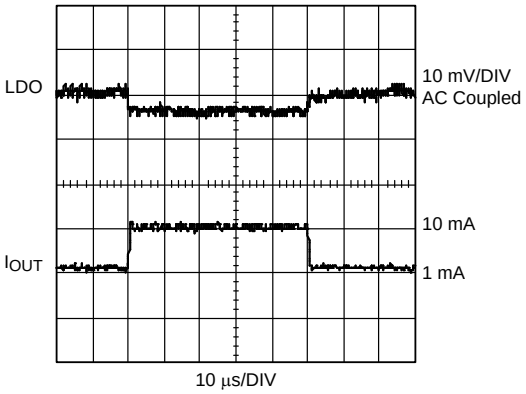


Figure 10.

LDO Voltage vs Supply Voltage

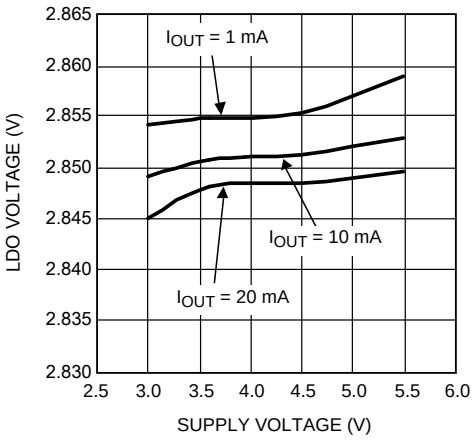


Figure 11.

LDO Voltage vs Temperature

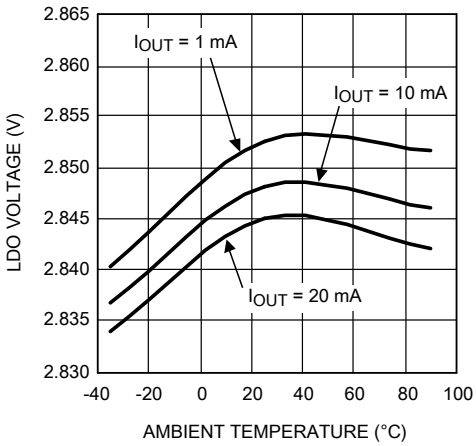


Figure 12.

LDO Dropout Voltage vs Output Current

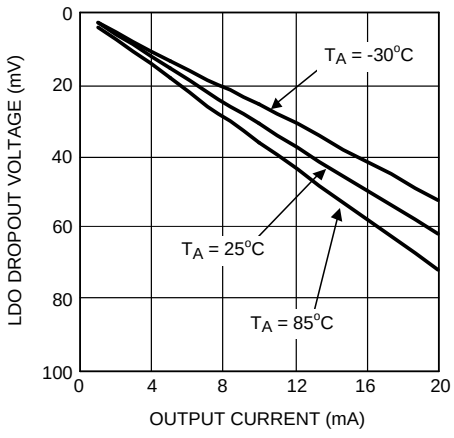


Figure 13.

LDO Voltage vs Output Current (V_{IN} = 3.6V)

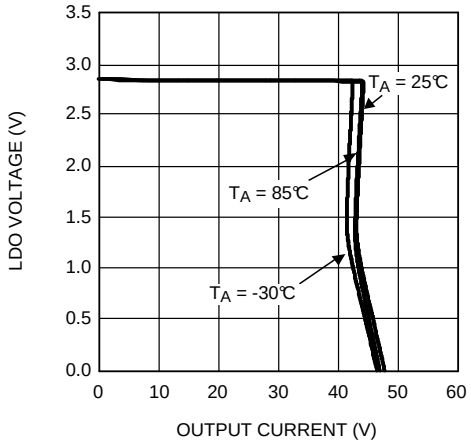


Figure 14.

Typical Performance Characteristics (continued)

(V_{IN} = EN_{BUCK} = 3.6V, EN_{LDOx} = BYP = 0V, T_A = 25°C, unless otherwise noted)

PWM Startup (V_{CON} = 1.13V)

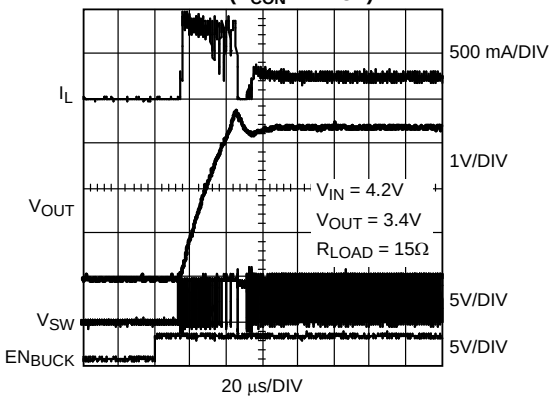


Figure 15.

PWM Shutdown Response (V_{CON} = 1.08V)

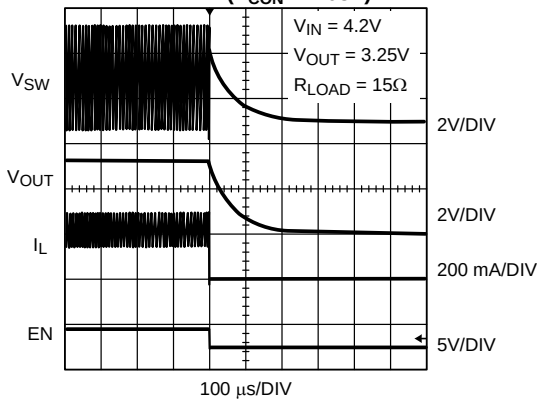


Figure 16.

Automatic Bypass Operation (V_{IN} = 4.2V to 3.0V)

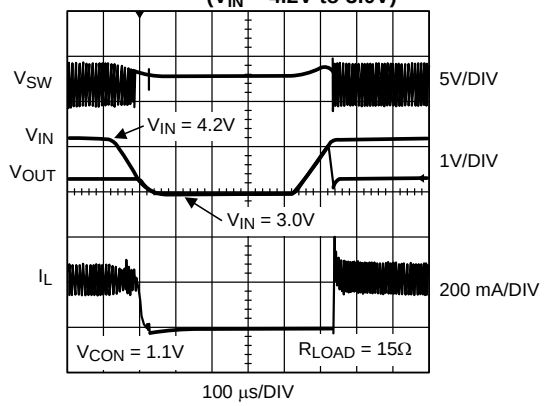


Figure 17.

Forced Bypass Operation (V_{IN} = 3.0V)

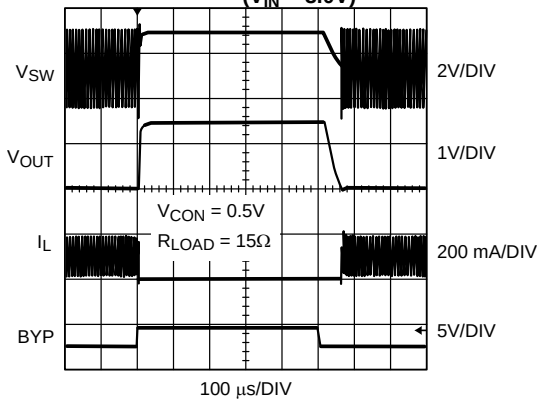


Figure 18.

Line Transient Response (V_{IN} = 3.0V to 3.6V)

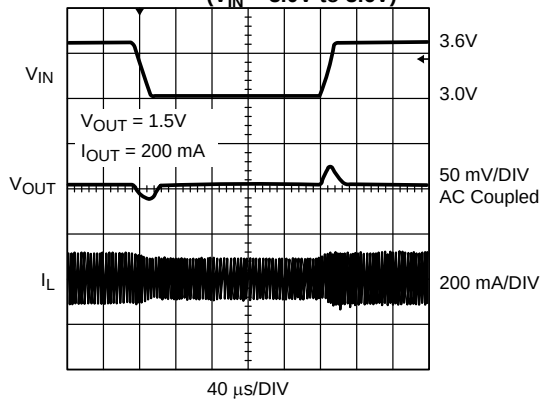


Figure 19.

Load Transient Response (V_{CON} = 0.5V)

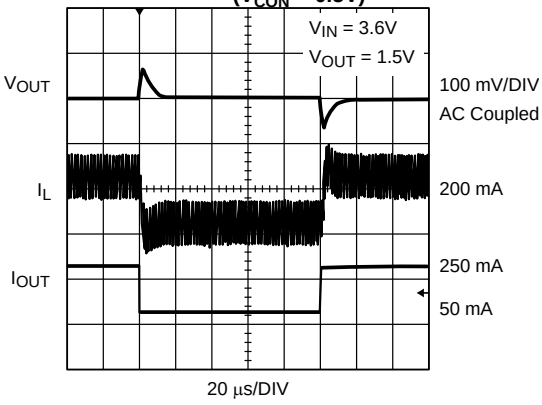


Figure 20.

Typical Performance Characteristics (continued)

(V_{IN} = EN_{BUCK} = 3.6V, EN_{LDOx} = BYP = 0V, T_A = 25°C, unless otherwise noted)

V_{CON} Voltage Response
(V_{IN} = 4.2V, V_{CON} = 0.5V / 1.1V)

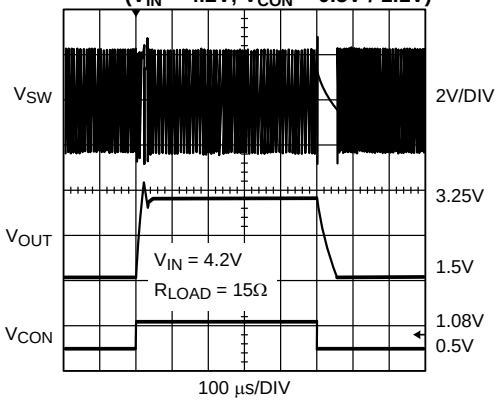


Figure 21.

Timed Current Limit Response
(Normal Operation to Short Circuit)

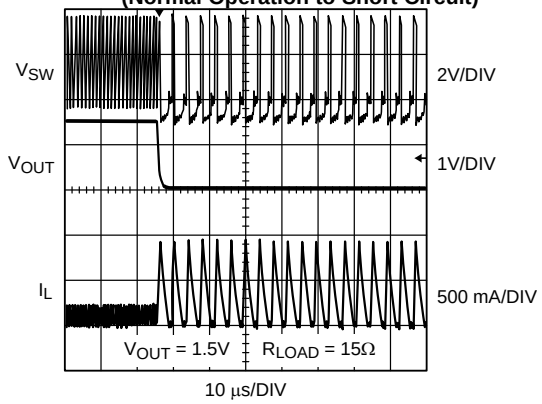


Figure 22.

Output Voltage Ripple
(V_{OUT} = 1.5V)

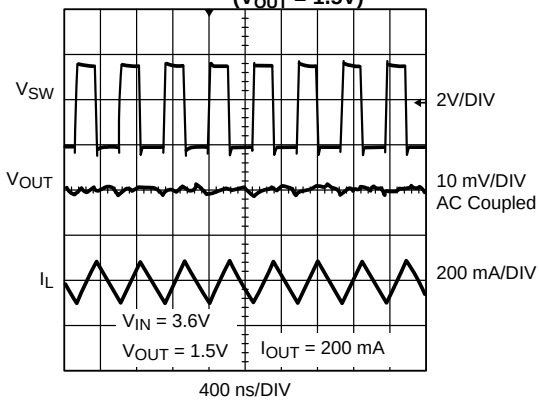


Figure 23.

Output Voltage Ripple in Dropout
(V_{IN} = 3.75V, V_{OUT} = 3.25V, I_{OUT} = 200mA)

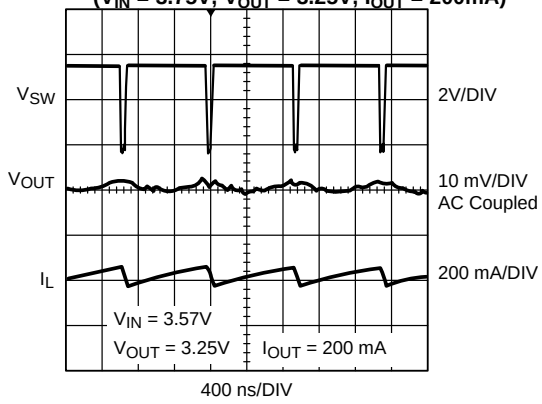


Figure 24.

Switching Frequency Variation
vs
Temperature (V_{OUT} = 1.5V)

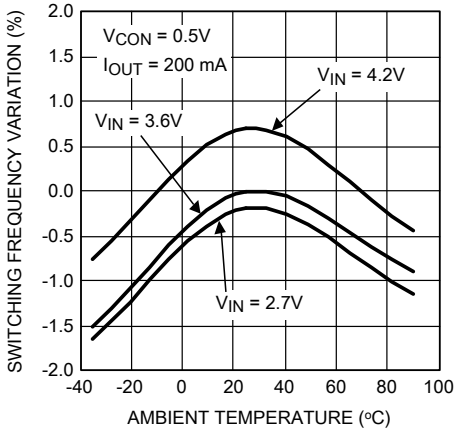


Figure 25.

R_{DSON}
vs
Temperature (Bypass FET)

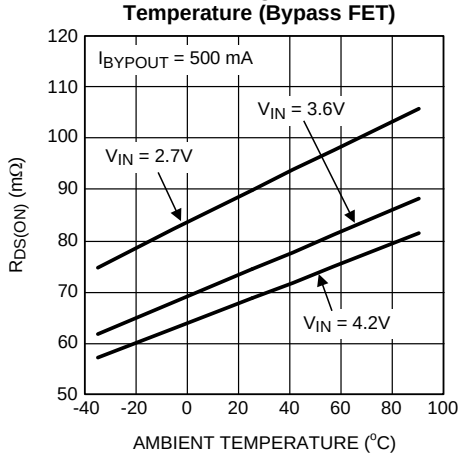


Figure 26.

Typical Performance Characteristics (continued)

(V_{IN} = EN_{BUCK} = 3.6V, EN_{LDOx} = BYP = 0V, T_A = 25°C, unless otherwise noted)

R_{DSON} vs Temperature (P-FET)

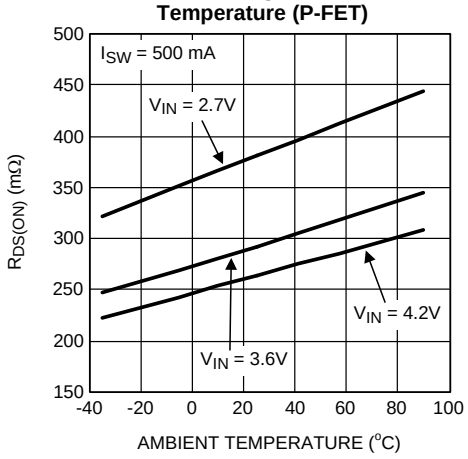


Figure 27.

R_{DSON} vs Temperature (N-FET)

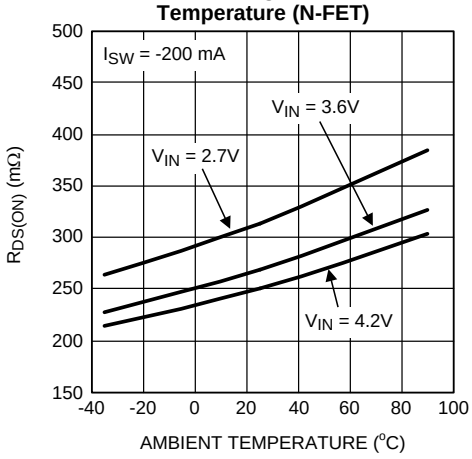


Figure 28.

PWM Output Voltage vs Supply Voltage (V_{OUT} = 1.5V)

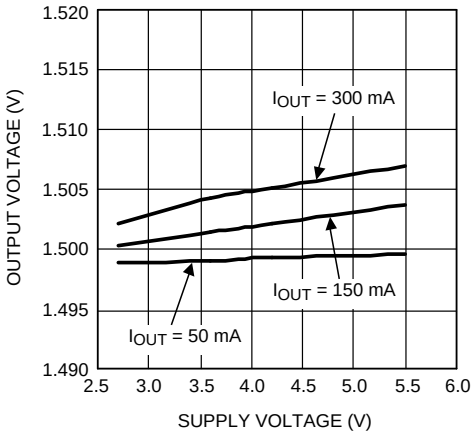


Figure 29.

PWM Output Voltage vs Temperature (V_{OUT} = 1.5V)

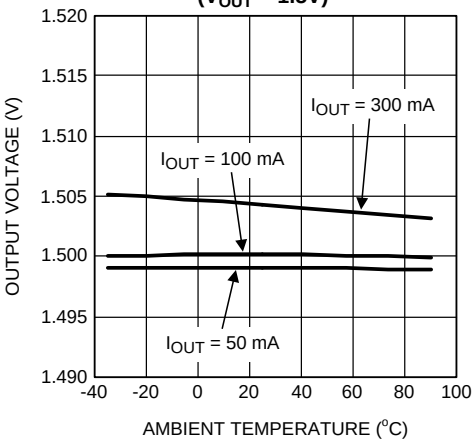


Figure 30.

Typical Performance Characteristics (continued)

(V_{IN} = EN_{BUCK} = 3.6V, EN_{LDOx} = BYP = 0V, T_A = 25°C, unless otherwise noted)

Open/Closed Loop Current Limit vs Temperature (PWM mode)

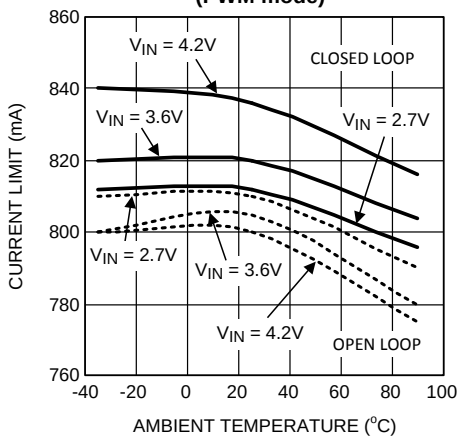


Figure 31.

Dropout Voltage vs Output Current (Bypass mode, V_{IN} = BYP = 3.6V)

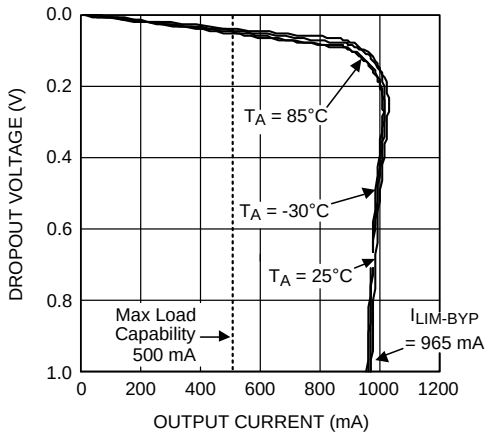


Figure 32.

V_{CON} Voltage vs PWM Output Voltage (I_{OUT} = 200mA)

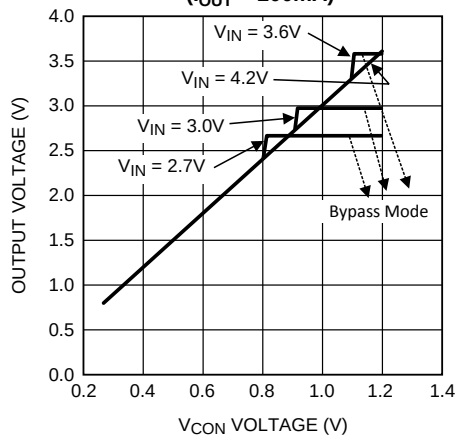


Figure 33.

Low V_{CON} Voltage vs Output Voltage (R_{LOAD} = 15Ω)

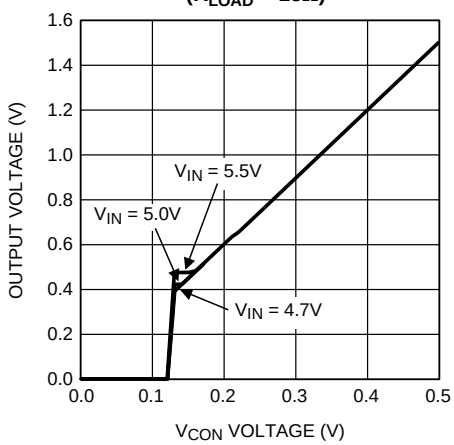


Figure 34.

Typical Performance Characteristics (continued)

(V_{IN} = EN_{BUCK} = 3.6V, EN_{LDOx} = BYP = 0V, T_A = 25°C, unless otherwise noted)

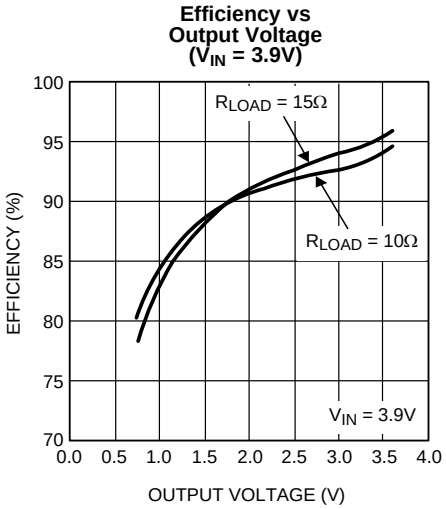


Figure 35.

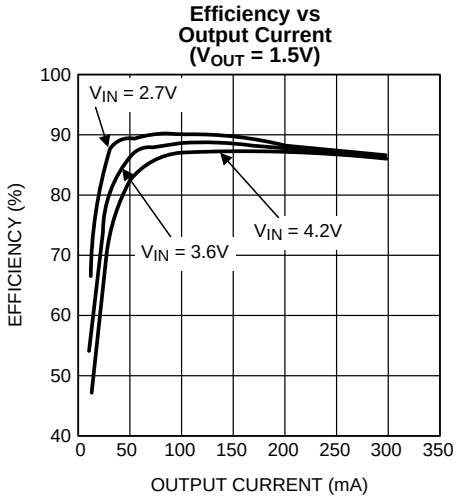


Figure 36.

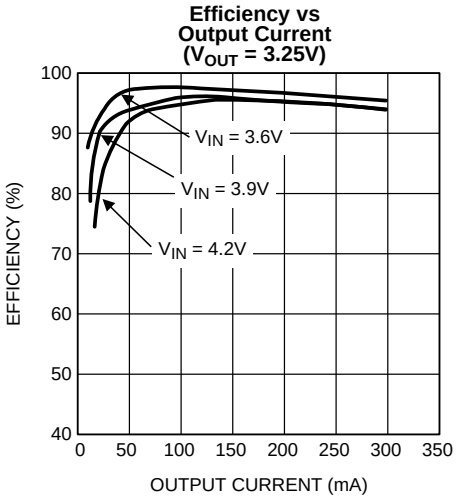


Figure 37.

BLOCK DIAGRAM

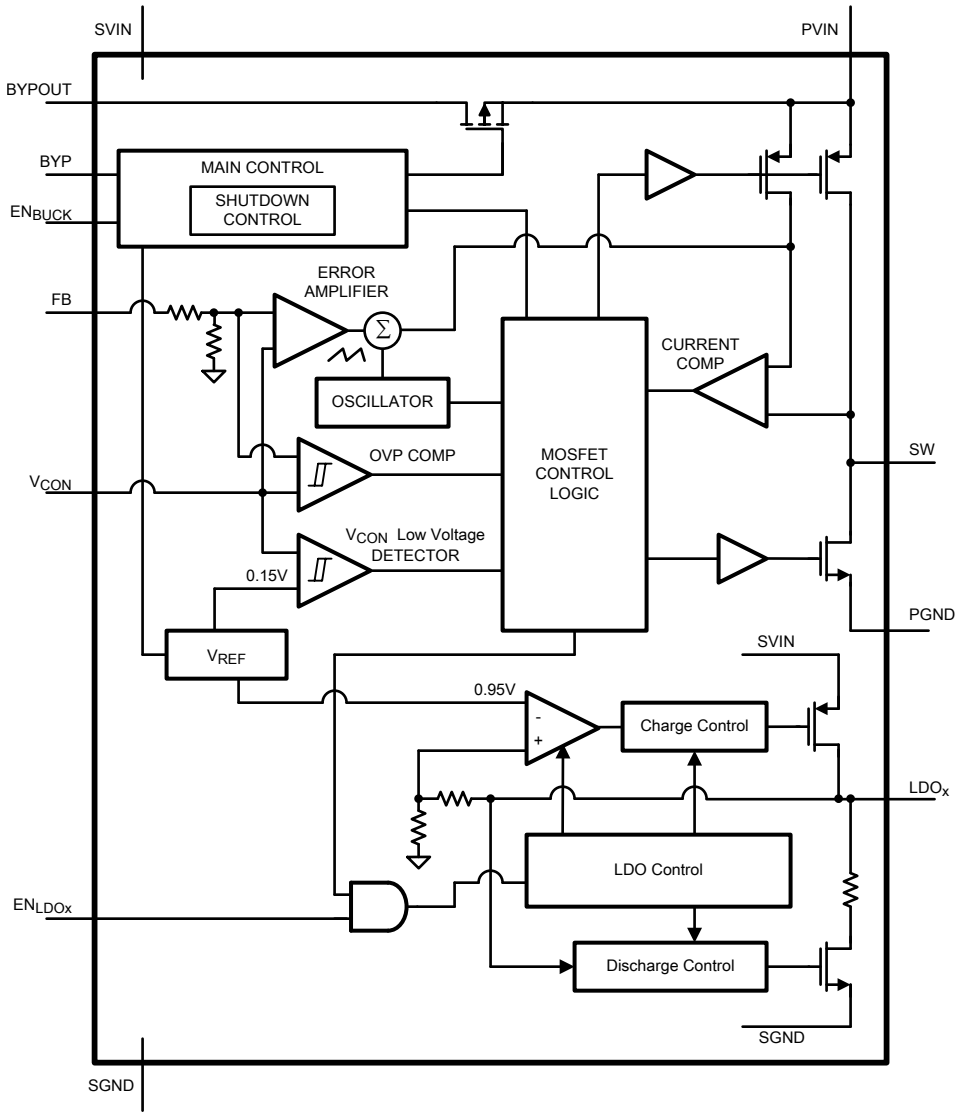


Figure 38. Functional Block Diagram

DEVICE INFORMATION

The LM3280 a multi-functional Power Management Unit, optimized for low-power handheld applications such as Cellular Phones. It incorporates one adjustable voltage PWM DC-DC converter with an internal Bypass FET and three LDOs. It also provides a separate enable pin for each output. The buck converter output voltage can be programmed from 0.8V to 3.6V in PWM mode. The buck converter is designed for a maximum load capability of 300mA in PWM mode and 500mA in Bypass mode. Maximum load range may vary from this depending on input voltage, output voltage and the inductor chosen. The LDO operates a nominal output voltage of 2.85V and maximum load current capability of 20mA.

The buck converter is designed to allow the RF PA (Power Amplifier) to operate at maximum efficiency over a wide range of power levels from a single Li-Ion battery cell. It is based on current-mode buck architecture, with synchronous rectification for high efficiency. It has three of pin-selectable operating modes. Fixed-frequency PWM operation offers regulated output at high efficiency while minimizing interference with sensitive IF and data acquisition circuits. Bypass mode (Forced or Automatic) turns on an internal FET bypass switch to power the PA directly from the battery. This helps the RF PA maintain its operating power during low battery conditions by reducing the dropout voltage across the buck converter. Shutdown mode turns the device off and reduces battery consumption to 0.1µA (typ.).

DC PWM mode output voltage precision is +/-2% for $3.6V_{OUT}$. Efficiency is typically around 96% for a 120mA load with 3.2V output, 3.6V input. PWM mode quiescent current is 0.72mA typ. The output voltage is dynamically programmable from 0.8V to 3.6V by adjusting the voltage on the control pin (V_{CON}) without the need for external feedback resistors.

An LDO is used to provide a regulated 2.85V reference voltage supply to each RF PA. Since each LDO has its own enable pin, it can be used to enable or disable its respective PA. The LDO can be enabled only after the buck converter is activated. The LDO will automatically be disabled whenever the EN_{BUCK} or EN_{LDOx} is disabled. Single LDO must be turned on at the same time. Each LDO provides an active charge circuit. The LDO output is pulled to ground potential via an internal resistor when the EN_{BUCK} or EN_{LDOx} pin is low.

Additional features include current overload protection and thermal shutdown. The buck converter also provides over voltage protection.

The LM3280 is constructed using a chip-scale 16-pin DSBGA package. This package offers the smallest possible size, for space-critical applications such as cell phones, where board area is an important design consideration. Use of a DSBGA package requires special design considerations for implementation. (See DSBGA PACKAGE ASSEMBLY AND USE.) Its fine bump-pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also, the system controller should set EN_{BUCK} low during power-up and other low supply voltage conditions. (See Shutdown Mode.)

Buck Converter

CIRCUIT OPERATION

Referring to Figure 1 and Figure 38, the buck converter operates as follows. During the first part of each switching cycle, the control block in the buck converter turns on the internal PFET (P-channel MOSFET) switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around $(V_{IN} - V_{OUT}) / L$, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET (N-channel MOSFET) synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around V_{OUT} / L. The output filter capacitor stores charge when the inductor current is going high, and releases it when inductor current is going low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM MODE

While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency (2MHz typ.) and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse width to control the peak inductor current. This is done by comparing the PFET drain current to a slope-compensated reference current generated by the error amplifier. At the beginning of each cycle, the clock turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator turns off the PFET switch and turns on the NFET synchronous rectifier, ending the first part of the cycle. If an increase in load pulls the output down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET. This increases the average current sent to the output and adjusts for the increase in the load. The minimum on-time of PFET in PWM mode is 50ns (typ.).

BYPASS MODE

The buck converter contains an internal PFET switch for bypassing the PWM DC-DC converter during Bypass mode. In Bypass mode, this PFET is turned on to power the PA directly from the battery for maximum RF output power. Bypass mode is more efficient than operating in PWM mode at 100% duty cycle because the resistance of the bypass PFET is less than the series resistance of the PWM PFET and inductor. This translates into higher voltage available on the output in Bypass mode, for a given battery voltage. The part can be placed in bypass mode by sending BYP pin high. This is called Forced Bypass Mode and it remains in bypass mode until BYP pin goes low.

Alternatively the part can go into Bypass mode automatically. This is called Auto-bypass mode or Automatic Bypass mode. The bypass switch turns on when the difference between the input voltage and programmed output voltage is less than 250mV (typ.) for more than the bypass delay time of 15µs (typ.). The bypass switch turns off when the input voltage is higher than the programmed output voltage by 450mV (typ.) for longer than the bypass delay time. The bypass delay time is provided to prevent false triggering into Automatic Bypass mode by either spikes or dips in V_{IN}. This method is very system resource friendly in that the Bypass PFET is turned on automatically when the input voltage gets close to the output voltage, typical scenario of a discharging battery. It is also turned off automatically when the input voltage rises, typical scenario of a charger connected. Another scenario could be changes made to V_{CON} voltage causing Bypass PFET to turn on and off automatically. It is recommended to connect BYPOUT pin directly to the output capacitor with a separate trace and not to the FB pin.

OPERATING MODE SELECTION CONTROL

The BYP digital input pin is used to select between PWM/Auto-bypass and Bypass operating mode. Setting BYP pin high (>1.2V) places the device in Forced Bypass mode. Setting BYP pin low (<0.4V) or leaving it floating places the device in PWM/Auto-bypass mode.

Bypass and PWM operation overlap during the transition between the two modes. This transition time is approximately 31µs when changing from PWM to Bypass mode, and 15µs when changing from Bypass to PWM mode. This helps prevent under or overshoots during the transition period between PWM and Bypass modes.

DYNAMICALLY ADJUSTABLE OUTPUT VOLTAGE

The LM3280 buck converter features dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.8V to 3.6V by changing the voltage on the analog V_{CON} pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances, the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life. See BUCK CONVERTER SETTING THE OUTPUT VOLTAGE for further details.

OVER VOLTAGE PROTECTION

The buck converter has an over voltage comparator that prevents the output voltage from rising too high, when the device is left in PWM mode under light-load conditions, during output voltage steps, or during startup. When the output voltage rises to 330mV over its target, the OVP comparator inhibits PWM operation to skip pulses until the output voltage returns to the target. During the over voltage protection mode, both the PWM PFET and the NFET synchronous rectifier are off. When the part comes out of the over voltage protection mode, the NFET synchronous rectifier remains off for approximately 3.5µs to avoid inductor current going negative.

INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the buck converter uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

With medium and heavy loads, the internal NFET synchronous rectifier is turned on during the inductor current down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. There is no zero cross detect, which means that the NFET can conduct current in both directions and inductor current is always continuous. The advantage of this method is that the part remains in PWM mode at light loads or no load conditions. The NFET has a current limit. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

CURRENT LIMITING

A current limit feature allows the buck converter to protect itself and external components during overload conditions. In PWM mode, a 940mA (max.) cycle-by-cycle current limit is normally used. If an excessive load pulls the output voltage down to below approximately 0.375V, indicating a possible short to ground, then the device switches to a timed current limit mode. In timed current limit mode, the internal PFET switch is turned off after the current comparator trips, and the beginning of the next cycle is inhibited for 3.5µs to force the instantaneous inductor current to ramp down to a safe value. After the 3.5µs interval, the internal PFET is turned on again. This cycle is repeated until the load is reduced and the output voltage exceeds approximately 0.375V. Therefore, the device may not startup if an excessive load is connected to the output when the device is enabled. The synchronous rectifier is off in the timed current limit mode. Timed current limit prevents the loss of current control seen in some products when the output voltage is pulled low in serious overload conditions.

A current limit is also provided for the NFET. This is approximately −500mA. Both the NFET and the PFET are turned off in negative current limit until the PFET is turned on again at the beginning of the next cycle. The negative current limit inhibits buildup of excessive negative inductor current.

In the Bypass mode, the bypass current limit is 1000mA (typ.). The output voltage drops when the bypass current limit kicks in.

LDO

LDO OPERATION

The LDO provides a nominal output voltage of 2.85V. Each LDO can be enabled when the respective enable pin is set high (>1.2V) after the buck converter has been enabled. The LDO will automatically be disabled whenever the EN_{BUCK} or EN_{LDOx} is disabled. Only one LDO may be enabled on at a time. A 2µs period of time needs to occur between disabled one LDO and enabling another. Otherwise, all LDOs are disabled.

CHARGE AND DISCHARGE

Each LDO includes an active charge circuit. 7.5us (typ.) after the LDO is enabled, the current limit of the LDO is set to 60mA. A 1µF load capacitor will be charged to 90% of the nominal output voltage in approximately 50us (typ.). (Note: This number is based on the assumption that the PWM loop has been enabled and given time to stabilize before the LDO is enabled.) The current limit is then reduced to 40mA.

An internal pull-down resistor is also included in each LDO. The LDO discharges the output capacitor through the pull-down resistor when LDO is disabled.

Shutdown Mode

Setting the EN_{BUCK} digital pin low (<0.4V) places the LM3280 in a 0.1µA (typ.) Shutdown mode. During shutdown, the PFET switch, NFET synchronous rectifier, reference voltage source, control and bias circuitry of the LM3280 are turned off. Setting EN_{BUCK} high (>1.2V) enables normal operation.

EN_{BUCK} should be set low to turn off the LM3280 during power-up and under voltage conditions when the power supply is less than the 2.7V minimum operating voltage. The LM3280 is designed for compact portable applications, such as cellular phones. In such applications, the system controller determines power supply sequencing and requirements for small package size outweigh the benefit of including UVLO (Under Voltage Lock-Out) circuitry.

Thermal Overload Protection

The LM3280 has a thermal overload protection function to protect the device from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off in PWM mode, and the Bypass PFET is turned off in Bypass mode. The LDO is also turned off. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device.

APPLICATION INFORMATION

BUCK CONVERTER SETTING THE OUTPUT VOLTAGE

The buck converter features a pin-controlled variable output voltage to eliminate the need for external feedback resistors. It can be programmed for an output voltage from 0.8V to 3.6V by setting the voltage on the V_{CON} pin, as in the following formula:

$$V_{OUT} = 3 \times V_{CON} \quad (1)$$

When V_{CON} is between 0.267V and 1.20V, the output voltage will follow proportionally by 3 times of V_{CON}.

If V_{CON} is over 1.20V (V_{OUT} = 3.6V), sub-harmonic oscillation may occur because of insufficient slope compensation.

If V_{CON} voltage is less than 0.267V (V_{OUT} = 0.8V), the output voltage may not be regulated due to the required on-time being less than the minimum on-time (50ns). The output voltage can go lower than 0.8V providing a limited V_{IN} range is used. Refer to the Typical Performance Characteristics (Low V_{CON} Voltage vs. Output Voltage) for details. This curve is for a typical part and there could be part to part variation for output voltages less than 0.8V over the limited V_{IN} range. In addition, if the V_{CON} is less than approximately 0.15V, the PWM mode output is turned off, but the internal bias circuits are still active.

INDUCTOR SELECTION

A 2.2µH inductor with saturation current rating over 940mA is recommended for almost all applications. The inductor resistance should be less than 0.2Ω for better efficiency. Table 1 lists suggested inductors and suppliers.

Table 1. Suggested Inductors and Their Suppliers

Model	Size (WxLxH) [mm]	Vendor
DO3314-222MX	3.3 x 3.3 x 1.4	Coilcraft
LPS3010-222MLC	3.1 x 3.1 x 1.0	Coilcraft
LPS3008-222MLC	3.1 x 3.1 x 0.8	Coilcraft
MIPSA2520D2R2**	2.5 x 2.0 x 1.2	FDK
KSLI252010AG2R2*	2.5 x 2.0 x 1.0	Hitachi-Metal
VLF3010AT-2R2M1R0	2.6 x 2.8 x 1.0	TDK
NR3010T2R2M	3.0 x 3.0 x 1.0	Taiyo-Yuden
NR3012T2R2M	3.0 x 3.0 x 1.2	Taiyo-Yuden
1117AS-2R2M(DE2810C)	2.8 x 3.0 x 1.0	Toko

If a higher value inductor is used the LM3280 may become unstable and exhibit large under or over shoot during line, load and V_{CON} transients. If smaller inductance value is used, slope compensation maybe insufficient causing sub-harmonic oscillations. The device has been tested with inductor values in the range 1.55µH to 3.1µH to account for inductor tolerances.

For low-cost applications, an un-shielded bobbin inductor can be used. For noise-critical applications, an un-shielded or shielded-bobbin inductor should be used. A good practice is to layout the board with footprints accommodating both types for design flexibility. This allows substitution of an un-shielded inductor, in the event that noise from low-cost bobbin models is unacceptable. Saturation occurs when the magnetic flux density from current through the windings of the inductor exceeds what the inductor's core material can support with a corresponding magnetic field. This can cause poor efficiency, regulation errors or stress to a DC-DC converter like the LM3280.

CAPACITOR SELECTION

The LM3280 is designed to be used with ceramic capacitors. Use a 10µF ceramic capacitor for the power input, a 4.7µF ceramic capacitor for the buck converter output, and a 1µF ceramic capacitor for the LDO and the signal input. Ceramic capacitors such as X5R, X7R and B are recommended for both filters. These provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. Table 2 lists suggested capacitors and suppliers.

Table 2. Suggested Capacitors and Their Suppliers

Model	Size (EIA)	Vendor
C1608X5R0J475M	1608 (0603)	TDK
C2012X5R0J106M	2012 (0805)	TDK
GRM188B10J105KA01	1608 (0603)	Murata
LMK107BJ105KA	1608 (0603)	Taiyo-Yuden
C1608JB1C105K	1608 (0603)	TDK

The DC bias characteristics of the capacitor must be considered when making the selection. If smaller case size such as 1608 (0603) is selected, the DC bias could reduce the cap value by as much as 40%, in addition to the 20% tolerances and 15% temperature coefficients. Request DC bias curves from manufacturer when making selection. The buck converter has been designed to be stable with output capacitors as low as 3µF to account for capacitor tolerances. The LDO has been done with output capacitors as low as 0.5µF. These values include DC bias reduction, manufacturing tolerances and temp coefficients.

The input filter capacitor supplies AC current drawn by the PFET switch of the LM3280 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. A 1µF capacitor is also recommended close to SVIN pin. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

DSBGA PACKAGE ASSEMBLY AND USE

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in National Semiconductor Application Note 1112. Refer to the section, *Surface Mount Technology (SMD) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 for specific instructions how to do this. The 16-Bump package used for the LM3280 has 300 micron solder balls and requires 10.82 mil pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 6-7 mil wide, for a section approximately 6 mil long or longer, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3280 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps B4, C4 and D4. Because PVIN and PGND are typically connected to large copper planes, inadequate thermal relief can result in inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, Thin Micro DSBGA devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

Do not use or power-up the LM3280 while subjecting it to high intensity red or infrared light; otherwise degraded, unpredictable or erratic operation may result. Examples of light sources with high red or infrared content include the sun and halogen lamps. Place the device in a case opaque to red or infrared light.

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance. Good layout for the LM3280 can by implemented by following a few simple design rules.

1. Place the LM3280 on 10.82 mil pads. As a thermal relief, connect to each pad with a 7 mil wide, approximately 7 mil long traces, and when incrementally increase each trace to its optimal width. The important criterion is symmetry to ensure the solder bumps on the LM3280 re-flow evenly (see DSBGA PACKAGE ASSEMBLY AND USE).
2. Place the LM3280, inductor and filter capacitors close together and make the trace short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor close to the LM3280. The input capacitor should be placed right next to the device between PVIN and PGND pin.
3. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the LM3280 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3280 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction, prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
4. Connect the ground pins of the LM3280, and filter capacitors together using generous component side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This reduces ground plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3280 by giving it a low impedance ground connection.
5. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
6. Route noise sensitive traces, such as the voltage feedback trace, away from noisy traces and components. The voltage feedback trace must remain close to the LM3280 circuit and should be routed directly from FB pin to V_{OUT} at the output capacitor. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and the layer on which the feedback trace is routed. This reduces EMI radiation on to the DC-DC converter's own voltage feedback trace.
7. It is recommended to connect BYPOUT pin to V_{OUT} at the output capacitor using a separate trace, instead of connecting it directly to the FB pin for better noise immunity.

REVISION HISTORY

Changes from Revision A (February 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3280TL-275/NOPB	ACTIVE	DSBGA	YZR	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	V002	Samples
LM3280TL/NOPB	ACTIVE	DSBGA	YZR	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	V001	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

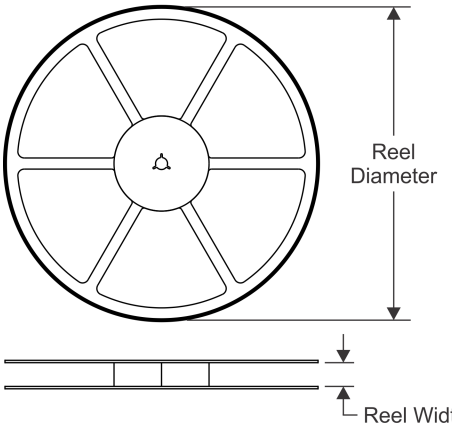
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

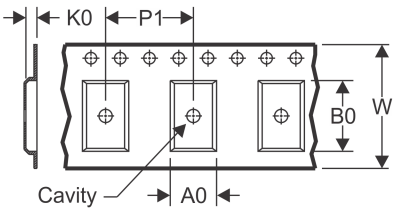
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

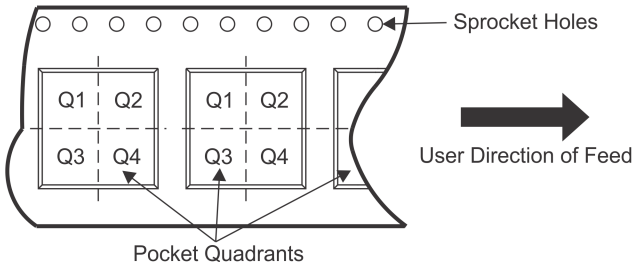


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

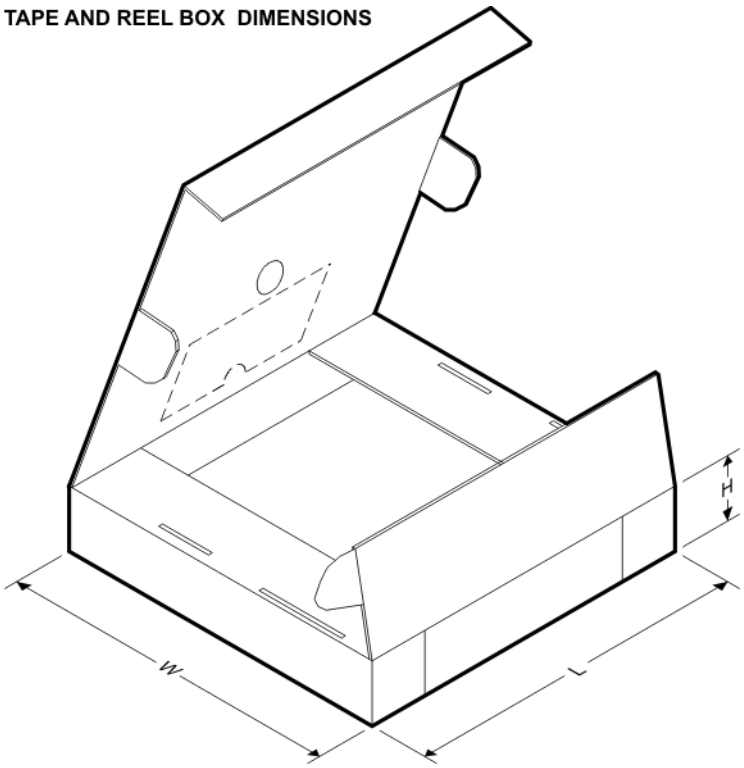
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3280TL-275/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.69	2.69	0.76	4.0	8.0	Q1
LM3280TL/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.69	2.69	0.76	4.0	8.0	Q1

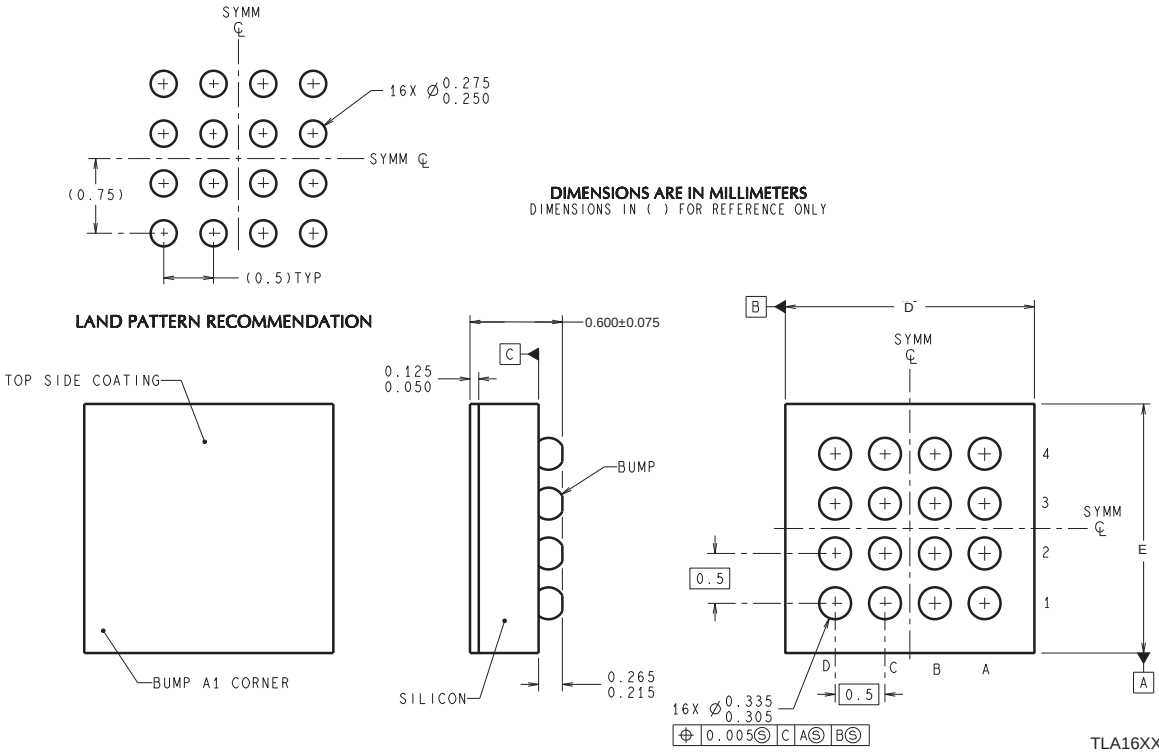
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3280TL-275/NOPB	DSBGA	YZR	16	250	210.0	185.0	35.0
LM3280TL/NOPB	DSBGA	YZR	16	250	210.0	185.0	35.0

YZR0016



D: Max = 2.385 mm, Min =2.325 mm

E: Max = 2.385 mm, Min =2.325 mm

4215051/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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