LM48312 Boomer™ Audio Power Amplifier Series 2.6W, Ultra-Low EMI, Filterless, Mono Class D Audio Power Amplifier with E^2S

Check for Samples: LM48312

FEATURES

- **Passes FCC Class B Radiated Emissions with 20 Inches of Cable**
- **E^2S System Reduces EMI While Preserving Audio Quality and Efficiency**
- **Output Short Circuit Protection with Auto-Recovery**
- **No Output Filter Required**
- **Improved Audio Quality**
- **Minimum External Components**
- **Five Logic Selectable Gain Settings (0, 3, 6, 9, 12dB)**
- **Low Power Shutdown Mode**
- **Click and Pop Suppression**
- **Available in Space-Saving DSBGA Package**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Laptops**

KEY SPECIFICATIONS

- **Efficiency at 3.6V, 400mW into 8Ω, 84% (Typ)**
- **Efficiency at 5V, 1W into 8Ω, 88% (Typ)**
- **Quiescent Power Supply Current at 5V, 3.1mA**
- **Power Output at V_{DD} = 5V, R_L = 4Ω**
  - **THD+N ≤ 10%, 2.6W (Typ)**
  - **THD+N ≤ 1%, 2.1W (Typ)**
- **Power Output at V_{DD} = 5V, R_L = 8Ω**
  - **THD+N ≤ 10%, 1.6W (Typ)**
  - **THD+N ≤ 1%, 1.3W (Typ)**
- **Shutdown Current, 0.01µA (Typ)**

DESCRIPTION

The LM48312 is a single supply, high efficiency, mono, 2.6W, filterless switching audio amplifier. The LM48312 features TI's Enhanced Emissions Suppression (E^2S) system, that features a unique patented ultra low EMI, spread spectrum, PWM architecture, that significantly reduces RF emissions while preserving audio quality and efficiency. The E^2S system improves battery life, reduces external component count, board area consumption, and system cost, simplifying design.

The LM48312 is designed to meet the demands of portable multimedia devices. Operating from a single 5V supply, the device is capable of delivering 2.6W of continuous output power to a 4Ω load with less than 10% THD+N. Flexible power supply requirements allow operation from 2.4V to 5.5V. The LM48312 features both a spread spectrum modulation scheme, and an advanced, patented edge rate control (ERC) architecture that significantly reduces emissions, while maintaining high quality audio reproduction (THD+N = 0.03%) and high efficiency (η = 88%).

The LM48312 features high efficiency compared to conventional Class AB amplifiers, and other low EMI Class D amplifiers. When driving an 8Ω speaker from a 5V supply, the device operates with 88% efficiency at P_O = 1W. The LM48312 features five gain settings, selected through a single logic input, further reducing solution size. A low power shutdown mode reduces supply current consumption to 0.01µA.

Advanced output short circuit protection with auto-recovery prevents the device from being damaged during fault conditions. Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown.

Typical Application

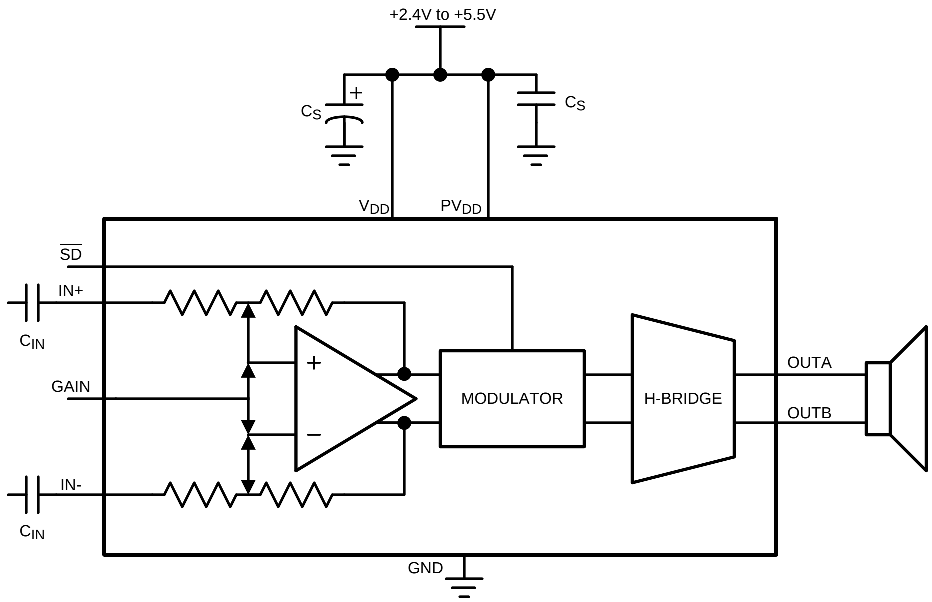

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

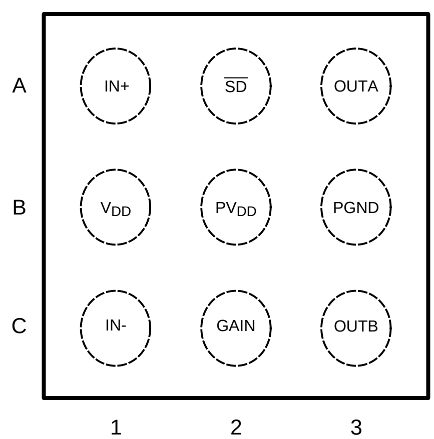

Figure 2. DSBGA Package
1.539mm x 1.565mm x 0.6mm
Top View
See Package Number YZR0009

BUMP DESCRIPTION

Pin	Name	Description
A1	IN+	Non-Inverting Input
A2	$\overline{SD}$	Active Low Shutdown Input. Connect to V_{DD} for normal operation.
A3	OUTA	Non-Inverting Output
B1	V_{DD}	Power Supply
B2	PV_{DD}	H-Bridge Power Supply
B3	PGND	Ground
C1	IN-	Inverting Input
C2	GAIN	Gain Select: GAIN = FLOAT: A_V = 0dB GAIN = V_{DD}: A_V = 3dB GAIN = GND: A_V = 6dB GAIN = 20kΩ to GND = 9dB GAIN = 20kΩ to V_{DD} = 12dB
C3	OUTB	Inverting Output

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		− 0.3V to V_{DD} +0.3V
Power Dissipation(4)		Internally Limited
ESD Rating(5)		2000V
ESD Rating(6)		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JA}	70°C/W
Soldering Information		
See AN-1112 (SNVA009) "DSBGA Wafer Level Chip Scale Package."		

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the*Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions*indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in*Absolute Maximum Ratings*, whichever is lower.
(5) Human body model, applicable std. JESD22-A114C.
(6) Machine model, applicable std. JESD22-A115-A.

Operating Ratings(1)(2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
	Supply Voltage (V_{DD}, PV_{DD})	$2.4V \le V_{DD} \le 5.5V$

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the*Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions*indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

Electrical Characteristics $V_{DD} = PV_{DD} = 5V$ (1) (2)

The following specifications apply for A_V = 6dB, R_L = 8Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48312 Min (3)	LM48312 Typ (4)	LM48312 Max (3)	Units (Limits)
V_{DD}	Supply Voltage Range		2.4		5.5	V
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0, R_L = 8Ω V_{DD} = 3.3V V_{DD} = 5V		 2.6 3.1	 3.3 3.9	 mA mA
I_{SD}	Shutdown Current	Shutdown enabled		0.01	1.0	µA
V_{OS}	Differential Output Offset Voltage	V_{IN} = 0	–48	10	48	mV
V_{IH}	Logic Input High Voltage		1.4			V
V_{IL}	Logic Input Low Voltage				0.4	V
T_{WU}	Wake Up Time			7.5		ms
f_{SW}	Switching Frequency			300±30		kHz
A_V	Gain	GAIN = FLOAT GAIN = V_{DD} GAIN = GND GAIN = 20kΩ to GND GAIN = 20kΩ to V_{DD}	–0.5 2.5 5.5 8.5 11.5	0 3 6 9 12	0.5 3.5 6.5 9.5 12.5	dB dB dB dB dB
R_{IN}	Input Resistance	A_V = 0dB A_V = 3dB A_V = 6dB A_V = 9dB A_V = 12dB	 20	56 49 42 35 27		kΩ kΩ kΩ kΩ kΩ
P_O	Output Power	R_L = 4Ω, THD = 10% f = 1kHz, 22kHz BW V_{DD} = 5V V_{DD} = 3.3V V_{DD} = 2.5V		 2.6 1.1 580		 W W mW
		R_L = 8Ω, THD = 10% f = 1kHz, 22kHz BW V_{DD} = 5V V_{DD} = 3.3V V_{DD} = 2.5V		 1.6 660 354		 W mW mW
		R_L = 4Ω, THD = 1% f = 1kHz, 22kHz BW V_{DD} = 5V V_{DD} = 3.3V V_{DD} = 2.5V		 2.1 900 460		 W mW mW
		R_L = 8Ω, THD = 1% f = 1kHz, 22kHz BW V_{DD} = 5V V_{DD} = 3.3V V_{DD} = 2.5V	 1.1 450	 1.3 530 286		 W (min) mW mW
THD+N	Total Harmonic Distortion + Noise	P_O = 200mW, R_L = 8Ω, f = 1kHz		0.027		%
		P_O = 100mW, R_L = 8Ω, f = 1kHz		0.03		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} Sine, Inputs AC GND, A_V = 0dB, C_{IN} = 1µF f_{RIPPLE} = 217Hz f_{RIPPLE} = 1kHz		 71 70		 dB dB
CMRR	Common Mode Rejection Ratio	V_{RIPPLE} = 1V_{P-P} , f_{RIPPLE} = 217Hz A_V = 0dB		65		dB

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(2) R_L is a resistive load in series with two inductors to simulate an actual speaker load. For R_L = 8Ω, the load is 15µH + 8Ω, +15µH. For R_L = 4Ω, the load is 15µH + 4Ω + 15µH.
(3) Datasheet min/max specification limits are specified by test or statistical analysis.
(4) Typical values represent most likely parametric norms at T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

Electrical Characteristics $V_{DD} = PV_{DD} = 5V$[1][2] (continued)

The following specifications apply for A_V = 6dB, R_L = 8Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48312			Units (Limits)
			Min (3)	Typ (4)	Max (3)	
η	Efficiency	V_{DD} = 5V, P_{OUT} = 1W V_{DD} = 3.3V, P_{OUT} = 400mW		88 85		% %
SNR	Signal to Noise Ratio	P_O = 1W		95		dB
CMVR	Common Mode Input Voltage Range		0	V_{DD} – 0.25		V
$ε_{OS}$	Output Noise	Un-weighted, A_V = 0dB A-weighted, A_V = 0dB		69 48		μV μV

Test Circuits

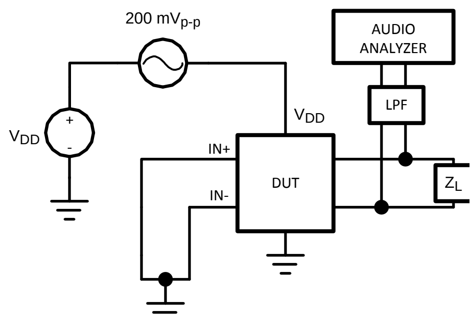

Figure 3. PSRR Test Circuit

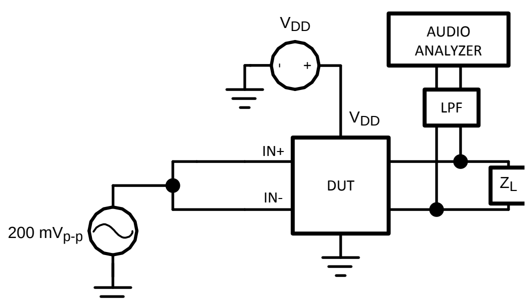

Figure 4. CMRR Test Circuit

Typical Performance Characteristics

For all performance graphs, the Output Gains are set to 0dB, unless otherwise noted.

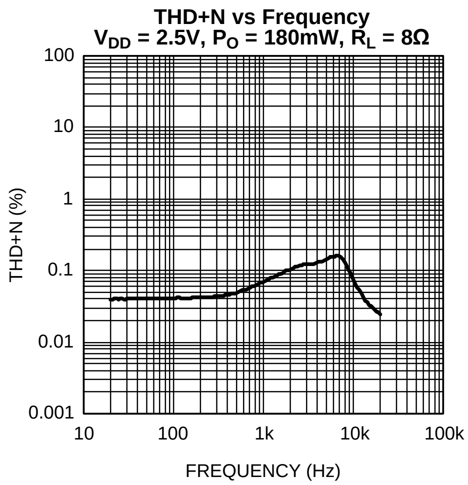

Figure 5.

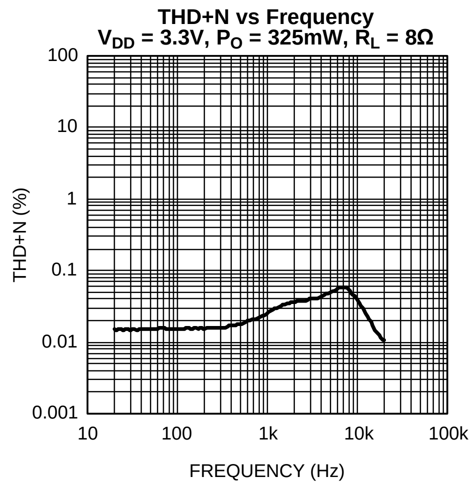

Figure 6.

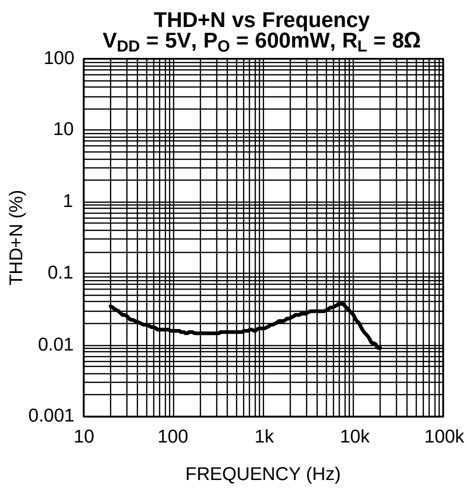

Figure 7.

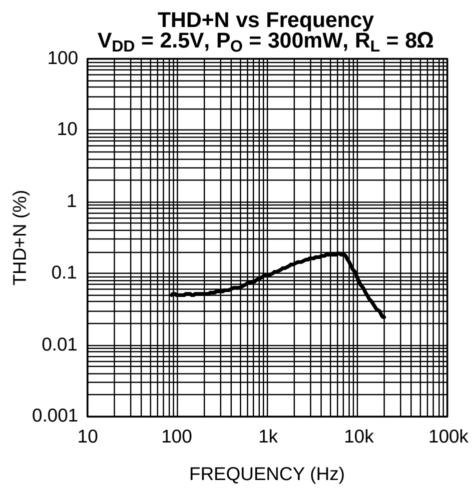

Figure 8.

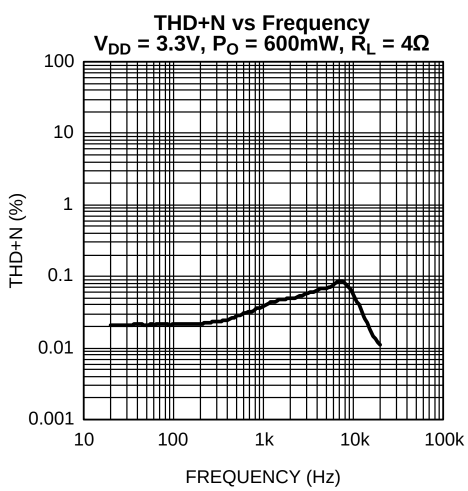

Figure 9.

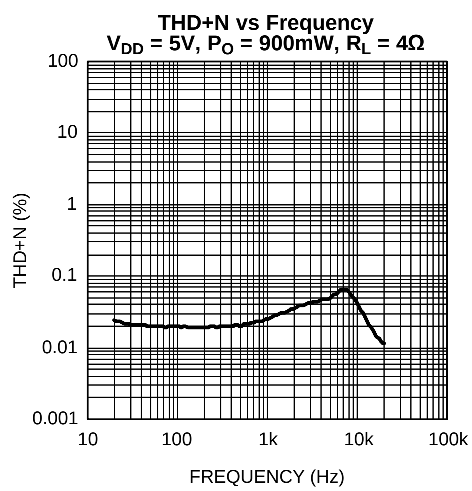

Figure 10.

Typical Performance Characteristics (continued)

For all performance graphs, the Output Gains are set to 0dB, unless otherwise noted.

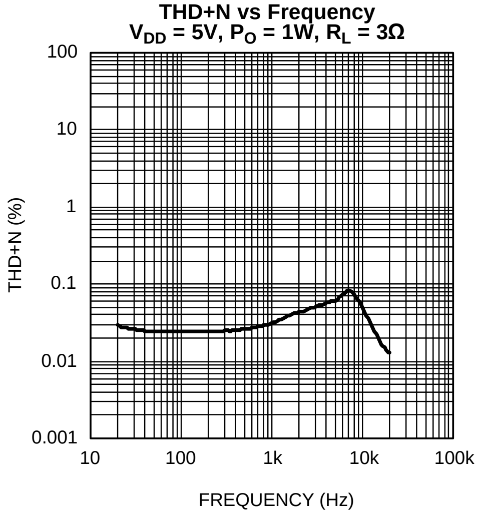

Figure 11.

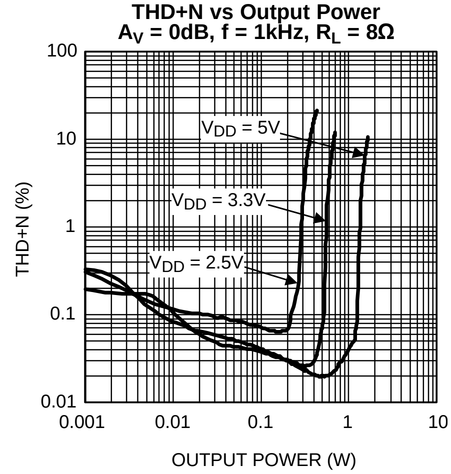

Figure 12.

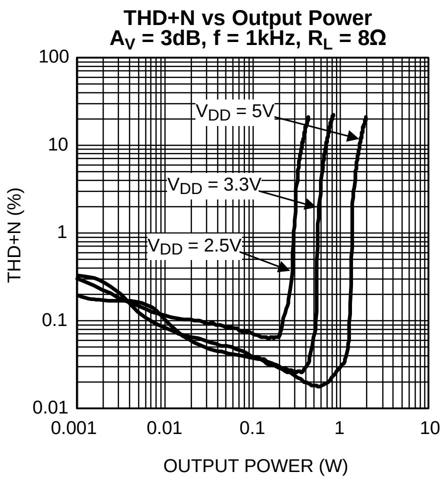

Figure 13.

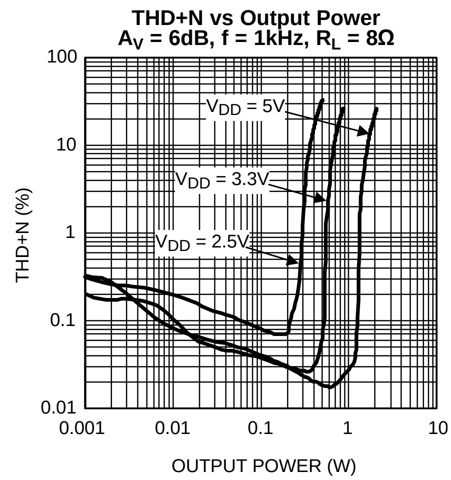

Figure 14.

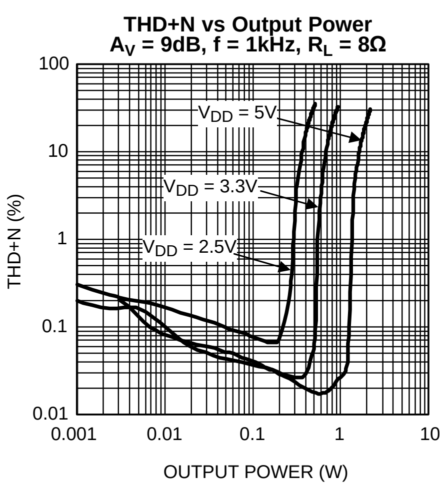

Figure 15.

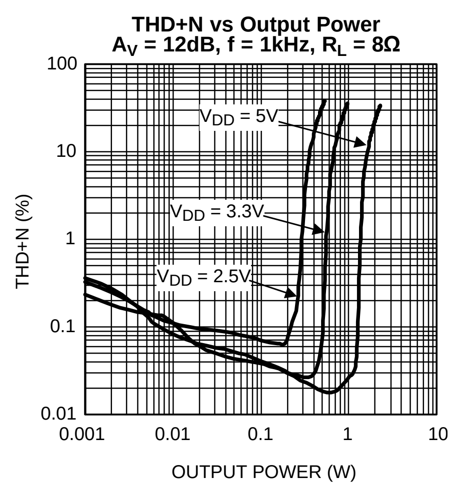

Figure 16.

Typical Performance Characteristics (continued)

For all performance graphs, the Output Gains are set to 0dB, unless otherwise noted.

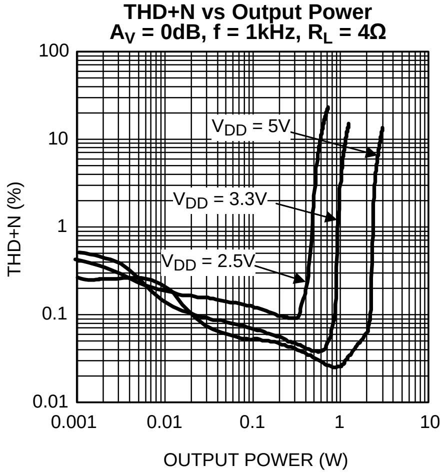

Figure 17.

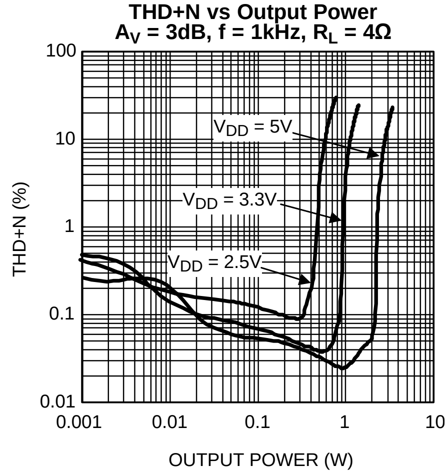

Figure 18.

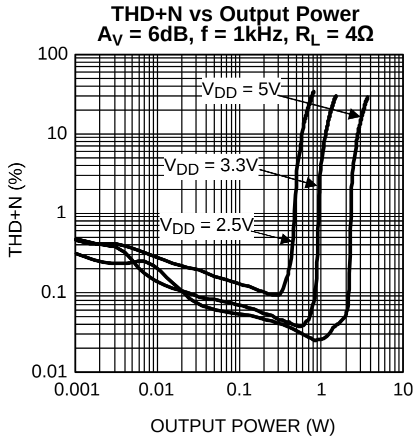

Figure 19.

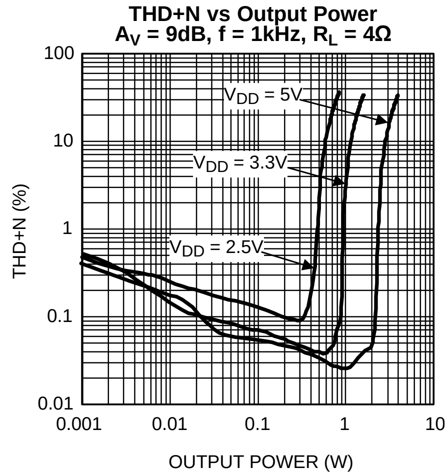

Figure 20.

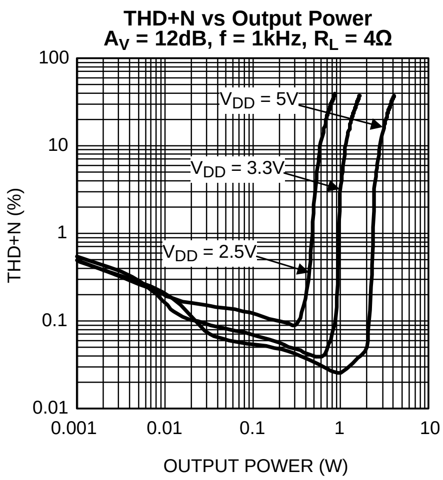

Figure 21.

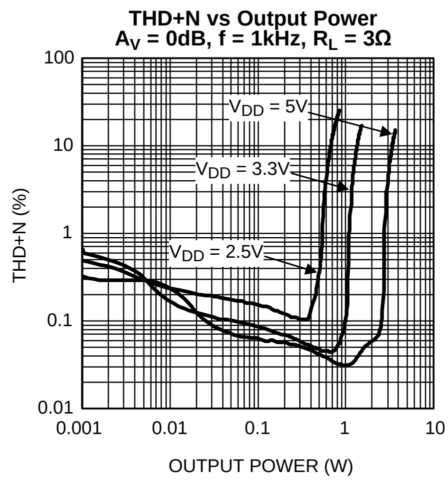

Figure 22.

Typical Performance Characteristics (continued)

For all performance graphs, the Output Gains are set to 0dB, unless otherwise noted.

THD+N vs Output Power
A_V = 3dB, f = 1kHz, R_L = 3Ω

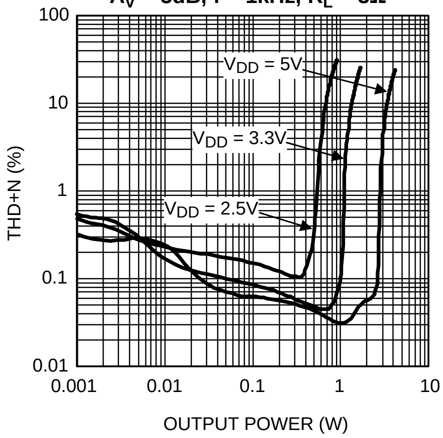

Figure 23.

THD+N vs Output Power
A_V = 6dB, f = 1kHz, R_L = 3Ω

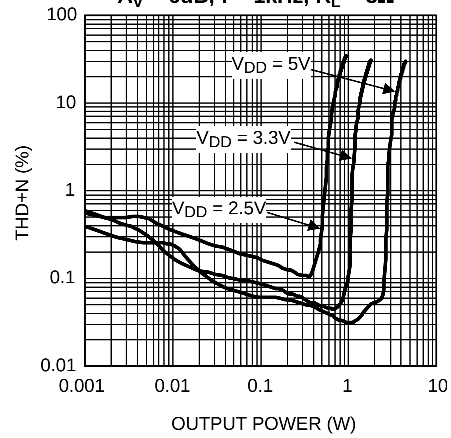

Figure 24.

THD+N vs Output Power
A_V = 9dB, f = 1kHz, R_L = 3Ω

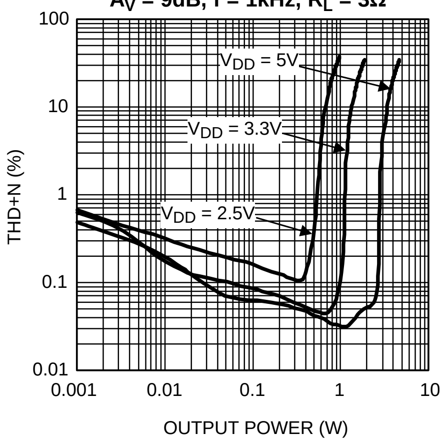

Figure 25.

THD+N vs Output Power
A_V = 12dB, f = 1kHz, R_L = 3Ω

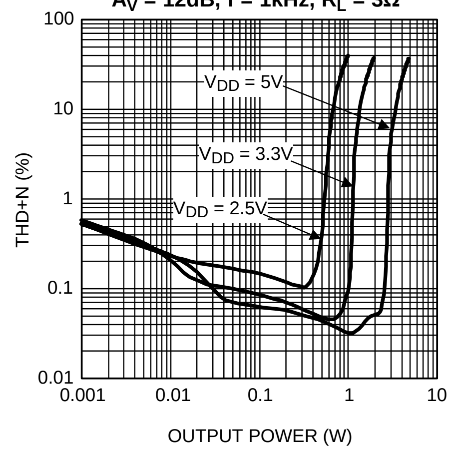

Figure 26.

Efficiency vs Output Power
f = 1kHz, R_L = 4Ω

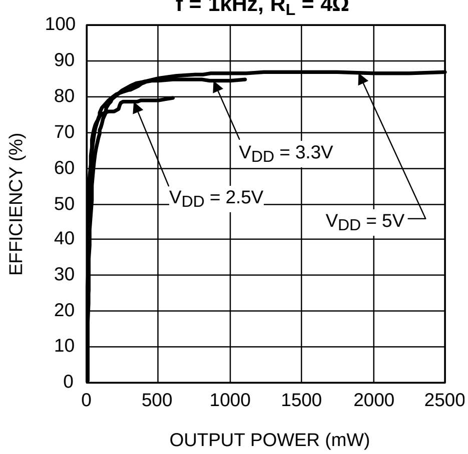

Figure 27.

Efficiency vs Output Power
f = 1kHz, R_L = 8Ω

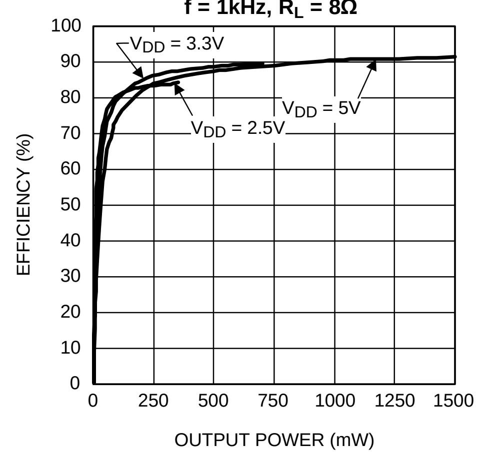

Figure 28.

Typical Performance Characteristics (continued)

For all performance graphs, the Output Gains are set to 0dB, unless otherwise noted.

Power Dissipation vs Output Power
f = 1kHz, R_L = 4Ω

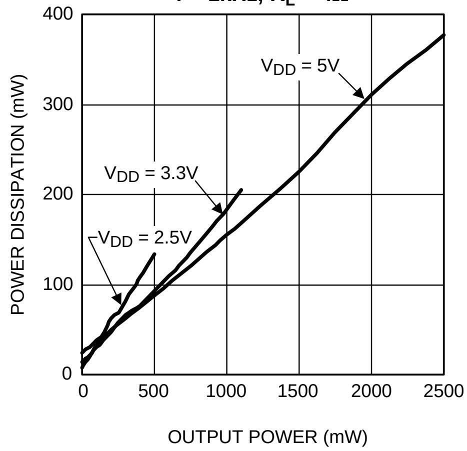

Figure 29.

Power Dissipation vs Output Power
f = 1kHz, R_L = 8Ω

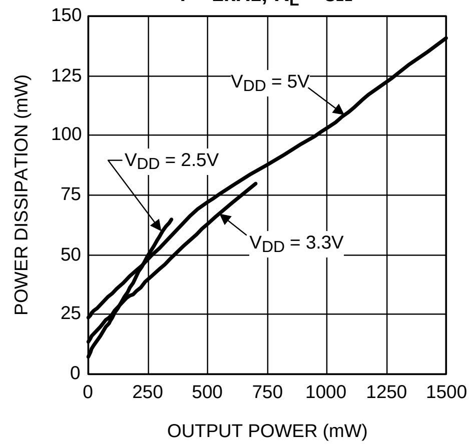

Figure 30.

Output Power vs Supply Voltage
f = 1kHz, R_L = 4Ω

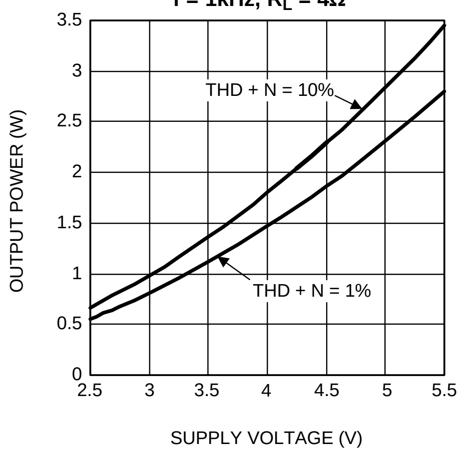

Figure 31.

Output Power vs Supply Voltage
f = 1kHz, R_L = 8Ω

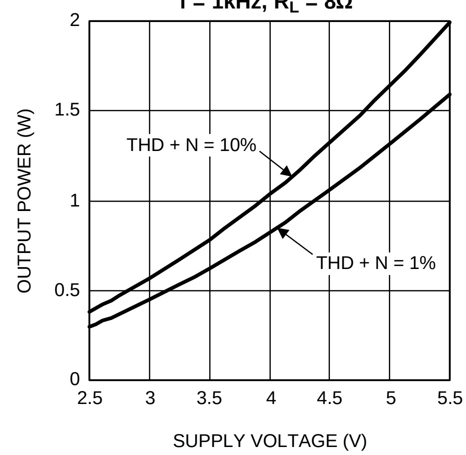

Figure 32.

PSRR vs Frequency
V_{DD} = 5V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω

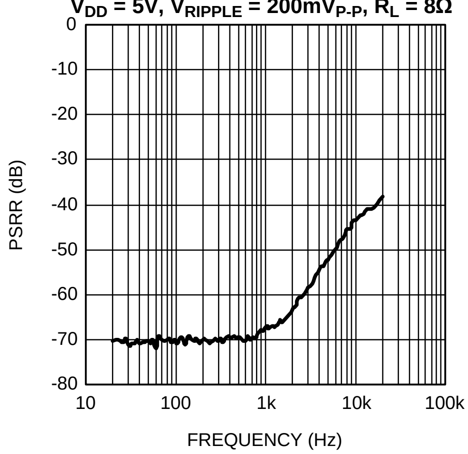

Figure 33.

CMRR vs Frequency
V_{DD} = 5V, V_{RIPPLE} = 1V_{P-P}, R_L = 8Ω

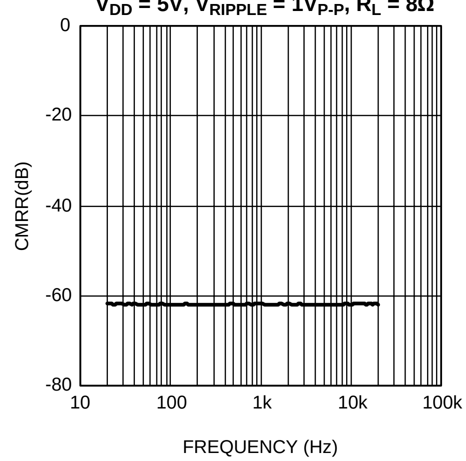

Figure 34.

Typical Performance Characteristics (continued)

For all performance graphs, the Output Gains are set to 0dB, unless otherwise noted.

Spread Spectrum Output Spectrum vs Frequency
V_{DD} = 5V, V_{IN} = 1V_{RMS}, R_L = 8Ω

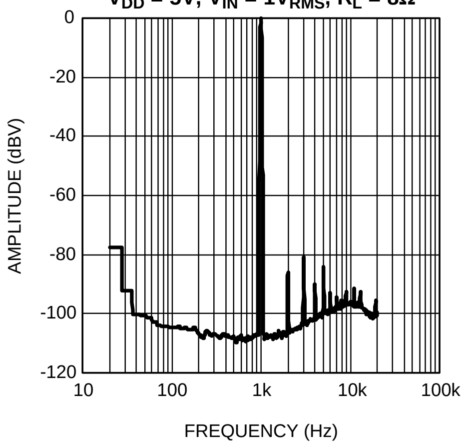

Figure 35.

Wideband Spread Spectrum Output Spectrum vs Frequency
V_{DD} = 5V, R_L = 8Ω

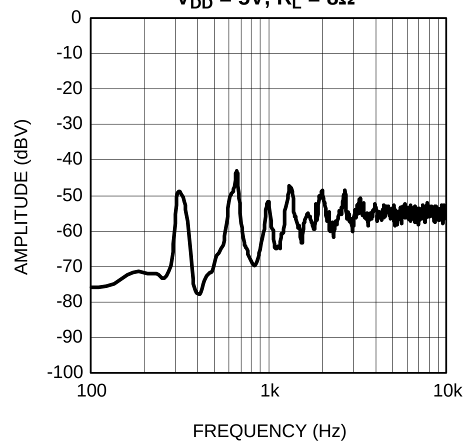

Figure 36.

Supply Current vs Supply Voltage No Load

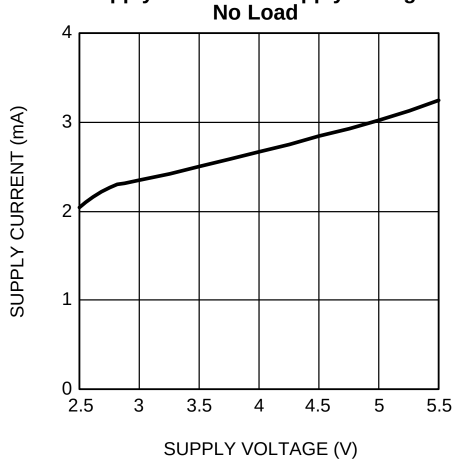

Figure 37.

Shutdown Supply Current vs Supply Voltage No Load

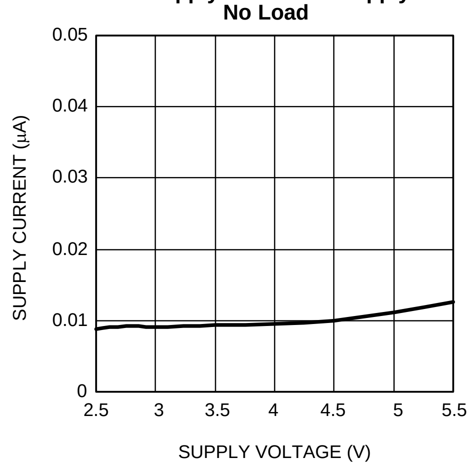

Figure 38.

APPLICATION INFORMATION

GENERAL AMPLIFIER FUNCTION

The LM48312 mono Class D audio power amplifier features a filterless modulation scheme that reduces external component count, conserving board space and reducing system cost. The outputs of the device transition from V_{DD} to GND with a 300kHz switching frequency. With no signal applied, the outputs (V_{OUTA} and V_{OUTB}) switch with a 50% duty cycle, in phase, causing the two outputs to cancel. This cancellation results in no net voltage across the speaker, thus there is no current to the load in the idle state.

With the input signal applied, the duty cycle (pulse width) of the LM48312 outputs changes. For increasing output voltage, the duty cycle of V_{OUTA} increases, while the duty cycle of V_{OUTB} decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yields the differential output voltage.

ENHANCED EMISSIONS SUPPRESSION SYSTEM (E^2S)

The LM48312 features TI's patented E^2S system that reduces EMI, while maintaining high quality audio reproduction and efficiency. The E^2S system features spread spectrum and advanced edge rate control (ERC). The LM48312 ERC greatly reduces the high frequency components of the output square waves by controlling the output rise and fall times, slowing the transitions to reduce RF emissions, while maximizing THD+N and efficiency performance. The overall result of the E^2S system is a filterless Class D amplifier that passes FCC Class B radiated emissions standards with 20in of twisted pair cable, with excellent 0.03% THD+N and high 88% efficiency.

SPREAD SPECTRUM

The spread spectrum modulation reduces the need for output filters, ferrite beads or chokes. The switching frequency varies randomly by 30% about a 300kHz center frequency, reducing the wideband spectral contend, improving EMI emissions radiated by the speaker and associated cables and traces. Where a fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency, the spread spectrum architecture of the LM48312 spreads that energy over a larger bandwidth (See Typical Performance Characteristics). The cycle-to-cycle variation of the switching period does not affect the audio reproduction, efficiency, or PSRR.

DIFFERENTIAL AMPLIFIER EXPLANATION

As logic supplies continue to shrink, system designers are increasingly turning to differential analog signal handling to preserve signal to noise ratios with restricted voltage signs. The LM48312 features a fully differential speaker amplifier. A differential amplifier amplifies the difference between the two input signals. Traditional audio power amplifiers have typically offered only single-ended inputs resulting in a 6dB reduction of SNR relative to differential inputs. The LM48312 also offers the possibility of DC input coupling which eliminates the input coupling capacitors. A major benefit of the fully differential amplifier is the improved common mode rejection ratio (CMRR) over single ended input amplifiers. The increased CMRR of the differential amplifier reduces sensitivity to ground offset related noise injection, especially important in noisy systems.

POWER DISSIPATION AND EFFICIENCY

The major benefit of a Class D amplifier is increased efficiency versus a Class AB. The efficiency of the LM48312 is attributed to the region of operation of the transistors in the output stage. The Class D output stage acts as current steering switches, consuming negligible amounts of power compared to their Class AB counterparts. Most of the power loss associated with the output stage is due to the IR loss of the MOSFET on-resistance, along with switching losses due to gate charge.

GAIN SETTING

The LM48312 features five internally configured gain settings, 0, 3, 6, 9, and 12dB. The device gain is selected through a single pin (GAIN). The gain settings are shown in Table 1. The gain of the LM48312 is determined at startup. When the LM48312 is powered up or brought out of shutdown, the device checks the state of GAIN, and sets the amplifier gain accordingly. Once the gain is set, the state of GAIN is ignored and the device gain cannot be changed until the device is either shutdown or powered down.

Table 1. Gain Setting

GAIN	GAIN SETTING
FLOAT	0dB
V_{DD}	3dB
GND	6dB
20kΩ to GND	9dB
20kΩ to V_{DD}	12dB

For proper gain selection:

1. Use 20kΩ resistors with 10% tolerance or better for the 9dB and 12dB gain settings.
2. Short GAIN to either V_{DD} or GND through 100Ω or less for the 3dB and 6dB gain settings.
3. FLOAT = 20MΩ or more for the 0dB gain setting.

SHUTDOWN FUNCTION

The LM48312 features a low current shutdown mode. Set $\overline{SD}$ = GND to disable the amplifier and reduce supply current to 0.01µA.

Switch $\overline{SD}$ between GND and V_{DD} for minimum current consumption is shutdown. The LM48312 may be disabled with shutdown voltages in between GND and V_{DD}, the idle current will be greater than the typical 0.1µA value. Increased THD+N may also be observed when a voltage of less than V_{DD} is applied to $\overline{SD}$.

The LM48312 shutdown input has and internal pulldown resistor. The purpose of this resistor is to eliminate any unwanted state changes when $\overline{SD}$ is floating. To minimize shutdown current, $\overline{SD}$ should be driven to GND or left floating. If $\overline{SD}$ is not driven to GND or floating, an increase in shutdown supply current will be noticed.

PROPER SELECTION OF EXTERNAL COMPONENTS

Audio Amplifier Power Supply Bypassing/Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Typical applications employ a voltage regulator with 10µF and 0.1µF bypass capacitors that increase supply stability. These capacitors do not eliminate the need for bypassing of the LM48312 supply pins. A 1µF capacitor is recommended.

Audio Amplifier Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48312. The input capacitors create a high-pass filter with the input resistors R_{IN}. The -3dB point of the high pass filter is found using Equation 1 below.

$$f = 1 / 2\pi R_{IN} C_{IN} \tag{1}$$

Where R_{IN} is the value of the input resistor given in the *Electrical Characteristics* table.

The input capacitors can also be used to remove low frequency content from the audio signal. Small speakers cannot reproduce, and may even be damaged by low frequencies. High pass filtering the audio signal helps protect the speakers. When the LM48312 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

Single-Ended Audio Amplifier Configuration

The LM48312 is compatible with single-ended sources. When configured for single-ended inputs, input capacitors must be used to block and DC component at the input of the device. Figure 39 shows the typical single-ended applications circuit.

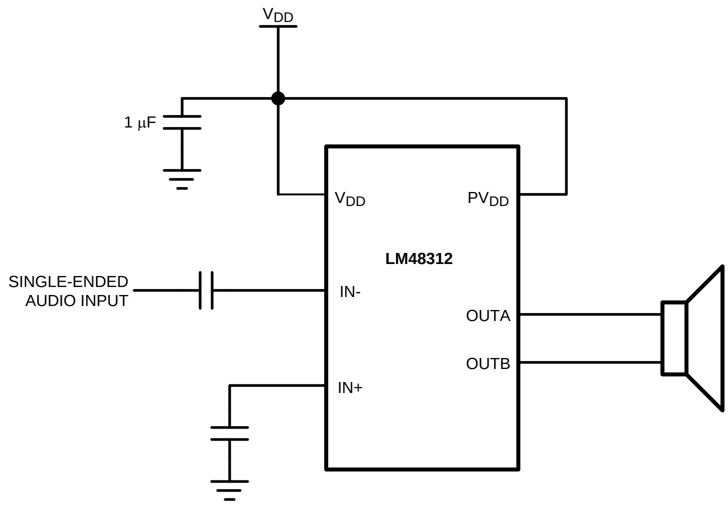

Figure 39. Single-Ended Input Configuration

PCB LAYOUT GUIDELINES

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load and power supply create a voltage drop. The voltage loss due to the traces between the LM48312 and the load results in lower output power and decreased efficiency. Higher trace resistance between the supply and the LM48312 has the same effect as a poorly regulated supply, increasing ripple on the supply line, and reducing peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. In addition to reducing trace resistance, the use of power planes creates parasitic capacitors that help to filter the power supply line.

The inductive nature of the transducer load can also result in overshoot on one of both edges, clamped by the parasitic diodes to GND and V_{DD} in each case. From an EMI standpoint, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. In is essential to keep the power and output traces short and well shielded if possible. Use of ground planes beads and micros-strip layout techniques are all useful in preventing unwanted interference.

As the distance from the LM48312 and the speaker increases, the amount of EMI radiation increases due to the output wires or traces acting as antennas become more efficient with length. Ferrite chip inductors places close to the LM48312 outputs may be needed to reduce EMI radiation.

Demo Board Schematic

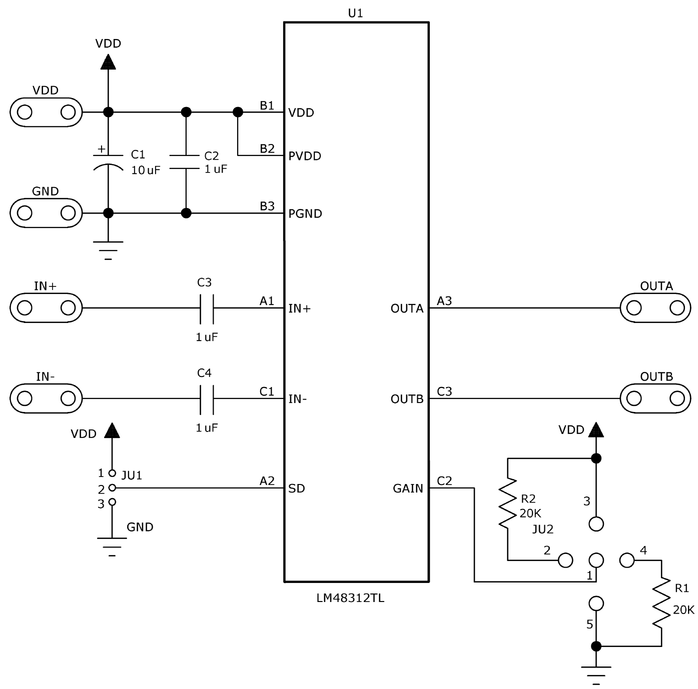

Figure 40. LM48312 Demoboard Schematic

LM48312TL Demoboard Bill of Materials

Designator	Quantity	Description
C1	1	10µF ±10% 16V Tantalum Capacitor (B Case) AVX TPSB106K016R0800
C2	1	1µF ±10% 16V X5R Ceramic Capacitor (603) Panasonic ECJ-1VB1C105K
C3, C4	2	1µF ±10% 16V X7R Ceramic Capacitor (1206) Panasonic ECJ-3YB1C105K
R1, R2	2	20kΩ ± 5% 1/10W Thick Film Resistor (603) Vishay CRCW060320R0JNEA
LM48312TL	1	LM48312TL (9-Bump DSBGA)

PC Board Layout

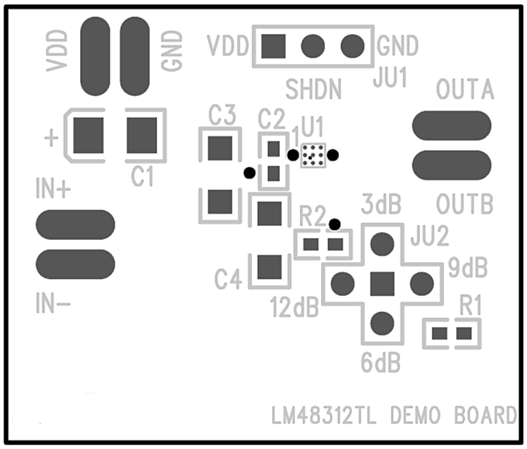

Figure 41. Top Silkscreen

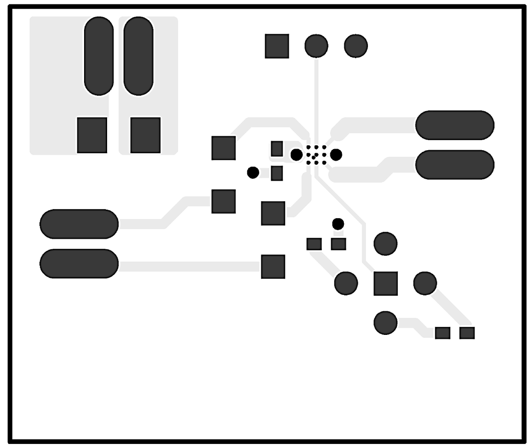

Figure 42. Top Layer

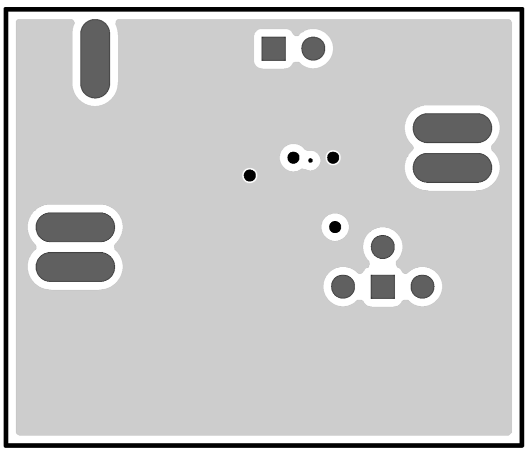

Figure 43. Layer 2 (GND)

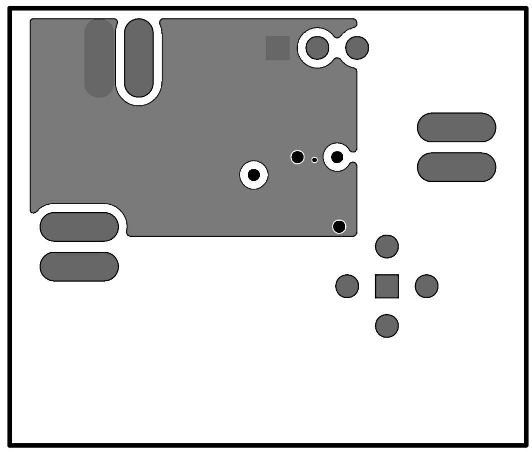

Figure 44. Layer 3 (V_{DD})

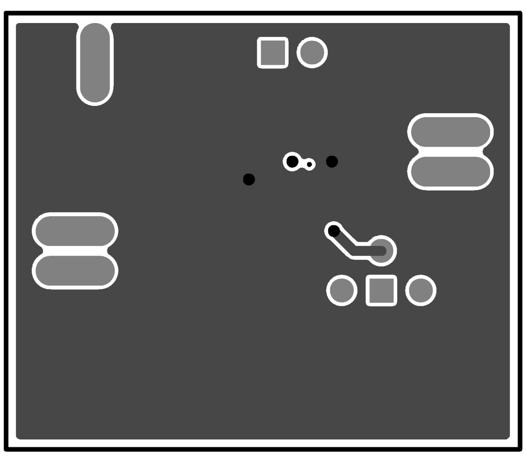

Figure 45. Bottom Layer

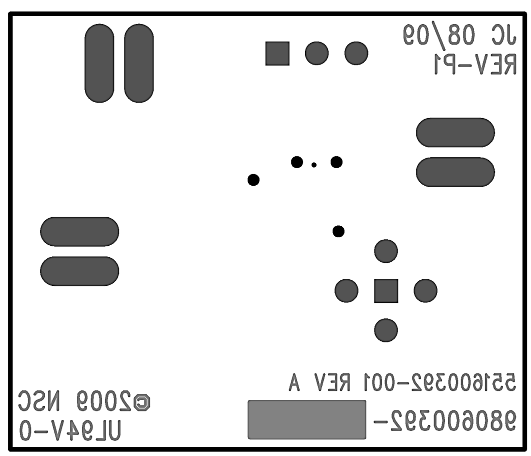

Figure 46. Bottom Silkscreen

REVISION HISTORY

Rev	Date	Description
1.0	01/20/10	Initial WEB released.
1.01	03/19/10	Text edits under the ENHANCED EMISSIONS section.
1.02	05/13/10	Edited Table 1.
1.03	07/25/12	Corrected the cover page (at WEB) (TI) from LM483127 to LM48312.

Changes from Revision C (May 2013) to Revision D — Page

- Changed layout of National Data Sheet to TI format 16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM48312TLE/NOPB	ACTIVE	DSBGA	YZR	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	G N4	Samples
LM48312TLX/NOPB	ACTIVE	DSBGA	YZR	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	G N4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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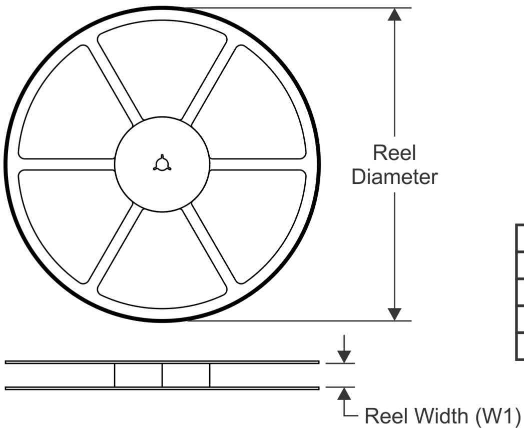
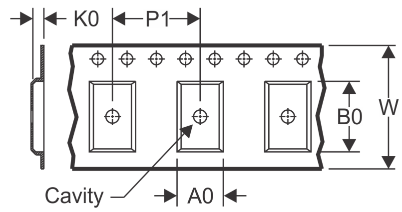
TAPE AND REEL INFORMATION

REEL DIMENSIONS

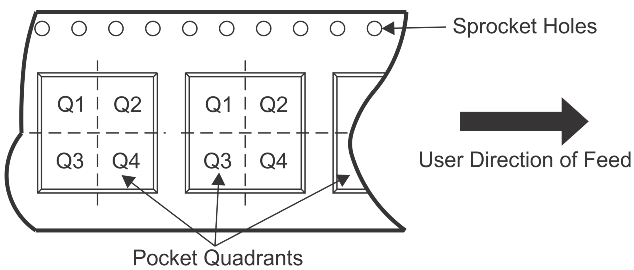


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

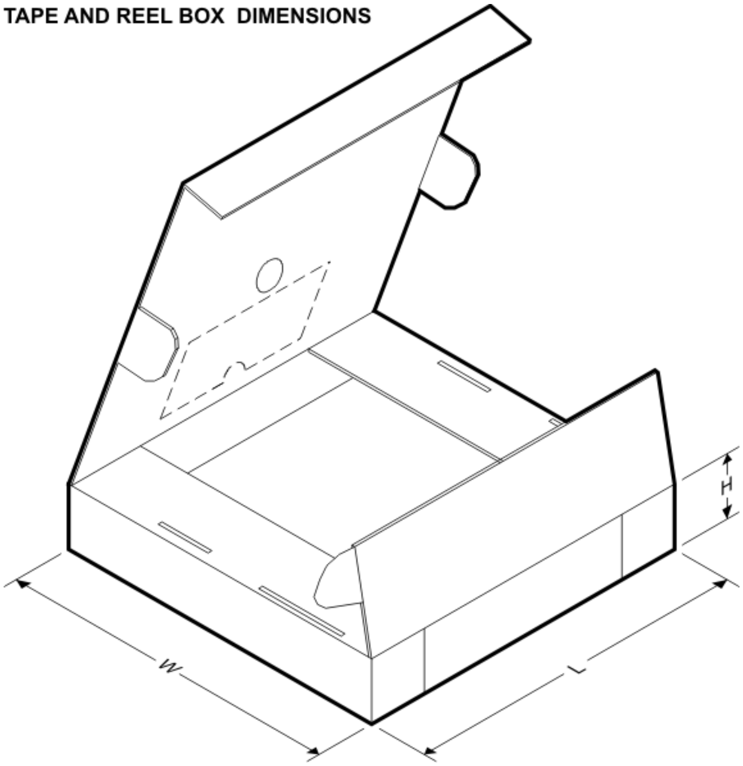
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

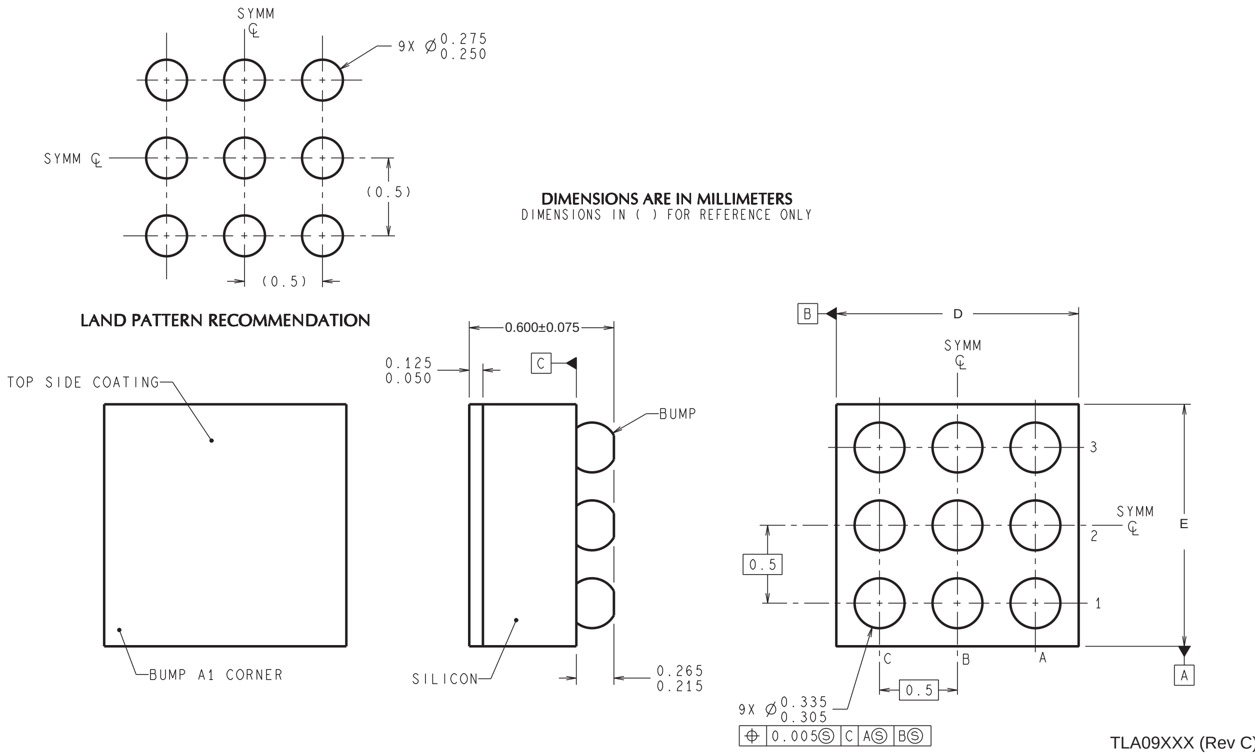
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48312TLE/NOPB	DSBGA	YZR	9	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LM48312TLX/NOPB	DSBGA	YZR	9	3000	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48312TLE/NOPB	DSBGA	YZR	9	250	210.0	185.0	35.0
LM48312TLX/NOPB	DSBGA	YZR	9	3000	210.0	185.0	35.0



D: Max = 1.581 mm, Min =1.521 mm

E: Max = 1.557 mm, Min =1.497 mm

4215046/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.