LP5524 Four-Channel LED Driver With Dual-PWM Brightness Control

1 Features

- Wide Input Voltage Range: 2.7 V to 5.5 V
- High-Side LED Driver
- Drives Four LEDs With up to 25 mA per LED
- 0.4% Typical Current Matching
- PWM Brightness Control
- Overcurrent Protection
- Fast Transient Response
- Optional External ISET Resistor
- Ultra-Small Solution Size:
  - No External Components
  - 9-Pin DSBGA Package with 0.4-mm pitch:
    - 1.24 mm × 1.24 mm × 0.6 mm (L × W × H, maximum)

2 Applications

- Sub-Display Backlight
- Keypad LED Backlight
- Indicator LED

3 Description

The LP5524 device is a highly integrated dual-zone LED driver that can drive up to four LEDs in parallel with a total output current of 100 mA. Regulated high-side internal current sources deliver excellent current and brightness matching in all LEDs.

The LP5524 provides overcurrent protection and pulse-width modulation (PWM) control of four indicator LEDs without the need for external components.

LED driver current sources are split into two independently controlled banks for driving secondary displays, keypad and indicator LEDs. Brightness control is achieved by applying PWM signals to each enable pin. Default LED current is factory-programmable and an optional external resistor can be used to set LED current to user programmable values.

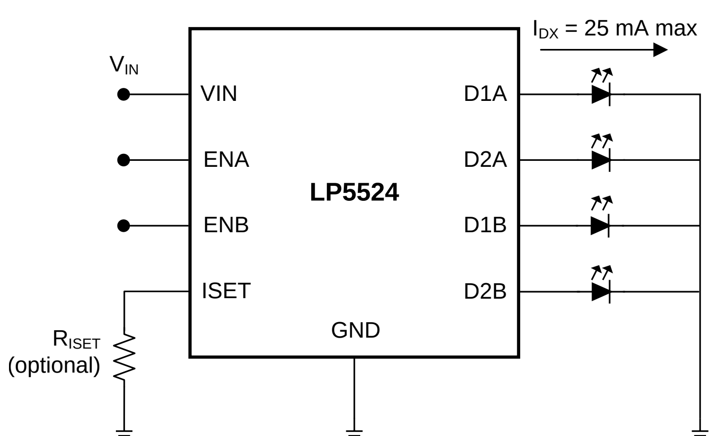
The LP5524 is available in a tiny, 9-pin, thin DSBGA package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP5524	DSBGA (9)	1.21 mm × 1.21 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2016) to Revision C — **Page**

- Changed wording of data sheet title ... 1

Changes from Revision A (May 2013) to Revision B — **Page**

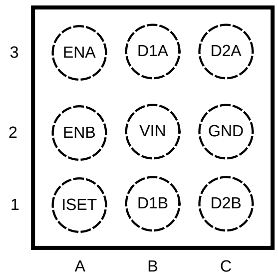
- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted lead temperature and soldering rows from *Abs Max* table - information in POA ... 4
- Added *Thermal Information* table with revised $R_{\theta JA}$ value (from "80 - 125°C/W" to "101.9°C/W") and added additional thermal values. ... 4

Changes from Original (April 2013) to Revision A — **Page**

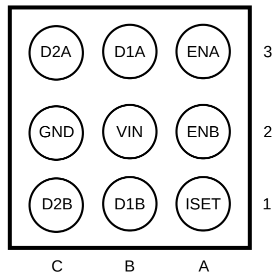
- Changed layout of National Data Sheet to TI format ... 10

5 Pin Configuration and Functions

YFQ Package
9-Pin DSBGA
Top View



YFQ Package
9-Pin DSBGA
Bottom View



Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NUMBER	NAME		
A1	ISET	AI	Current set input
A2	ENB	DI	Enable for bank B
A3	ENA	DI	Enable for bank A
B1	D1B	AO	Current source output, bank B LED1
B2	VIN	P	Power supply pin
B3	D1A	AO	Current source output, bank A LED1
C1	D2B	AO	Current source output, bank B LED2
C2	GND	G	Ground
C3	D2A	AO	Current source output, bank A LED2

(1) A: Analog Pin D: Digital Pin G: Ground Pin P: Power Pin I: Input Pin O: Output Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)(4)

	MIN	MAX	UNIT
V (VIN, DX, ISET)	–0.3	6	V
Voltage on logic pins (ENA, ENB)	–0.3	6	V
Continuous power dissipation(5)	Internally limited		
Junction temperature, $T_{J\text{-}MAX}$		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) All voltages are with respect to the potential at the GND pin.
(4) For detailed soldering specifications and information, refer to *AN-1112 DSBGA Wafer Level Chip Scale Package* and *Absolute Maximum Ratings for Soldering*.
(5) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typical) and disengages at T_J=140°C (typical).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage on power pin (VIN)	2.7	5.5	V
Junction temperature, T_J	–40	125	°C
Ambient temperature, T_A(1)	–40	85	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

6.4 Thermal Information

THERMAL METRIC(1)		LP5524 YFQ (DSBGA) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	101.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

6.5 Electrical Characteristics

Unless otherwise noted, specifications apply to the *Functional Block Diagram* with: V_{IN} = 3.6 V, R_{ISET} = 32.4 kΩ, C_{IN} = 100 nF, T_J = 25°C.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VIN}	Shutdown supply current	ENA = ENB = 0 V		0.2		µA
		ENA = ENB = 0V, T_J = –40°C to 85°C			1	
	Active mode supply current	ENA = ENB = H, ISET = open		170		µA
		ENA = ENB = H, ISET = open T_J = –40°C to 85°C			210	
I_{DX}	Recommended LED current		3		25	mA
I_{OUT}	LED output current accuracy	I_{DX} = 5 mA, V_{DX} = V_{IN} – 0.2V ISET = open		0.5%		
		I_{DX} = 5 mA, V_{DX} = V_{IN} – 0.2V ISET = open, T_J = –40°C to 85°C			5%	
		I_{DX} = 15.9 mA, V_{DX} = V_{IN} – 0.2 V		0.5%		
		I_{DX} = 15.9 mA, V_{DX} = V_{IN} – 0.2 V T_J = –40°C to 85°C			4%	
I_{MATCH}	LED current matching(3)	I_{DX} = 15.9 mA		0.4%		
		I_{DX} = 15.9 mA, T_J = –40°C to 85°C			2.5%	
$\Delta I_{DX}\%/\Delta V_{IN}$	Line regulation			1		%/V
$\Delta I_{DX}\%/\Delta V_{DX}$	Load regulation	V_{DX} < V_{IN} – 0.2V		0.4		%/V
V_{HR}	Minimum headroom voltage (V_{IN} – V_{DX})(4)	I_{DX} set to 5 mA		10		mV
		I_{DX} set to 15 mA		30		mV
		I_{DX} set to 15 mA, T_J = –40°C to 85°C			75	
I_{MIRROR}	External R_{ISET} to LED current mirroring ratio			1:416		
V_{ISET}	ISET reference voltage			1.237		V
I_{ISET}		T_J = –40°C to 85°C	2.5		62.5	µA
$t_{PWM\ MIN}$	Recommended minimum ON time for PWM signal			33		µs
V_{IL}	Logic input low level	T_J = –40°C to 85°C			0.4	V
V_{IH}	Logic input high level	T_J = –40°C to 85°C	1.2			V
I_{IN}	CTRL input current	ENA / ENB = 1.2 V		1.2		µA
		ENA / ENB = 1.2 V, T_J = –40°C to 85°C			1.9	
t_{SD}	Shutdown delay time	Delay from ENA and ENB = low to I_{DX} = 0.1 × I_{DX} nom		20	25	µs

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers represent the most likely norm.
(3) Matching is the maximum difference from the average.
(4) The current source is connected internally between V_{IN} an V_{DX}. The voltage across the current source, (V_{IN} – V_{DX}), is referred to a headroom voltage (V_{HR}). Minimum headroom voltage is defined as the V_{HR} voltage when the LED current has dropped 20% from the value measured at V_{DX} = V_{IN} – 1 V.

6.6 LED Driver Typical Characteristics

T_J = 25°C. Unless otherwise noted, typical performance characteristics apply to the *Functional Block Diagram* with V_{IN} = 3.6 V, R_{ISET} = 32.4 kΩ, C_{IN} = 100 nF.

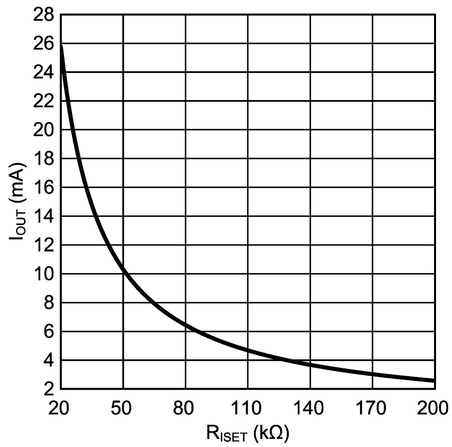


Figure 1. Output Current vs R_{ISET} (Expanded Range)

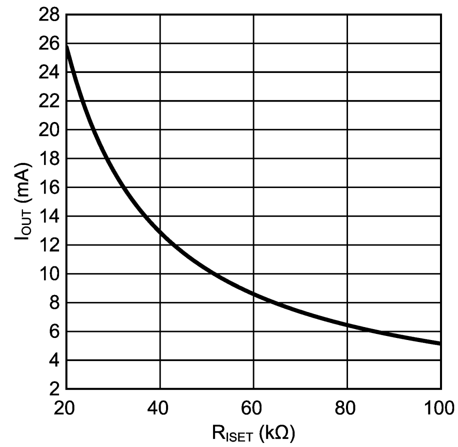


Figure 2. Output Current vs R_{ISET}

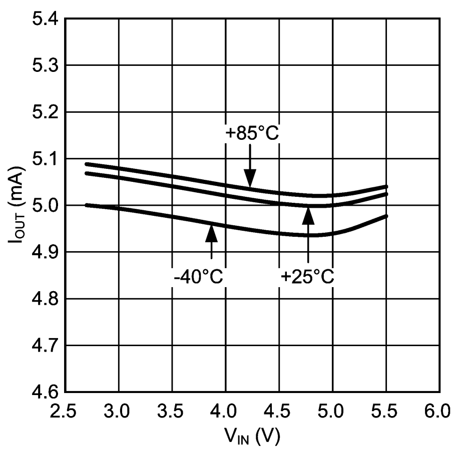


Figure 3. Output Current vs Input Voltage (ISET Connected to VDD)

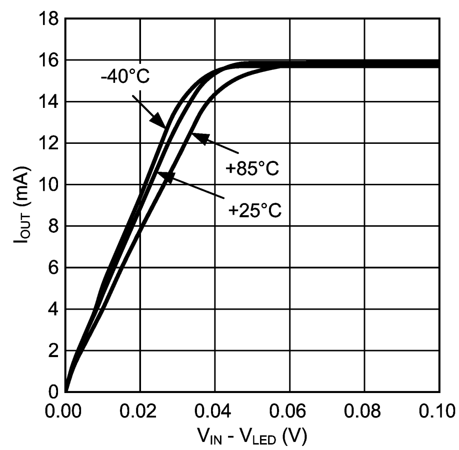


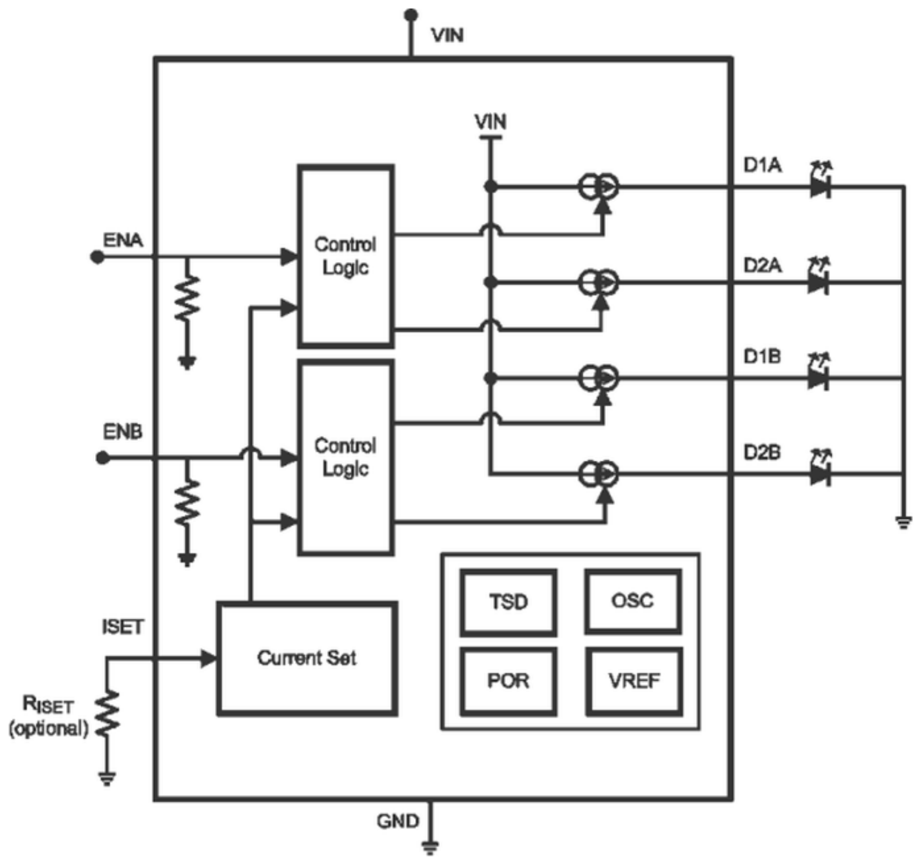
Figure 4. Output Current vs Headroom Voltage

7 Detailed Description

7.1 Overview

The LP5524 is an easy-to-use high side current source capable of driving 4 indicator LEDs with up to 25 mA per LED. The device operates over the 2.7-V to 5.5-V input voltage range. The output current is user-programmable via the optional external ISET resistor.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 LED

Forward voltage of LED must be less than minimum input voltage minus minimum headroom voltage (V_{HR}). For example with 2.7-V input voltage and 20-mA LED current the maximum LED forward voltage is 2.7 V – 100 mV = 2.6 V.

7.3.2 LED Headroom Voltage

A single current source is connected internally between VIN and DX outputs (D1A, D2A, D1B and D2B). The voltage across the current source, (V_{IN} – V_{DX}), is referred to as headroom voltage (V_{HR}). The current source requires a sufficient amount of headroom voltage to be present across it in order to regulate properly.

Figure 4 shows how output current of the LP5524 varies with respect to headroom voltage. On the flat part of the graph, the current is regulated properly as there is sufficient headroom voltage for regulation. On the sloping part of the graph the headroom voltage is too small, the current source is squeezed, and the current drive capability is limited. Thus, operating the LP5524 with insufficient headroom voltage across the current source must be avoided.

Feature Description (continued)

7.3.3 LED Outputs

If more than 25 mA of output current is required LED outputs can be connected parallel. Connecting LED outputs of different group parallel generates a simply two stage brightness control. With I_{DX} set to 25 mA, enabling one group sets the LED current to 25 mA. Enabling second bank increases the LED current to 50 mA. Unused LED outputs can be left floating or tied to VIN.

7.3.4 PWM Brightness Control

The brightness of LEDs can be linearly varied from zero up to the maximum programmed current level by applying a pulse–width–modulated signal to the ENx pin of the LP5524. The following procedures illustrate how to program the LED drive current and adjust the output current level using a PWM signal.

1. Determine the maximum desired LED current. Use Equation 1 to calculate R_{ISET}.
2. Brightness control can be implemented by pulsing a signal at the ENx pin. LED brightness is proportional to the duty cycle (D) of the PWM signal.

For linear brightness control over the full duty cycle adjustment range, the LP5524 uses a special turnoff time delay to compensate the turn–on time of the device.

If the PWM frequency is much less than 100 Hz, flicker may be seen in the LEDs. For the LP5524, zero duty cycle turns off the LEDs and a 50% duty cycle results in an average I_{DX} being half of the programmed LED current. For example, if R_{ISET} is set to program LED current to 15 mA, a 50% duty cycle results in an average I_{DX} of 7.5mA.

7.4 Device Functional Modes

7.4.1 Enable Mode

The LP5524 has four constant current LED outputs, which are split into two independently controlled banks. Each bank has its own enable input. ENA is used to control bank A and ENB is used to control bank B. Both enables are active high and have internal pulldown resistors. When both enables are low part is in low power standby mode. Driving either enable high activates the device and corresponding LED outputs.

7.4.2 ISET Pin

An external resistor (R_{ISET}) connected to ISET pin sets the output current of all the LEDs. The internal current mirror sets the LEDs output current with a 416:1 ratio to the current through R_{ISET}. Equation 1 approximates the LED current:

$$I_{DX} = 515 / R_{ISET} \text{ (Amps)} \quad (1)$$

The use of R_{ISET} is optional. If R_{ISET} is not used the ISET pin can be left floating or connected to V_{IN}. In these cases LED current is set to default current.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5524 device provides an easy-to-use solution for driving up to 4 indicator LEDs.

8.2 Typical Application

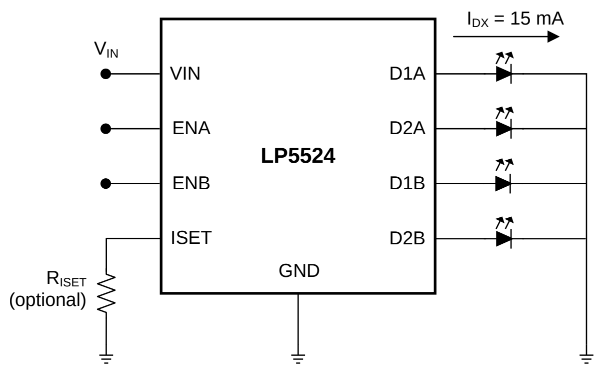

Figure 5. LP5524 Typical Application

8.2.1 Design Requirements

For typical LED-driver applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.7 V
ISET resistance	34 kΩ
Output current	60 mA
Maximum LED V_f	2.625 V

8.2.2 Detailed Design Procedure

8.2.2.1 Recommended External Components

8.2.2.1.1 Input Capacitor, C_{IN}

Although not required for normal operation, a capacitor can be added to V_{IN} to reduce line noise. TI recommends using a surface-mount multi-layer ceramic capacitor (MLCC). MLCCs with a X7R or X5R temperature characteristic are preferred.

Table 2. List Of Recommended External Components

PARAMETER		VALUE	UNIT	TYPE
C_{IN}	VDD bypass capacitor	100	nF	Ceramic, X7R or X5R
R_{ISET}	Current set resistor for 15.9-mA LED current	32.4	kΩ	1%
LEDs		User defined		

8.2.2.1.2 Current Set Resistor, R_{ISET}

If other than 5 mA current is required, R_{ISET} resistor can be used to adjust the current. For a 15.9-mA current a 32.4 kΩ resistor is required. Accuracy of the resistor directly effects to the accuracy of the LED current. TI recommends accuracy of 1% or better.

$$I_{DX} = 515 / R_{ISET} \text{ (Amps)} \quad (2)$$

Table 3. Recommended E96 Series (1% Tolerance) Current Set Resistors

R_{ISET} (kΩ)	I_{DX} (mA)	R_{ISET} (kΩ)	I_{DX} (mA)
169	3.0	34.0	15.1
127	4.1	32.4	15.9
102	5.0	30.1	17.1
84.5	6.1	28.7	17.9
73.2	7.0	26.7	19.3
64.9	7.9	25.5	20.2
56.2	9.2	24.3	21.2
51.1	10.1	23.2	22.2
46.4	11.1	22.1	23.3
42.2	12.2	21.5	24.0
39.2	13.1	20.5	25.1
36.5	14.1		

8.2.3 Application Curves

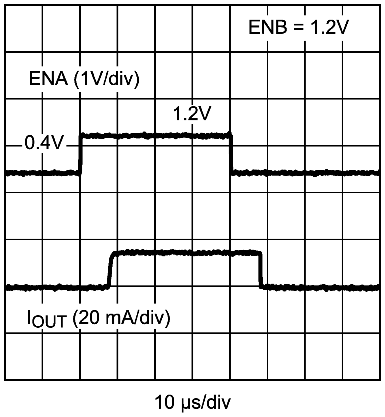

Figure 6. PWM Response (Both Channels)

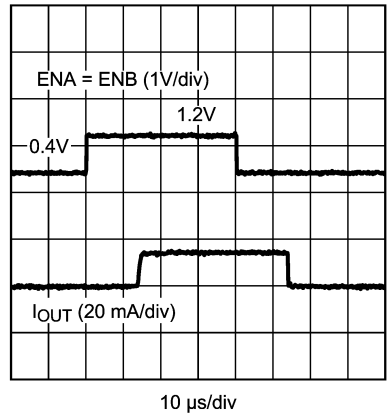

Figure 7. PWM Response (Single Channel)

9 Power Supply Recommendations

The LP5524 is designed to operate from an input supply range of 2.7 V to 5.5 V. This input supply must be well regulated and able to provide the peak current required by the LED configuration without voltage drop under load transients (enable on/off). The resistance of the input supply rail must be low enough such that the input current transient does not cause the LP5524 supply voltage to droop below 2.65 V. Additional bulk decoupling located close to the VIN pin may be required to minimize the impact of the input-supply-rail resistance.

10 Layout

10.1 Layout Guidelines

The LP5524 high-side current source outputs provide a fast load transient (350 nsec typical) to the external load. Design the PCB to provide a low resistive/inductive path to the VIN and GND pins. If the optional input capacitor (C_{IN}) is used, place it close to the LP5524 VIN and GND pins.

10.2 Layout Example

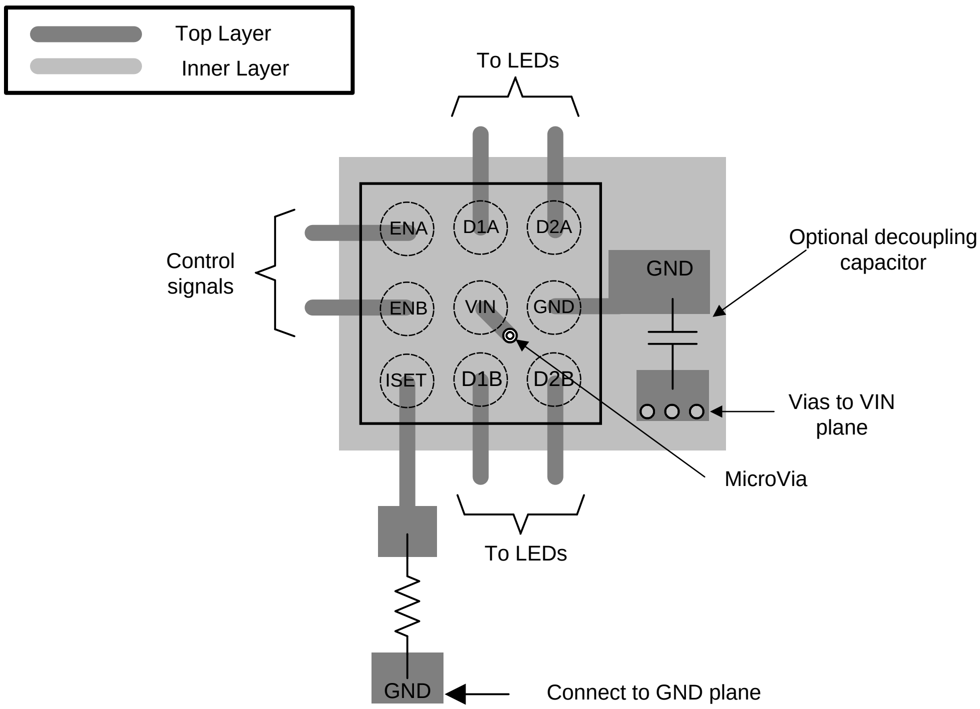

Figure 8. LP5524 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For additional information, see the following:

AN-1112 DSBGA Wafer Level Chip Scale Package

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5524TM-5/NOPB	ACTIVE	DSBGA	YFQ	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	V2	Samples
LP5524TMX-5/NOPB	ACTIVE	DSBGA	YFQ	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	V2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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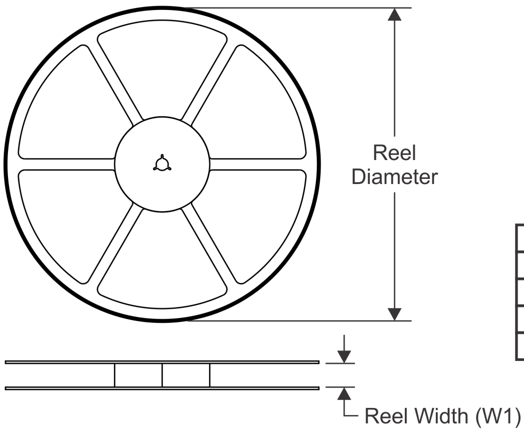
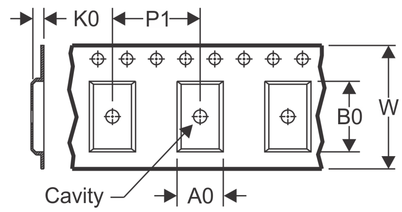
TAPE AND REEL INFORMATION

REEL DIMENSIONS

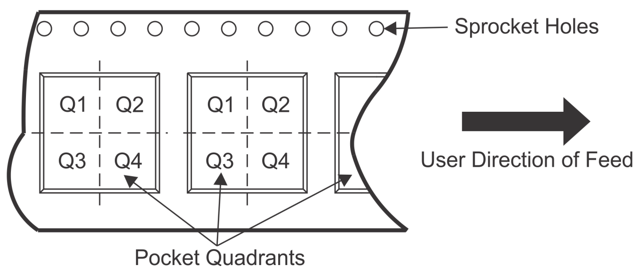


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

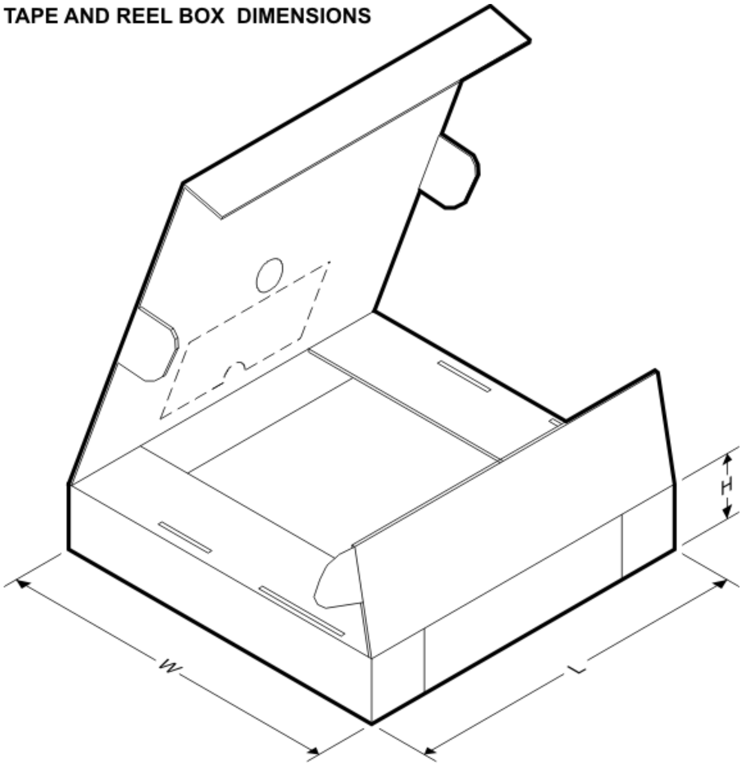
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5524TM-5/NOPB	DSBGA	YFQ	9	250	178.0	8.4	1.35	1.35	0.76	4.0	8.0	Q1
LP5524TMX-5/NOPB	DSBGA	YFQ	9	3000	178.0	8.4	1.35	1.35	0.76	4.0	8.0	Q1

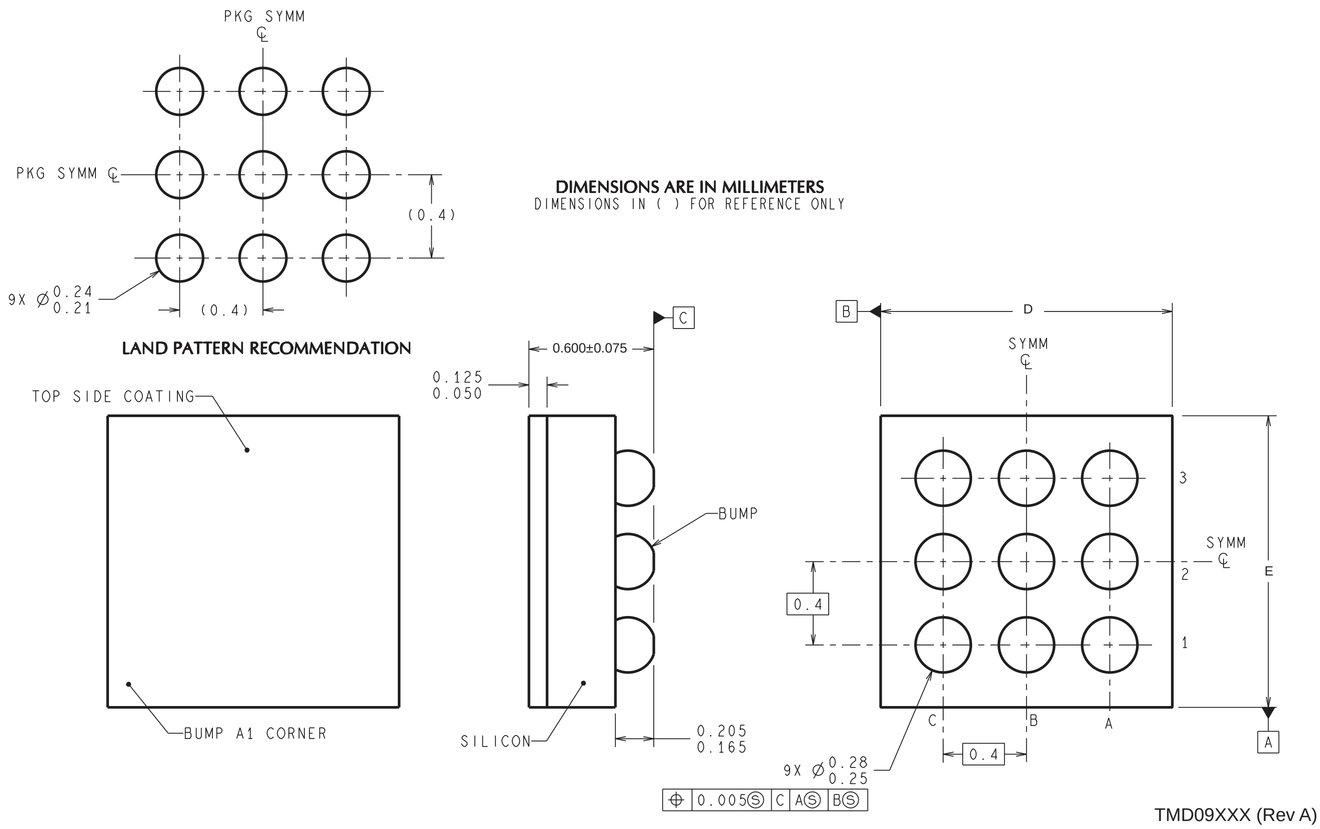
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5524TM-5/NOPB	DSBGA	YFQ	9	250	210.0	185.0	35.0
LP5524TMX-5/NOPB	DSBGA	YFQ	9	3000	210.0	185.0	35.0

YFQ0009



D: Max = 1.24 mm, Min = 1.18 mm

E: Max = 1.24 mm, Min = 1.18 mm

4215077/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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