



LP8551 High-Efficiency LED Backlight Driver for Notebooks

1 Features

- High-Voltage DC/DC Boost Converter with Integrated FET; Four Switching Frequency Options: 156/312/625/1250 kHz
- 2.7-V to 22-V Input Voltage Range to Support 1x to 5x Cell Li-Ion Batteries
- 50-mA High-Precision LED Current Sinks
- Adaptive LED Current Sink Headroom Control for Maximum System Efficiency
- Programmable PWM Resolution 8 to 13 Bits
- I²C and PWM Input Duty Cycle Brightness Control
- PWM Output Frequency and LED Current Set Through Resistors
- 4 LED Outputs with LED Fault (short/open) Detection
- Low Input Voltage, Overtemperature, Overcurrent Detection, and Shutdown
- Minimum Number of External Components

2 Applications

- Notebook and Tablet LCD Display LED Backlight
- LED Lighting

3 Description

The LP8551 is a white LED driver with integrated boost converter. It has four adjustable current sinks which can be controlled by PWM input or with I²C-compatible serial interface.

The boost converter has adaptive output voltage control based on the LED driver voltages. This feature minimizes the power consumption by adjusting the voltage to lowest sufficient level in all conditions.

LED outputs have 8-bit current resolution and up to 13-bit PWM resolution to achieve smooth and precise brightness control. Proprietary Phase Shift PWM control is used for LED outputs to reduce peak current from the boost converter, thus making the boost capacitors smaller. The Phase Shifting scheme also eliminates audible noise.

Internal EEPROM is used for storing the configuration data. This makes it possible to have minimum external component count and make the solution very small.

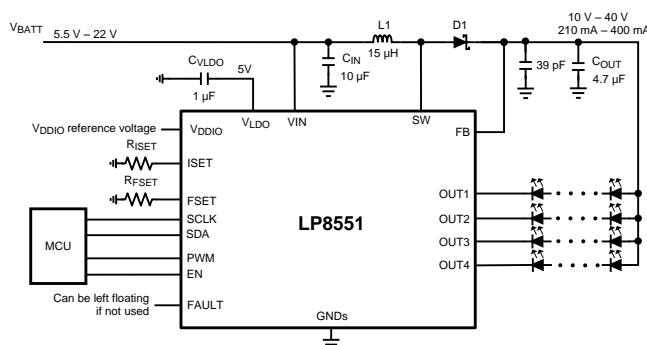
The LP8551 has safety features which make it possible to detect LED outputs with open or short fault. As well, low input voltage and boost overcurrent conditions are monitored, and chip is turned off in case of these events. Thermal de-rating function prevents overheating of the device by reducing backlight brightness when set temperature has been reached.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LP8551	DSBGA (25)	2.49 mm x 2.49 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



LED Drive Efficiency

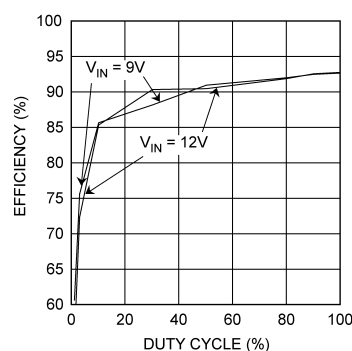


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2014) to Revision E	Page
<ul style="list-style-type: none"> Changed formatting to match new TI datasheet guidelines; added Device Information and Handling Ratings tables, Layout, and Device and Documentation Support sections; reformatted Functional Description to Detailed Description and Applications to Applications and Implementation sections, added note to beginning of Apps & Implementations section; moved some waveforms to new Applications Plots subsection. 	1

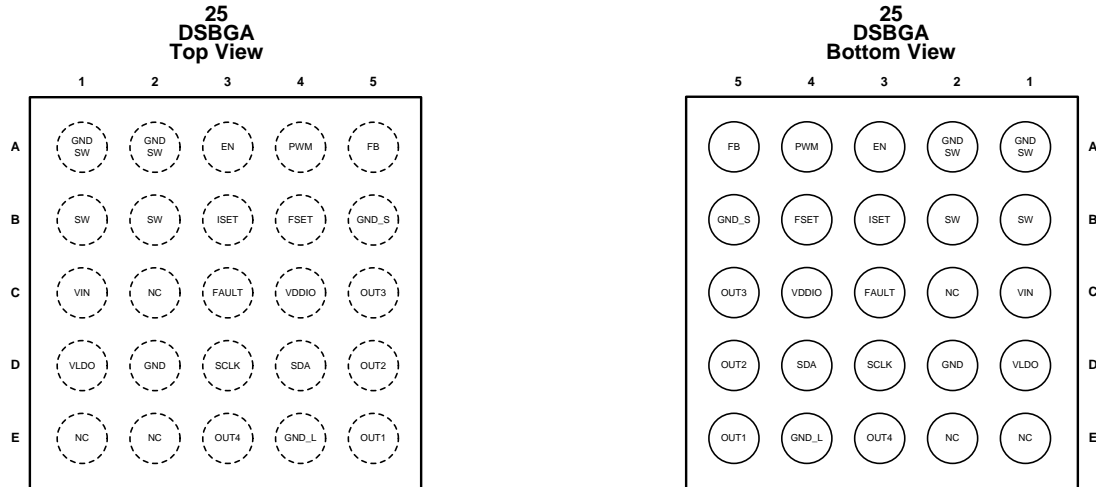
Changes from Revision C (April 2013) to Revision D	Page
<ul style="list-style-type: none"> Added EEPROM note 	24
<ul style="list-style-type: none"> Added EEPROM note 	28

5 Device Default Values

Table 1. Default EEPROM Memory Values

ADDRESS	DEFAULT VALUES LP8551
A0H	0111 1111
A1H	1011 0101
A2H	1010 1110
A3H	0111 1011
A4H	0010 0000
A5H	0000 1001
A6H	0000 0000
A7H	0000 0101

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NUMBER	NAME		
A1	GND_SW	G	Boost switch ground
A2	GND_SW	G	Boost switch ground
A3	EN	I	Enable input pin
A4	PWM	A	PWM dimming input. This pin must be connected to GND if not used.
A5	FB	A	Boost feedback input
B1	SW	A	Boost switch
B2	SW	A	Boost switch
B3	ISET	A	Set resistor for LED current. This pin can be left floating if not used.
B4	FSET	A	PWM frequency set resistor. This pin can be left floating if not used.
B5	GND_S	G	Signal ground
C1	VIN	P	Input power supply up to 22 V. If $2.7\text{ V} \leq V_{\text{BATT}} < 5.5\text{ V}$ (Figure 25) then an external 5-V rail must be used for V_{LDO} and V_{IN} .
C2	NC	-	Not connected
C3	FAULT	OD	Fault indication output. If not used, can be left floating.
C4	VDDIO	P	Digital IO reference voltage (1.65 V to 5 V) for I ² C interface. If brightness is controlled with PWM input pin then this pin can be connected to GND.
C5	OUT3	A	Current sink output
D1	VLDO	P	LDO output voltage. External 5-V rail can be connected to this pin in low voltage application.
D2	GND	G	Ground
D3	SCLK	I	Serial clock. This pin must be connected to GND if not used.
D4	SDA	I/O	Serial data. This pin must be connected to GND if not used.
D5	OUT2	A	Current sink output
E1	NC	-	Not connected
E2	NC	-	Not connected
E3	OUT4	A	Current sink output
E4	GND_L	G	LED ground
E5	OUT1	A	Current sink output

(1) A: Analog Pin, G: Ground Pin, P: Power Pin, I: Input Pin, I/O: Input/Output Pin, O: Output Pin, OD: Open Drain Pin

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

	MIN	MAX	UNIT
V _{IN}	–0.3	24	V
V _{LDO}	–0.3	6	
Voltage on logic pins (PWM, EN, SCLK, SDA)	–0.3	6	
Voltage on logic pin (FAULT)	–0.3	to VDDIO + 0.3	
Voltage on analog pins (VDDIO, ISET, FSET)	–0.3	6	
V (OUT1...OUT4, SW, FB)	–0.3	44	
Continuous power dissipation ⁽²⁾	Internally limited		
Junction temperature (T _{J-MAX})		125	°C
Maximum lead temperature (soldering) ⁽³⁾			

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).
- (3) For detailed soldering specifications and information, please refer to TI's AN-1112 ([SNVA009](#)): *DSBGA Wafer Level Chip Scale Package*.

7.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		−65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	−2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	−1000	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions ⁽¹⁾⁽²⁾

Over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage (V _{IN}) (Figure 22)	5.5		22	V
Input voltage (V _{IN} + V _{LDO}) (Figure 25)	4.5		5.5	
V _{DDIO}	1.65		5	
V(OUT1 to OUT4, SW, FB)	0		40	
Junction temperature (T _J)	–30		125	°C
Ambient temperature (T _A) ⁽³⁾	–30		85	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pins.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} – (R_{θJA} × P_{D-MAX}).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DSBGA (YZR)	UNIT
		25 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽²⁾	40 to 73	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

7.5 Electrical Characteristics⁽¹⁾⁽²⁾

Limits are for $T_A = 25^\circ\text{C}$ and $V_{IN} = 12\text{ V}$, $V_{DDIO} = 2.8\text{ V}$, $C_{VLDO} = 1\text{ }\mu\text{F}$, $L1 = 15\text{ }\mu\text{H}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, unless otherwise specified. $R_{ISET} = 16\text{ k}\Omega$ ⁽³⁾

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN}	Standby supply current	Internal LDO disabled EN=L and PWM=L			1 ⁽⁴⁾	μA
	Normal mode supply current	LDO enabled, boost enabled, no current going through LED outputs 5-MHz PLL Clock		3		mA
		10-MHz PLL Clock		3.7		
		20-MHz PLL Clock		4.7		
		40-MHz PLL Clock		6.7		
f_{OSC}	Internal oscillator frequency accuracy		-4% -7% ⁽⁴⁾		4% 7% ⁽⁴⁾	
V_{LDO}	Internal LDO voltage		4.5 ⁽⁴⁾	5	5.5 ⁽⁴⁾	V
I_{LDO}	Internal LDO external loading				5	mA

(1) All voltages are with respect to the potential at the GND pins.

(2) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis. Typical numbers are not specified, but do represent the most likely norm.

(3) Low-ESR surface-mount ceramic capacitors (MLCCs) used in setting electrical characteristics.

(4) Limits apply over the full operating ambient temperature range ($-30^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$).

7.6 Boost Converter Electrical Characteristics

Limits are for $T_A = 25^\circ\text{C}$ and $V_{IN} = 12\text{ V}$, $V_{DDIO} = 2.8\text{ V}$, $C_{VLDO} = 1\text{ }\mu\text{F}$, $L1 = 15\text{ }\mu\text{H}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, unless otherwise specified. $R_{ISET} = 16\text{ k}\Omega$ ⁽¹⁾

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS_{ON}}$	Switch ON resistance	$I_{SW} = 0.5\text{ A}$		0.12		Ω
V_{MAX}	Boost maximum output voltage			40		V
I_{LOAD}	Maximum continuous load current	$9\text{ V} \leq V_{BATT}$, $V_{OUT} = 35\text{ V}$		450		mA
		$6\text{ V} \leq V_{BATT}$, $V_{OUT} = 35\text{ V}$		300		
		$3\text{ V} \leq V_{BATT}$, $V_{OUT} = 25\text{ V}$		180		
V_{OUT}/V_{IN}	Conversion ratio	$f_{SW} = 1.25\text{ MHz}$			10	
f_{SW}	Switching frequency	BOOST_FREQ = 00 BOOST_FREQ = 01 BOOST_FREQ = 10 BOOST_FREQ = 11		156 312 625 1250		kHz
V_{OV}	Overvoltage protection voltage			$V_{BOOST} + 1.6\text{ V}$		V
t_{PULSE}	Switch pulse minimum width	no load		50		ns
$t_{STARTUP}$	Start-up time	See ⁽²⁾		6		ms
I_{MAX}	SW pin current limit	IMAX_SEL = 0		1.4		A
		IMAX_SEL = 1		2.5		

(1) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

(2) Start-up time is measured from the moment boost is activated until the V_{OUT} crosses 90% of its target value.

7.7 LED Driver Electrical Characteristics

Limits are for $T_A = 25^\circ\text{C}$ and $V_{IN} = 12\text{ V}$, $V_{DDIO} = 2.8\text{ V}$, $C_{VLDO} = 1\text{ }\mu\text{F}$, $L1 = 15\text{ }\mu\text{H}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, unless otherwise specified. $R_{ISET} = 16\text{ k}\Omega^{(1)}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAKAGE}$	Leakage current	Outputs OUT1...OUT4, $V_{OUT} = 40\text{ V}$		0.1	1	μA
I_{MAX}	Maximum source current OUT1...OUT4	EN_I_RES = 0, CURRENT[7:0] = FFh		30		mA
		EN_I_RES = 1, CURRENT[7:0] = FFh		50		
I_{OUT}	Output current accuracy ⁽²⁾	Output current set to 23 mA, EN_I_RES = 1	-3% -4% ⁽³⁾		3% 4% ⁽³⁾	
I_{MATCH}	Matching ⁽²⁾	Output current set to 23 mA, EN_I_RES = 1		0.5%		
PWM_{RES}	PWM output resolution ⁽⁴⁾	$f_{LED} = 5\text{ kHz}$, $f_{PLL} = 5\text{ MHz}$		10		bits
		$f_{LED} = 10\text{ kHz}$, $f_{PLL} = 5\text{ MHz}$		9		
		$f_{LED} = 20\text{ kHz}$, $f_{PLL} = 5\text{ MHz}$		8		
		$f_{LED} = 5\text{ kHz}$, $f_{PLL} = 40\text{ MHz}$		13		
		$f_{LED} = 10\text{ kHz}$, $f_{PLL} = 40\text{ MHz}$		12		
		$f_{LED} = 20\text{ kHz}$, $f_{PLL} = 40\text{ MHz}$		11		
f_{LED}	LED switching frequency ⁽⁴⁾	PWM_FREQ[4:0] = 00000b PLL clock 5 MHz		600		Hz
		PWM_FREQ[4:0] = 11111b PLL clock 5 MHz		19.2k		
V_{SAT}	Saturation voltage ⁽⁵⁾	Output current set to 20 mA		105	220 ⁽³⁾	mV
		Output current set to 30 mA		160	290 ⁽³⁾	

(1) Low-ESR surface-mount ceramic capacitors (MLCCs) used in setting electrical characteristics.

(2) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUT1 to OUT4), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN)/AVG. The largest number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts. Note that some manufacturers have different definitions in use.

(3) Limits apply over the full operating ambient temperature range ($-30^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$).

(4) PWM output resolution and frequency depend on the PLL settings. Please see section [PWM Frequency Setting](#) for full description.

(5) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1 V.

7.8 PWM Interface Characteristics

Limits are for $T_A = 25^\circ\text{C}$ and $V_{IN} = 12\text{ V}$, $V_{DDIO} = 2.8\text{ V}$, $C_{VLDO} = 1\text{ }\mu\text{F}$, $L1 = 15\text{ }\mu\text{H}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, unless otherwise specified. $R_{ISET} = 16\text{ k}\Omega^{(1)}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PWM}	PWM frequency range		0.1		25	kHz
t_{MIN_ON}	Minimum pulse ON time			1		μs
t_{MIN_OFF}	Minimum pulse OFF time			1		
$t_{STARTUP}$	Turnon delay from standby to backlight on	PWM input active, EN pin rise from low to high		6		ms
T_{STBY}	Turnoff Delay	PWM input low time for turn off, slope disabled		50		ms
PWM_{RES}	PWM Input Resolution	$f_{IN} < 9\text{ kHz}$		10		bits
		$f_{IN} < 4.5\text{ kHz}$		11		
		$f_{IN} < 2.2\text{ kHz}$		12		
		$f_{IN} < 1.1\text{ kHz}$		13		

(1) Low-ESR surface-mount ceramic capacitors (MLCCs) used in setting electrical characteristics.

7.9 Undervoltage Protection

Limits are for $T_A = 25^\circ\text{C}$ and $V_{IN} = 12\text{ V}$, $V_{DDIO} = 2.8\text{ V}$, $C_{VLDO} = 1\text{ }\mu\text{F}$, $L1 = 15\text{ }\mu\text{H}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, unless otherwise specified. $R_{ISET} = 16\text{ k}\Omega^{(1)}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	V_{IN} UVLO Threshold Voltage	UVLO[1:0] = 00	Disabled			V
		UVLO[1:0] = 01, falling	2.55	2.70	2.94	
		UVLO[1:0] = 01, rising	2.62	2.76	3.00	
		UVLO[1:0] = 10, falling	5.11	5.40	5.68	
		UVLO[1:0] = 10, rising	5.38	5.70	5.98	
		UVLO[1:0] = 11, falling	7.75	8.10	8.45	
		UVLO[1:0] = 11, rising	8.36	8.73	9.20	

(1) Low-ESR surface-mount ceramic capacitors (MLCCs) used in setting electrical characteristics.

7.10 Logic Interface Characteristics

Limits apply over the full operating ambient temperature range ($-30^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$), and $V_{IN} = 12\text{ V}$, $V_{DDIO} = 2.8\text{ V}$, $C_{VLDO} = 1\text{ }\mu\text{F}$, $L1 = 15\text{ }\mu\text{H}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, unless otherwise specified. $R_{ISET} = 16\text{ k}\Omega^{(1)}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT EN						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.2			V
I_I	Input current		-1		1	μA
LOGIC INPUT PWM						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		2.2			V
I_I	Input current		-1		1	μA
LOGIC INPUTS SCL, SDA						
V_{IL}	Input low level				$0.2 \times V_{DDIO}$	V
V_{IH}	Input high level		$0.8 \times V_{DDIO}$			V
I_I	Input current					μA
LOGIC OUTPUTS SDA, FAULT						
V_{OL}	Output low level	$I_{OUT} = 3\text{ mA}$ (pullup current)		$0.3^{(2)}$	0.5	V
I_L	Output leakage current	$V_{OUT} = 2.8\text{ V}$	-1		1	μA

(1) Low-ESR surface-mount ceramic capacitors (MLCCs) used in setting electrical characteristics.

(2) Limits are $T_A = 25^\circ\text{C}$.

7.11 I²C Serial Bus Timing Parameters (SDA, SCLK)⁽¹⁾

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCLK}	Clock frequency		400	kHz
1	Hold time (repeated) START condition	0.6		μ s
2	Clock low time	1.3		μ s
3	Clock high time	600		ns
4	Setup time for a repeated START condition	600		ns
5	Data hold time	50		ns
6	Data setup time	100		ns
7	Rise time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall time of SDA and SCL	$15+0.1C_b$	300	ns
9	Setup time for STOP condition	600		ns
10	Bus free time between a STOP and a START condition	1.3		μ s
C_b	Capacitive load parameter for each bus line Load of 1 pF corresponds to 1 ns.	10	200	ns

(1) Specified by design. $V_{DDIO} = 1.65$ V to 5.5 V.

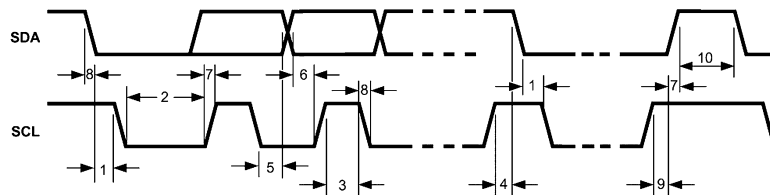


Figure 1. I²C Timing Parameters

7.12 Typical Characteristics

Unless otherwise specified: $V_{BATT} = 12\text{ V}$, $C_{VLD0} = 1\text{ }\mu\text{F}$, $L1 = 33\text{ }\mu\text{H}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$.

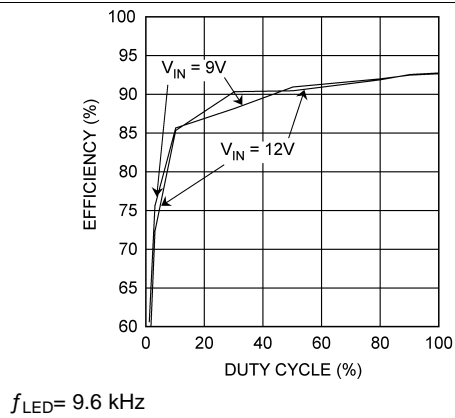


Figure 2. LED Drive Efficiency

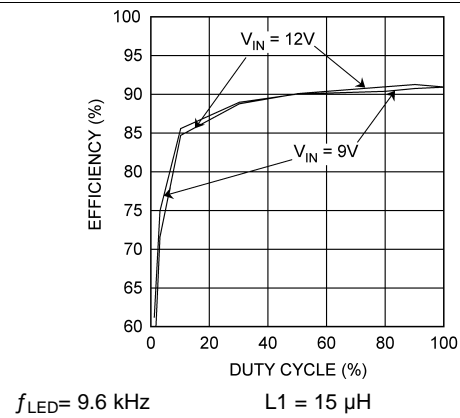


Figure 3. LED Drive Efficiency

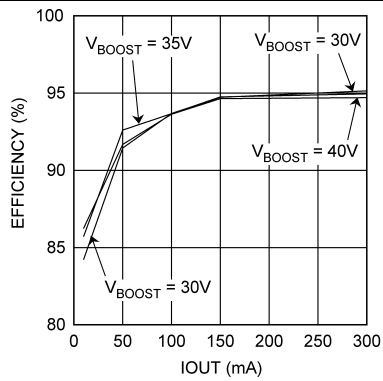


Figure 4. Boost Converter Efficiency

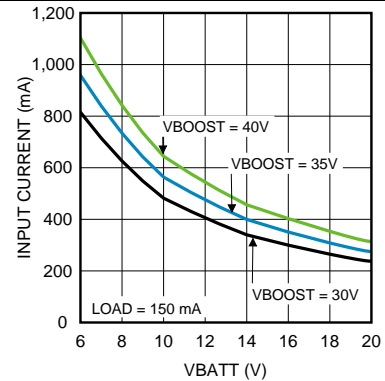


Figure 5. Battery Current

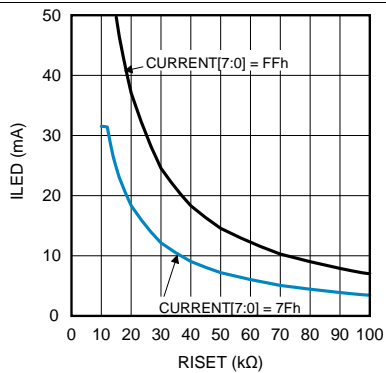


Figure 6. I_{LED} vs. R_{ISET}

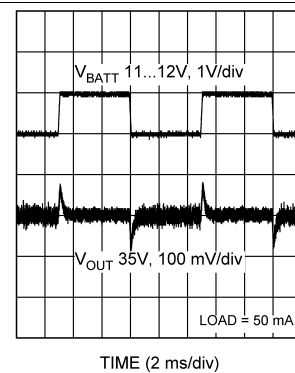


Figure 7. Boost Line Transient Response

8.3 Feature Description

8.3.1 Clock Generation

The LP8551 has internal 5-MHz oscillator which is used for clocking the boost converter, state machine, PWM outputs, PWM input duty cycle measurement, internal timings such as slope time for output brightness changes.

For PWM output generation the 5-MHz clock can be multiplied with the internal PLL to achieve higher resolution. The higher the clock frequency for PWM generation block, the higher the resolution but the tradeoff is higher I_Q of the part. Clock multiplication is set with <PWM_RESOLUTION[1:0]> EEPROM Bits.

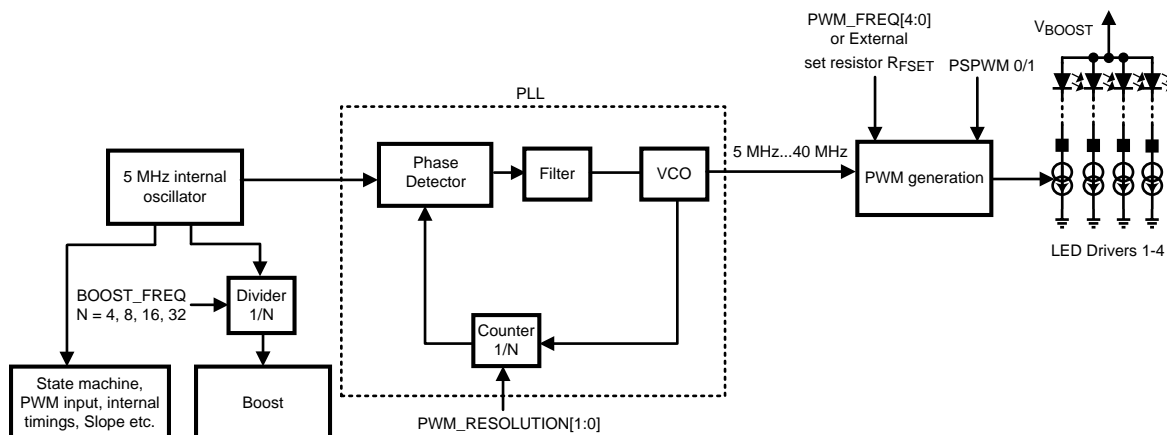


Figure 8. Principle of the Clock Generation

8.3.2 Brightness Control Methods

The LP8551 controls the brightness of the backlight with PWM. PWM control is received either from PWM input pin or from I²C register bits. The PWM source selection is done with <BRT_MODE[1:0]> bits as follows:

BRT_MODE[1]	BRT_MODE[0]	PWM SOURCE
0	0	PWM input pin duty cycle control. Default.
0	1	PWM input pin duty cycle control.
1	0	Brightness register
1	1	PWM direct control (PWM in = PWM out)

8.3.2.1 PWM Input Duty Cycle

With PWM input pin duty cycle control the output PWM is controlled by PWM input duty cycle. PWM detector block measures the duty cycle in the PWM pin and uses this 13-bit value to generate the output PWM. Output PWM can have different frequency than input in this mode and also phase shift PWM mode can be used. Slope is effective in this mode. PWM input resolution is defined by the input PWM clock frequency.

8.3.2.2 Brightness Register Control

With brightness register control the output PWM is controlled with 8-bit resolution <BRT7:0> register bits. Phase shift scheme can be used with this, and the output PWM frequency can be freely selected. Slope is effective in this mode.

8.3.2.3 PWM Direct Control

With PWM direct control the output PWM directly follows the input PWM. Due to the internal logic structure the input is anyway clocked with the 5 MHz clock or the PLL clock. PSPWM mode is not possible in this mode. Slope is not effective in this mode.

8.3.2.4 PWM Calculation Data Flow

Figure 9 shows the PWM calculation data flow. In PWM direct control mode most of the blocks are bypassed, and this flow chart does not apply.

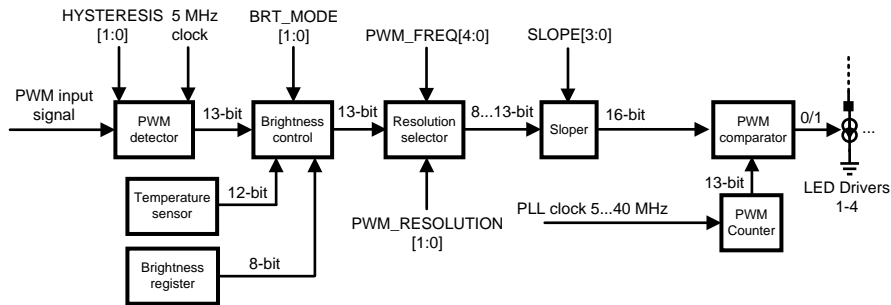


Figure 9. PWM Calculation Data Flow

8.3.2.5 PWM Detector

The PWM detector block measures the duty cycle of the input PWM signal. Resolution depends on the input signal frequency. Hysteresis selection sets the minimum allowable change to the input. If smaller change is detected, it is ignored. With hysteresis the constant changing between two brightness values is avoided if there is small jitter in the input signal.

8.3.2.6 Brightness Control

Brightness control block gets 13-bit value from the PWM detector, 12-bit value from the temperature sensor, and also 8-bit value from the brightness register. <BRT_MODE[1:0]> selects whether to use PWM input duty cycle value or the brightness register value as described earlier. Based on the temperature sensor value the duty cycle is reduced if the temperature has reached the temperature limit set to the <TEMP_LIM[1:0]> EEPROM bits.

8.3.2.7 Resolution Selector

Resolution selector takes the necessary MSB bits from the input data to match the output resolution. For example if 11-bit resolution is used for output, then 11 MSB bits are selected from the input.

8.3.2.8 Sloper

Sloper makes the smooth transition from one brightness value to another. Slope time can be adjusted from 0 to 500 ms with <SLOPE[3:0]> EEPROM bits. The sloper output is 16-bit value.

8.3.2.9 PWM Comparator

The PWM counter clocks the PWM comparator based on the duty cycle value. Output of the PWM comparator controls directly the LED drivers. If PSPWM mode is used, then the signal to each LED output is delayed certain amount.

8.3.2.10 Current Setting

Maximum current of the LED outputs is controlled with CURRENT[7:0] EEPROM register bits linearly from 0 to 30 mA. If <EN_I_RES> = 1 the maximum LED output current can be scaled also with external resistor, R_{ISET} . R_{ISET} controls the LED current as follows:

$$I_{LED} = \frac{600 * 1.23V}{R_{ISET}} * \frac{CURRENT [7:0]}{255} \quad (1)$$

Default value for CURRENT[7:0] = 7Fh (127d). Therefore, the output current can be calculated as follows:

$$R_{ISET} = \frac{600 * 1.23}{I_{LED}} * \frac{1}{2} = \frac{369}{I_{LED}} \quad (2)$$

For example, if a 16-kΩ R_{ISET} resistor is used, then the LED maximum current is 23 mA.

NOTE

Formula is only approximation for the actual current.

8.3.2.11 PWM Frequency Setting

PWM frequency is selected with PWM_FREQ[4:0] EEPROM register. If PLL clock frequency multiplication is used, it affects the output PWM frequency as well. <PWM_RESOLUTION[1:0]> EEPROM bits select the PLL output frequency and hence the PWM frequency and resolution. PWM resolution setting affects the PLL clock frequency (5 MHz to 40 MHz). Highlighted frequencies with boldface can be selected also with external resistor R_{FSET} . To activate R_{FSET} frequency selection the <EN_F_RES> EEPROM bit must be 1.

PWM_RES[1:0]	00	01	10	11	RESOLUTION (BITS)
PWM_FREQ[4:0]	5 MHz	10 MHz	20 MHz	40 MHz	
11111	19232	-	-	-	8
11110	16828	-	-	-	8
11101	14424	-	-	-	8
11100	12020	-	-	-	8
11011	9616	19232	-	-	9
11010	7963	15927	-	-	9
11001	6386	12771	-	-	9
11000	4808	9616	19232	-	10
10111	4658	9316	18631	-	10
10110	4508	9015	18030	-	10
10101	4357	8715	17429	-	10
10100	4207	8414	16828	-	10
10011	4057	8114	16227	-	10
10010	3907	7813	15626	-	10
10001	3756	7513	15025	-	10
10000	3606	7212	14424	-	10
01111	3456	6912	13823	-	10
01110	3306	6611	13222	-	10
01101	3155	6311	12621	-	10
01100	3005	6010	12020	-	10
01011	2855	5710	11419	-	10
01010	2705	5409	10818	-	10
01001	2554	5109	10217	-	10
01000	2404	4808	9616	19232	11
00111	2179	4357	8715	17429	11
00110	1953	3907	7813	15626	11
00101	1728	3456	6912	13823	11
00100	1503	3005	6010	12020	11
00011	1202	2404	4808	9616	12
00010	1052	2104	4207	8414	12
00001	826	1653	3306	6611	12
00000	601	1202	2404	4808	13

R_{FSET} resistance values with corresponding PWM frequencies:

PWM_RES[1:0]	00		01		10		11	
RFSET (kΩ)	5 MHz CLOCK	RESOLUTION	10 MHz CLOCK	RESOLUTION	20 MHz CLOCK	RESOLUTION	40 MHz CLOCK	RESOLUTION
10...15	19232	8	19232	9	19232	10	19232	11
26...29	16828	8	15927	9	16227	10	17429	11
36...41	14424	8	12771	9	14424	10	15626	11
50...60	12020	8	9616	10	12020	10	12020	11
85...100	9616	9	8715	10	9616	11	9616	12
135...150	7963	9	7813	10	7813	11	8414	12
200...300	6386	9	6311	10	6010	11	6811	12
450...	4808	10	4808	11	4808	12	4808	13

8.3.2.12 Phase Shift PWM (PSPWM) Scheme

The PSPWM scheme allows delaying the time when each LED output is active. When the LED output are not activated simultaneously, the peak load current from the boost output is greatly decreased. This reduces the ripple seen on the boost output and allows smaller output capacitors. Reduced ripple also reduces the output ceramic capacitor audible ringing. PSPWM scheme also increases the load frequency seen on boost output by x4 and therefore transfers the possible audible noise to so high frequency that human ear cannot hear it.

Description of the PSPWM mode is seen on the following diagram. PSPWM mode is enabled by setting <EN_PSPWM> EEPROM bit to 1. Shift time is the delay between outputs and it is defined as $1 / (f_{PWM} \times 4)$. If the <EN_PSPWM> bit is 0, then the delay is 0 and all outputs are active simultaneously.

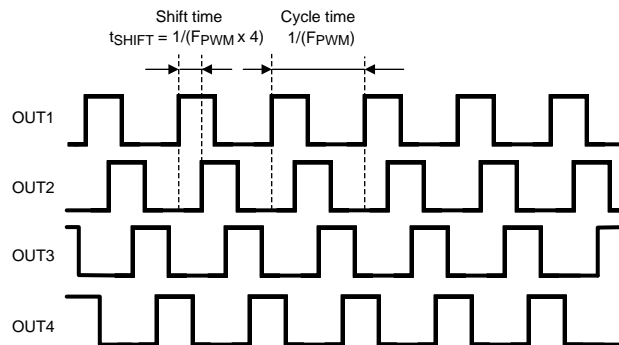


Figure 10. PSPWM Mode

8.3.2.13 Slope

Slope time can be programmed with EEPROM bits <SLOPE[3:0]> from 0 to 500 ms. The same slope time is used for sloping up and down. Advanced slope makes brightness changes smooth for eye.

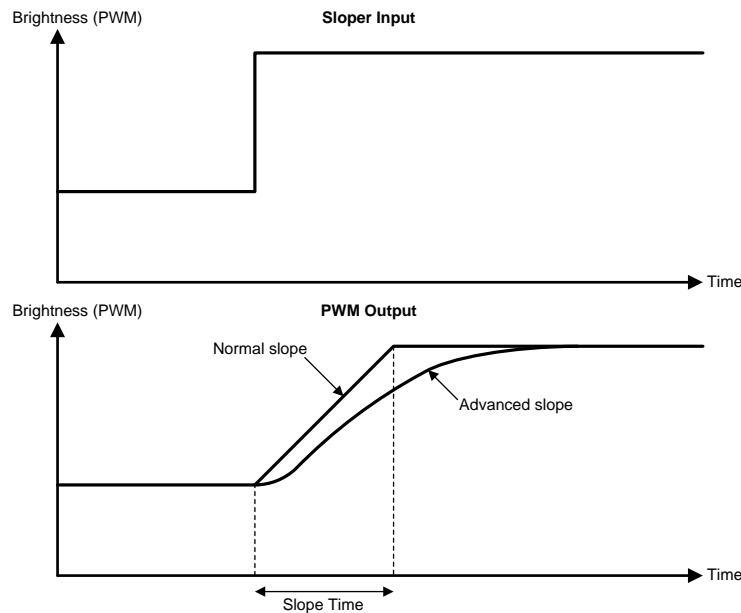


Figure 11. Sloper Operation

8.3.2.14 Driver Headroom Control

Driver headroom can be controlled with `<DRV_HEADR[2:0]>` EEPROM bits. Driver headroom control sets the minimum threshold for the voltage over the LED output which has the smallest driver headroom and controls the boost output voltage accordingly. Boost output voltage step size is 125 mV. The LED output which has the smallest forward voltage is the one which has highest V_F across the LEDs. The strings with highest forward voltage is detected automatically. To achieve best possible efficiency smallest possible headroom voltage should be selected. If there is high variation between LED strings, the headroom can be raised slightly to prevent any visual artifacts.

8.3.3 Boost Converter

8.3.3.1 Operation

The LP8551 boost DC/DC converter generates a 10-V to 40-V supply voltage for the LEDs from 2.7-V to 22-V input voltage. The output voltage can be controlled either with EEPROM register bits `<VBOOST[4:0]>` or automatic adaptive voltage control can be used. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. The topology of the magnetic boost converter is called CPM (current programmed mode) control, where the inductor current is measured and controlled with the feedback. Switching frequency is selectable between 156 kHz and 1.25 MHz with EEPROM bit `<BOOST_FREQ[1:0]>`. When `<EN_BOOST>` EEPROM register bit is set to 1, then boost activates automatically when backlight is enabled.

In adaptive mode the boost output voltage is adjusted automatically based on LED driver headroom voltage. Boost output voltage control step size is, in this case, 125 mV, to ensure as small as possible driver headroom and high efficiency. Enabling the adaptive mode is done with `<EN_ADAPT>` EEPROM bit. If boost is started with adaptive mode enabled, then the initial boost output voltage value is defined with the `<VBOOST[4:0]>` EEPROM register bits in order to eliminate long output voltage iteration time when boost is started for the first time. [Figure 12](#) shows the boost topology with the protection circuitry:

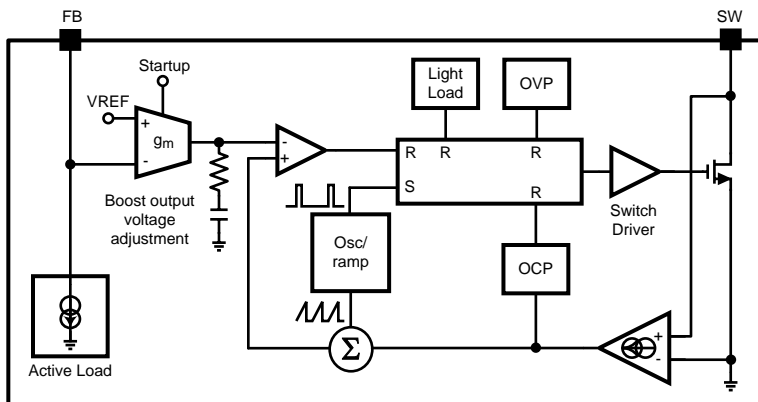


Figure 12. Boost Topology with Protection Circuitry

8.3.3.2 Protection

Three different protection schemes are implemented:

1. Overvoltage protection, limits the maximum output voltage.
 - Overvoltage protection limit changes dynamically based on output voltage setting.
 - Keeps the output below breakdown voltage.
 - Prevents boost operation if battery voltage is much higher than desired output.
2. Overcurrent protection, limits the maximum inductor current.
3. Duty cycle limiting.

8.3.3.3 Manual Output Voltage Control

User can control the boost output voltage with <VBOOST[4:0]> EEPROM register bits when adaptive mode is disabled.

VBOOST[4:0]		VOLTAGE (TYPICAL)
BIN	DEC	VOLTS
00000	0	10
00001	1	11
00010	2	12
00011	3	13
00100	4	14
...
11101	29	39
11110	30	40
11111	31	40

8.3.3.4 Adaptive Boost Control

Adaptive boost control function adjusts the boost output voltage to the minimum sufficient voltage for proper LED driver operation. The output with highest V_F LED string is detected and boost output voltage adjusted accordingly. Driver headroom can be adjusted with <DRIVER_HEADR[2:0]> EEPROM bits from approximately 300 mV to 1200 mV. Boost adaptive control voltage step size is 125 mV. Boost adaptive control operates similarly with and without PSPWM.

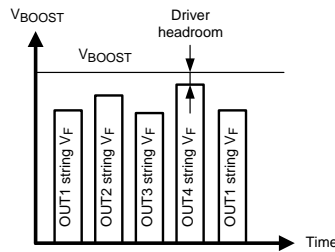


Figure 13. Boost Adaptive Control Principle with PSPWM

8.3.4 Fault Detection

The LP8551 has fault detection for LED fault, low-battery voltage, overcurrent, and thermal shutdown. The open drain output pin (FAULT) can be used to indicate occurred fault. The cause for the fault can be read from status register. Reading the fault register also resets the fault. Setting the EN pin low also resets the faults, even if an external 5-V line is used to power VLDO pin.

8.3.4.1 LED Fault Detection

With LED fault detection, the voltages across the LED drivers are constantly monitored. LED fault detection is enabled with <EN_LED_FAULT> EEPROM bit. Shorted or open LED string is detected.

If LED fault is detected:

- The corresponding LED string is taken out of boost adaptive control loop;
- Fault bits are set in the fault register to identify whether the fault has been open/short and how many strings are faulty; and
- Fault open-drain pin is pulled down.

LED fault sensitivity can be adjusted with <LED_FAULT_THR> EEPROM bit which sets the allowable variation between LED output voltage to 3.3 V or 5.3 V. Depending on application and how much variation there can be in normal operation between LED string forward voltages this setting can be adjusted.

Fault is cleared by setting EN pin low or by reading the fault register.

8.3.4.2 Undervoltage Detection

The LP8551 has detection for too-low VIN voltage. Threshold level for the voltage is set with EEPROM register bits as seen in [Table 2](#):

Table 2.

UVLO[1:0]	THRESHOLD (V)
00	OFF
01	2.7V
10	5.4V
11	8.1V

When undervoltage is detected, the LED outputs and boost shut down, the FAULT pin is pulled down, and corresponding fault bit is set in fault register. LEDs and boost starts again when the voltage has increased above the threshold level. Hysteresis is implemented to threshold level to avoid continuous triggering of fault when threshold is reached.

Fault is cleared by setting EN pin low or by reading the fault register.

8.3.4.3 Overcurrent Protection

The LP8551 has detection for too-high loading on the boost converter. When overcurrent fault is detected, the LP8551 shuts down.

Fault is cleared by setting EN pin low or by reading the fault register.

8.3.4.4 Device Thermal Regulation

The LP8551 has an internal temperature sensor which can be used to measure the junction temperature of the device and protect the device from overheating. During thermal regulation, LED PWM is reduced by 2% of full scale per °C whenever the temperature threshold is reached. Temperature regulation is enabled automatically when chip is enabled. 11-bit temperature value can be read from Temp MSB and Temp LSB registers, MSB should be read first. Temperature limit can be programmed in EEPROM as shown in the following table.

Thermal regulation function does not generate fault signal.

TEMP_LIM[1:0]	OVER-TEMP LIMIT (°C)
00	OFF
01	110
10	120
11	130

8.3.4.5 Thermal Shutdown

If the LP8551 reaches thermal shutdown temperature (150°C), the LED outputs and boost shut down to protect it from damage. Also the FAULT pin is pulled down to indicate the fault state. The device activates again when temperature drops below 130°C degrees.

Fault is cleared by setting EN pin low or by reading the fault register.

8.4 Device Functional Modes

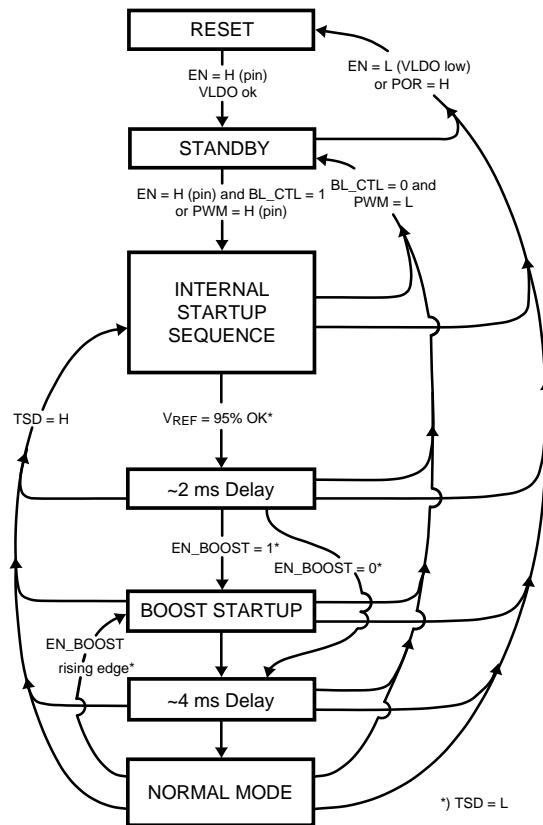


Figure 14. Modes of Operation

8.4.1 Modes of Operation

- RESET:** In the RESET mode all the internal registers are reset to the default values. Reset is entered always when V_{LDO} voltage is low. EN pin is enable for the internal LDO. Power On Reset (POR) activates during the chip startup or when the supply voltage V_{LDO} fall below POR level. Once V_{LDO} rises above POR level, POR inactivates, and the chip continues to the STANDBY mode.
- STANDBY:** The STANDBY mode is entered if the register bit BL_CTL is LOW and external PWM input is not active and POR is not active. This is the low power consumption mode, when only internal 5-V LDO is enabled. Registers can be written in this mode and the control bits are effective immediately after start up.
- START-UP:** When BL_CTL bit is written high or PWM signal is high, the INTERNAL START-UP SEQUENCE powers up all the needed internal blocks (V_{REF} , Bias, Oscillator etc.). Internal EPROM and EEPROM are read in this mode. To ensure the correct oscillator initialization etc., a 2-ms delay is generated by the internal state-machine. If the chip temperature rises too high, the Thermal Shutdown (TSD) disables the chip operation and STARTUP mode is entered until no thermal shutdown event is present.
- BOOST START-UP:** Soft start for boost output is generated in the BOOST START-UP mode. The boost output is raised in low current PWM mode during the 4-ms delay generated by the state-machine. All LED outputs are off during the 4-ms delay to ensure smooth startup. The Boost start-up is entered from Internal Start-up Sequence if EN_BOOST is HIGH.
- NORMAL:** During NORMAL mode the user controls the chip using the external PWM input or with Control Registers through I²C. The registers can be written in any sequence and any number of bits can be altered in a register in one write.

8.5 Programming

8.5.1 I²C-Compatible Serial Bus Interface

8.5.1.1 Interface Bus Overview

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA) and the Serial Clock Line (SCLK). These lines should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the SCLK. The LP8551 is always a slave device.

8.5.1.2 Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock SCLK. Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCLK and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCLK state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

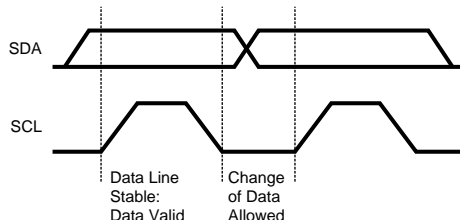


Figure 15. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

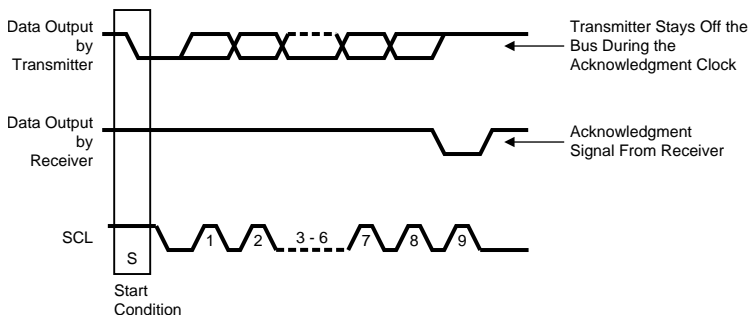


Figure 16. Start and Stop

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCLK) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCLK is high indicates a Stop Condition.

Programming (continued)

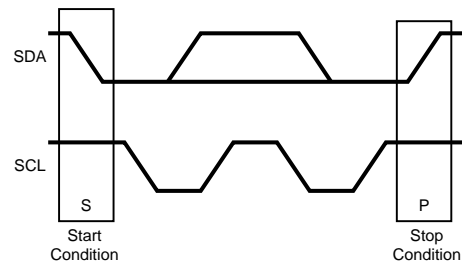


Figure 17. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

8.5.1.3 Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

8.5.1.4 “Acknowledge After Every Byte” Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the “acknowledge after every byte” rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

8.5.1.5 Addressing Transfer Formats

Each device on the bus has a unique slave address. The LP8551 operates as a slave device with 7-bit address combined with data direction bit. Slave address is 2Ch as 7-bit or 58h for write and 59h for read in 8-bit format.

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.



Figure 18. I²C Chip Address

8.5.1.6 Control Register Write Cycle

- Master device generates start condition.

Programming (continued)

- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master sends further data bytes the control register address is incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

8.5.1.7 Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address is incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

Table 3. Data Read and Write Cycles

	ADDRESS MODE
Data Read	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = 1>[Ack] [Register Data]<Ack or NAck> ... additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w='0'>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] ... additional writes to subsequent register address possible <Stop Condition>

8.5.1.8 Register Read and Write Detail

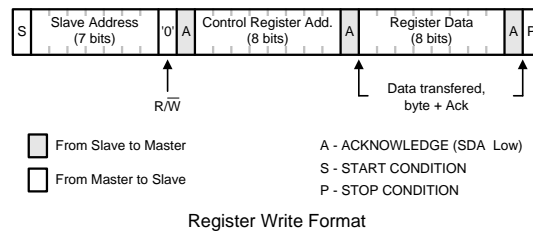


Figure 19. LP8551 Register Write Format

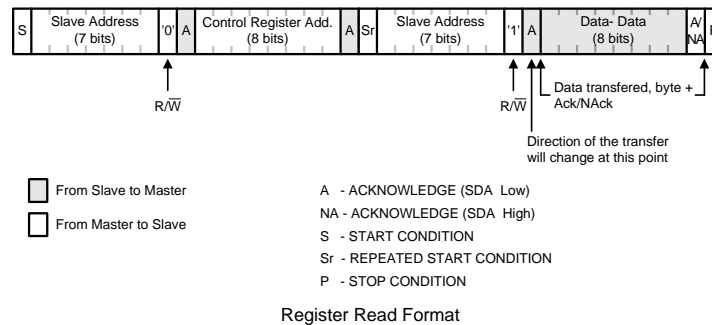


Figure 20. LP8551 Register Read Format

8.5.2 EEPROM

EEPROM memory stores various parameters for chip control. The 64-bit EEPROM memory is organized as 8 x 8 bits. The EEPROM structure consists of a register front-end and the non-volatile memory (NVM). Register data can be read and written through the serial interface, and data is effective immediately. To read and program NVM, separate commands need to be sent. Erase and program voltages are generated on-chip charge pump, no other voltages than normal input voltage are required. A complete EEPROM memory map is shown in the [Device Default Values](#) section.

NOTE

EEPROM NVM can be programmed or read by customer for bench validation. Programming for production devices should be done in TI production test, where appropriate checks are performed to confirm EEPROM validity. Writing to EEPROM Control register of production devices is not recommended. If special EEPROM configuration is required, please contact the TI Sales Office for availability.

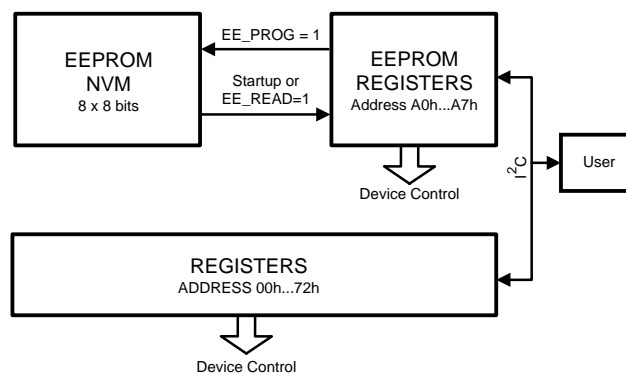


Figure 21. EEPROM Control Structure

8.6 Register Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00H	Brightness Control	BRT[7:0]								0000 0000
01H	Device Control						BRT_MODE[1:0]		BL_CTL	0000 0000
02H	Fault	OPEN	SHORT	2_CHANNELS	1_CHANNEL	BL_FAULT	OCF	TSD	UVLO	0000 0000
03H	ID	PANEL	MFG[3:0]				REV[2:0]			1111 1100
04H	Direct Control					OUT[4:1]				0000 0000
05H	Temp MSB	TEMP[10:3]								0000 0000
06H	Temp LSB	TEMP[2:0]								0000 0000
72H	EEPROM_control	EE_READY					EE_INIT	EE_PROG	EE_READ	0000 0000

8.6.1 Register Bit Explanations

8.6.1.1 Brightness Control

Address 00h

Reset value 0000 0000b

BRIGHTNESS CONTROL REGISTER							
7	6	5	4	3	2	1	0
BRT[7:0]							
Name	Bit	Access	Description				
BRT	7:0	R/W	Backlight PWM 8-bit linear control.				

8.6.1.2 Device Control

Address 01h

Reset value 0000 0000b

DEVICE CONTROL REGISTER							
7	6	5	4	3	2	1	0
					BRT_MODE[1:0]		BL_CTL
Name	Bit	Access	Description				
BRT_MODE	2:1	R/W	PWM source mode				
			00b = PWM input pin duty cycle control (default)				
			01b = PWM input pin duty cycle control				
			10b = Brightness register				
			11b = Direct PWM control from PWM input pin				
BL_CTL	0	R/W	Enable backlight				
			0 = Backlight disabled and chip turned off if BRT_MODE[1:0] = 10. In external PWM pin control the state of the chip is defined with the PWM pin, and this bit has no effect.				
			1 = Backlight enabled and chip turned on if BRT_MODE[1:0] = 10. In external PWM pin control the state of the chip is defined with the PWM pin, and this bit has no effect.				

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8.6.1.3 Fault

Address 02h

Reset value 0000 0000b

FAULT REGISTER							
7	6	5	4	3	2	1	0
OPEN	SHORT	2_CHANNELS	1_CHANNEL	BL_FAULT	OCP	TSD	UVLO
Name	Bit	Access	Description				
OPEN	7	R	LED open fault detection				
			0 = No fault				
			1 = LED open fault detected. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.				
SHORT	6	R	LED short fault detection				
			0 = No fault				
			1 = LED short fault detected. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.				
2_CHANNELS	5	R	LED fault detection				
			0 = No fault				
			1 = 2 or more channels have generated either short or open fault. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.				
1_CHANNEL	4	R	LED fault detection				
			0 = No fault				
			1 = 1 channel has generated either short or open fault. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.				
BL_FAULT	3	R	LED fault detection				
			0 = No fault				
			1 = LED fault detected. Generated with OR function of all LED faults. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.				
OCP	2	R	Overcurrent protection				
			0 = No fault				
			1 = Overcurrent detected in boost output. OCP detection block monitors the boost output and if the boost output has been too low for more than 50 ms it generates an OCP fault and disables the boost. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low. After clearing the fault boost starts up again.				
TSD	1	R	Thermal shutdown				
			0 = No fault				
			1 = Thermal fault generated, 150°C reached. Boost is converted, and LED outputs are disabled until the temperature has dropped down to 130°C. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.				
UVLO	0	R	Undervoltage detection				
			0 = No fault				
			1 = Undervoltage detected in VIN pin. Boost is converted, and LED outputs are disabled until V _{IN} voltage is above the threshold voltage. Threshold voltage is set with EEPROM bits from 3V...9V. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.				

8.6.1.4 Identification

Address 03h

Reset value 1111 1100b

IDENTIFICATION REGISTER							
7	6	5	4	3	2	1	0
PANEL	MFG[3:0]				REV[2:0]		
Name	Bit	Access	Description				
PANEL	7	R	Panel ID code				
MFG	6:3	R	Manufacturer ID code				
REV	2:0	R	Revision ID code				

8.6.1.5 Direct Control

Address 04h

Reset value 0000 0000b

DIRECT CONTROL REGISTER							
7	6	5	4	3	2	1	0
				OUT[4:1]			
Name	Bit	Access	Description				
OUT	3:0	R/W	Direct control of the LED outputs				
			0 = Normal operation. LED output are controlled with PWM.				
			1 = LED output is forced to 100% PWM.				

8.6.1.6 Temp MSB

Address 05h

Reset value 0000 0000b

Temp MSB register							
7	6	5	4	3	2	1	0
TEMP[10:3]							
Name	Bit	Access	Description				
TEMP	7:0	R	Device internal temperature sensor reading first 8 MSB. MSB must be read before LSB, because reading of MSB register latches the data.				

8.6.1.7 Temp LSB

Address 06h

Reset value 0000 0000b

TEMP LSB REGISTER							
7	6	5	4	3	2	1	0
TEMP[2:0]							
Name	Bit	Access	Description				
TEMP	7:5	R	Device internal temperature sensor reading last 3 LSB. MSB must be read before LSB, because reading of MSB register latches the data.				

8.6.1.8 EEPROM Control

Address 72h

Reset value 0000 0000b

EEPROM CONTROL REGISTER							
7	6	5	4	3	2	1	0
EE_READY					EE_INIT	EE_PROG	EE_READ
Name	Bit	Access	Description				
EE_READY	7	R	EEPROM ready				
			0 = EEPROM programming or read in progress				
			1 = EEPROM ready, not busy				
EE_INIT	2	R/W	EEPROM initialization bit. This bit must be written 1 before EEPROM read or programming.				
EE_PROG	1	R/W	EEPROM programming.				
			0 = Normal operation				
			1 = Start the EEPROM programming sequence. EE_INIT must be written 1 before EEPROM programming can be started. Programs data currently in the EEPROM registers to non volatile memory (NVM). Programming sequence takes about 200 ms. Programming voltage is generated inside the chip.				
EE_READ	0	R/W	EEPROM read				
			0 = Normal operation				
			1 = Reads the data from NVM to the EEPROM registers. Can be used to restore default values if EEPROM registers are changed during testing.				

Programming sequence (program data permanently from registers to NVM):

1. Turn on the chip by writing BL_CTL bit to 1 and BRT_MODE[1:0] to 10b (05h to address 01h)
2. Write data to EEPROM registers (address A0h...A7h)
3. Write EE_INIT to 1 in address 72h. (04h to address 72h)
4. Write EE_PROG to 1 and EE_INIT to 0 in address 72h. (02h to address 72h)
5. Wait 200 ms.
6. Write EE_PROG to 0 in address 72h. (00h to address 72h)

Read sequence (load data from NVM to registers):

1. Turn on the chip by writing BL_CTL bit to 1 and BRT_MODE[1:0] to 10b (05h to address 01h).
2. Write EE_INIT to 1 in address 72h. (04h to address 72h)
3. Write EE_READ to 1 and EE_INIT to 0 in address 72h. (01h to address 72h)
4. Wait 200 ms.
5. Write EE_READ to 0 in address 72h. (00h to address 72h)

NOTE

Data written to EEPROM registers is effective immediately even if the EEPROM programming sequence has not been done. When power is turned off, the device, however, loses the data if it is not programmed to the NVM. During start-up the device automatically loads the data from NVM to registers.

NOTE

EEPROM NVM can be programmed or read by customer for bench validation. Programming for production devices should be done in TI production test, where appropriate checks are performed to confirm EEPROM validity. Writing to EEPROM Control register of production devices is not recommended. If special EEPROM configuration is required, please contact the TI Sales Office for availability.

8.6.2 EEPROM Bit Explanations

8.6.2.1 EEPROM Register Map

ADD R	REGIST ER	D7	D6	D5	D4	D3	D2	D1	D0
A0H	eeeprom addr 0	CURRENT[7:0]							
A1H	eeeprom addr 1	BOOST_FREQ[1:0]		EN_LED_FAULT	TEMP_LIM[1:0]		SLOPE[2:0]		
A2H	eeeprom addr 2	ADAPTIVE_SPEED[1:0]		ADV_SLOPE		EN_ADAPT	EN_BOOST	BOOST_IMAX	
A3H	eeeprom addr 3	UVLO[1:0]		EN_PSPWM		PWM_FREQ[4:0]			
A4H	eeeprom addr 4	PWM_RESOLUTION[1:0]		EN_I_RES	LED_FAULT_THR		DRV_HEADR[2:0]		
A5H	eeeprom addr 5				VBOOST[4:0]				
A6H	eeeprom addr 6								
A7H	eeeprom addr 7						EN_F_RES	HYSTERESIS[1:0]	

8.6.2.2 EEPROM Address 0

Address A0h

EEPROM ADDRESS 0 REGISTER							
7	6	5	4	3	2	1	0
CURRENT[7:0]							
Name	Bit	Access	Description				
CURRENT	7:0	R/W	Backlight current adjustment. If EN_I_RES = 0 the maximum backlight current is defined only with these bits as described below. If EN_I_RES = 1, then the external resistor connected to ISET pin also scales the LED current. With 16 kΩ resistor and CURRENT set to 7Fh the output current is then 23 mA.				
					EN_I_RES = 0	EN_I_RES = 1	
			0000 0000		0 mA	0 mA	
			0000 0001		0.12 mA	$(1/255) \times 600 \times 1.23V/R_{ISET}$	
			0000 0010		0.24 mA	$(2/255) \times 600 \times 1.23V/R_{ISET}$	
			
			0111 1111		15.00 mA	$(127/255) \times 600 \times 1.23V/R_{ISET}$	
			
			1111 1101		29.76 mA	$(253/255) \times 600 \times 1.23V/R_{ISET}$	
			1111 1110		29.88 mA	$(254/255) \times 600 \times 1.23V/R_{ISET}$	
			1111 1111		30.00 mA	$(255/255) \times 600 \times 1.23V/R_{ISET}$	

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8.6.2.3 EEPROM Address 1

Address A1h

EEPROM ADDRESS 1 U							
7	6	5	4	3	2	1	0
BOOST_FREQ[1:0]		EN_LED_FAULT	TEMP_LIM[1:0]		SLOPE[2:0]		
Name	Bit	Access	Description				
BOOST_FREQ	7:6	R/W	Boost Converter Switch Frequency				
			00 = 156 kHz				
			01 = 312 kHz				
			10 = 625 kHz				
			11 = 1250 kHz				
EN_LED_FAULT	5	R/W	Enable LED fault detection				
			0 = LED fault detection disabled				
			1 = LED fault detection enabled				
TEMP_LIM	4:3	R/W	Thermal deration function temperature threshold				
			00 = thermal deration function disabled				
			01 = 110°C				
			10 = 120°C				
			11 = 130°C				
SLOPE	2:0	R/W	Slope time for brightness change				
			000 = Slope function disabled, immediate brightness change				
			001 = 50 ms				
			010 = 75 ms				
			011 = 100 ms				
			100 = 150 ms				
			101 = 200 ms				
			110 = 300 ms				
			111 = 500 ms				

8.6.2.4 EEPROM Address 2

Address A2h

EEPROM ADDRESS 2 REGISTER							
7	6	5	4	3	2	1	0
ADAPTIVE_SPEED[1:0]		ADV_SLOPE		EN_ADAPT	EN_BOOST	BOOST_IMAX	
Name	Bit	Access	Description				
ADAPTIVE_SPEED[1]	7	R/W	Boost converter adaptive control speed adjustment				
			0 = Normal mode				
			1 = Adaptive mode optimized for light loads. Activating this helps the voltage droop with light loads during boost / backlight start-up.				
ADAPTIVE_SPEED[0]	6	R/W	Boost converter adaptive control speed adjustment				
			0 = Adjust boost once for each phase shift cycle or normal PWM cycle				
			1 = Adjust boost every 16th phase shift cycle or normal PWM cycle				
ADV_SLOPE	5	R/W	Advanced slope				
			0 = Advanced slope is disabled				
			1 = Use advanced slope for brightness change to make brightness changes smooth for eye				
EN_ADAPT	3	R/W	Enable boost converter adaptive mode				
			0 = adaptive mode disabled, boost converter output voltage is set with VBOOST EEPROM register bits				
			1 = adaptive mode enabled. Boost converter startup voltage is set with VBOOST EEPROM register bits, and after startup voltage is reached the boost converter adapts to the highest LED string V_F . LED driver output headroom is set with DRV_HEADR EEPROM control bits.				
EN_BOOST	2	R/W	Enable boost converter				
			0 = boost is disabled				
			1 = boost is enabled and turns on automatically when backlight is enabled				
BOOST_IMAX	1	R/W	Boost converter inductor maximum current				
			0 = 1.4 A				
			1 = 2.5 A (recommended)				

8.6.2.5 EEPROM Address 3

Address A3h

EEPROM ADDRESS 3 REGISTER							
7	6	5	4	3	2	1	0
UVLO[1:0]		EN_PSPWM	PWM_FREQ[4:0]				
Name	Bit	Access	Description				
UVLO	7:6	R/W	00 = Disabled				
			01 = 2.7 V				
			10 = 5.4 V				
			11 = 8.1 V				
EN_PSPWM	5	R/W	Enable phase shift PWM scheme				
			0 = phase shift PWM disabled, normal PWM mode used				
			1 = phase shift PWM enabled				
PWM_FREQ	4:0	R/W	PWM output frequency setting. See PWM Frequency Setting for full description of selectable PWM frequencies.				

8.6.2.6 EEPROM Address 4

Address A4h

EEPROM ADDRESS 4 REGISTER							
7	6	5	4	3	2	1	0
PWM_RESOLUTION[1:0]		EN_I_RES	LED_FAULT_THR		DRV_HEADR[2:0]		
Name	Bit	Access	Description				
PWM_RESOLUTION	7:6	R/W	PWM output resolution selection. Actual resolution depends also on the output frequency. See <i>PWM Frequency Setting</i> for full description.				
			00 = 8...10 bits (19.2 kHz...4.8 kHz)				
			01 = 9...11 bits (19.2 kHz... 4.8 kHz)				
			10 = 10...12 bits (19.2 kHz...4.8 kHz)				
			11 = 11...13 bits (19.2 kHz...4.8 kHz)				
EN_I_RES	5	R/W	Enable LED current set resistor				
			0 = Resistor is disabled and current is set only with CURRENT EEPROM register bits				
			1 = Enable LED current set resistor. LED current is defined by the R _{ISET} resistor and the CURRENT EEPROM register bits.				
LED_FAULT_THR	4	R/W	LED fault detector thresholds. V _{SAT} is the saturation voltage of the driver, typically 200 mV.				
			0 = 3.3V				
			1 = 5.3V				
DRV_HEADR	2:0	R/W	LED output driver headroom control. V _{SAT} is the saturation voltage of the driver, typically 200 mV.				
			000 = V _{SAT} + 125 mV				
			001 = V _{SAT} + 250 mV				
			010 = V _{SAT} + 375 mV				
			011 = V _{SAT} + 500 mV				
			100 = V _{SAT} + 625 mV				
			101 = V _{SAT} + 750 mV				
			110 = V _{SAT} + 875 mV				
			111 = V _{SAT} + 1000 mV				

8.6.2.7 EEPROM Address 5

Address A5h

EEPROM ADDRESS 5 REGISTER							
7	6	5	4	3	2	1	0
			VBOOST[4:0]				
Name	Bit	Access	Description				
VBOOST	4:0	R/W	Boost voltage control from 10V to 40V with 1V step. If adaptive boost control is enabled, this sets the initial start voltage for the boost converter. If adaptive mode is disabled, this directly sets the output voltage of the boost converter.				
			0 0000 = 10V				
			0 0001 = 11V				
			0 0010 = 12V				
			...				
			1 1101 = 39V				
			1 1110 = 40V				
			1 1111 = 40V				

8.6.2.8 EEPROM Address 7

Address A7h

EEPROM ADDRESS 7 REGISTER							
7	6	5	4	3	2	1	0
					EN_F_RES	HYSTERESIS[1:0]	
Name	Bit	Access	Description				
EN_F_RES	2	R/W	Enable PWM output frequency set resistor				
			0 = Resistor is disabled and PWM output frequency is set with PWM_FREQ EEPROM register bits				
			1 = PWM frequency set resistor is enabled. R _{FSET} defines the output PWM frequency. See PWM Frequency Setting for full description of the PWM frequencies.				
HYSTERESIS	1:0	R/W	PWM input hysteresis function. Defines how small changes in the PWM input are ignored to remove constant switching between two values.				
			00 = OFF				
			01 = 1-bit hysteresis with 11-bit resolution				
			10 = 1-bit hysteresis with 10-bit resolution				
			11 = 1-bit hysteresis with 8-bit resolution				

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP8551 is designed for LCD backlighting for portable devices, such as laptops and tablets. 4 LED current sinks allow driving up to 40 LEDs with high efficiency. Boost converter optimizes the system efficiency by adjusting the LED current driver headroom to optimal level in each case. Due to a flexible input voltage configuration, the LP8551 can be used also in various applications since the input voltage supports 1x to 5x series Li-Ion cells. Main limiting factor for output power is inductor current limit, which is calculated in the Detailed Design Procedure. The following design procedure can be used to select component values for the LP8551.

9.2 Typical Applications

9.2.1 Application Using Internal LDO

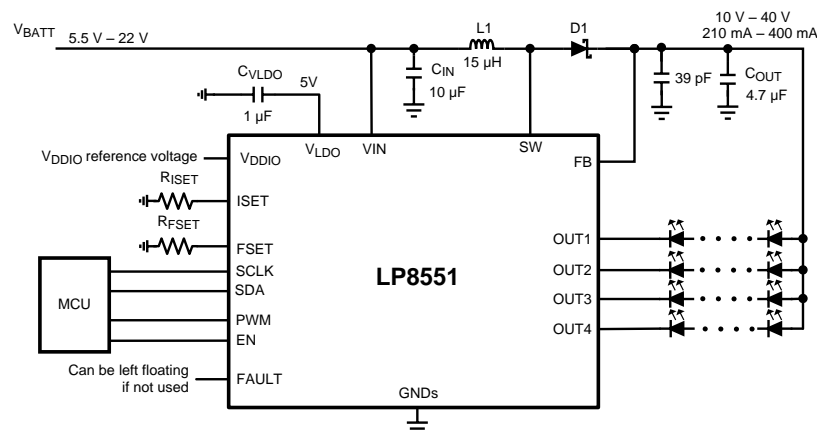


Figure 22. LP8551 with Internal LDO

9.2.1.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 22 V
Brightness Control	PWM input duty cycle (default), I ² C can be used as well
PWM output frequency	With R _{FSET} resistor 85 kΩ to 100 kΩ; 9.8 kHz with PSPWM enabled
LED Current	With R _{ISET} resistor 15 kΩ; 25 mA / channel
Brightness slopes	200-ms linear slope + advanced slope
External set resistors	Enabled
Inductor	10 μH to 33 μH, with 2.5-A saturation current
Boost SW frequency	625 kHz
SW current limit	2.5 A

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Recommended External Components

9.2.1.2.1.1 Inductor Selection

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and should be preferred.

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current.

Equation 3 below shows the worst case conditions.

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \text{ and } D' = (1 - D)$$

- I_{RIPPLE} : Average to peak inductor current
- I_{OUTMAX} : Maximum load current
- V_{IN} : Maximum input voltage in application
- L : Min inductor value including worst case tolerances
- f : Minimum switching frequency
- D : Duty cycle for CCM Operation
- V_{OUT} : Output voltage

(3)

Example using above equations:

- $V_{IN} = 12 \text{ V}$
- $V_{OUT} = 38 \text{ V}$
- $I_{OUT} = 400 \text{ mA}$
- $L = 15 \mu\text{H} - 20\% = 12 \mu\text{H}$
- $f = 1.25 \text{ MHz}$
- $I_{SAT} = 1.6 \text{ A}$

As a result the inductor should be selected according to the I_{SAT} . A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 2.5 A. A 15- μH inductor with a saturation current rating of 2.5 A is recommended for most applications. The inductor's resistance should be less than 300 m Ω for good efficiency. For high efficiency choose an inductor with high frequency core material such as ferrite to reduce core losses. To minimize radiated noise, use shielded core inductor. Inductor should be placed as close to the SW pin and the IC as possible. Special care should be used when designing the PCB layout to minimize radiated noise and to get good performance from the boost converter. For more information on the PCB layout recommendations, please see [Layout Guidelines](#).

9.2.1.2.1.2 Output Capacitor

A ceramic capacitor with 50-V voltage rating or higher is recommended for the output capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. For light loads a 4.7- μF capacitor is sufficient. Effectively the capacitance should be 4 μF for < 150-mA loads. For maximum output voltage/current 10- μF capacitor (or two 4.7- μF capacitors) is recommended to minimize the output ripple.

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9.2.1.2.1.3 LDO Capacitor

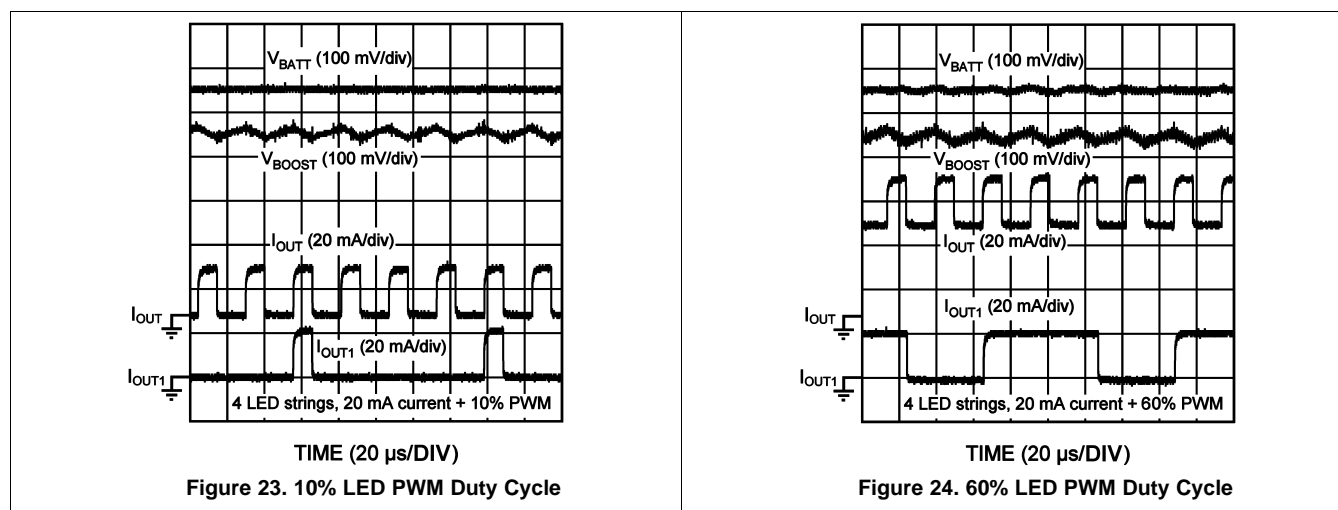
A 1- μ F ceramic capacitor with 10-V voltage rating is recommended for the LDO capacitor.

9.2.1.2.1.4 Output Diode

A Schottky diode should be used for the output diode. Peak repetitive current should be greater than inductor peak current (2.5 A) to ensure reliable operation. Average current rating should be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown voltage of the Schottky diode significantly larger (approximately 60 V) than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

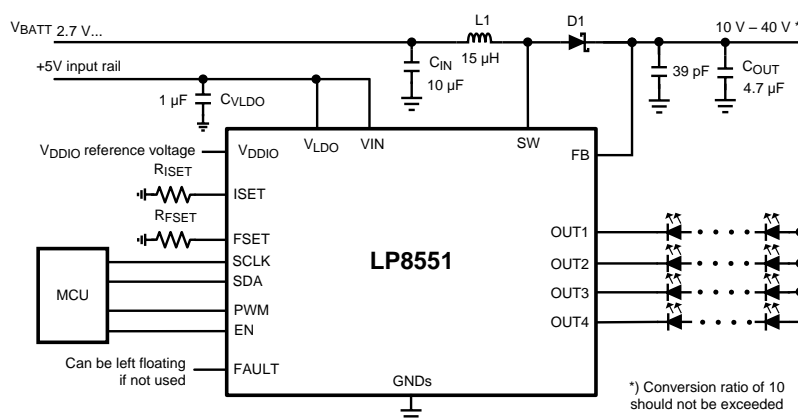
9.2.1.3 Application Curves

Typical Boost and LED Current waveforms with $f_{LED} = 9.6$ kHz.



9.2.2 Application with Low-Input Voltage

In Single Li-Ion cell powered application the internal circuitry of LP8551 can be powered from external 5-V rail. Boost is powered directly from Li-Ion battery and V_{LDO} and V_{IN} pins are connected to external 5-V rail. Current draw from the 5-V rail is maximum 10 mA. A separate 5-V rail to V_{IN}/V_{LDO} can be used also in higher input voltage application to improve efficiency or add increase input voltage range above 22 V in some cases. There are no power sequencing requirement for V_{IN}/V_{LDO} and V_{BATT} other than V_{BATT} must be available when enabling backlight to prevent a false overcurrent fault.



9.2.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range, V_{BATT}	2.7 V to V_{OUT}
5-V input rail, V_{LDO}/V_{IN}	4.5 V to 5.5 V, 10 mA
Brightness Control	PWM input duty cycle (default), I ² C can be used as well
PWM output frequency	With R_{FSET} resistor 85 k Ω to 100 k Ω ; 9.8 kHz with PSPWM enabled
LED Current	With R_{ISET} resistor 15 k Ω ; 25 mA / channel
Brightness slopes	200-ms linear slope + advanced slope
External set resistors	Enabled
Inductor	10 μ H to 33 μ H, with 2.5-A saturation current
Boost SW frequency	625 kHz
SW current limit	2.5 A

9.2.2.2 Detailed Design Procedure

Component selection follows [Detailed Design Procedure](#) section above. V_{LDO} capacitor voltage rating can be set based on the 5-V rail voltage specification, which must be <5.5 V in all cases. Note that UVLO is detected from the VIN pin voltage, not from the V_{BATT} voltage.

9.2.2.3 Application Curves

Typical Boost and LED current behavior is seen in the [Application Curves](#) section.

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7 V and 22 V. This input supply should be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition (start-up or rapid brightness change). The resistance of the input supply rail should be low enough that the input current transient does not cause drop high enough in the LP8551 supply voltage that can cause false UVLO fault triggering.

If a separate 5-V power rail is used to power LP8551 V_{LDO}/V_{IN} pins, this voltage must be stable 4.5 V to 5 V. Excessive noise or ripple in this rail can have adverse effect on device performance, so good grounding and sufficient bypass capacitors must be used.

If the input supply is located more than a few inches from the LP8551 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. Depending on device EPROM configuration and usage case the boost converter is configured to operate optimally with certain input voltage range. Examples are seen in the [Detailed Design Procedure](#) section. In uncertain cases, it is recommended to contact a TI Sales Representative for confirmation of the compatibility of the use case, EPROM configuration, and input voltage range.

11 Layout

11.1 Layout Guidelines

[Figure 27](#) is a layout recommendation for the LP8551. The figure is used for demonstrating the principle of good layout. This layout can be adapted to the actual application layout if/where possible.

It is important that all boost components are close to the chip and the high current traces should be wide enough. By placing the boost component on one side of the chip it is easy to keep the ground plane intact below the high current paths. This way other chip pins can be routed more easily without splitting the ground plane. If the chip is placed in the center of the boost components, the I²C lines, LED lines, etc. cut the ground plane below the high current paths, and it makes the layout design more difficult.

V_{IN} and V_{LDO} need to be as noise-free as possible. Place the bypass capacitors near the corresponding pins and ground them to as noise-free ground as possible.

Here are some main points to help the PCB layout work:

1. Current loops need to be minimized:
 - (a) For low frequency the minimal current loop can be achieved by placing the boost components as close to the SW and SW_GND pins as possible. Input and output capacitor grounds need to be close to each other.
 - (b) Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High frequency return currents try to find route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the “positive” current route in the ground plane, if the ground plane is intact under the route. Traces from inner pads of the LP8551 need to be routed from below the part in the second layer so that traces do not split the ground plane under the boost traces or components.
2. GND plane needs to be intact under the high current boost traces to provide shortest possible return path and smallest possible current loops for high frequencies.
3. Current loops when the boost switch is conducting and not conducting needs to be on the same direction in optimal case.
4. Inductor placement should be so that the current flows in the same direction as in the current loops. Rotating inductor 180 degrees changes current direction.
5. Use separate “noisy” and “silent” grounds. Noisy ground is used for boost converter return current and silent ground for more sensitive signals, like V_{IN} and V_{LDO} bypass capacitor grounding.
6. Boost output voltage to LEDs need to be taken out “after” the output capacitors, not straight from the diode cathode.
7. Small (such as 39 pF) bypass capacitor should be placed close to the FB pin.
8. R_{SET} resistor should be grounded to silent ground, since possible ground ripple will show at the LED current.
9. V_{IN} line should be separated from the high current supply path to the boost converter to prevent high frequency ripple affecting the chip behavior. Separate 100-nF bypass capacitor is used for V_{IN} line and it is grounded to noise-free ground.
10. Input and output capacitors need strong grounding (wide traces, vias to GND plane).
11. If two output capacitors are used they need symmetrical layout to get both capacitors working ideally.
12. Output capacitors DC-bias effect. If the output capacitance is too low, it can cause boost to become unstable on some loads and this increases EMI. DC bias characteristics need to be obtained from the component manufacturer; it is not taken into account on component tolerance. 50-V 1210-size X5R/X7R capacitors are recommended.

Layout Guidelines (continued)

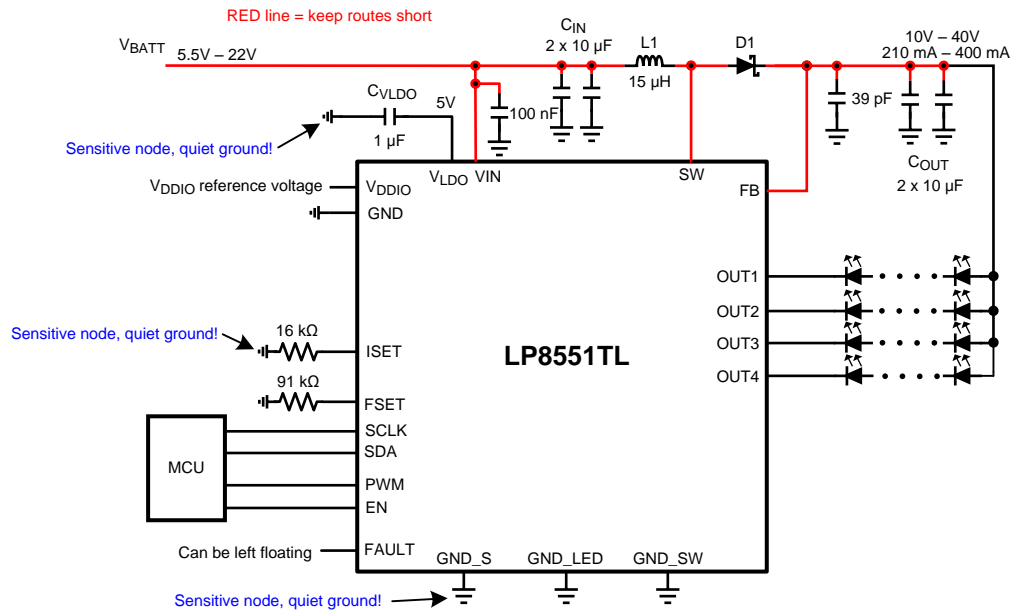


Figure 26. LP8551 Application Schematic

11.2 Layout Example

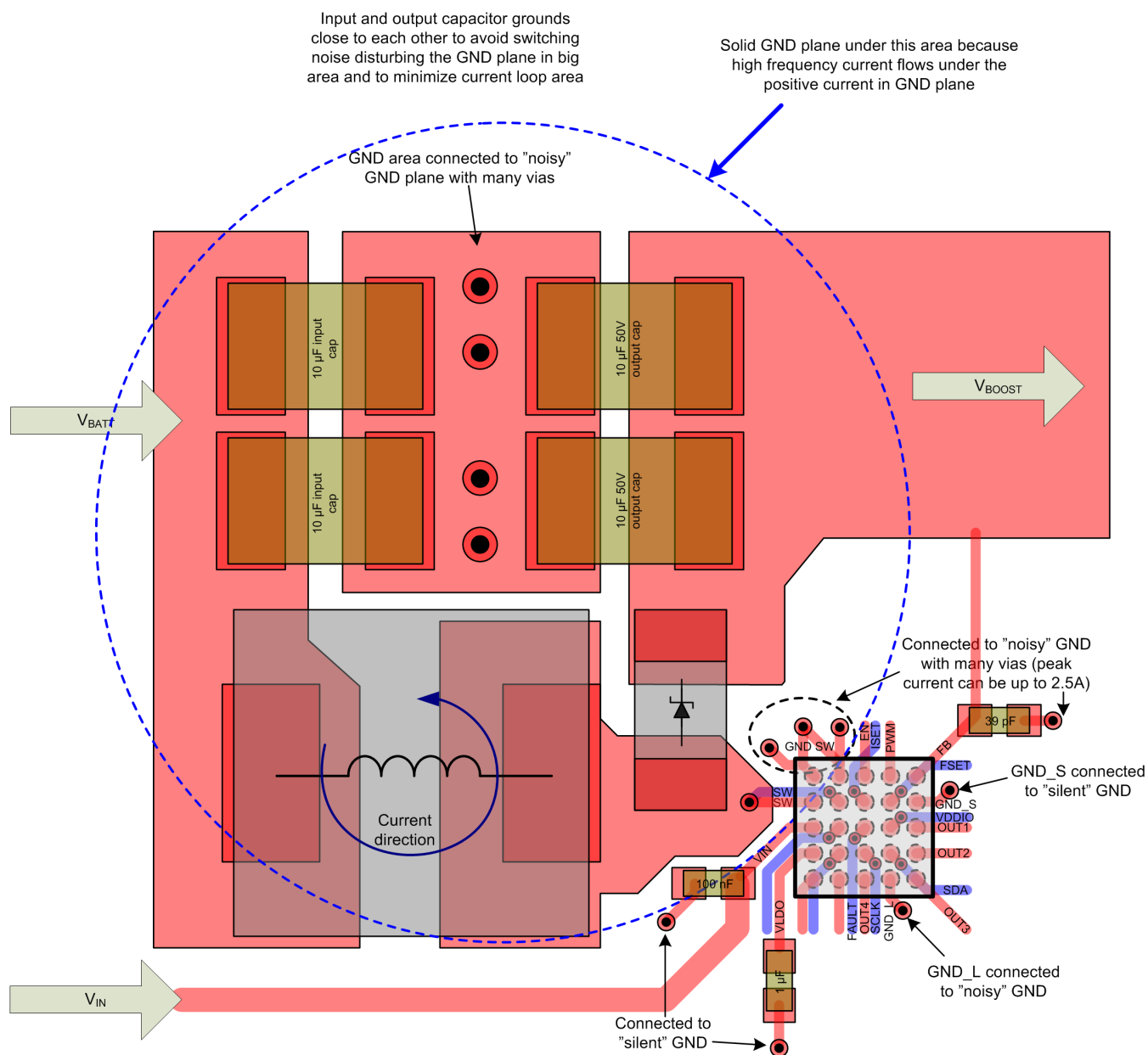


Figure 27. LP8551 Layout

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8551TLE/NOPB	ACTIVE	DSBGA	YZR	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		8551	Samples
LP8551TLX/NOPB	ACTIVE	DSBGA	YZR	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	8551	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8551TLE/NOPB	DSBGA	YZR	25	250	178.0	8.4	2.69	2.69	0.76	4.0	8.0	Q1
LP8551TLX/NOPB	DSBGA	YZR	25	3000	178.0	8.4	2.69	2.69	0.76	4.0	8.0	Q1

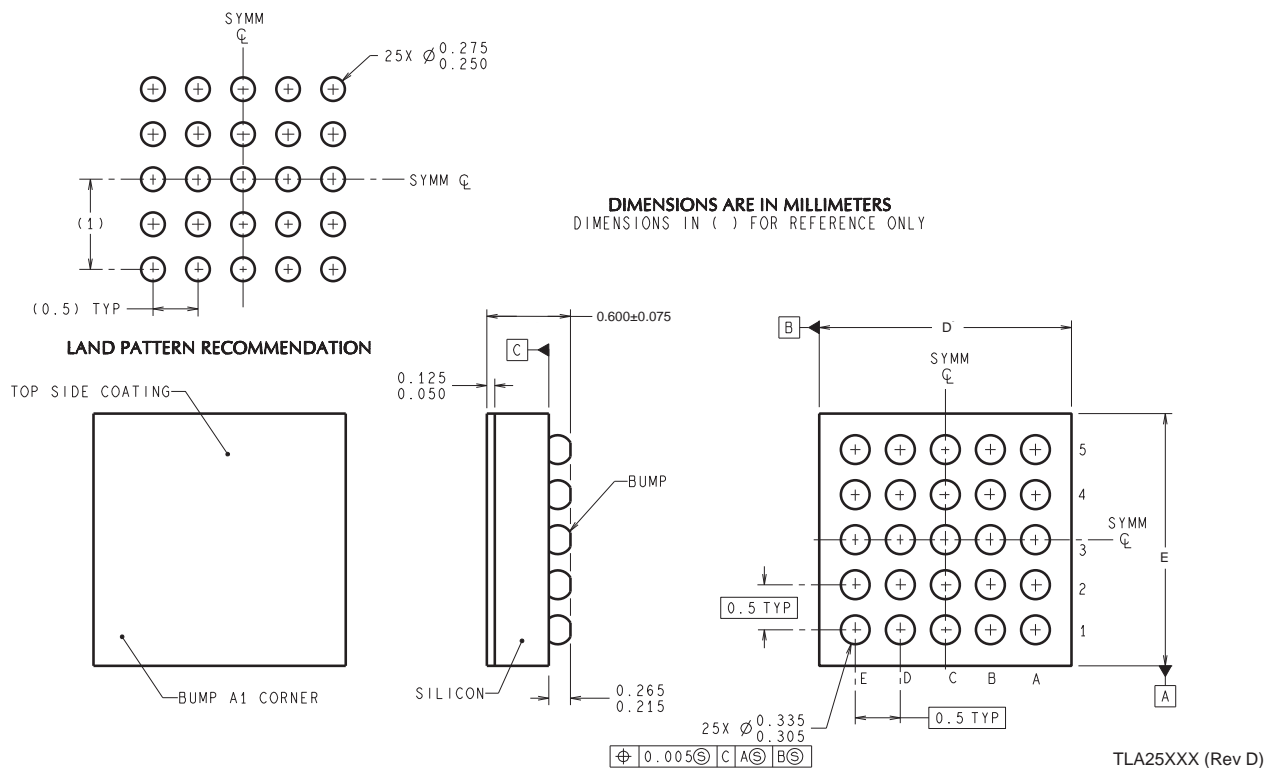
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8551TLE/NOPB	DSBGA	YZR	25	250	210.0	185.0	35.0
LP8551TLX/NOPB	DSBGA	YZR	25	3000	210.0	185.0	35.0

YZR0025



D: Max = 2.49 mm, Min = 2.43 mm

E: Max = 2.49 mm, Min = 2.43 mm

4215055/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.

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