

SN65LVDM1676 SN65LVDM1677

SLLS430D-NOVEMBER 2000-REVISED JUNE 2007

HIGH-SPEED DIFFERENTIAL LINE TRANSCEIVERS

FEATURES

- Sixteen Low-Voltage Differential Transceivers. Designed for Signaling Rates up to 200 Mbps per Receiver or 650 Mbps per Transmitter.
- Simplex (Point-to-Point) or Half-Duplex (Multipoint) Interface
- Typical Differential Output Voltage of 340 mV Into a 50- Ω Load
- Integrated 110-Ω Line Termination on 'LVDM1677 Product
- Propagation Delay Time:
 - Driver: 2.5 ns Typ
 - Receiver: 3 ns Typ
- Driver is High Impedance When Disabled or With V_{CC} < 1.5 V for Power Up/Down Glitch-Free Performance and Hot-Plugging Events
- Bus-Terminal ESD Protection Exceeds 12 kV
- Low-Voltage TTL (LVTTL) Logic Input Levels Are 5-V Tolerant
- Packaged in Thin Shrink Small-Outline Package With 20 mil Terminal Pitch

DESCRIPTION

The SN65LVDM1676 and SN65LVDM1677 (integrated termination) are sixteen differential line transmitters or receivers (tranceivers) that use low-voltage differential signaling (LVDS) to achieve signaling rates up to 200 Mbps per transceiver configured as a receiver and up to 650 Mbps per transceiver configured as a transmitter. These products are similar to TIA/EIA-644 standard compliant devices (SN65LVDS) counterparts except that the output current of the drivers are doubled. This modification provides a minimum differential output voltage magnitude of 247 mV into a 50- Ω load and allows double-terminated lines and half-duplex operation. The receivers detect a voltage difference of 100 mV with up to 1 V of ground potential difference between a transmitter and receiver.

SN65LVDM1676DGG (Marked as LVDM1676)
SN65LVDM1677DGG (Marked as LVDM1677)
(TOP VIEW)

	(,	
		$\sum_{i=1}^{n}$	1 <u>4 1 v</u>
		62	
VCCL	2	03	
	3	62] A21
	4	61] ^2Z
	5	60] A31
	6	59	
	1	58	
	8	57	
	9	56	
BIX/RX [10	55	J B1Z
B1A [11	54	J B2Y
B2A	12	53	J B2Z
B3A L	13	52	B3Y
B4A	14	51	B3Z
GND [15	50] B4Y
V _{CC}	16	49] B4Z
V _{CC}	17	48] C1Y
GND [18	47] C1Z
C1A [19	46] C2Y
C2A [20	45] C2Z
СЗА [21	44] C3Y
C4A [22	43] C3Z
CTX/RX [23	42] C4Y
D1A [24	41] C4Z
D2A [25	40] D1Y
D3A [26	39] D1Z
D4A [27	38] D2Y
DTX/RX [28	37] D2Z
GND [29	36] D3Y
V _{CC}	30	35] D3Z
V _{CC}	31	34] D4Y
GND [32	33] D4Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN65LVDM1676 SN65LVDM1677 SLLS430D-NOVEMBER 2000-REVISED JUNE 2007



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω . The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of transceivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The SN65LVDM1676 and SN65LVDM1677 are characterized for operation from -40°C to 85°C.

INPUTS		OUTPUTS	6		
(Y – Z)	TX/RX	А	Y	Z	А
V _{ID} ≥ 100 mV	L	NA	Z	Z	Н
-100 mV < V _{ID} < 100 mV	L	NA	Z	Z	?
$V_{ID} \le -100 \text{ mV}$	L	NA	Z	Z	L
Open circuit	L	NA	Z	Z	Н
NA	Н	L	L	Н	Z
NA	н	Н	Н	L	Z

FUNCTION TABLE⁽¹⁾

(1) H = high level, L= low level, Z= high impedance, ? = indeterminate

LVD Transceiver





LOGIC DIAGRAM (POSITIVE LOGIC)







SLLS430D-NOVEMBER 2000-REVISED JUNE 2007

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS







ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

			RATING
V_{CC}	Supply voltage range		–0.5 V to 4 V
v		A, TX/RX	–0.5 V to 6 V
v ₁	Input voltage lange	Y or Z	–0.5 V to 4 V
$ V_{ID} $	Differential input voltage magnitu	de, (SN65LVDM1677 only)	1 V
I _O	Receiver output current		±20 mA
P_D	Continuous power dissipation		See the Dissipation Rating Table
	Electrostatic discharge (3)	Y, Z, and GND	Class 3, A: 8 kV, B: 600 V
ESD	Electrostatic discharge (%)	All Pins	Class 3, A: 7 kV, B: 500 V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(2) All voltage values, except differential I/O bus voltages, are
 (3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

$\begin{array}{cc} PACKAGE & T_{A} \leq 25^\circC \\ POWER \ RATING \end{array}$		DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 85°C POWER RATING
DGG	2094 mW	16.7 mW/°C	1089 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	3	3.3	3.6	
VIH	High-level input voltage	2			
V _{IL}	Low-level input voltage			0.8	
$ V_{ID} $	Magnitude of differential input voltage	0.1		0.6	V
V _{IC}	Common-mode input voltage	$\frac{ V_{ID} }{2}$		$2.4 - \frac{ V_{ID} }{2}$	
				V _{CC} -0.8	V
I _{OL}	Receiver low-level output current			8	~^
I _{OH}	Receiver high-level output current	-8 ⁽¹⁾			ШA
T _A	Operating free-air temperature	-40		85	°C

(1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

SN65LVDM1676 SN65LVDM1677

SLLS430D-NOVEMBER 2000-REVISED JUNE 2007



ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TES	MIN	TYP(1)	MAX	UNIT	
DRIVER		I		I			I
Icc	Supply current	Driver enabled, receiver disabled $R_L = 50 \Omega$ ('LVDM1676) or $R_L = 100 \Omega$ ('LVDM1677)			140	175	mA
00		Driver disabled, rece	iver enabled, no load		45	60	
V _{OD}	Differential output voltage magnitude	R _L = 50 Ω ('LVDM16	76) or	247	340	454	
$\Delta V_{OD} $	Change in differential output voltage magnitude between logic states	$R_L = 100 \Omega$ ('LVDM1 See Figure 2 and Fig	677), jure 1	-50		50	mV
V _{OC(SS)}	Steady-state common-mode output voltage			1.125		1.37 5	V
ΔV _{OC(S} s)	Change in steady-state common-mode output voltage between logic states	$R_L = 50 \Omega$ ('LVDM16 $R_L = 100 \Omega$ ('LVDM1	76) or 677), See Figure 3	-50		50	mV
V _{OC(PP)}	Peak-to-peak common-mode output voltage				50	150	mV
I _{IH}	High-level input current	V _{IH} = 2 V			3	20	μA
IIL	Low-level input current	V _{IL} = 0.8 V			2	10	μA
	Short circuit output ourront	V_{OY} or $V_{OZ} = 0 V$				10	mA
IOS	Short-circuit output current	$V_{OD} = 0 V$				10	mA
I _{O(OFF)}	Power-off output current	$V_{CC} = 1.5 V,$	$V_0 = 2.4 V$	-10		10	μA
C _{IN}	Input capacitance	$V_{I} = 0.4 \sin (4E6\pi t) +$	- 0.5 V		5		pF
RECEIV	ER						
V _{IT+}	Positive-going differential input voltage threshold					100	
V _{IT-}	Negative-going differential input voltage threshold	See Figure 6 and 1a		-100			mv
V _{OH}	High-level output voltage	I _{OH} = -8 mA		2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 8 mA				0.4	V
	Input ourrest (V or 7 inputs)	$V_{IY} = V_{IZ} = 0 V$		-40	-24		
1	input current (1 of 2 inputs)	$V_{IY} = V_{IZ} = 2.4 V$			-8	-1.2	μΑ
		'LVDM1676	V_{IY} = 0 V and V_{IZ} = 100 mV, V_{IY} = 2.4 V and V_{IZ} = 2.3 V		5	10	μΑ
'ID	Dimenential input current μ_{IY} – μ_{ZI} (inputs)	'LVDM1677	V_{IY} = 0.2 V and V_{IZ} = 0 V, V_{IY} = 2.4 V and V_{IZ} = 2.2 V	1.5		2.2	mA
I _{I(OFF)}	Power-off input current (Y or Z inputs)	$V_{CC} = 0 V, V_{I} = 2.4 V$		-25		25	μA

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
DRIVER		L				
t _{PLH}	Propagation delay time, low-to-high-level output		1.3	2.5	3.6	
t _{PHL}	Propagation delay time, high-to-low-level output		1.3	2.5	3.6	
t _r	Differential output signal rise time	$B_{\rm L} = 50 \ \Omega$ (' VDM1676) or		0.5	1.2	
t _f	Differential output signal fall time	$R_{L} = 100 \Omega (LVDM1677),$		0.5	1.2	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})	$C_L = 10 \text{ pF}$, See Figure 4		0.1	0.6	
t _{sk(o)}	Channel-to-channel output skew ⁽²⁾			0.1	0.4	ns
t _{sk(pp)}	Part-to-part skew ⁽³⁾				1	
t _{PZH}	Propagation delay time, high-impedance-to-high-level output			11	20	
t _{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 5		10	20	
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output			3	10	
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output			3	10	
RECEIV	ER					
t _{PLH}	Propagation delay time, low-to-high-level output		1.5	3	4.5	
t _{PHL}	Propagation delay time, high-to-low-level output		1.5	3	4.5	
t _r	Output signal rise time			0.6	1.6	
t _f	Output signal fall time	C _L = 10 pF, See Figure 7		0.6	1.6	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			0.2	0.8	
t _{sk(o)}	Channel-to-channel output skew ⁽⁴⁾			0.7	1.2	ns
t _{sk(pp)}	Part-to-part skew ⁽⁵⁾				1	
t _{PZH}	Propagation delay time, high-impedance-to-high-level output			9	15	
t _{PZL}	Propagation delay time, high-impedance-to-low-level output	Soo Eiguro 8		8	15	
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output			12	20	
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output			11	20	

(1) All typical values are at 25° C and with a 3.3-V supply.

(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

(3) t_{sk(PP)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(4) $t_{sk(0)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

(5) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION







Figure 2. Driver V_{OD} Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of V_{OC(PP)} is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.





NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



Figure 6. Voltage Definitions

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE
VIY	V _{IZ}	V _{ID}	V _{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V

 Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 7. Timing Test Circuit and Waveforms



NOTE: All input pulses are supplied by a generator having the following characteristics: t_{f} or $t_{f} \leq$ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 \pm 10 ns. C_{L} includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.



A V_{OH} - 0.5 V - - - - V_{OH} V_{CC}/2

Figure 8. Enable/Disable Time Test Circuit and Waveforms





TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

DRIVER EYE PATTERN

TEST CONDITIONS

- V_{CC} = 3.6 V
- $T_A = 25^{\circ}C$ (ambient temperature)
- All 16 channels switching simultaneously with NRZ data. Scope is triggered at the same frequency with pulse. Input signal level = 0 V to 3 V single ended.
- Resistive loading with no added capacitance

EQUIPMENT

- Hewlett Packard HP6624A DC power supply
- Tektronix TDS6604 Digital Storage Scope
- Agilent ParBERT E4832A



Figure 14. Equipment Setup

TYPICAL CHARACTERISTICS (continued)



(a) representative Transceiver configured as Rx @ 200 Mbps (Ch1 = xyA)



(b) representative Transceiver configured as Tx @ 650 Mbps (M1 = xyY-xyZ)

NOTE: x represents transceiver group A, B, C, or D, and y represents transceiver 1, 2, 3, or 4.

Figure 15. Typical Driver Eye Pattern for the SN65LVDM1676 With 12 Transceivers Configured as Rx and 4 Transceivers Configured as Tx all Switching Frequency Asynchronous Data $(T_A = 25^{\circ}C; V_{CC} = 3.6 \text{ V}; \text{PRBS} = 2^{23-1})$



APPLICATION INFORMATION

FAIL SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –50 mV and 50 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different, however, in how it handles the open-input circuit situation.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-k Ω resistors as shown in Figure 16. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level, regardless of the differential input voltage.



Figure 16. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 50-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

V TEXAS NSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package	Package	Pins	Package	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LVDM1676DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1676DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1676DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1676DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1677DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1677DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1677DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1677DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	All dimensions are nominal													
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant		
SN65LVDM1676DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1		
SN65LVDM1677DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1		



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	is SPQ Length (mm) Width (mm) H		Height (mm)	
SN65LVDM1676DGGR	TSSOP	DGG	64	2000	346.0	346.0	41.0
SN65LVDM1677DGGR	TSSOP	DGG	64	2000	346.0	346.0	41.0

MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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