SBOS303C − JUNE 2004 − REVISED AUGUST 2008

Unity-Gain Stable, Low-Noise, Voltage-Feedback Operational Amplifier

FEATURES

- HIGH BANDWIDTH (240MHz, G = +2)
- HIGH OUTPUT CURRENT (±110mA)
- LOW INPUT NOISE (2.5nV/√Hz)
- LOW SUPPLY CURRENT (5.6mA)
- FLEXIBLE SUPPLY VOLTAGE:
  Dual ±2.5V to ±6V
  Single +5V to +12V
- EXCELLENT DC ACCURACY:
  Maximum 25°C Input Offset Voltage = ±750µV
  Maximum 25°C Input Offset Current = ±400nA

APPLICATIONS

- LOW-COST VIDEO LINE DRIVERS
- ADC PREAMPLIFIERS
- ACTIVE FILTERS
- LOW-NOISE INTEGRATORS
- PORTABLE TEST EQUIPMENT
- OPTICAL CHANNEL AMPLIFIERS
- LOW-POWER, BASEBAND AMPLIFIERS
- CCD IMAGING CHANNEL AMPLIFIERS
- OPA650 AND OPA620 UPGRADE

DESCRIPTION

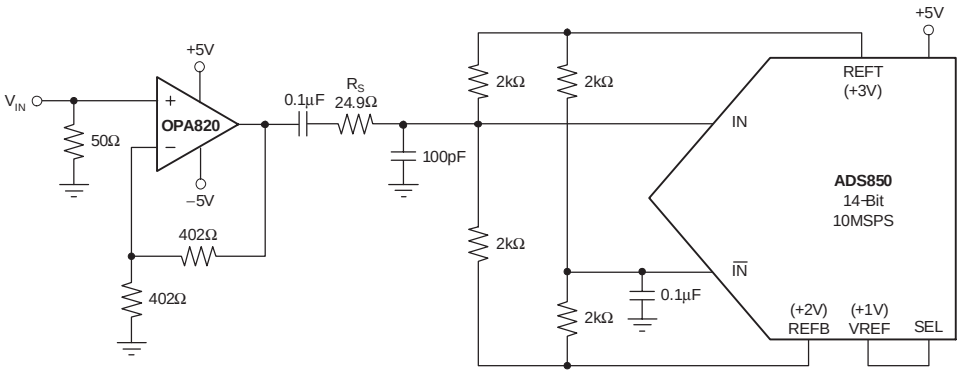
The OPA820 provides a wideband, unity-gain stable, voltage-feedback amplifier with a very low input noise voltage and high output current using a low 5.6mA supply current. At unity-gain, the OPA820 gives > 800MHz bandwidth with < 1dB peaking. The OPA820 complements this high-speed operation with excellent DC precision in a low-power device. A worst-case input offset voltage of ±750µV and an offset current of ±400nA give excellent absolute DC precision for pulse amplifier applications.

Minimal input and output voltage swing headroom allow the OPA820 to operate on a single +5V supply with > $2V_{PP}$ output swing. While not a rail-to-rail (RR) output, this swing will support most emerging analog-to-digital converter (ADC) input ranges with lower power and noise than typical RR output op amps.

Exceptionally low dG/dP (0.01%/0.03°) supports low-cost composite video line driver applications. Existing designs can use the industry-standard pinout SO-8 package while emerging high-density portable applications can use the SOT23-5. Offering the industry's lowest thermal impedance in a SOT package, along with full specification over both the commercial and industrial temperature ranges, gives solid performance over a wide temperature range.

RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	QUADS	FEATURES
OPA354	OPA2354	—	OPA4354	CMOS RR Output
OPA690	OPA2690	OPA3690	—	High Slew Rate
—	OPA2652	—	—	SOT23-8
—	OPA2822	—	—	Low Noise
—	—	—	OPA4820	Quad OPA820



AC-Coupled, 14-Bit ADS850 Interface

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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±6.5V$_{DC}$
Internal Power Dissipation	See Thermal Information
Differential Input Voltage	±1.2V
Input Common-Mode Voltage Range	±V_S
Storage Temperature Range	−65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating	
Human Body Model (HBM)	+3000V
Charge Device Model (CDM)	+1000V
Machine Model (MM)	+300V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

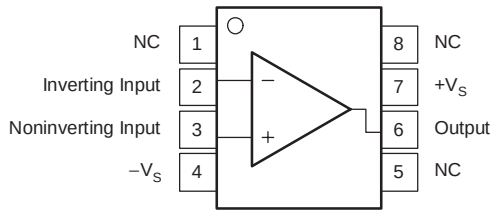
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA820	SO-8	D	−45°C to +85°C	OPA820	OPA820ID	Rails, 100
″	″	″	″	″	OPA820IDR	Tape and Reel, 2500
OPA820	SOT23-5	DBV	−45°C to +85°C	NSO	OPA820IDBVT	Tape and Reel, 250
″	″	″	″	″	OPA820IDBVR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

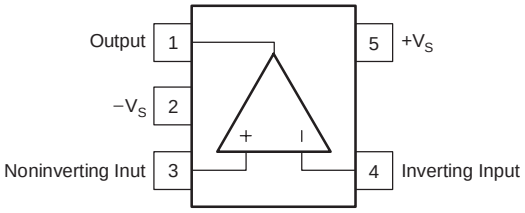
PIN CONFIGURATION

TOP VIEW **SO**



NC = No Connection

TOP VIEW **SOT**



Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, unless otherwise noted.

PARAMETER	CONDITIONS	OPA820ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	−40°C to +85°C(2)			
AC PERFORMANCE								
Small-Signal Bandwidth	G = +1, $V_O = 0.1V_{PP}$, $R_F = 0\Omega$	800				MHz	typ	C
	G = +2, $V_O = 0.1V_{PP}$	240	170	160	155	MHz	min	B
	G = +10, $V_O = 0.1V_{PP}$	30	23	21	20	MHz	min	B
Gain-Bandwidth Product	G ≥ 20	280	220	204	200	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +2, $V_O = 0.1V_{PP}$	38				MHz	typ	C
Peaking at a Gain of +1	$V_O = 0.1V_{PP}$, $R_F = 0$	0.5				dB	typ	C
Large-Signal Bandwidth	G = +2, $V_O = 2V_{PP}$	85				MHz	typ	C
Slew Rate	G = +2, 2V Step	240	192	186	180	V/µs	min	B
Rise Time and Fall Time	G = +2, V_O = 0.2V Step	1.5				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	22				ns	typ	C
to 0.1%	G = +2, V_O = 2V Step	18				ns	typ	C
Harmonic Distortion	G = +2, f = 1MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 200\Omega$	−85	−81	−80	−79	dBc	max	B
	$R_L \geq 500\Omega$	−90	−85	−83	−81	dBc	max	B
3rd-Harmonic	$R_L = 200\Omega$	−95	−90	−89	−88	dBc	max	B
	$R_L \geq 500\Omega$	−110	−105	−102	−100	dBc	max	B
Input Voltage Noise	f > 100kHz	2.5	2.7	2.8	2.9	nV/√Hz	max	B
Input Current Noise	f > 100kHz	1.7	2.6	2.8	3.0	pA/√Hz	max	B
Differential Gain	G = +2, PAL, $V_O = 1.4V_{PP}$, $R_L = 150\Omega$	0.01				%	typ	C
Differential Phase	G = +2, PAL, $V_O = 1.4V_{PP}$, $R_L = 150\Omega$	0.03				°	typ	C
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V, Input-Referred	66	**62**	61	60	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±0.2	**±0.75**	±1.0	±1.2	mV	max	A
Average Input Offset Voltage Drift	V_{CM} = 0V			4	4	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	−9	**−17**	−19	−23	µA	max	A
Average Input Bias Current Drift	V_{CM} = 0V			30	50	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±100	**±400**	±600	±700	nA	max	A
Inverting Input Bias Current Drift	V_{CM} = 0V			5	5	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)(5)		±4.0	**±3.8**	±3.7	±3.6	V	min	A
Common-Mode Rejection Ratio	V_{CM} = 0V, Input-Referred	85	**76**	75	73	dB	min	A
Input Impedance								
Differential Mode	V_{CM} = 0V	18 ‖0.8				kΩ ‖pF	typ	C
Common Mode	V_{CM} = 0V	6 ‖1.0				MΩ ‖pF	typ	C
OUTPUT								
Output Voltage Swing	No Load	±3.7	**±3.5**	±3.45	±3.4	V	min	A
	$R_L = 100\Omega$	±3.6	**±3.5**	±3.45	±3.4	V	min	A
Output Current	V_O = 0	±110	**±90**	±80	±75	mA	min	A
Short-Circuit Output Current	Output Shorted to Ground	±125				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.04				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			**±6.0**	±6.0	±6.0	v	max	A
Maximum Quiescent Current	V_S = ±5V	5.6	**5.75**	6.2	6.4	mA	max	A
Minimum Quiescent Current	V_S = ±5V	5.6	**5.45**	5.0	4.8	mA	min	A
Power-Supply Rejection Ratio (−PSRR)	Input Referred	72	**64**	63	62	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IDBV		−40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-8	Junction-to-Ambient	125				°C/W	typ	C
DBV SOT23-5	Junction-to-Ambient	150				°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +9°C at high temperature limit for over temperature.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted.

PARAMETER	CONDITIONS	OPA820ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	−40°C to +85°C(2)			
AC PERFORMANCE								
Small-Signal Bandwidth	G = +1, V_O = 0.1V_{PP}, R_F = 0Ω	550				MHz	typ	C
	G = +2, V_O = 0.1V_{PP}	230	168	155	151	MHz	min	B
	G = +10, V_O = 0.1V_{PP}	28	21	20	19	MHz	min	B
Gain-Bandwidth Product	G ≥ 20	260	200	190	185	MHz	min	B
Peaking at a Gain of 1	V_O = 0.1V_{PP}, R_F = 0Ω	0.5				dB	typ	C
Large-Signal Bandwidth	G = +2, V_O = 2V_{PP}	70				MHz	typ	C
Slew Rate	G = +2, 2V Step	200	145	140	135	V/µs	min	B
Rise Time and Fall Time	G = +2, V_O = 2V Step	1.7				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	24				ns	typ	C
to 0.1%	G = +2, V_O = 2V Step	21				ns	typ	C
Harmonic Distortion	G = +2, f = 1MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 200Ω	−80	−76	−75	−74	dBc	max	B
	R_L ≥ 500Ω	−83	−79	−77	−75	dBc	max	B
3rd-Harmonic	R_L = 200Ω	−100	−92	−91	−90	dBc	max	B
	R_L ≥ 500Ω	−98	−95	−93	−92	dBc	max	B
Input Voltage Noise	f > 100kHz	2.5	2.8	2.9	3.0	nV/√Hz	max	B
Input Current Noise	f > 100kHz	1.6	2.5	2.7	2.9	pA/√Hz	max	B
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 2.5V, R_L = 100Ω	65	**60**	59	58	dB	min	A
Input Offset Voltage	V_{CM} = 2.5V	±0.3	**±1.1**	±1.4	±1.6	mV	max	A
Average Input Offset Voltage Drift	V_{CM} = 2.5V			4	4	µV/°C	max	B
Input Bias Current	V_{CM} = 2.5V	−8	**−16**	−18	−22	µA	max	A
Average Input Bias Current Drift	V_{CM} = 2.5V			30	50	nA/°C	max	B
Input Offset Current	V_{CM} = 2.5V	±100	**±400**	±600	±700	nA	max	A
Inverting Input Bias Current Drift	V_{CM} = 2.5V			5	5	nA/°C	max	B
INPUT								
Least Positive Input Voltage		0.9	**1.1**	1.2	1.3	V	min	A
Most Positive Input Voltage		4.5	**4.2**	4.1	4.0	V	max	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 2.5V, Input-Referred	83	**74**	73	72	dB	min	A
Input Impedance								
Differential Mode	V_{CM} = 2.5V	15 ‖1				kΩ ‖pF	typ	C
Common Mode	V_{CM} = 2.5V	5 ‖1.3				MΩ ‖pF	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	+3.9	**+3.8**	+3.75	+3.7	V	min	A
	R_L = 100Ω to 2.5V	+3.8	**+3.7**	+3.65	+3.6	V	min	A
Least Positive Output Voltage	No Load	+1.2	**+1.3**	+1.35	+1.4	V	max	A
	R_L = 100Ω to 2.5V	+1.2	**+1.3**	+1.35	+1.4	V	max	A
Output Current	V_O = 2.5V	±105	**±80**	±70	±65	mA	min	A
Short-Circuit Output Current	Output Shorted to Ground	±115				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.04				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		+5				V	typ	C
Maximum Operating Voltage			**+12**	+12	+12	V	max	A
Maximum Quiescent Current	V_S = +5V	5.0	**5.4**	5.5	5.6	mA	max	A
Minimum Quiescent Current	V_S = +5V	5.0	**4.4**	4.25	4.1	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input-Referred	68				dB	typ	C
THERMAL CHARACTERISTICS								
Specification: ID, IDBV		−40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-8	Junction-to-Ambient	125				°C/W	typ	C
DBV SOT23-5	Junction-to-Ambient	150				°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.

(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +7°C at high temperature limit for over temperature.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

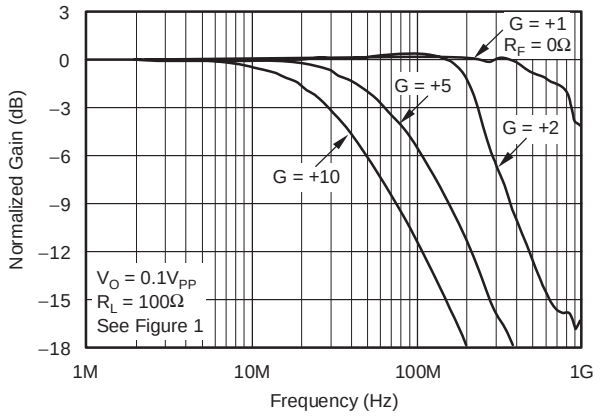
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

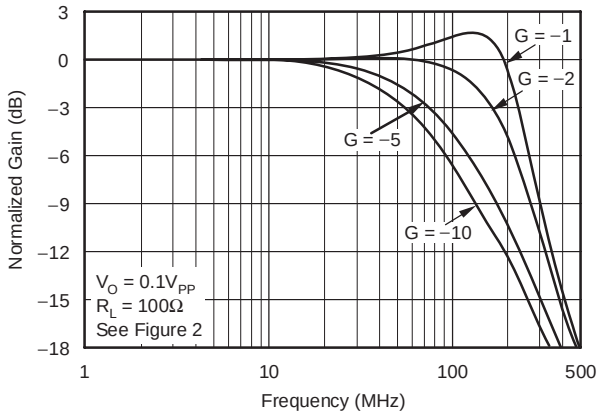
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, unless otherwise noted.

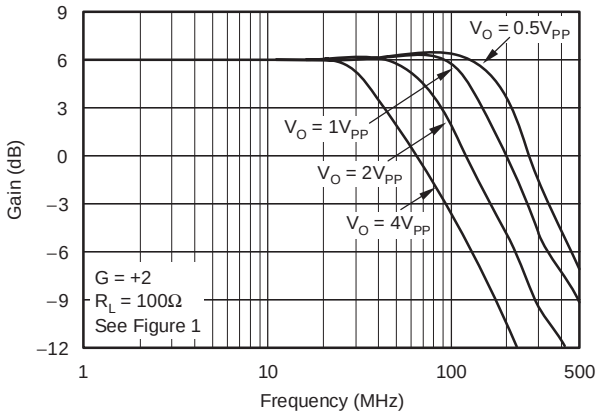
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



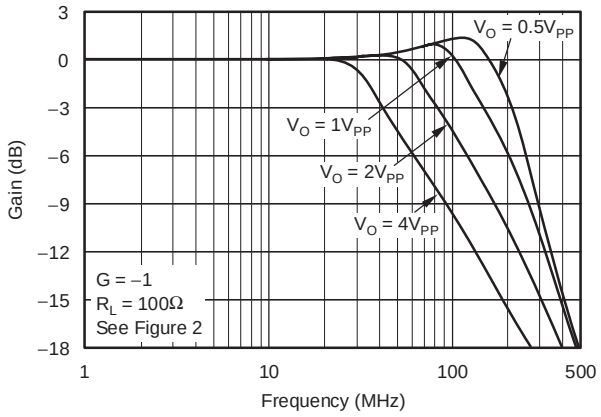
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



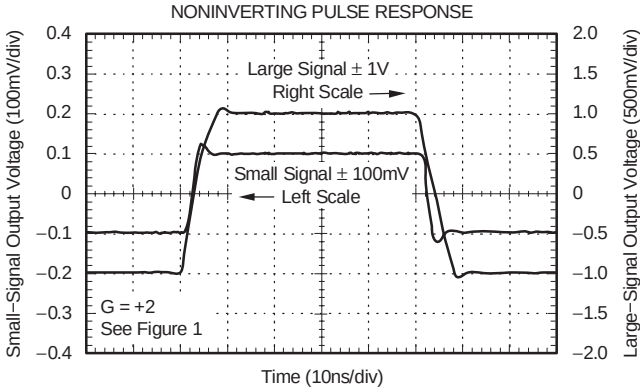
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



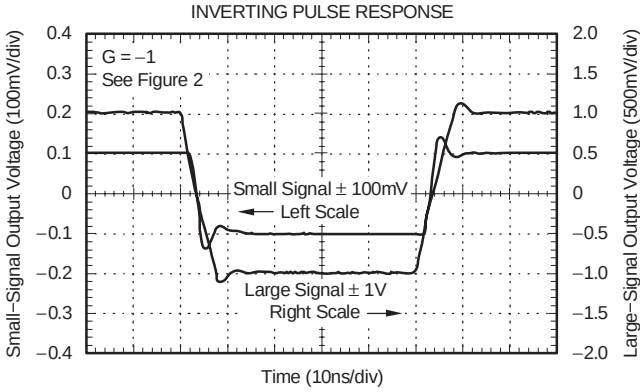
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



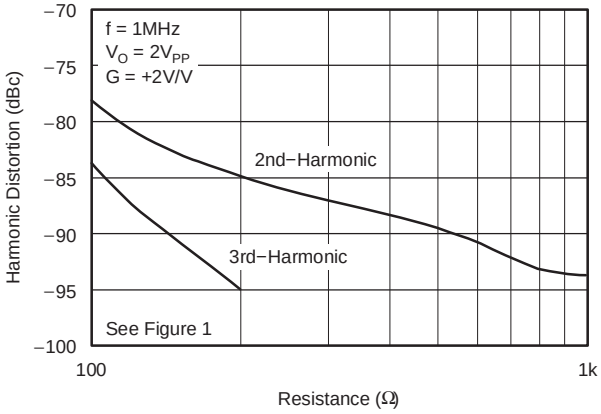
INVERTING PULSE RESPONSE



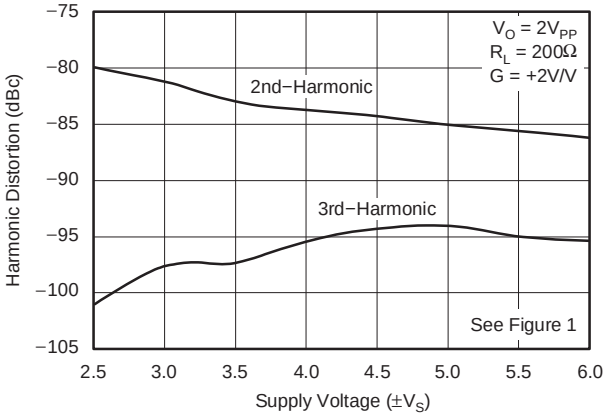
TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted.

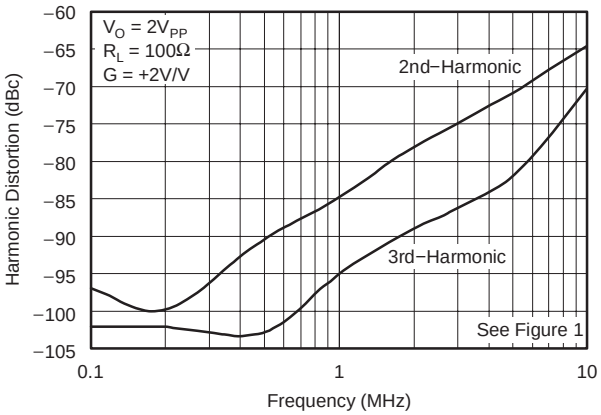
HARMONIC DISTORTION vs LOAD RESISTANCE



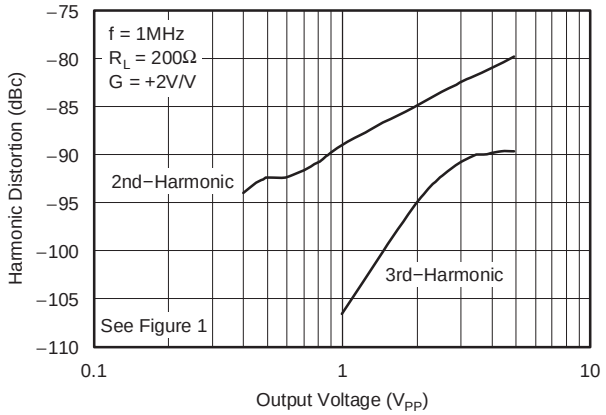
1MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



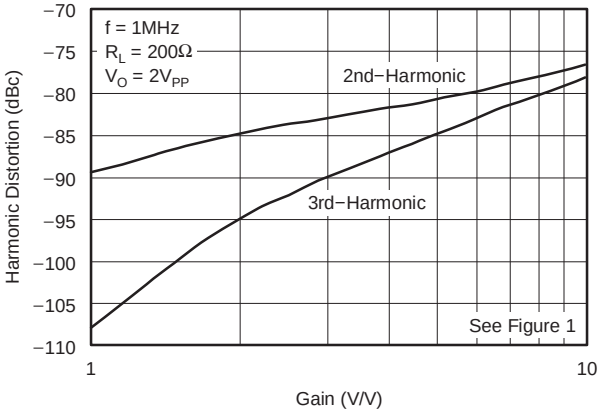
HARMONIC DISTORTION vs FREQUENCY



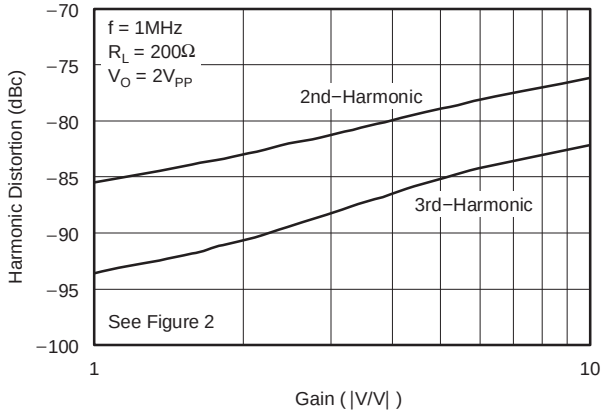
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



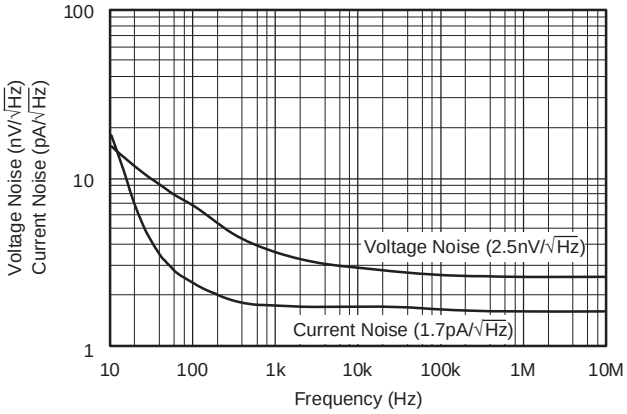
HARMONIC DISTORTION vs INVERTING GAIN



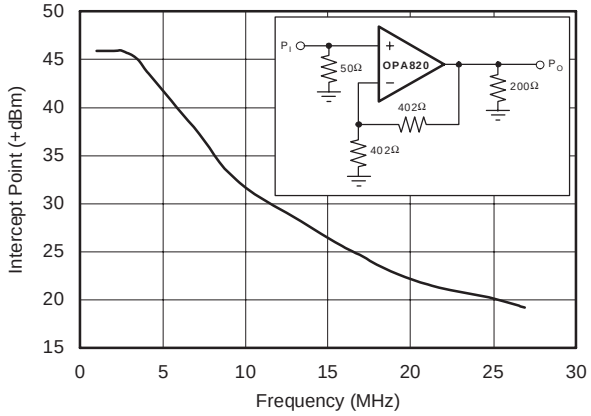
TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted.

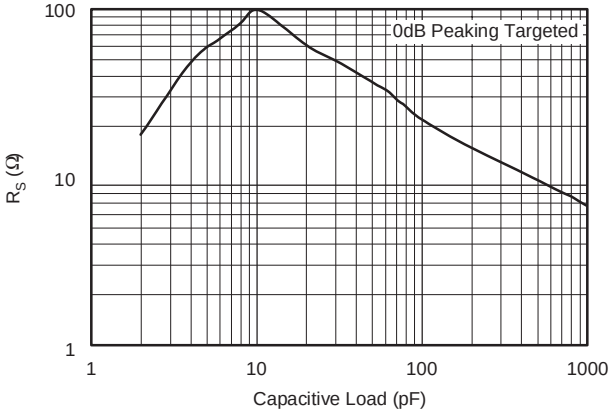
INPUT VOLTAGE AND CURRENT NOISE



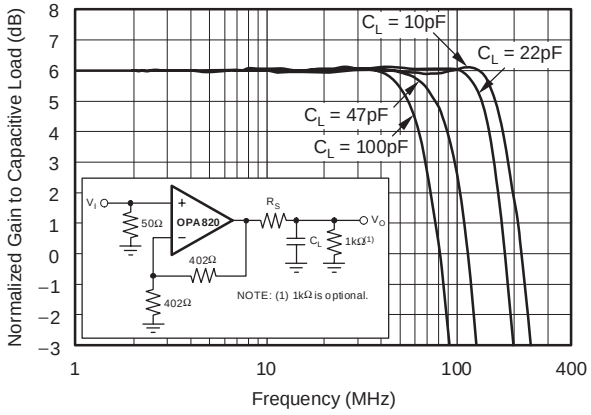
TWO−TONE, 3RD−ORDER
INTERMODULATION INTERCEPT



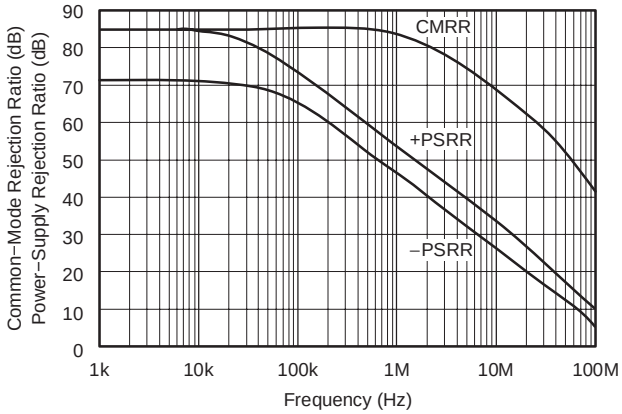
RECOMMENDED R_S vs CAPACITIVE LOAD



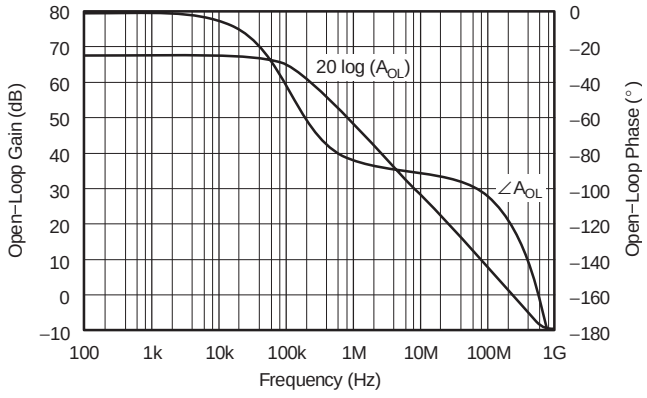
FREQUENCY RESPONSE vs CAPACITIVE LOAD



CMRR AND PSRR vs FREQUENCY



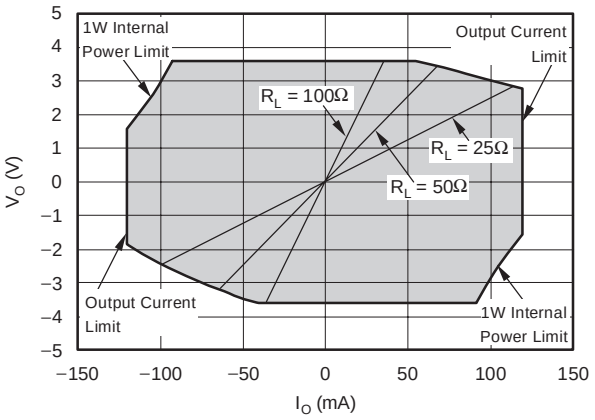
OPEN−LOOP GAIN AND PHASE



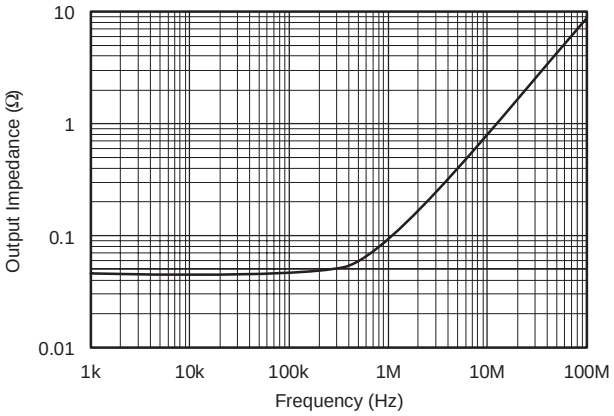
TYPICAL CHARACTERISTICS: $V_S = \pm5V$ (continued)

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, unless otherwise noted.

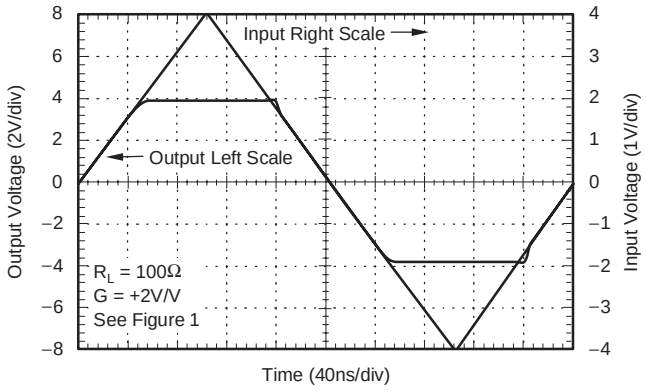
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



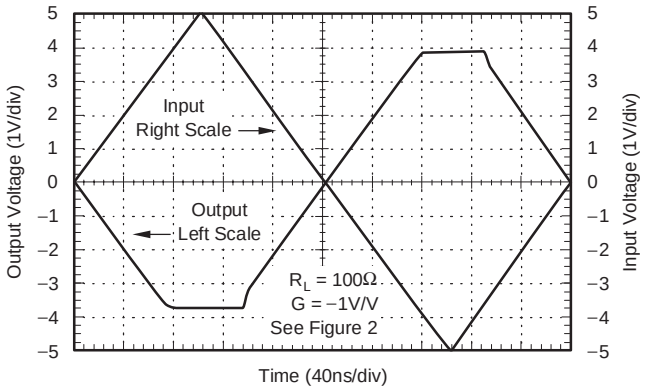
CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY



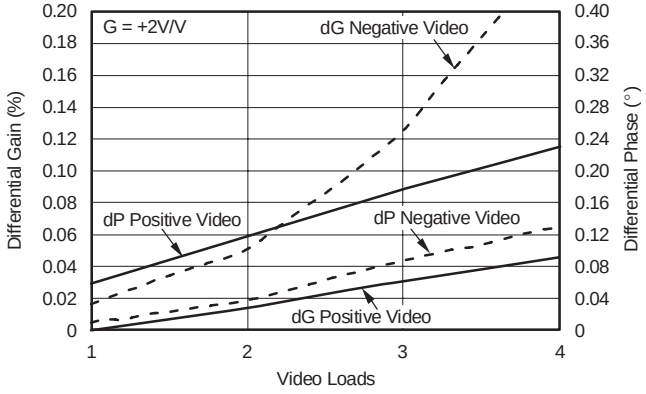
NONINVERTING OVERDRIVE RECOVERY



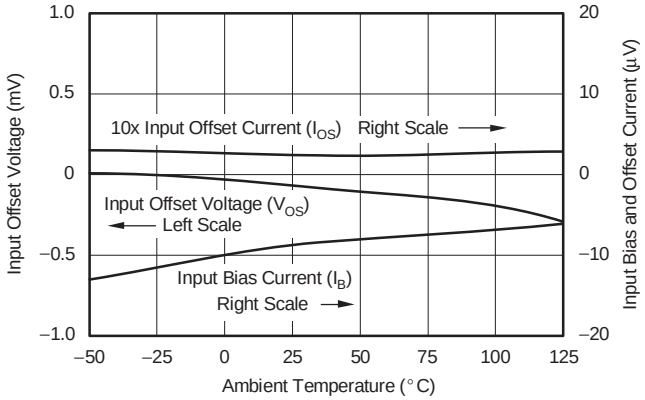
INVERTING OVERDRIVE RECOVERY



COMPOSITE VIDEO dG/dP



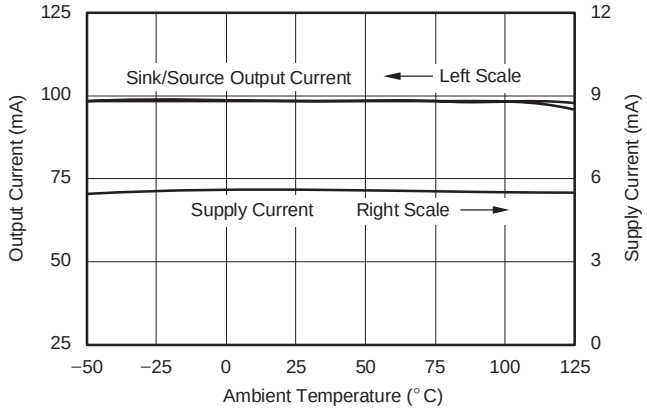
TYPICAL DC DRIFT OVER TEMPERATURE



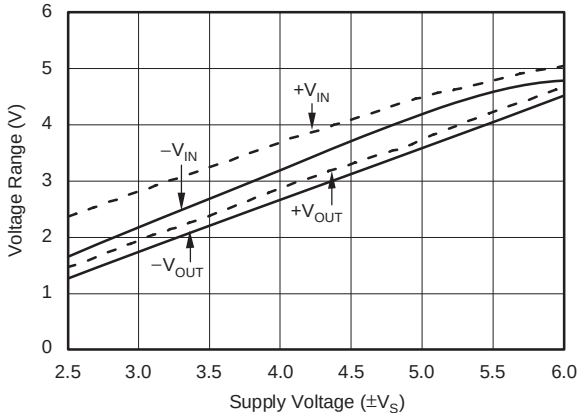
TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted.

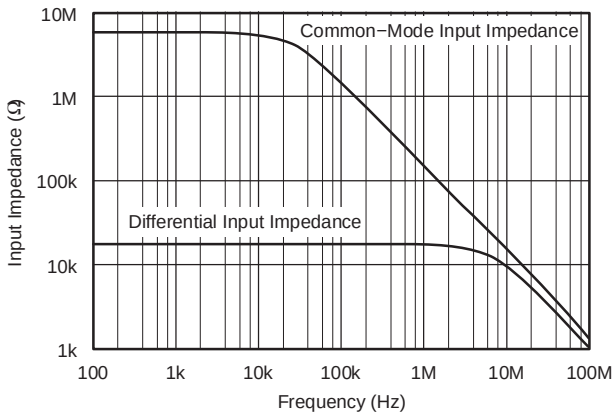
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



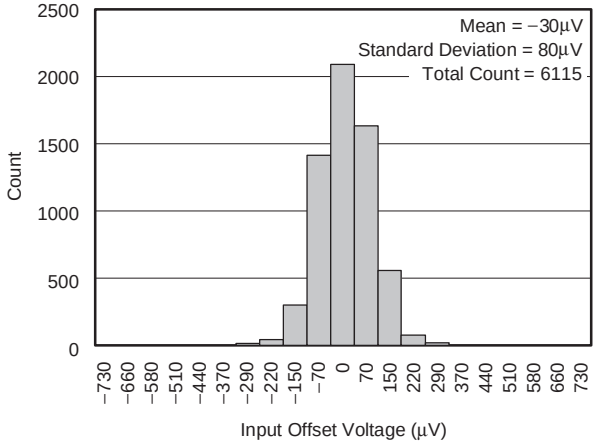
COMMON−MODE INPUT RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE



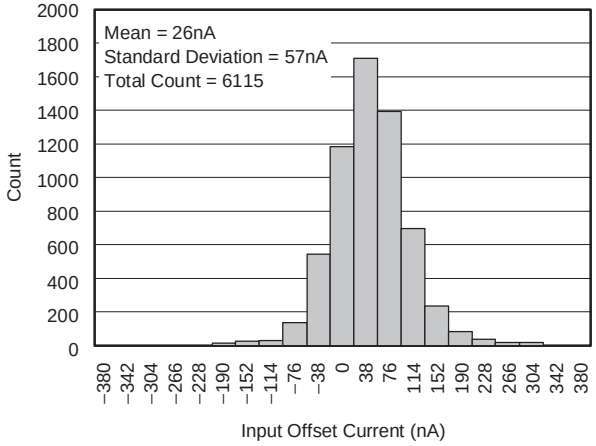
COMMON−MODE AND DIFFERENTIAL INPUT IMPEDANCE



TYPICAL INPUT OFFSET VOLTAGE DISTRIBUTION



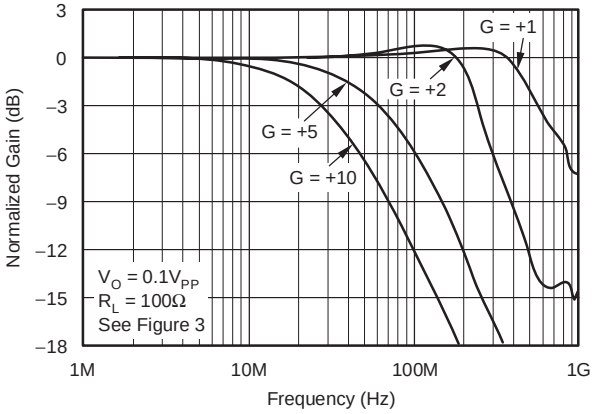
TYPICAL INPUT OFFSET CURRENT DISTRIBUTION



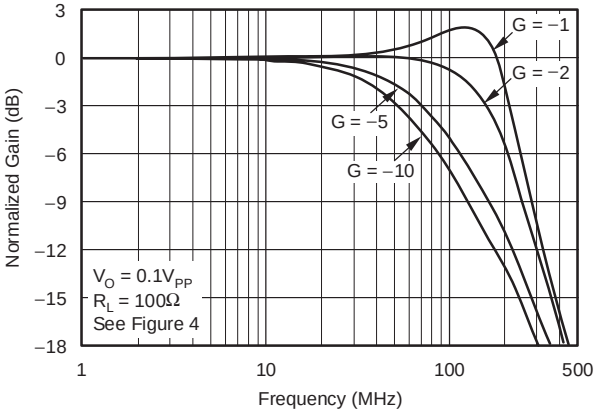
TYPICAL CHARACTERISTICS: V_S = +5V

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted.

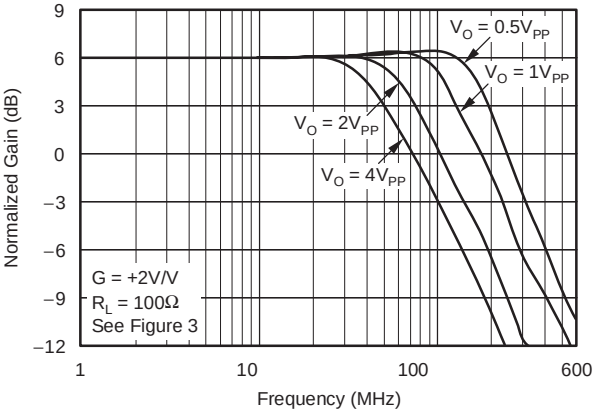
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



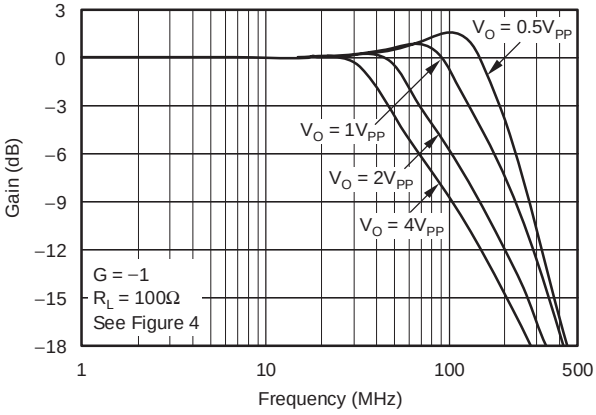
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



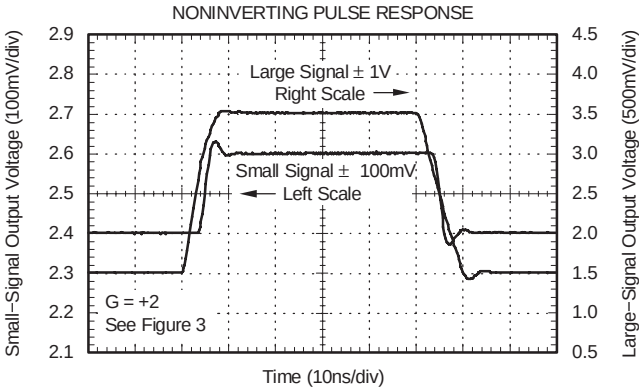
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



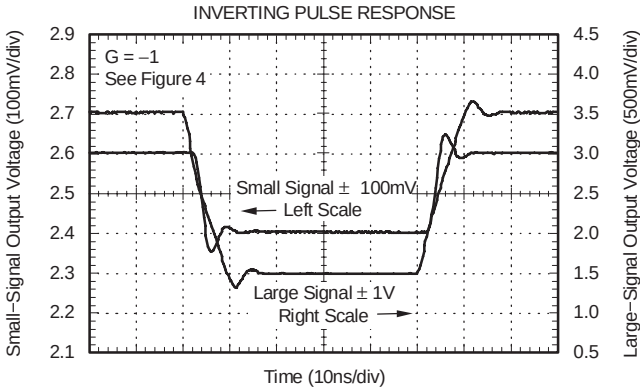
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



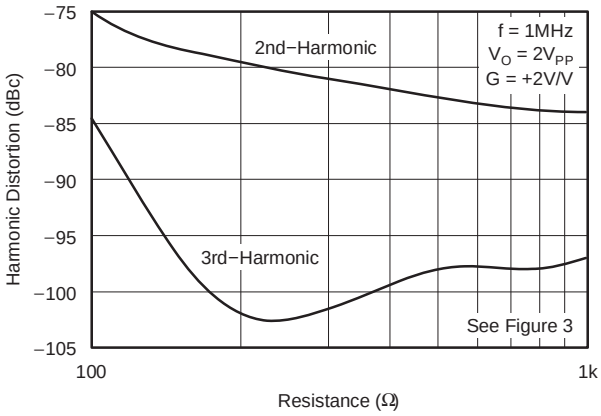
INVERTING PULSE RESPONSE



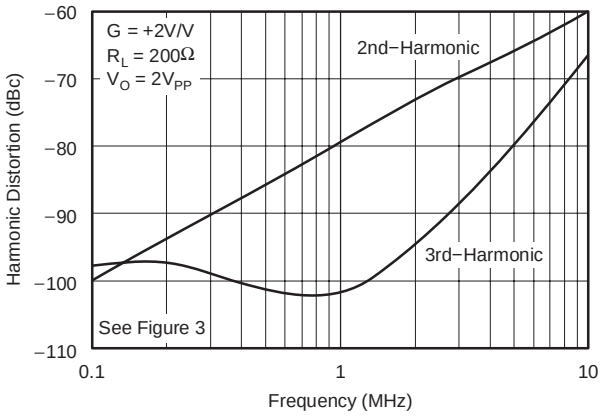
TYPICAL CHARACTERISTICS: V_S = +5V (continued)

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted.

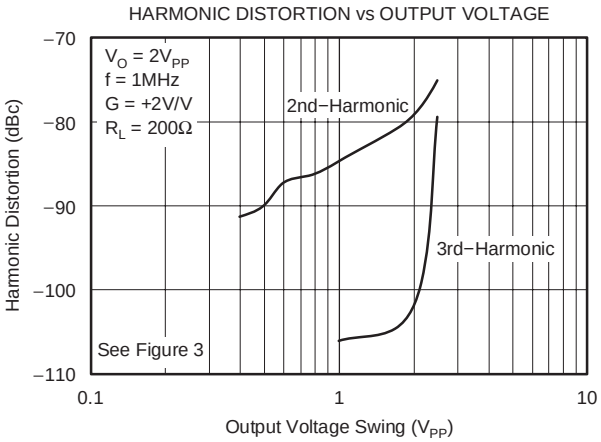
HARMONIC DISTORTION vs LOAD RESISTANCE



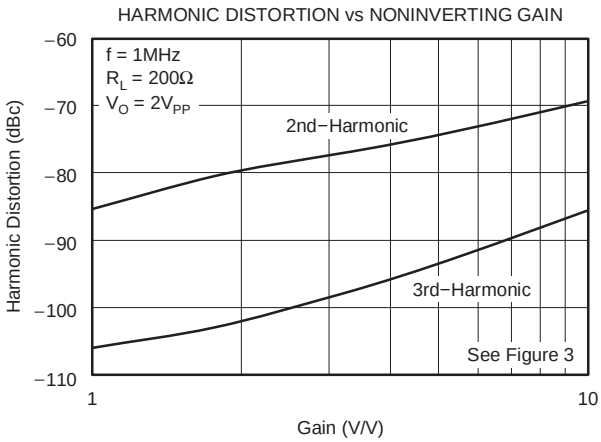
HARMONIC DISTORTION vs FREQUENCY



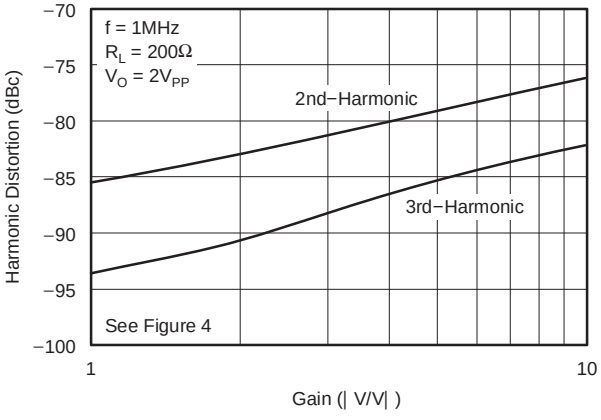
HARMONIC DISTORTION vs OUTPUT VOLTAGE



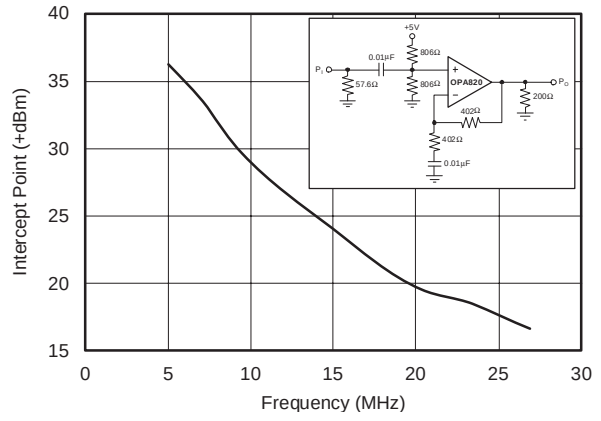
HARMONIC DISTORTION vs NONINVERTING GAIN



HARMONIC DISTORTION vs INVERTING GAIN



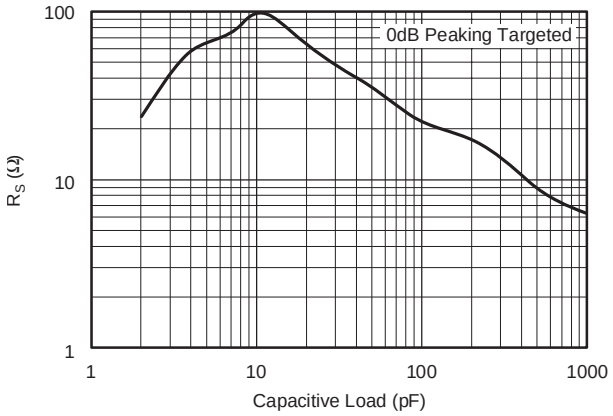
TWO−TONE, 3RD−ORDER
INTERMODULATION INTERCEPT



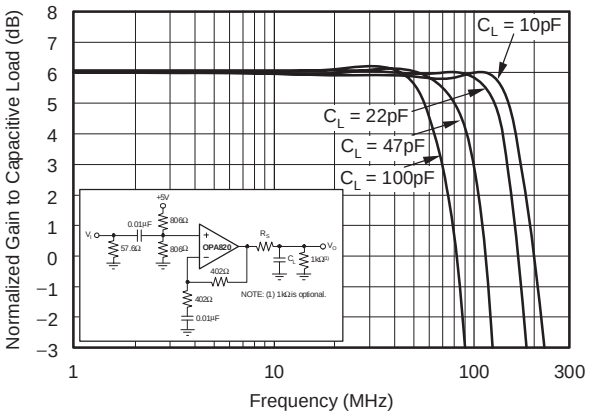
TYPICAL CHARACTERISTICS: V_S = +5V (continued)

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted.

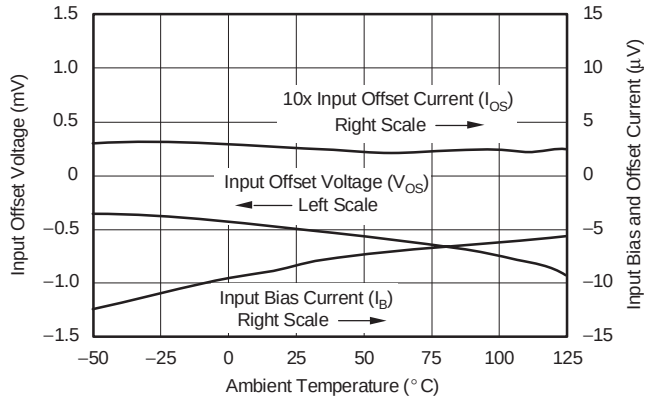
RECOMMENDED R_S vs CAPACITIVE LOAD



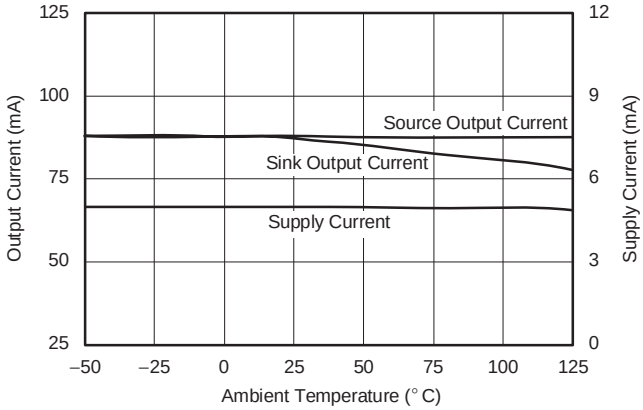
FREQUENCY RESPONSE vs CAPACITIVE LOAD



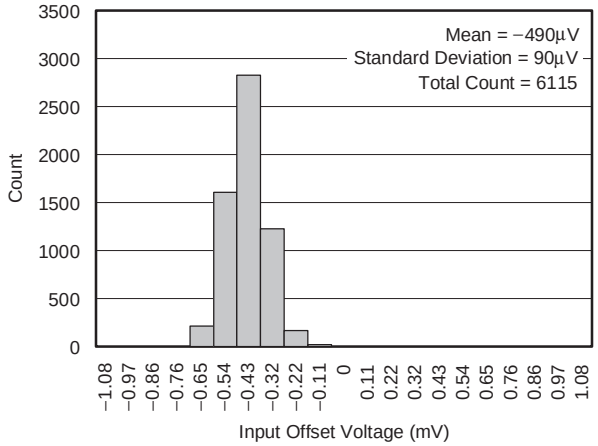
TYPICAL DC DRIFT OVER TEMPERATURE



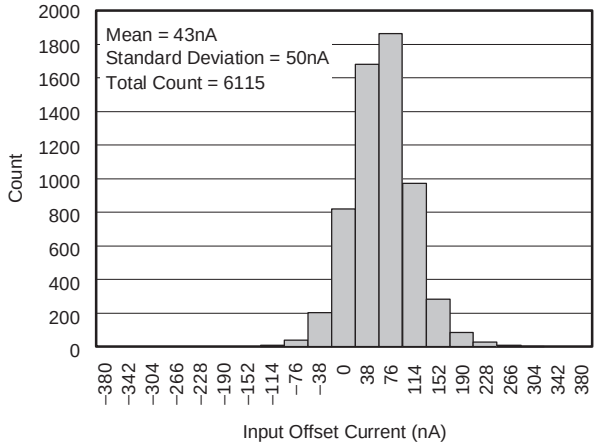
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



TYPICAL INPUT OFFSET VOLTAGE DISTRIBUTION



TYPICAL INPUT OFFSET CURRENT DISTRIBUTION



APPLICATIONS INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The combination of speed and dynamic range offered by the OPA820 is easily achieved in a wide variety of application circuits, providing that simple principles of good design practice are observed. For example, good power-supply decoupling, as shown in Figure 1, is essential to achieve the lowest possible harmonic distortion and smooth frequency response.

Proper PC board layout and careful component selection will maximize the performance of the OPA820 in all applications, as discussed in the following sections of this data sheet.

Figure 1 shows the gain of +2 configuration used as the basis for most of the typical characteristics. Most of the curves were characterized using signal sources with 50Ω driving impedance and with measurement equipment presenting 50Ω load impedance. In Figure 1, the 50Ω shunt resistor at the V_I terminal matches the source impedance of the test generator while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet specifications refer to the voltage swings at the output pin (V_O in Figure 1). The 100Ω load, combined with the 804Ω total feedback network load, presents the OPA820 with an effective load of approximately 90Ω in Figure 1.

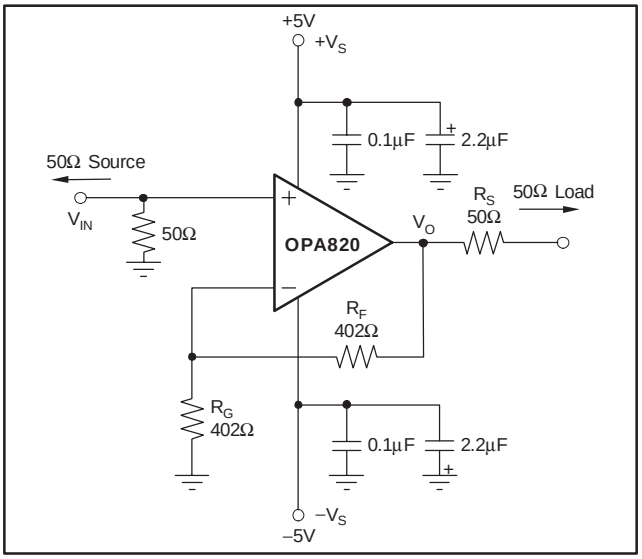


Figure 1. Gain of +2, High-Frequency Application and Characterization Circuit

WIDEBAND INVERTING OPERATION

Operating the OPA820 as an inverting amplifier has several benefits and is particularly useful when a matched 50Ω source and input impedance is required. Figure 2 shows the inverting gain of −1 circuit used as the basis of the inverting mode typical characteristics.

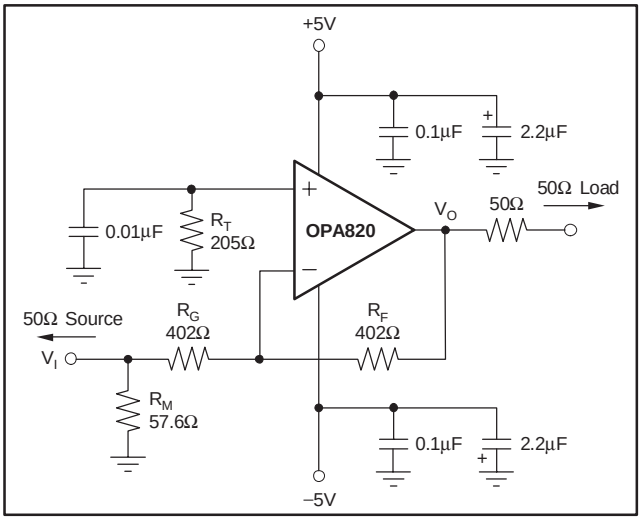


Figure 2. Inverting G = −1 Specifications and Test Circuit

In the inverting case, just the feedback resistor appears as part of the total output load in parallel with the actual load. For the 100Ω load used in the typical characteristics, this gives a total load of 80Ω in this inverting configuration. The gain resistor is set to get the desired gain (in this case 402Ω for a gain of −1) while an additional input matching resistor (R_M) can be used to set the total input impedance equal to the source if desired. In this case, R_M = 57.6Ω in parallel with the 402Ω gain setting resistor gives a matched input impedance of 50Ω. This matching is only needed when the input needs to be matched to a source impedance, as in the characterization testing done using the circuit of Figure 2.

The OPA820 offers extremely good DC accuracy as well as low noise and distortion. To take full advantage of that DC precision, the total DC impedance looking out of each of the input nodes must be matched to get bias current cancellation. For the circuit of Figure 2, this requires the 205Ω resistor shown to ground on the noninverting input. The calculation for this resistor includes a DC-coupled 50Ω source impedance along with R_G and R_M. Although this resistor will provide cancellation for the bias current, it must be well decoupled (0.01µF in Figure 2) to filter the noise contribution of the resistor and the input current noise.

As the required R_G resistor approaches 50Ω at higher gains, the bandwidth for the circuit in Figure 2 will far exceed the bandwidth at that same gain magnitude for the noninverting circuit of Figure 1. This occurs due to the lower *noise gain* for the circuit of Figure 2 when the 50Ω source impedance is included in the analysis. For instance, at a signal gain of −10 (R_G = 50Ω, R_M = open, R_F = 499Ω) the noise gain for the circuit of Figure 2 will be 1 + 499Ω/(50Ω + 50Ω) = 6 as a result of adding the 50Ω source in the noise gain equation. This gives considerable higher bandwidth than the noninverting gain of +10. Using the 240MHz gain bandwidth product for the OPA820, an inverting gain of −10 from a 50Ω source to a 50Ω R_G gives 55MHz bandwidth, whereas the noninverting gain of +10 gives 30MHz.

WIDEBAND SINGLE-SUPPLY OPERATION

Figure 3 shows the AC-coupled, single +5V supply, gain of +2V/V circuit configuration used as a basis for the +5V only Electrical and Typical Characteristics. The key requirement for single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors) to the noninverting input. The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 0.9V of the negative supply and 0.5V of the positive supply, giving a $3.6V_{PP}$ input signal range. The input impedance matching resistor (57.6Ω) used in Figure 3 is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1. This puts the input DC bias voltage (2.5V) on the output as well. On a single +5V supply, the output voltage can swing to within 1.3V of either supply pin while delivering more than 80mA output current giving 2.4V output swing into 100Ω (5.6dBm maximum at the matched load).

Figure 4 shows the AC-coupled, single +5V supply, gain of −1V/V circuit configuration used as a basis for the +5V only Typical Characteristic curves. In this case, the midpoint DC bias on the noninverting input is also decoupled with an additional 0.01µF decoupling capacitor. This reduces the source impedance at higher frequencies for the noninverting input bias current noise. This 2.5V bias on the noninverting input pin appears on the inverting input pin and, since R_G is DC blocked by the input capacitor, will also appear at the output pin.

The single-supply test circuits of Figure 3 and Figure 4 show +5V operation. These same circuits can be used over a single-supply range of +5V to +12V. Operating on a single +12V supply, with the Absolute Maximum Supply voltage specification of +13V, gives adequate design margin for the typical ±5% supply tolerance.

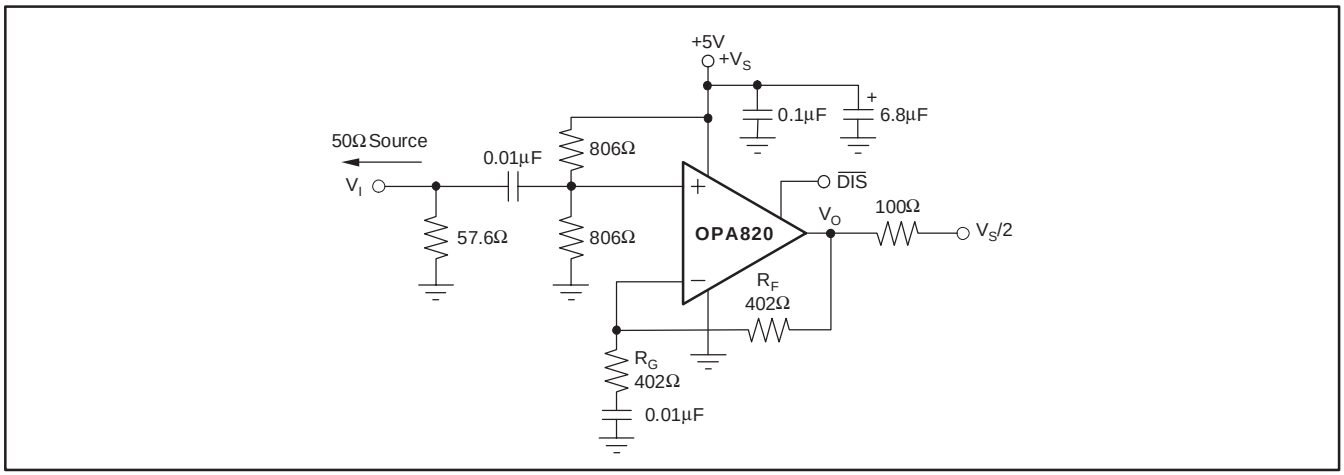


Figure 3. AC-Coupled, G = +2V/V, Single-Supply Specifications and Test Circuit

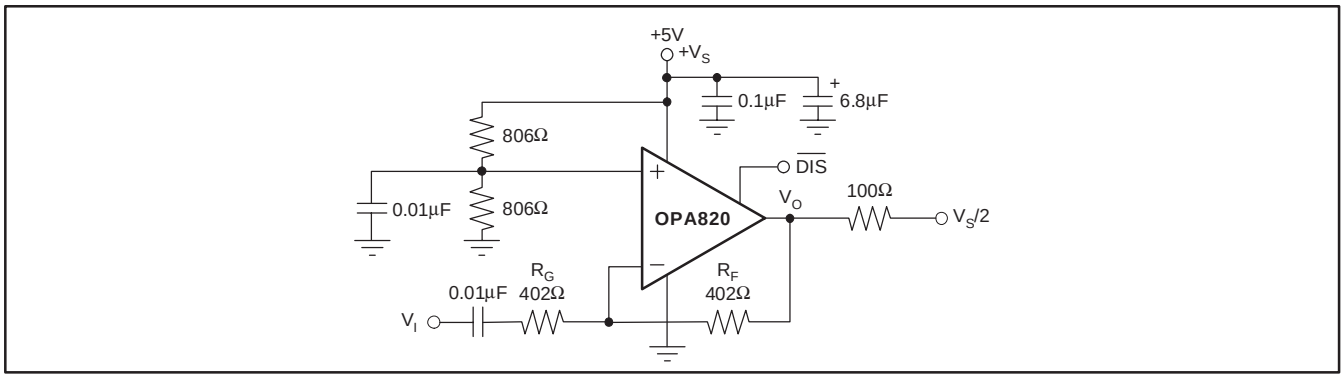


Figure 4. AC-Coupled, G = −1V/V, Single-Supply Specifications and Test Circuit

BUFFERING HIGH-PERFORMANCE ADCs

To achieve full performance from a high dynamic range ADC, considerable care must be exercised in the design of the input amplifier interface circuit. The example circuit on the front page shows a typical AC-coupled interface to a very high dynamic range converter. This AC-coupled example allows the OPA820 to be operated using a signal range that swings symmetrically around ground (0V). The $2V_{PP}$ swing is then level-shifted through the blocking capacitor to a midscale reference level, which is created by a well-decoupled resistive divider off the converter's internal reference voltages. To have a negligible effect (1dB) on the rated spurious-free dynamic range (SFDR) of the converter, the amplifier's SFDR should be at least 18dB greater than the converter. The OPA820 has minimal effect on the rated distortion of the ADS850, given its 79dB SFDR at $2V_{PP}$, 1MHz. The > 90dB (< 1MHz) SFDR for the OPA820 in this configuration implies a < 3dB degradation (for the system) from the converter's specification. For further SFDR improvement with the OPA820, a differential configuration is suggested.

Successful application of the OPA820 for ADC driving requires careful selection of the series resistor at the amplifier output, along with the additional shunt capacitor at the ADC input. To some extent, selection of this RC network will be determined empirically for each converter. Many high-performance CMOS ADCs, such as the ADS850, perform better with the shunt capacitor at the input pin. This capacitor provides low source impedance for the transient currents produced by the sampling process. Improved SFDR is often obtained by adding this external capacitor, whose value is often recommended in this converter data sheet. The external capacitor, in combination with the built-in capacitance of the ADC input, presents a significant capacitive load to the OPA820. Without a series isolation resistor, an undesirable peaking or loss of stability in the amplifier may result.

Since the DC bias current of the CMOS ADC input is negligible, the resistor has no effect on overall gain or offset accuracy. Refer to the typical characteristic *R_S vs Capacitive Load* to obtain a good starting value for the series resistor. This will ensure flat frequency response to the ADC input. Increasing the external capacitor value will allow the series resistor to be reduced. Intentionally bandlimiting using this RC network can also be used to limit noise at the converter input.

VIDEO LINE DRIVING

Most video distribution systems are designed with 75Ω series resistors to drive a matched 75Ω cable. In order to deliver a net gain of 1 to the 75Ω matched load, the amplifier is typically set up for a voltage gain of +2, compensating for the 6dB attenuation of the voltage divider formed by the series and shunt 75Ω resistors at either end of the cable.

The circuit of Figure 1 applies to this requirement if all references to 50Ω resistors are replaced by 75Ω values. Often, the amplifier gain is further increased to 2.2, which recovers the additional DC loss of a typical long cable run. This change would require the gain resistor (R_G) in Figure 1 to be reduced from 402Ω to 335Ω. In either case, both the gain flatness and the differential gain/phase performance of the OPA820 will provide exceptional results in video distribution applications. Differential gain and phase measure the change in overall small-signal gain and phase for the color sub-carrier frequency (3.58MHz in NTSC systems) versus changes in the large-signal output level (which represents luminance information in a composite video signal). The OPA820, with the typical 150Ω load of a single matched video cable, shows less than 0.01%/0.01° differential gain/phase errors over the standard luminance range for a positive video (negative sync) signal. Similar performance would be observed for multiple video signals, as shown in Figure 5.

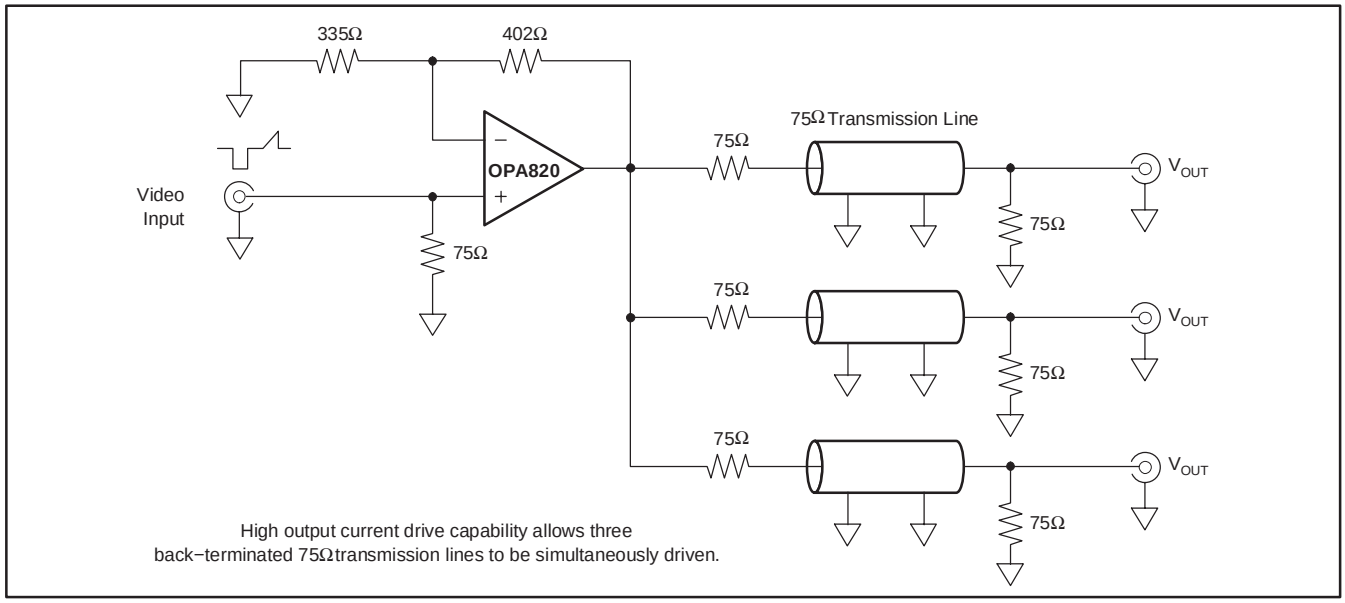


Figure 5. Video Distribution Amplifier

SINGLE OP AMP DIFFERENTIAL AMPLIFIER

The voltage-feedback architecture of the OPA820, with its high common-mode rejection ratio (CMRR), will provide exceptional performance in differential amplifier configurations. Figure 6 shows a typical configuration. The starting point for this design is the selection of the R_F value in the range of 200Ω to 2kΩ. Lower values reduce the required R_G, increasing the load on the V_2 source and on the OPA820 output. Higher values increase output noise as well as the effects of parasitic board and device capacitances. Following the selection of R_F, R_G must be set to achieve the desired inverting gain for V_2. Remember that the bandwidth will be set approximately by the gain bandwidth product (GBP) divided by the noise gain ($1 + R_F/R_G$). For accurate differential operation (that is, good CMRR), the ratio R_2/R_1 must be set equal to R_F/R_G.

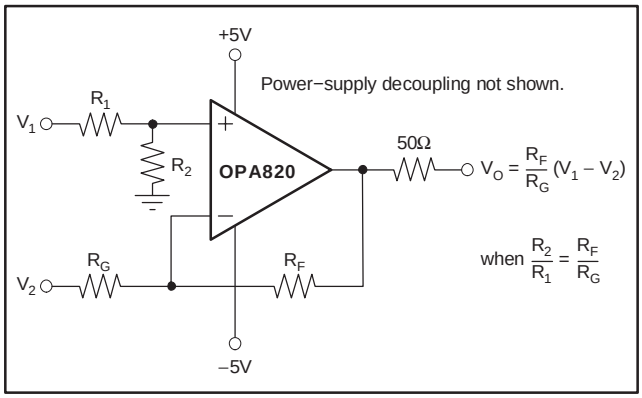


Figure 6. High-Speed, Single Differential Amplifier

Usually, it is best to set the absolute values of R_2 and R_1 equal to R_F and R_G, respectively; this equalizes the divider resistances and cancels the effect of input bias currents. However, it is sometimes useful to scale the values of R_2 and R_1 in order to adjust the loading on the driving source, V_1. In most cases, the achievable low-frequency CMRR will be limited by the accuracy of the resistor values. The 85dB CMRR of the OPA820 itself will not determine the overall circuit CMRR unless the resistor ratios are matched to better than 0.003%. If it is necessary to trim the CMRR, then R_2 is the suggested adjustment point.

THREE OP AMP DIFFERENCING (Instrumentation Topology)

The primary drawback of the single op amp differential amplifier is its relatively low input impedances. Where high impedance is required at the differential input, a standard instrumentation amplifier (INA) topology may be built using the OPA820 as the differencing stage. Figure 7 shows an example of this, in which the two input amplifiers are packaged together as a dual voltage-feedback op amp, the OPA2822. This approach saves board space, cost, and power compared to using two additional OPA820 devices, and still achieves very good noise and distortion performance as a result of the moderate loading on the input amplifiers.

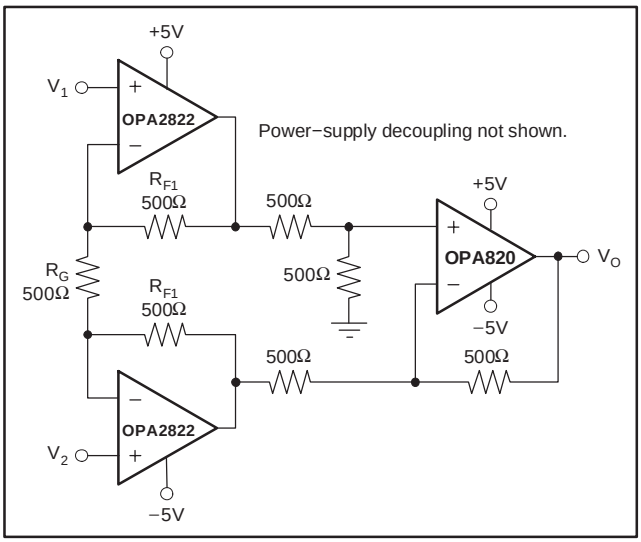


Figure 7. Wideband 3-Op Amp Differencing Amplifier

In this circuit, the common-mode gain to the output is always 1, because of the four matched 500Ω resistors, whereas the differential gain is set by ($1 + 2R_{F1}/R_G$), which is equal to 2 using the values in Figure 7. The differential to single-ended conversion is still performed by the OPA820 output stage. The high-impedance inputs allow the V_1 and V_2 sources to be terminated or impedance-matched as required. If the V_1 and V_2 inputs are already truly differential, such as the output from a signal transformer, then a single matching termination resistor may be used between them. Remember, however, that a defined DC signal path must always exist for the V_1 and V_2 inputs; for the transformer case, a center-tapped secondary connected to ground would provide an optimum DC operating point.

DAC TRANSIMPEDANCE AMPLIFIER

High-frequency Digital-to-Analog Converters (DACs) require a low-distortion output amplifier to retain their SFDR performance into real-world loads. See Figure 8 for a single-ended output drive implementation. In this circuit, only one side of the complementary output drive signal is used. The diagram shows the signal output current connected into the virtual ground-summing junction of the OPA820, which is set up as a transimpedance stage or *I-V converter*. The unused current output of the DAC is connected to ground. If the DAC requires its outputs to be terminated to a compliance voltage other than ground for operation, then the appropriate voltage level may be applied to the noninverting input of the OPA820.

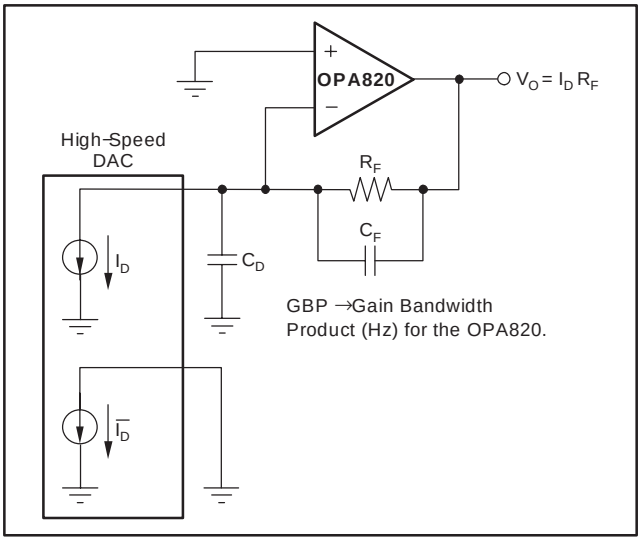


Figure 8. Wideband, Low-Distortion DAC Transimpedance Amplifier

The DC gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance (C_D) will produce a zero in the noise gain for the OPA820 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise-gain peaking. To achieve a flat transimpedance frequency response, this pole in the feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (1)$$

which will give a corner frequency f_{-3dB} of approximately:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \quad (2)$$

ACTIVE FILTERS

Most active filter topologies will have exceptional performance using the broad bandwidth and unity-gain stability of the OPA820. Topologies employing capacitive feedback require a unity-gain stable, voltage-feedback op amp. Sallen-Key filters simply use the op amp as a noninverting gain stage inside an RC network. Either current- or voltage-feedback op amps may be used in Sallen-Key implementations.

Figure 9 shows an example Sallen-Key low-pass filter, in which the OPA820 is set up to deliver a low-frequency gain of +2. The filter component values have been selected to achieve a maximally-flat Butterworth response with a 5MHz, −3dB bandwidth. The resistor values have been slightly adjusted to compensate for the effects of the 240MHz bandwidth provided by the OPA820 in this configuration. This filter may be combined with the ADC driver suggestions to provide moderate (2-pole) Nyquist filtering, limiting noise, and out-of-band harmonics into the input of an ADC. This filter will deliver the exceptionally low harmonic distortion required by high SFDR ADCs such as the ADS850 (14-bit, 10MSPS, 82dB SFDR).

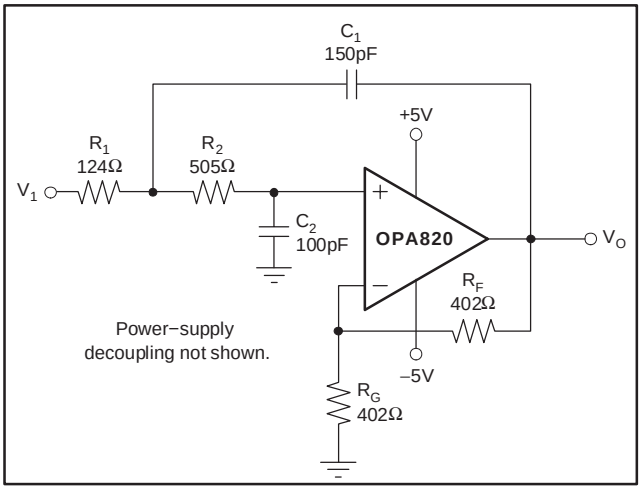


Figure 9. 5MHz Butterworth Low-Pass Active Filter

Another type of filter, a high-Q bandpass filter, is shown in Figure 10. The transfer function for this filter is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{s\frac{R_3 + R_4}{R_1 R_4 C_1}}{s^2 + s\frac{1}{R_1 C_1} + \frac{R_3}{R_2 R_4 R_5 C_1 C_2}} \quad (3)$$

$$\text{with} \quad \omega_O{}^2 = \frac{R_3}{R_2 R_4 R_5 C_1 C_2} \quad (4)$$

$$\text{and} \quad \frac{\omega_O}{Q} = \frac{1}{R_1 C_1} \quad (5)$$

For the values chosen in Figure 10:

$$f_O = \frac{w_O}{2\pi} \simeq 1\text{MHz} \quad (6)$$

and Q = 100

See Figure 11 for the frequency response of the filter shown in Figure 10.

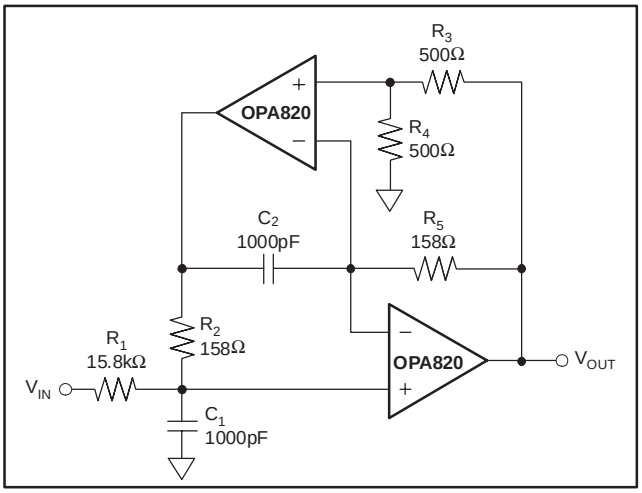


Figure 10. High-Q 1MHz Bandpass Filter

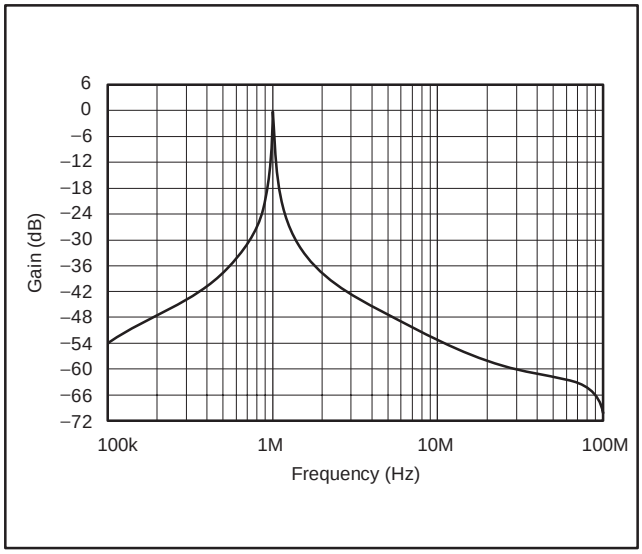


Figure 11. High-Q 1MHz Bandpass Filter Frequency Response

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA820 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with user's guide. The summary information for these fixtures is shown in the table below.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA820ID	SO-8	DEM-OPA-SO-1A	SBOU009
OPA820IDBV	SOT23-5	DEM-OPA-SOT-1A	SBOU010

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA820 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA820 and its circuit designs. This is particularly true for video and R_F amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA820 is available through the TI web page (www.ti.com). The applications department is also available for design assistance. These models predict typical small-signal AC, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

Since the OPA820 is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values may be used for the feedback and gain-setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. Usually, the feedback resistor value should be between 200Ω and 1kΩ. Below 200Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance of the OPA820. Above 1kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band limiting in the amplifier response. A direct short is suggested as a feedback for A_V = +1V/V.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 1) to be less than about 200Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \parallel R_G <$ 200Ω will keep this pole above 400MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, an additional design consideration must be noted. R_G becomes the input resistor and therefore the load impedance to the driving source. If impedance matching is desired, R_G may be set equal to the required termination value. However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2 with a 50Ω input matching resistor (= R_G) would require a 100Ω feedback resistor, which would contribute to output loading in parallel with the external load. In such a case, it would be preferable to increase both the R_F and R_G values, and then achieve the input matching impedance with a third resistor to ground (see Figure 2). The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

BANDWIDTH vs GAIN

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the GBP shown in the specifications. Ideally, dividing GBP by the noninverting signal gain (also called the noise gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low signal gains, most amplifiers will exhibit a more complex response with lower phase margin. The OPA820 is optimized to give a maximally-flat, 2nd-order Butterworth response in a gain of 2. In this configuration, the OPA820 has approximately 64° of phase margin and will show a typical −3dB bandwidth of 240MHz. When the phase margin is 64°, the closed-loop bandwidth is approximately $\sqrt{2}$ greater than the value predicted by dividing GBP by the noise gain.

Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 30MHz bandwidth shown in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 280MHz.

OUTPUT DRIVE CAPABILITY

The OPA820 has been optimized to drive the demanding load of a doubly-terminated transmission line. When a 50Ω line is driven, a series 50Ω into the cable and a terminating 50Ω load at the end of the cable are used. Under these conditions, the cable impedance will appear resistive over a wide frequency range, and the total effective load on the OPA820 is 100Ω in parallel with the resistance of the feedback network. The electrical characteristics show a ±3.6V swing into this load—which will then be reduced to a ±1.8V swing at the termination resistor. The ±75mA output drive over temperature provides adequate current drive margin for this load. Higher voltage swings (and lower distortion) are achievable when driving higher impedance loads.

A single video load typically appears as a 150Ω load (using standard 75Ω cables) to the driving amplifier. The OPA820 provides adequate voltage and current drive to support up to three parallel video loads (50Ω total load) for an NTSC signal. With only one load, the OPA820 achieves an exceptionally low 0.01%/0.03° dG/dP error.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. A high-speed, high open-loop gain amplifier like the OPA820 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. In simple terms, the capacitive load reacts with the open-loop output resistance of the amplifier to introduce an additional pole into the loop and thereby decrease the phase margin. This issue has become a popular topic of application notes and articles, and several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S *vs Capacitive Load* and the resulting frequency response at the load. The criterion for setting the recommended resistor is maximum bandwidth, flat frequency response at the load. Since there is now a passive low-pass filter between the output pin and the load capacitance, the response at the output pin itself is typically somewhat peaked, and becomes flat after the roll-off action of the RC network. This is not a concern in most applications, but can cause clipping if the desired signal swing at the load is very close to the amplifier's swing limit. Such clipping would be most likely to occur in pulse response applications where the frequency peaking is manifested as an overshoot in the step response.

Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA820. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA820 output pin (see the *Board Layout* section).

DISTORTION PERFORMANCE

The OPA820 is capable of delivering an exceptionally low distortion signal at high frequencies and low gains. The distortion plots in the Typical Characteristics show the typical distortion under a wide variety of conditions. Most of these plots are limited to 100dB dynamic range. The OPA820 distortion does not rise above −90dBc until either the signal level exceeds 0.9V and/or the fundamental frequency exceeds 500kHz. **Distortion in the audio band is ≤ −100dBc.**

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration this is the sum of $R_F + R_G$, whereas in the inverting configuration this is just R_F (see Figure 1). Increasing the output voltage swing increases harmonic distortion directly. Increasing the signal gain will also increase the 2nd-harmonic distortion. Again, a 6dB increase in gain will increase the 2nd- and 3rd-harmonic by 6dB even with a constant output power and frequency. Finally, the distortion increases as the fundamental frequency increases because of the roll-off in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open-loop pole at approximately 100kHz. Starting from the −85dBc 2nd-harmonic for $2V_{PP}$ into 200Ω, G = +2 distortion at 1MHz (from the Typical Characteristics), the 2nd-harmonic distortion will not show any improvement below 100kHz and will then be:

$$-100dB - 20\log(1MHz/100kHz) = -105dBc$$

NOISE PERFORMANCE

The OPA820 complements its low harmonic distortion with low input noise terms. Both the input-referred voltage noise and the two input-referred current noise terms combine to give a low output noise under a wide variety of operating conditions. Figure 12 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

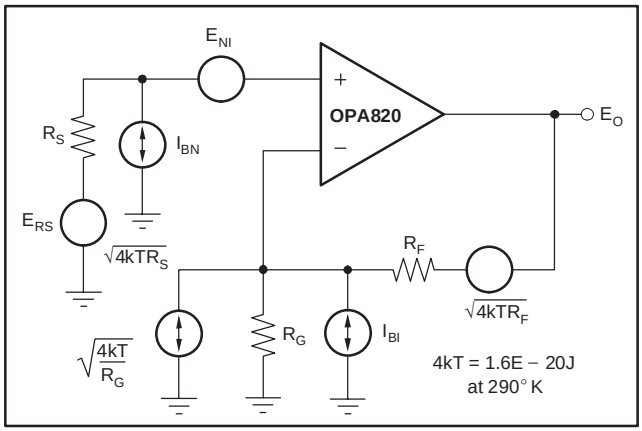


Figure 12. Op Amp Noise Analysis Model

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to get back to a spot noise voltage. Equation 7 shows the general form for this output noise voltage using the terms presented in Figure 12.

$$E_O = \sqrt{\left[E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right]NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (7)$$

Dividing this expression by the noise gain ($NG = 1 + R_F/R_G$) will give the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 8.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (8)$$

Evaluating these two equations for the OPA820 circuit presented in Figure 1 will give a total output spot noise voltage of 6.44nV/√Hz and an equivalent input spot noise voltage of 3.22nV/√Hz.

DC OFFSET CONTROL

The OPA820 can provide excellent DC signal accuracy because of its high open-loop gain, high common-mode rejection, high power-supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of this low input offset voltage, careful attention to input bias current cancellation is also required. The high-speed input stage for the OPA820 has a moderately high input bias current (9μA typ into the pins) but with a very close match between the two input currents—typically 100nA input offset current. The total output offset voltage may be considerably reduced by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 1 would be to insert a 175Ω series resistor into the noninverting input from the 50Ω terminating resistor. When the 50Ω source resistor is DC-coupled, this will increase the source impedance for the noninverting input bias current to 200Ω. Since this is now equal to the impedance looking out of the inverting input ($R_F \parallel R_G$), the circuit will cancel the gains for the bias currents to the output leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using a 402Ω feedback resistor, this output error will now be less than ±0.4μA × 402Ω = ±160μV at 25°C.

THERMAL ANALYSIS

The OPA820 will not require heatsinking or airflow in most applications. Maximum desired junction temperature would set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA820IDBV (SOT23-5 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C.

$$P_D = 10V(6.4mA) + 5^2/(4 \times (100\Omega \parallel 800\Omega)) = 134mW$$

$$\text{Maximum } T_J = +85°C + (134mW \times 150°C/W) = 105°C$$

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier such as the OPA820 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA820. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or a zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load-driving considerations. It has been suggested here that a good starting point for design would be to set $R_G \parallel R_F = 200\Omega$. Using this setting will automatically keep the resistor noise terms low, and minimize the effect of their parasitic capacitance.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA820 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA820 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA820 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA820 onto the board.

INPUT AND ESD PROTECTION

The OPA820 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 13.

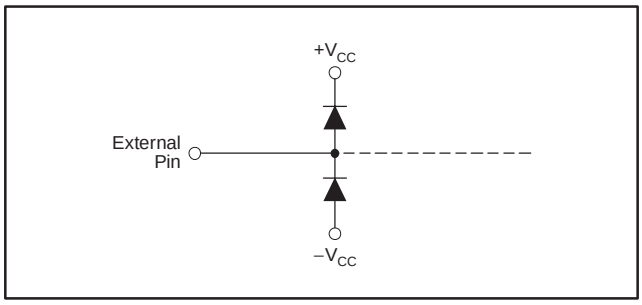


Figure 13. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA820), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Figure 14 shows an example protection circuit for I/O voltages that may exceed the supplies.

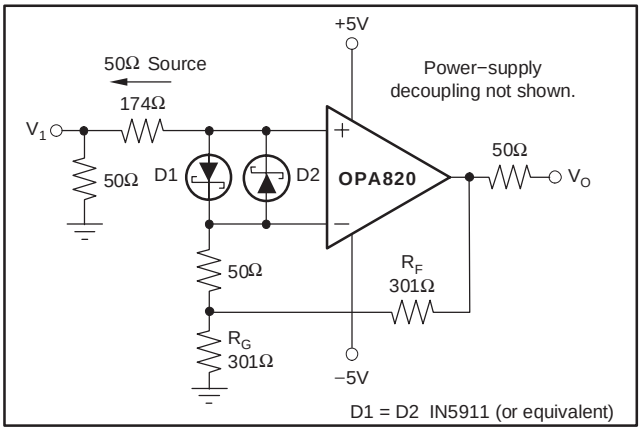


Figure 14. Gain of +2 with Input Protection

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
8/08	C	2	Absolute Maximum Ratings	Changed Storage Temperature minimum value from −40°C to −65°C.
3/06	B	18	Design-In Tools	Board part number changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA820ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 820	Samples
OPA820IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSO	Samples
OPA820IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSO	Samples
OPA820IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSO	Samples
OPA820IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSO	Samples
OPA820IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 820	Samples
OPA820IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 820	Samples
OPA820IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 820	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

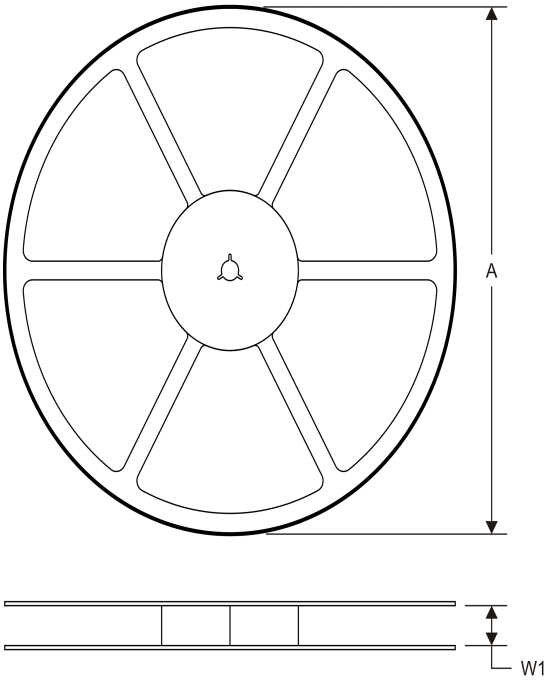
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA820 :

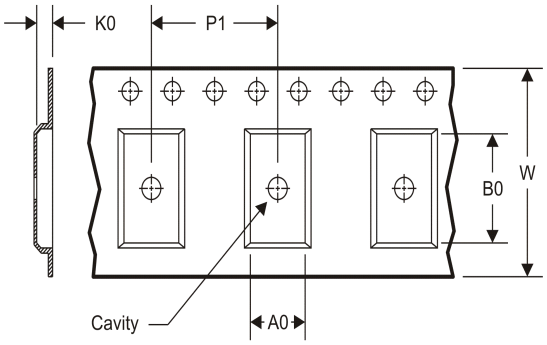
NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



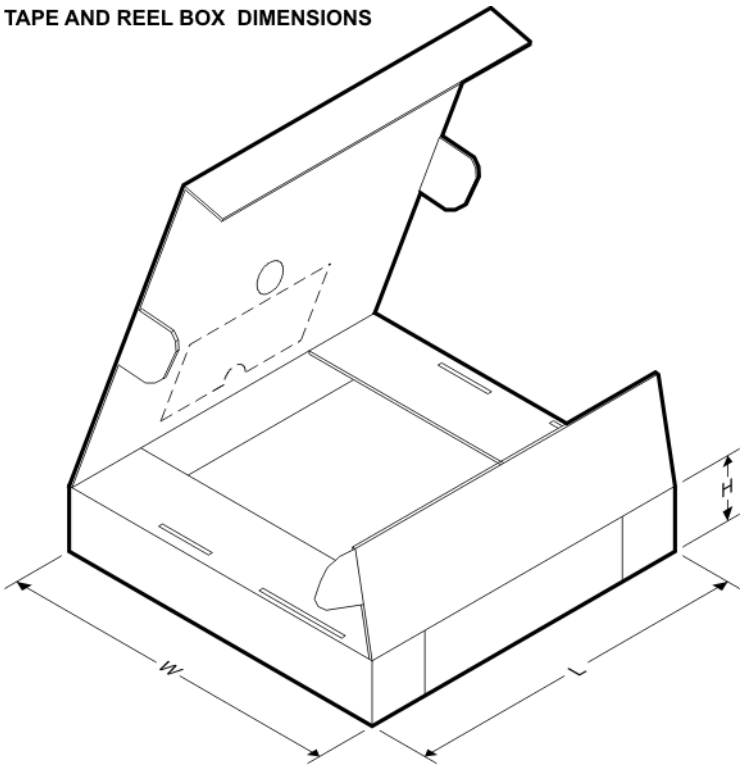
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA820IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA820IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA820IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

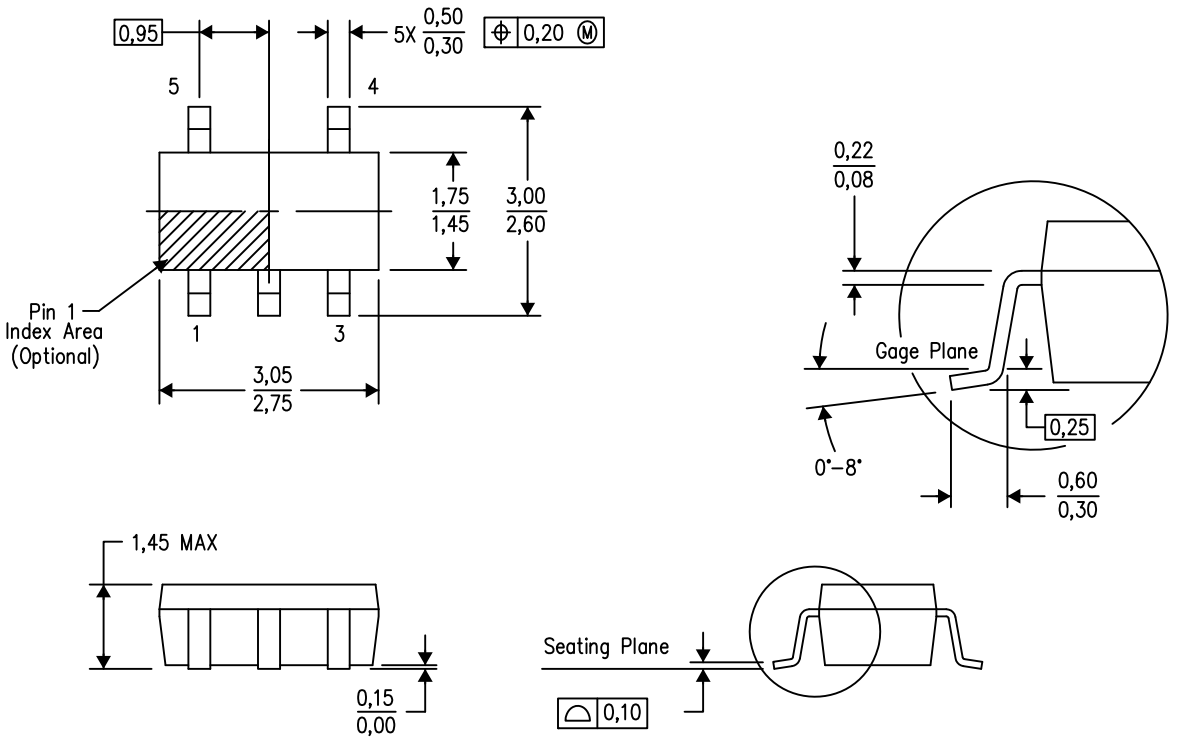
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA820IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA820IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA820IDR	SOIC	D	8	2500	367.0	367.0	35.0

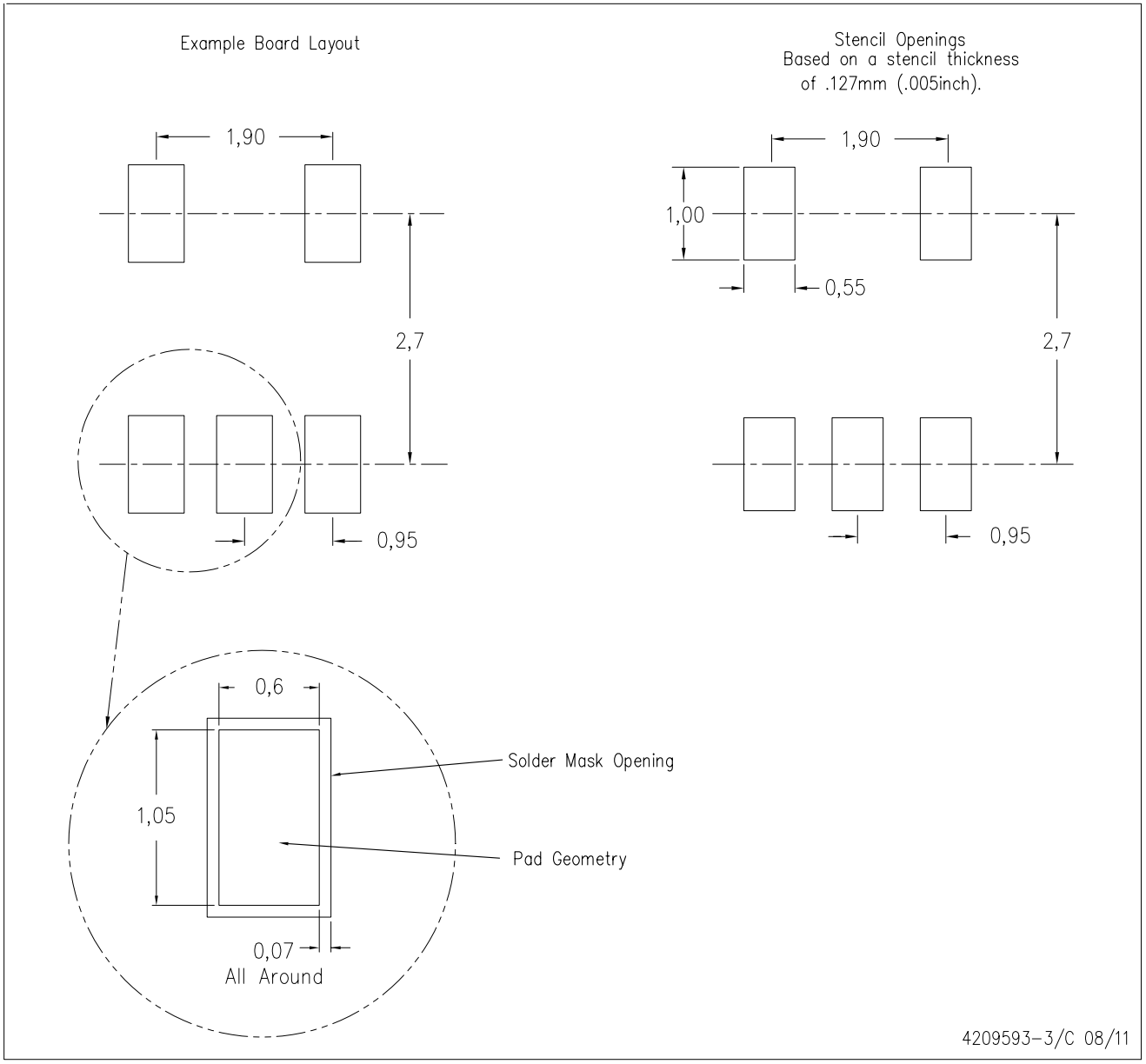
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

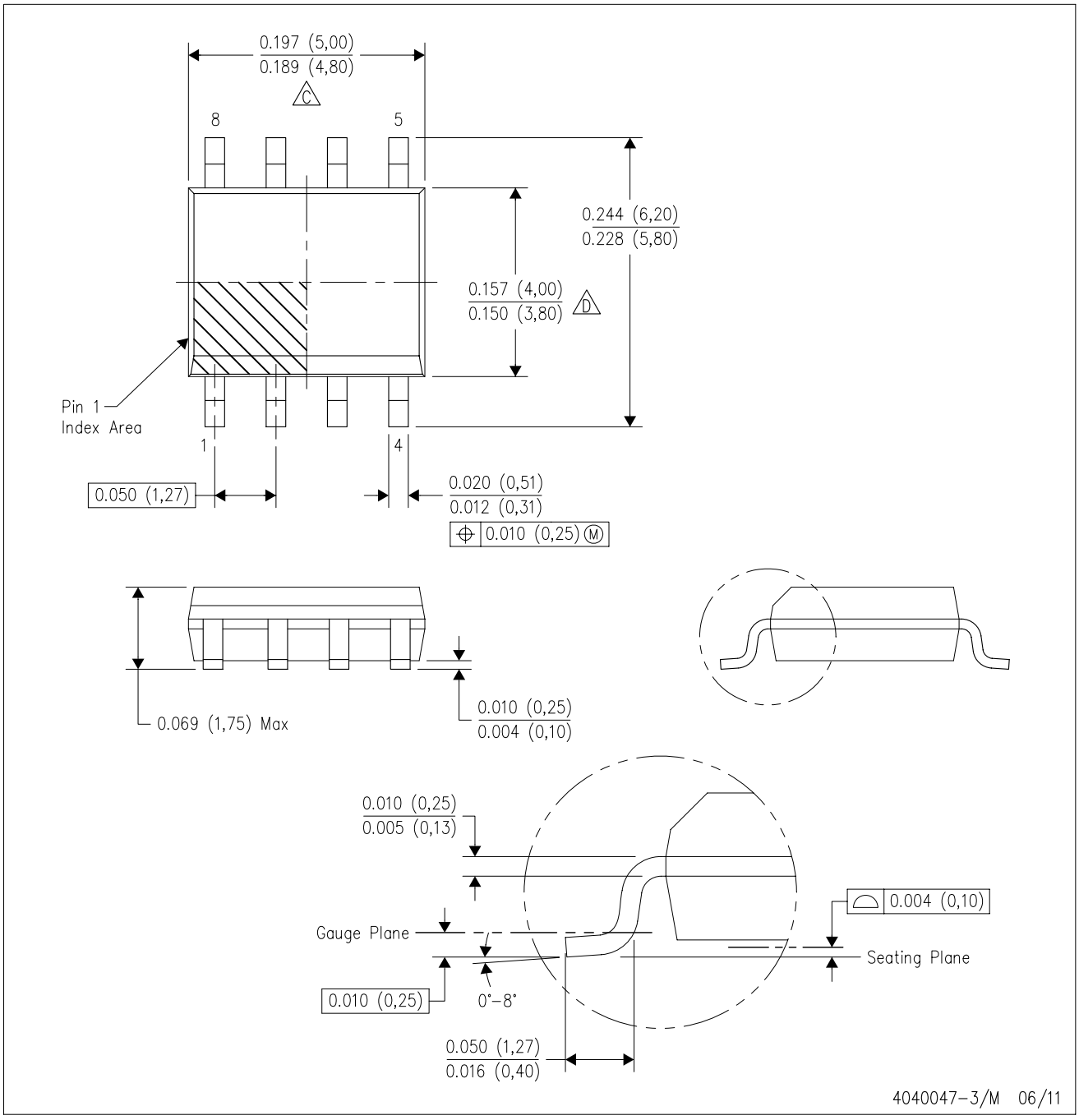
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



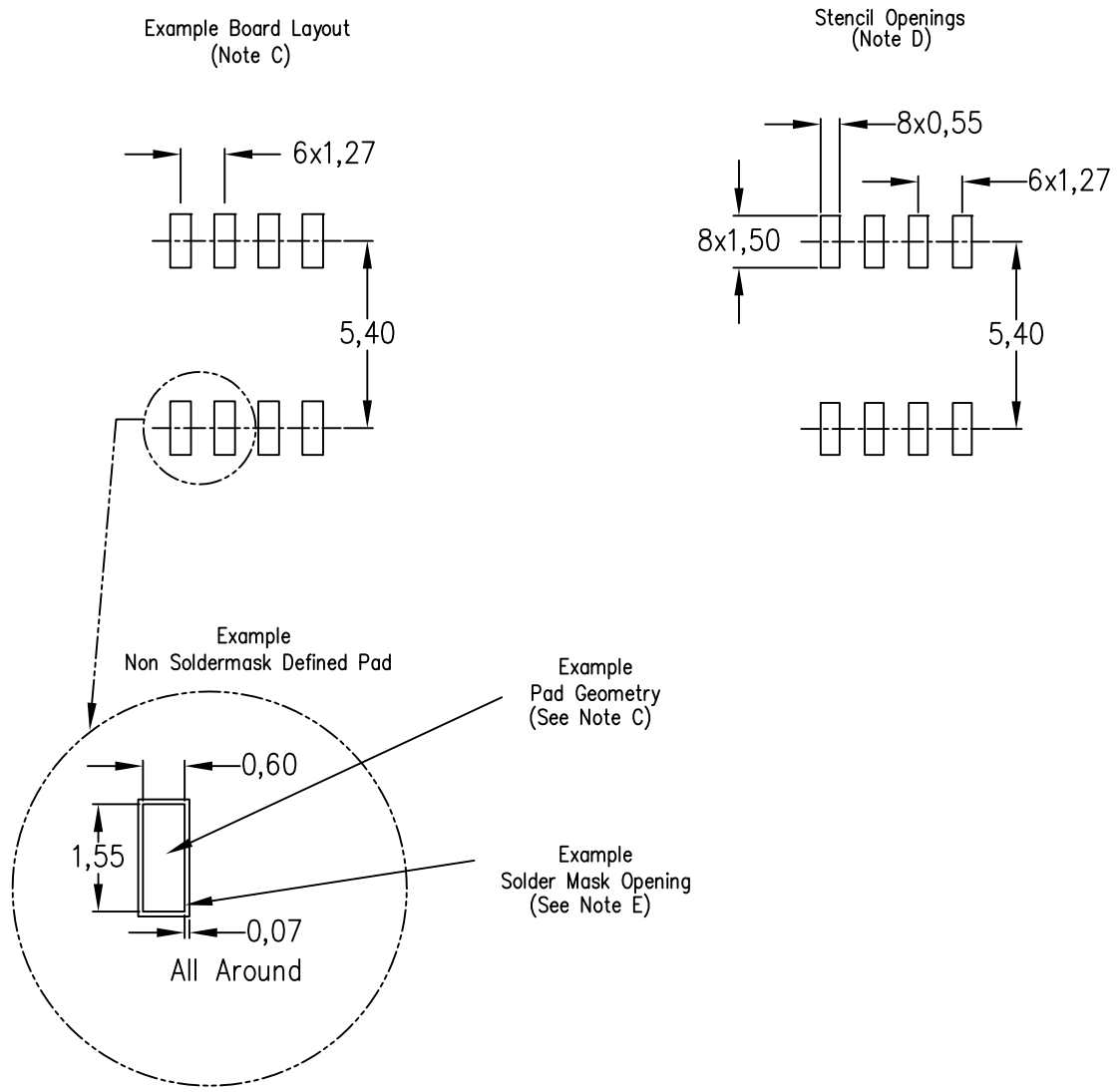
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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