4-CHANNEL HALF-DUPLEX M-LVDS LINE TRANSCEIVERS

Check for Samples: SN65MLVD040

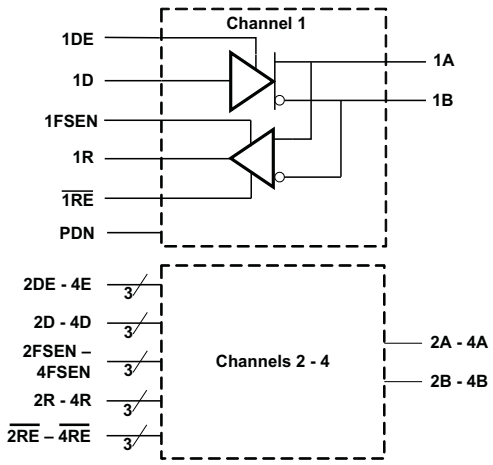
FEATURES

- **Low-Voltage Differential 30-Ω to 55-Ω Line Drivers and Receivers for Signaling Rates(1) Up to 250 Mbps; Clock Frequencies Up to 125 MHz**
- **Meets or Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange**
- **Controlled Driver Output Voltage Transition Times for Improved Signal Quality**
- **–1 V to 3.4 V Common-Mode Voltage Range Allows Data Transfer With 2 V of Ground Noise**
- **Bus Pins High Impedance When Driver Disabled or V_{CC} ≤ 1.5 V**
- **Independent Enables for each Driver and Receiver**
- **Enhanced ESD Protection: 7 kV HBM on all Pins**
- **48 pin 7 X 7 QFN (RGZ)**
- **M-LVDS Bus Power Up/Down Glitch Free**

APPLICATIONS

- **Parallel Multipoint Data and Clock Transmission Via Backplanes and Cables**
- **Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485**
- **Cellular Base Stations**
- **Central-Office Switches**
- **Network Switches and Routers(1)**

LOGIC DIAGRAM (POSITIVE LOGIC)
SN65MLVD040



(1) The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

DESCRIPTION

The SN65MLVD040 provides four half-duplex transceivers for transmitting and receiving Multipoint-Low-Voltage Differential Signals in full compliance with the TIA/EIA-899 (M-LVDS) standard, which are optimized to operate at signaling rates up to 250 Mbps. The driver outputs have been designed to support multipoint buses presenting loads as low as 30-Ω and incorporates controlled transition times to allow for stubs off of the backplane transmission line.

The M-LVDS standard defines two types of receivers, designated as Type-1 and Type-2. Type-1 receivers have thresholds centered about zero with 25 mV of hysteresis to prevent output oscillations with loss of input; Type-2 receivers implement a failsafe by using an offset threshold. The xFSEN pins is used to select the Type-1 and Type-2 receiver for each of the channels. In addition, the driver rise and fall times are between 1 ns and 2 ns, complying with the M-LVDS standard to provide operation at 250 Mbps while also accommodating stubs on the bus. Receiver outputs are slew rate controlled to reduce EMI and crosstalk effects associated with large current surges. The M-LVDS standard allows for 32 nodes on the bus providing a high-speed replacement for RS-485 where lower common-mode can be tolerated or when higher signaling rates are needed.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

The driver logic inputs and the receiver logic outputs are on separate pins rather than tied together as in some transceiver designs. The drivers have separate enables (DE) and so does the receivers ($\overline{RE}$). This arrangement of separate logic inputs, logic outputs, and enable pins allows for a listen-while-talking operation. The devices are characterized for operation from –40°C to 85°C.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1D–4D	35, 32, 28, 25	I	Data inputs for drivers
1R–4R	36, 33, 29, 26	O	Data output for receivers
1A–4A	47, 3, 9, 13	Bus I/O	M-LVDS bus non-inverting input/output
1B–4B	48, 4, 10, 14	Bus I/O	M-LVDS bus inverting input/output
GND	6, 7, 18, 23, 27, 31, 34, 38, 43		Circuit ground. **ALL GND pins must be connected to ground.**
V_{CC}	2, 11, 15, 16, 24, 37, 45, 46		Supply voltage. **ALL VCC pins must be connected to supply.**
$\overline{1RE}$–$\overline{4RE}$	40, 42, 19, 21	I	Receiver enable, active low, enable individual receivers. When this pin is left floating, internally this pin will be pulled to logic HIGH.
1DE–4DE	1, 5, 8, 12	I	Driver enable, active high, individual enables the drivers. When this pin is left floating, internally this pin will be pulled to logic LOW.
1FSEN–4FSEN	39, 41, 20, 22	I	Failsafe enable pin. When this pin is left floating, internally this pin will be pulled to logic HIGH. This pin enables the Type 2 receiver for the respective channel. xFSEN = L → Type 1 receiver inputs xFSEN = H → Type 2 receiver inputs
PDN	30	I	Power Down pin. When this pin is left floating, internally this pin will be pulled to logic LOW. When PDN is HIGH, the device is powered up. When PDN is LOW, the device overrides all other control and powers down. All outputs are Hi-Z.
NC	17		Not Connected
NC	44		Not Connected. Internal TI Test pin. This pin must be left unconnected.
PowerPAD™	–		Connected to GND

PIN ASSIGNMENTS

RGZ PACKAGE
(TOP VIEW)

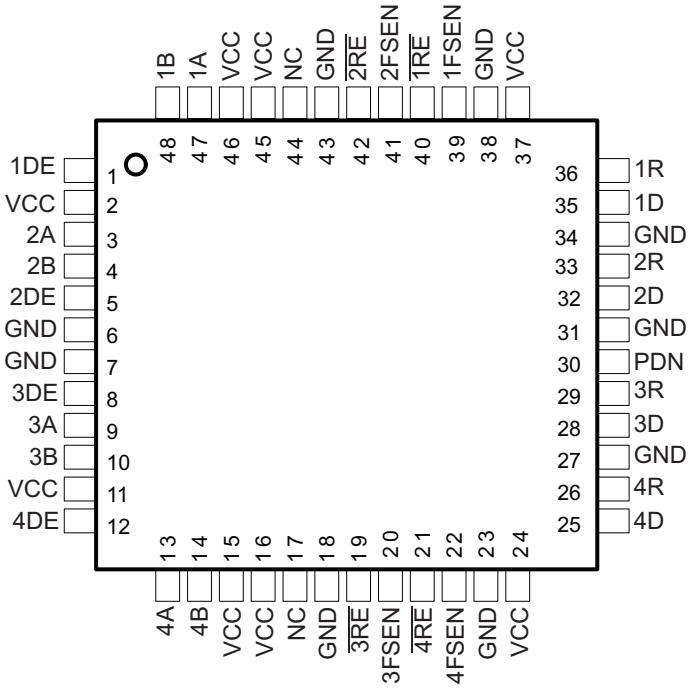


Table 1. Device Function Tables

RECEIVER							DRIVER			
INPUTS(1)				RECEIVER TYPE	OUTPUT(1)		INPUTS(1)		OUTPUTS(1)	
$V_{ID} = V_A - V_B$	PDN	FSEN	$\overline{RE}$		R		D	DE	A	B
V_{ID} > 35 mV	H	L	L	Type 1	H		L	H	L	H
–35 mV ≤ V_{ID} ≤ 35 mV	H	L	L	Type 1	?		H	H	H	L
V_{ID} < 35 mV	H	L	L	Type 1	L		OPEN	H	L	H
							X	OPEN	Z	Z
V_{ID} > 135 mV	H	H	L	Type 2	H		X	L	Z	Z
65 mV ≤ V_{ID} ≤ 135 mV	H	H	L	Type 2	?					
V_{ID} < 65 mV	H	H	L	Type 2	L					
Open Circuit	H	L	L	Type 1	?					
Open Circuit	H	H	L	Type 2	L					
X	H	X	H	X	Z					
X	H	X	OPEN	X	Z					
X	L	X	X	X	Z					

(1) H=high level, L=low level, Z=high impedance, X=Don't care, ?=indeterminate

ORDERING INFORMATION

PART NUMBER	RECEIVER TYPE	PACKAGE MARKING	PACKAGE/CARRIER
SN65MLVD040RGZR	Type 1, 2	MLVD040	48-Pin QFN/ Tape and Reeled
SN65MLVD040RGZT	Type 1, 2	MLVD040	48-Pin QFN/Small Tape and Reeled

PACKAGE DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
RGZ	Low-K(2)	1298 mW	12.98 mW/°C	519 mW
RGZ	High-K(3)	3448 mW	34.48 mW/°C	1379 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance			9		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			20		°C/W
$R_{\theta JP}$	Junction-to-pad thermal resistance			1.37		°C/W
P_D	Device power dissipation (See typical curves for additional information)	$\overline{RE}$ at 0 V, DE at 0 V, C_L = 15 pF, V_{ID} = 400 mW, 125 MHz, All others open			382	mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			SN65MLVD040
Supply voltage range(2), V_{CC}			–0.5 V to 4 V
Input voltage range	D, DE, $\overline{RE}$, FSEN		–0.5 V to 4 V
	A, B		–1.8 V to 4 V
Output voltage range	R		–0.3 V to 4 V
	A, or B		–1.8 V to 4 V
Electrostatic discharge	Human Body Model(3)	All pins	±7 kV
	Charged-Device Model(4)	All pins	±1500 V
Storage temperature range			–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-E. Bus pin stressed with respect to a common connection of GND and V_{CC}
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-D.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	GND		0.8	V
	Voltage at any bus terminal V_A or V_B	–1.4		3.8	V
$\lvert V_{ID} \rvert$	Magnitude of differential input voltage	0.05		V_{CC}	V
T_A	Operating free-air temperature	–40		85	°C
	Maximum junction temperature			140	°C

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	Driver only	$\overline{RE}$ and DE at V_{CC}, R_L = 50 Ω, 125MHz, All others open			76	mA
		Both disabled	$\overline{RE}$ at V_{CC}, DE at 0 V, R_L = No Load, 125MHz, All others open			10	
		Both enabled	$\overline{RE}$at 0 V, DE at V_{CC}, R_L = 50 Ω, C_L = 15 pF, All others open, 125MHz, No external RX stimulus			165	
		Receiver only	$\overline{RE}$at 0 V, DE at 0 V, C_L = 15 pF, V_{ID} = 400 mV, 125 MHz, All others open			100	
	Power down	PDN = L				5	mA

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
$\|V_{AB}\|$	Differential output voltage magnitude (A, B)	See Figure 2	480		650	mV
$\Delta\|V_{AB}\|$	Change in differential output voltage magnitude between logic states (A, B)		–50		50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage (A, B)	See Figure 3	0.7		1.1	V
$\Delta V_{OS(SS)}$	Change in steady-state common-mode output voltage between logic states (A, B)		–50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage (A, B)				150	mV
$V_{A(OC)}$	Maximum steady-state open-circuit output voltage (A, B)	See Figure 7	0		2.4	V
$V_{B(OC)}$	Maximum steady-state open-circuit output voltage (A, B)		0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output (A, B)	See Figure 5			1.2 V_{SS}	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output (A, B)		–0.2 V_{SS}			V
I_{IH}	High-level input current (D, DE)	V_{IH} = 2 V to V_{CC}			10	µA
I_{IL}	Low-level input current (D, DE)	V_{IL} = GND to 0.8 V			10	µA
$\|I_{OS}\|$	Differential short-circuit output current magnitude (A, B)	See Figure 4			24	mA
C_I	Input capacitance (D, DE)	V_I = 0.4 sin(30E6πt) + 0.5 V (3)		5		pF

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) All typical values are at 25°C and with a 3.3-V supply voltage.
(3) HP4194A impedance analyzer (or equivalent)

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold (A, B)	Type 1	See Table 2 and Table 3			35	mV
		Type 2				135	
V_{IT-}	Negative-going differential input voltage threshold (A, B)	Type 1		–35			mV
		Type 2		65			
V_{HYS}	Differential input voltage hysteresis, ($V_{IT+} – V_{IT-}$) (A, B)	Type 1			25		mV
		Type 2			0		
V_{OH}	High-level output voltage (R)		I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage (R)		I_{OL} = 8 mA			0.4	V
I_{IH}	High-level input current ($\overline{RE}$)		V_{IH} = 2 V to V_{CC}	–10			µA
I_{IL}	Low-level input current ($\overline{RE}$)		V_{IL} = GND to 0.8 V	–10			µA
I_{OZ}	High-impedance output current (R)		V_O = 0 V or V_{CC}	–10		15	µA

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

BUS INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
I_A	Receiver or transceiver with driver disabled input current	V_A = 3.8 V,	V_B = 1.2 V				32	µA
		V_A = –1.4 V,	V_B = 1.2 V		–32			
I_B	Receiver or transceiver with driver disabled input current	V_B = 3.8 V,	V_A = 1.2 V				32	µA
		V_B = –1.4 V,	V_A = 1.2 V		–32			
I_{AB}	Receiver or transceiver with driver disabled differential input current ($I_A – I_B$)	$V_A = V_B$,	1.4 ≤ V_A ≤ 3.8 V		–4		4	µA
$I_{A(OFF)}$	Receiver or transceiver power-off input current	V_A = 3.8 V,	V_B = 1.2 V,	0 V ≤ V_{CC}≤ 1.5 V			32	µA
		V_A = –1.4 V,	V_B= 1.2 V,	0 V ≤ V_{CC}≤ 1.5 V	–32			
$I_{B(OFF)}$	Receiver or transceiver power-off input current	V_B = 3.8 V,	V_A = 1.2 V,	0 V ≤ V_{CC}≤ 1.5 V			32	µA
		V_B = –1.4 V,	V_A = 1.2 V,	0 V ≤ V_{CC}≤ 1.5 V	–32			
$I_{AB(OFF)}$	Receiver input or transceiver power-off differential input current ($I_{A(off)} – I_{B(off)}$)	$V_A = V_B$, 0 V ≤ V_{CC} ≤ 1.5 V, –1.4 ≤ V_A ≤ 3.8 V			–4		4	µA
C_A	Transceiver with driver disabled input capacitance	V_A = 0.4 sin (30E6πt) + 0.5 V(2),	V_B = 1.2 V			5		pF
C_B	Transceiver with driver disabled input capacitance	V_B = 0.4 sin (30E6πt) + 0.5 V(2),	V_A = 1.2 V			5		pF
C_{AB}	Transceiver with driver disabled differential input capacitance	V_{AB} = 0.4 sin (30E6πt)V(2)					3	pF
$C_{A/B}$	Transceiver with driver disabled input capacitance balance, (C_A/C_B)				0.99		1.01	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) HP4194A impedance analyzer (or equivalent)

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	See Figure 5	1.3	1.9	2.4	ns
t_{pHL}	Propagation delay time, high-to-low-level output		1.3	1.9	2.4	ns
t_r	Differential output signal rise time		0.9		2	ns
t_f	Differential output signal fall time		0.9		2.2	ns
$t_{sk(o)}$	Output skew				200	ps
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				150	ps
$t_{sk(pp)}$	Part-to-part skew (2)				300	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(3)	All channels switching, 125 MHz clock input(4), see Figure 8			2	ps
$t_{jit(c-c)}$	Cycle-to-cycle jitter, rms(3)				9	ps
$t_{jit(det)}$	Deterministic jitter(3)	All channels switching, 250 Mbps 2^{15}–1 PRBS input(4), see Figure 8			290	ps
$t_{jit(r)}$	Random jitter (3)				4	ps
t_{PZH}	Enable time, high-impedance-to-high-level output	See Figure 6			7	ns
t_{PZL}	Enable time, high-impedance-to-low-level output				7	ns
t_{PHZ}	Disable time, high-level-to-high-impedance output				7	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output				7	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
(4) $t_r = t_f = 0.5$ ns (10% to 90%)

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output		C_L = 15 pF, See Figure 10	2.5	4.5	6	ns
t_{pHL}	Propagation delay time, high-to-low-level output			2.5	4.5	6	ns
t_r	Output signal rise time			1.4		2.35	ns
t_f	Output signal fall time			1.4		2.35	ns
$t_{sk(o)}$	Output skew					350	ps
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	Type 1			35	210	ps
		Type 2			150	470	
$t_{sk(pp)}$	Part-to-part skew(2)					800	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) (3)		All channels switching, 125 MHz clock input(4), See Figure 12			6	ps
$t_{jit(c-c)}$	Cycle-to-cycle jitter, rms(3)					13	ps
$t_{jit(det)}$	Deterministic jitter(3)	Type 1	All channels switching, 250 Mbps 2^{15}–1 PRBS input(4),See Figure 12			800	ps
		Type 2				945	ps
$t_{jit(r)}$	Random jitter (3)	Type 1				9	ps
		Type 2				8	ps
t_{PZH}	Enable time, high-impedance-to-high-level output		C_L = 15 pF, See Figure 11			15	ns
t_{PZL}	Enable time, high-impedance-to-low-level output					15	ns
t_{PHZ}	Disable time, high-level-to-high-impedance output					10	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output					10	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
(4) $t_r = t_f$ = 0.5 ns (10% to 90%)

PARAMETER MEASUREMENT INFORMATION

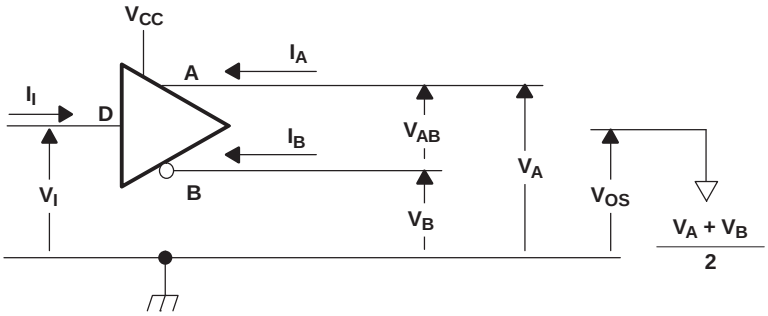
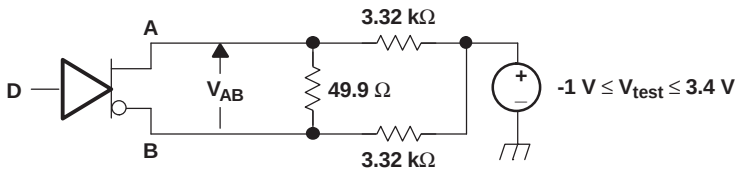
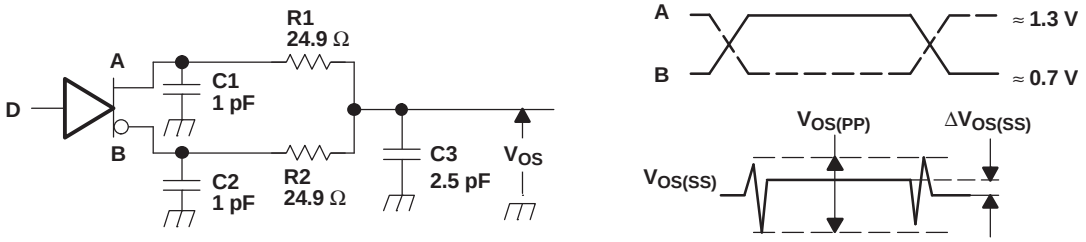


Figure 1. Driver Voltage and Current Definitions



NOTE: All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse frequency = 1 MHz, duty cycle = 50 ±5%.

B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.

C. R1 and R2 are metal film, surface mount, ±1%, and located within 2 cm of the D.U.T.

D. The measurement of $V_{OS(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

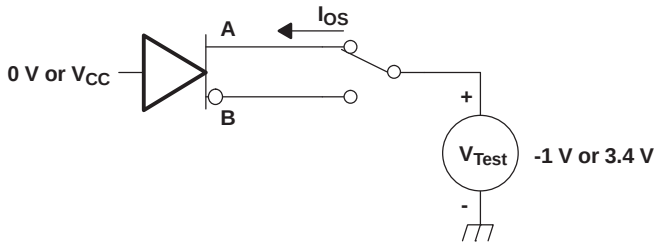
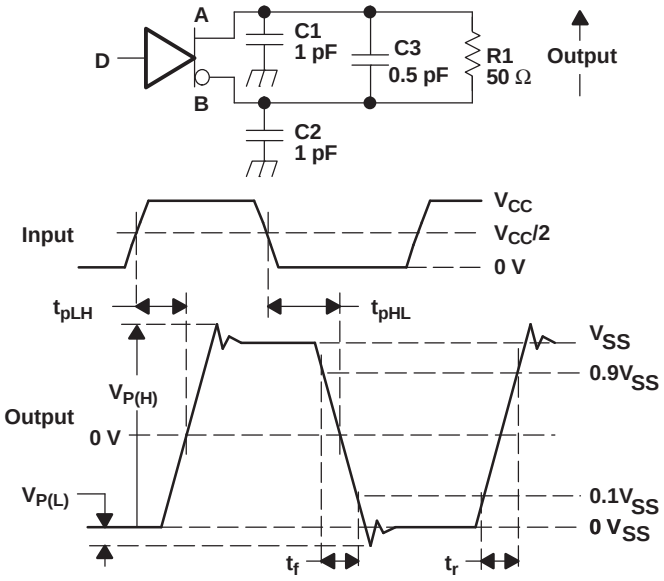


Figure 4. Driver Short-Circuit Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



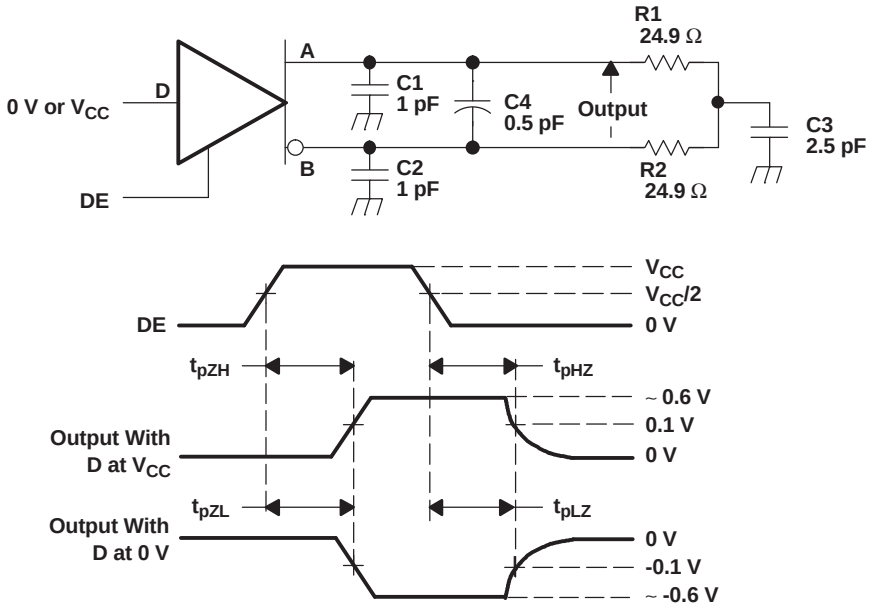
A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ±5%.

B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.

C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.

D. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ±5%.

B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.

C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.

D. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 6. Driver Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

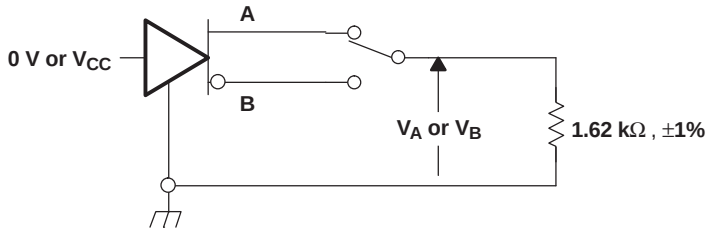
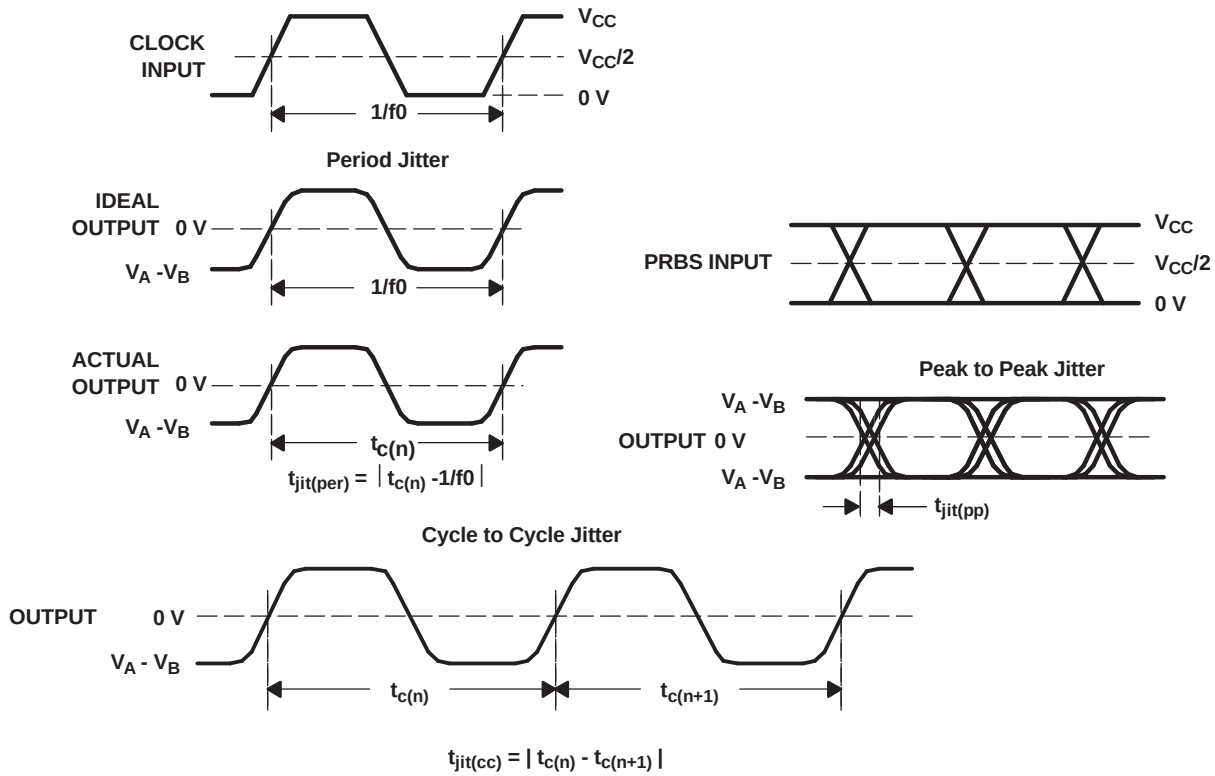


Figure 7. Maximum Steady State Output Voltage



$t_{jit(cc)} = | t_{c(n)} - t_{c(n+1)} |$

A. All input pulses are supplied by the Agilent 81250 Parallel BERT Stimulus System with plug-in E4832A.

B. The cycle-to-cycle measurement is made on a TEK TDS6604 running TDSJIT3 application software.

C. All other jitter measurements are made with an Agilent Infiniium DCA-J 86100C Digital Communications Analyzer.

D. Period jitter and cycle-to-cycle jitter are measured using a 125 MHz 50 ±1% duty cycle clock input. Measured over 75K samples.

E. Deterministic jitter and random jitter are measured using a 250 Mbps 2^{15}–1 PRBS input. Measured over BER = 10^{-12}

Figure 8. Driver Jitter Measurement Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

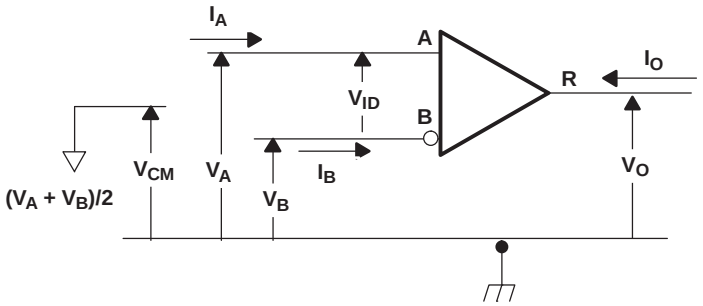


Figure 9. Receiver Voltage and Current Definitions

Table 2. Type-1 Receiver Input Threshold Test Voltages

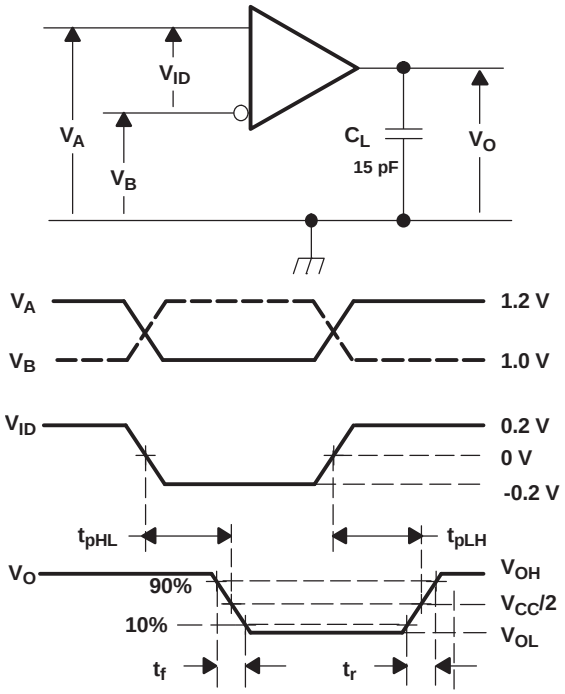
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.400	3.365	0.035	3.3825	H
3.365	3.400	–0.035	3.3825	L
–0.965	–1	0.035	–0.9825	H
–1	–0.965	–0.035	–0.9825	L

(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE}$ = L)

Table 3. Type-2 Receiver Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.400	3.265	0.135	3.3325	H
3.4000	3.335	0.065	3.3675	L
–0.865	–1	0.135	–0.9325	H
–0.935	–1	0.065	–0.9675	L

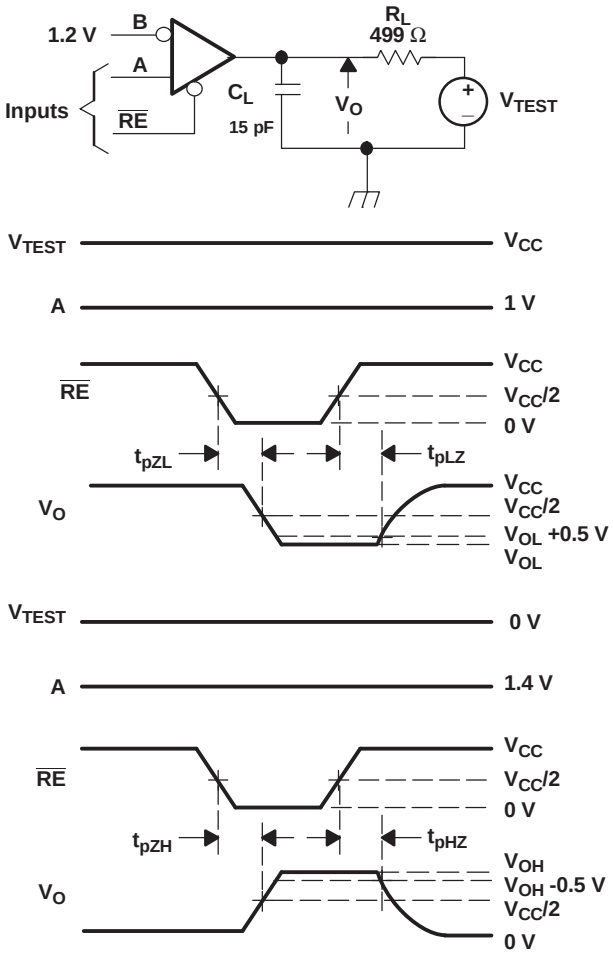
(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE}$ = L)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ±5%. C_L is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.

B. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 10. Receiver Timing Test Circuit and Waveforms

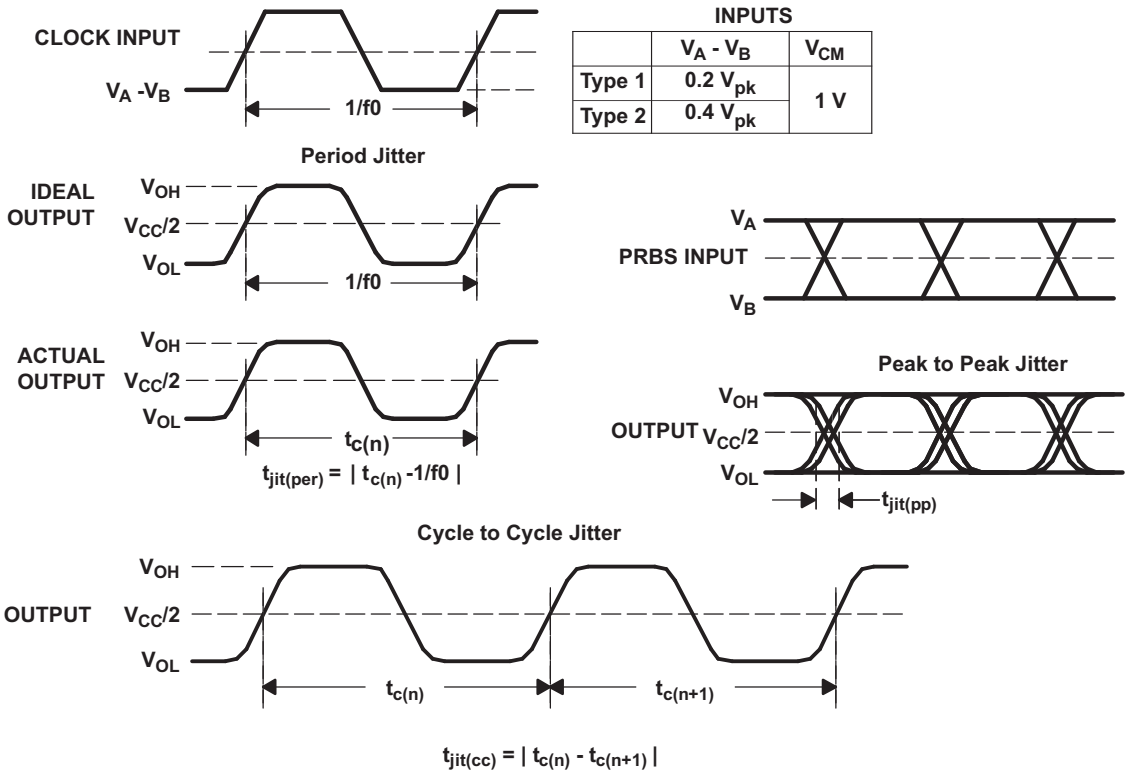


A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.

B. R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.

C. C_L is the instrumentation and fixture capacitance within 2 cm of the DUT and ±20%. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 11. Receiver Enable/Disable Time Test Circuit and Waveforms



A. All input pulses are supplied by the Agilent 81250 Parallel BERT Stimulus System with plug-in E4832A.

B. The cycle-to-cycle measurement is made on a TEK TDS6604 running TDSJIT3 application software.

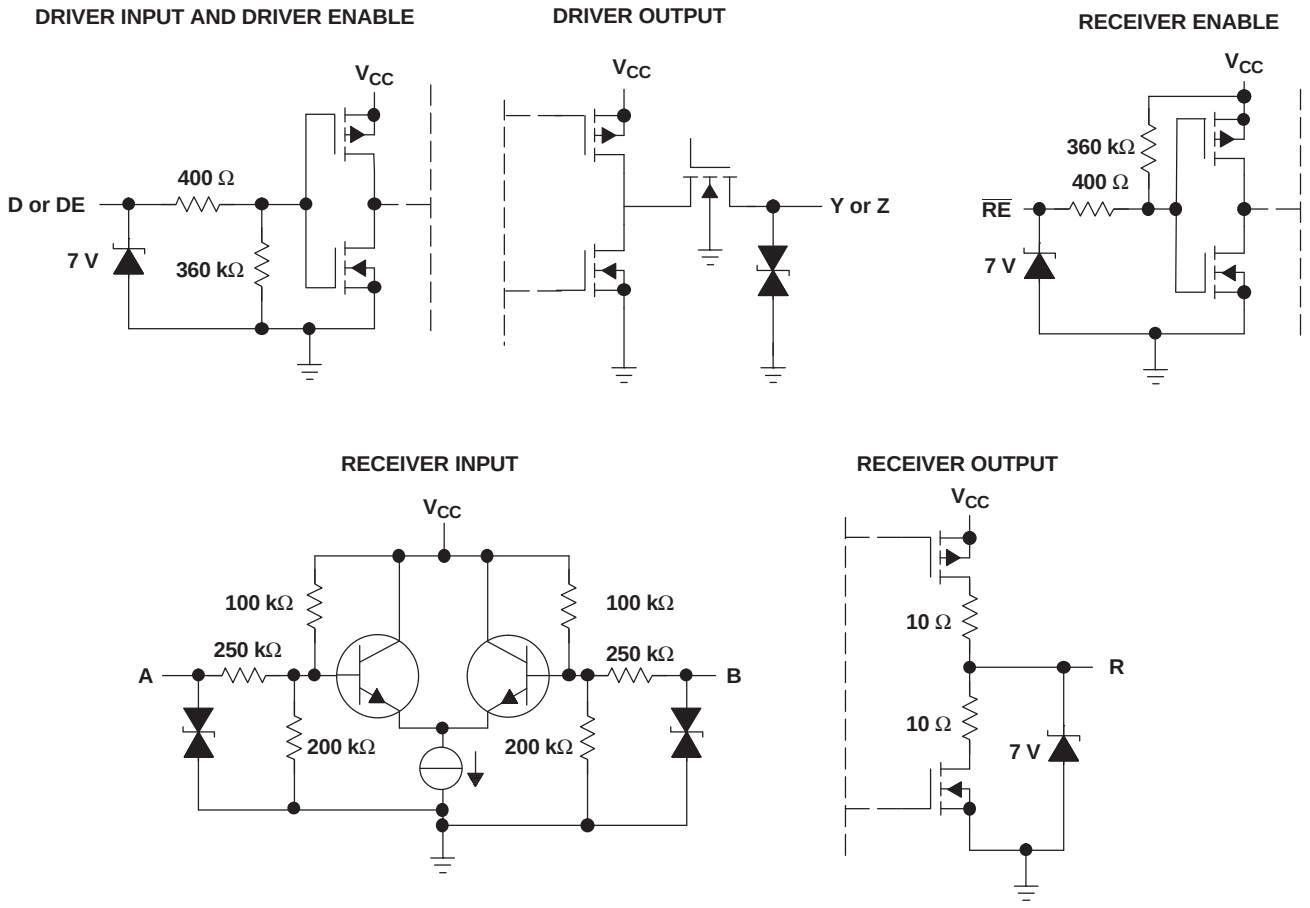
C. All other jitter measurements are made with an Agilent Infiniium DCA-J 86100C Digital Communications Analyzer.

D. Period jitter and cycle-to-cycle jitter are measured using a 125 MHz 50 ±1% duty cycle clock input. Measured over 75K samples.

E. Deterministic jitter and random jitter are measured using a 250 Mbps 2^{15}–1 PRBS input. Measured over BER = 10^{-12}

Figure 12. Receiver Jitter Measurement Waveforms

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TYPICAL CHARACTERISTICS

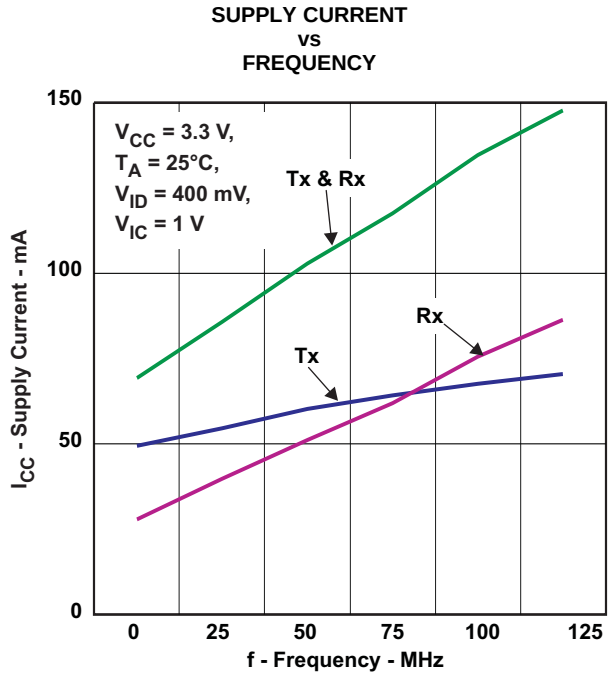


Figure 13.

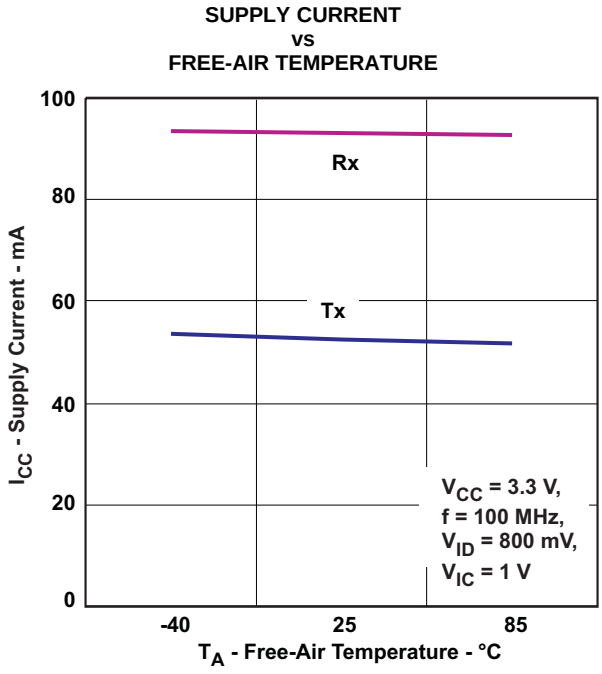


Figure 14.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL OUTPUT VOLTAGE
vs
FREQUENCY

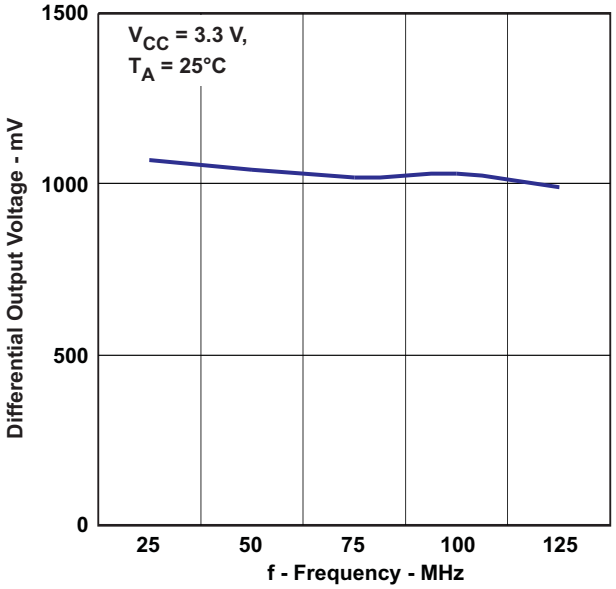


Figure 15.

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT RESISTANCE

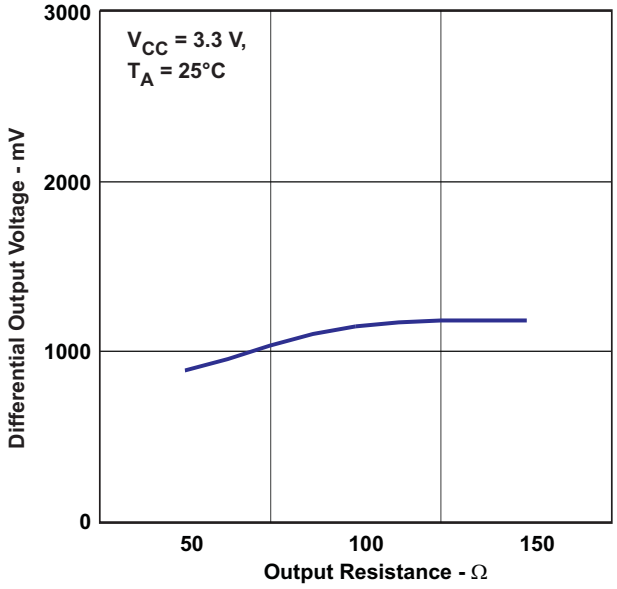


Figure 16.

DIFFERENTIAL OUTPUT VOLTAGE
vs
TRACE LENGTH

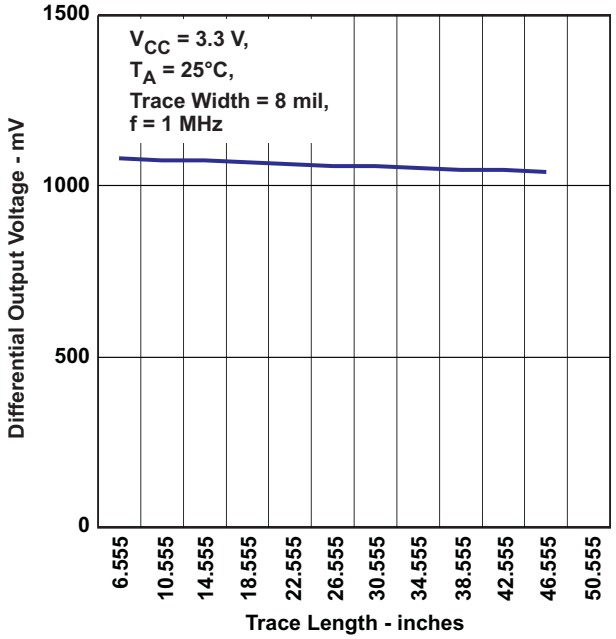


Figure 17.

DRIVER PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

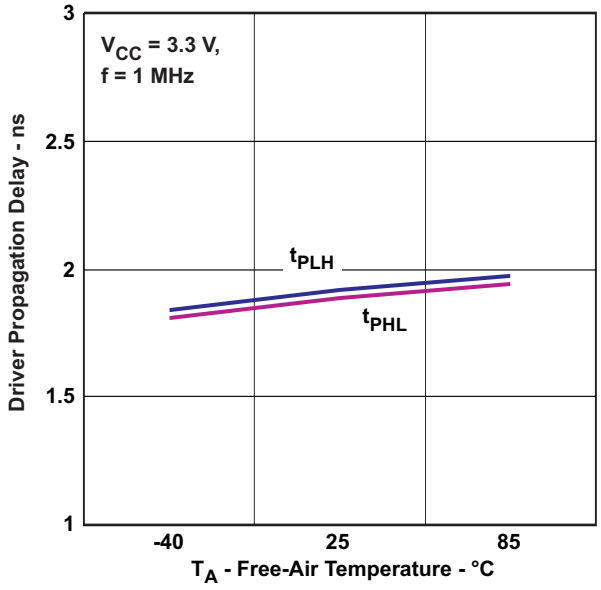


Figure 18.

TYPICAL CHARACTERISTICS (continued)

RECEIVER TYPE-1 PROPAGATION DELAY vs FREE-AIR TEMPERATURE

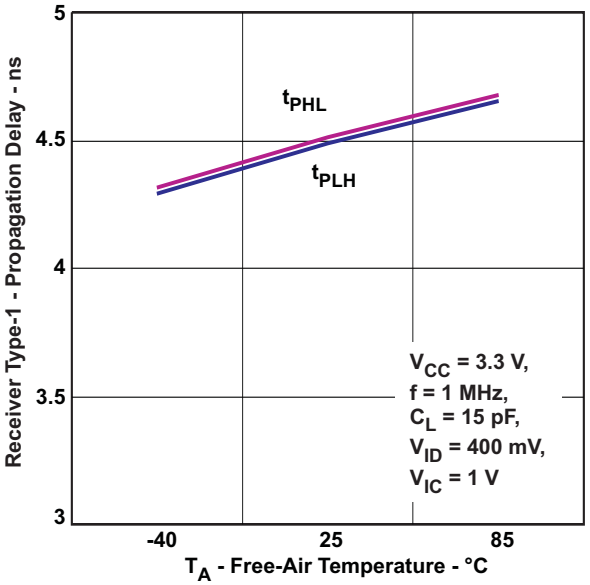


Figure 19.

RECEIVER TYPE-2 PROPAGATION DELAY vs FREE-AIR TEMPERATURE

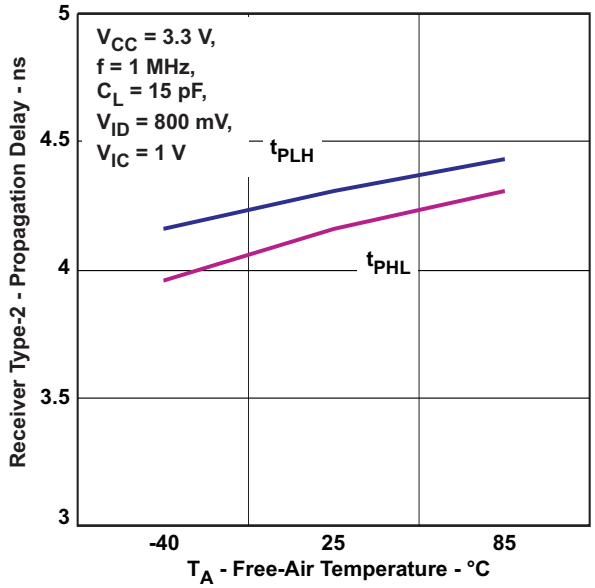


Figure 20.

DRIVER TRANSITION TIME vs FREE-AIR TEMPERATURE

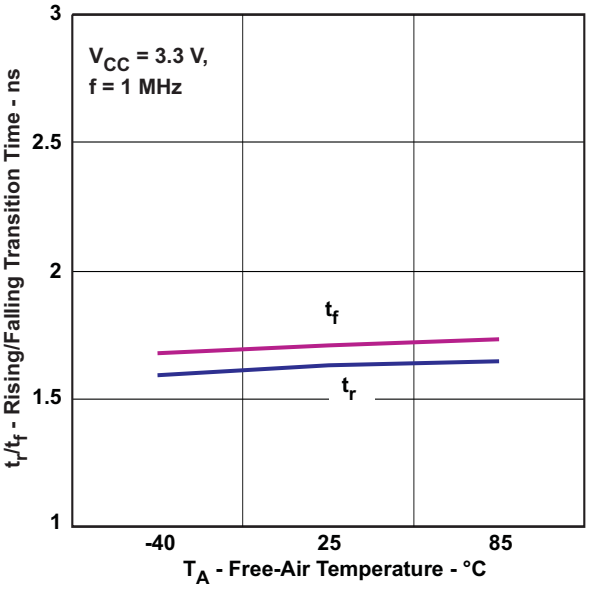


Figure 21.

TYPE-1 RECEIVER TRANSITION TIME vs FREE-AIR TEMPERATURE

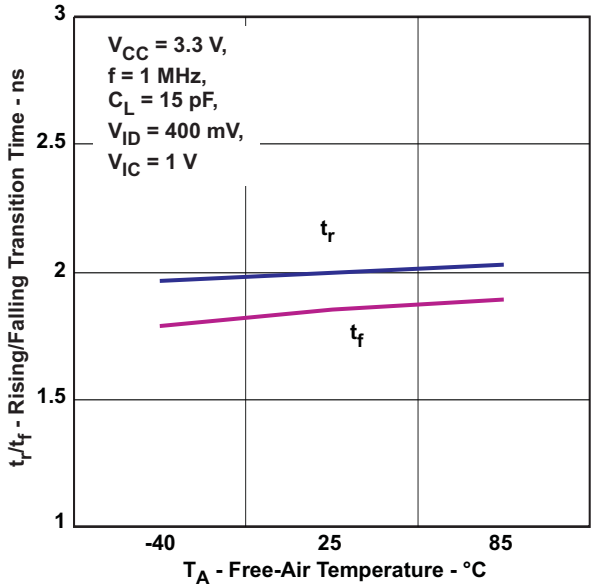


Figure 22.

TYPICAL CHARACTERISTICS (continued)

TYPE-2 RECEIVER TRANSITION TIME vs FREE-AIR TEMPERATURE

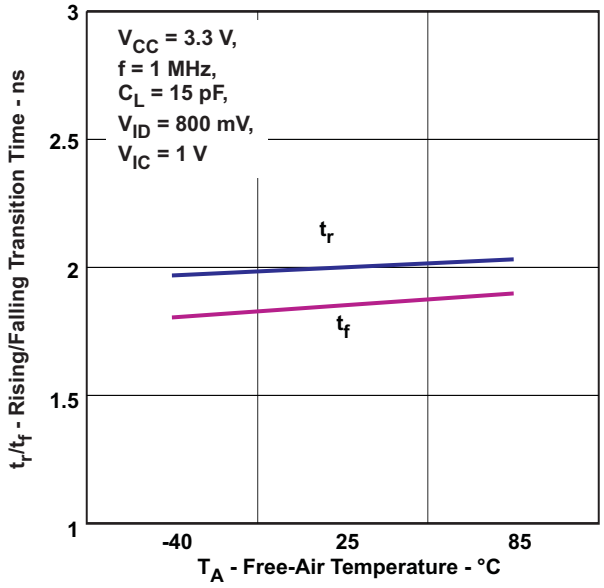


Figure 23.

ADDED RECEIVER TYPE-1 PERIOD JITTER vs FREQUENCY

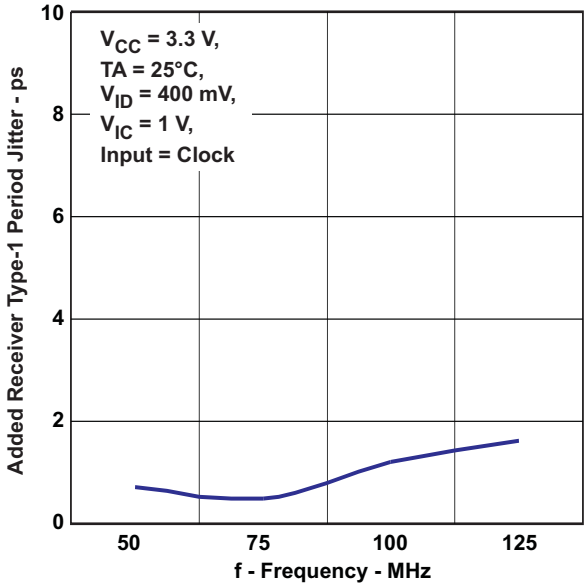


Figure 24.

ADDED RECEIVER TYPE-2 PERIOD JITTER vs FREQUENCY

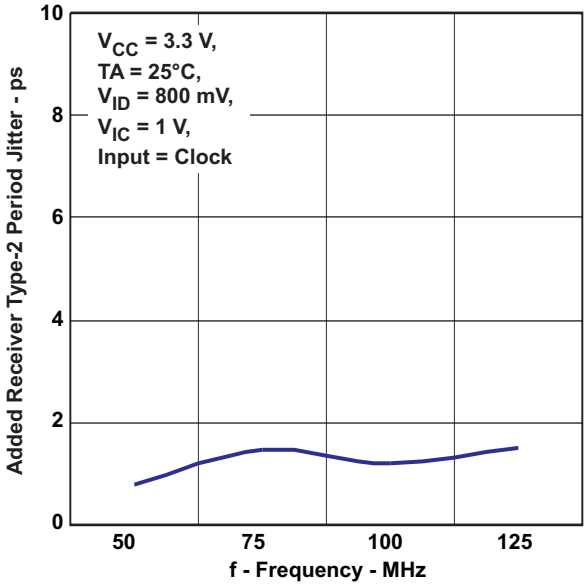


Figure 25.

ADDED DRIVER PERIOD JITTER vs FREQUENCY

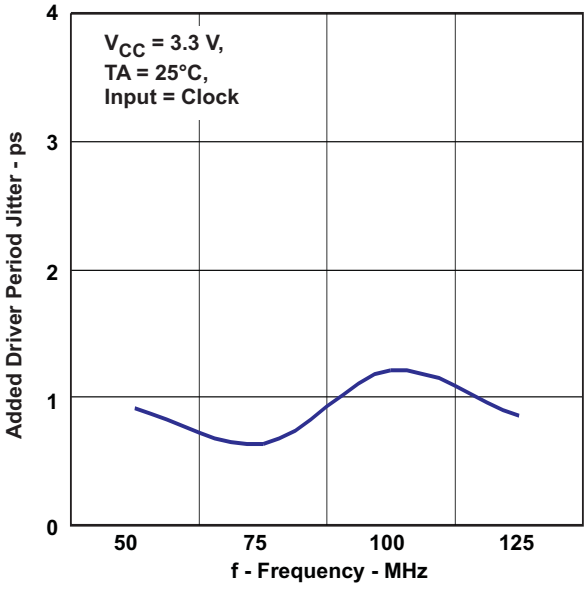


Figure 26.

TYPICAL CHARACTERISTICS (continued)

ADDED RECEIVER TYPE-1 CYCLE-TO-CYCLE JITTER
vs
FREQUENCY

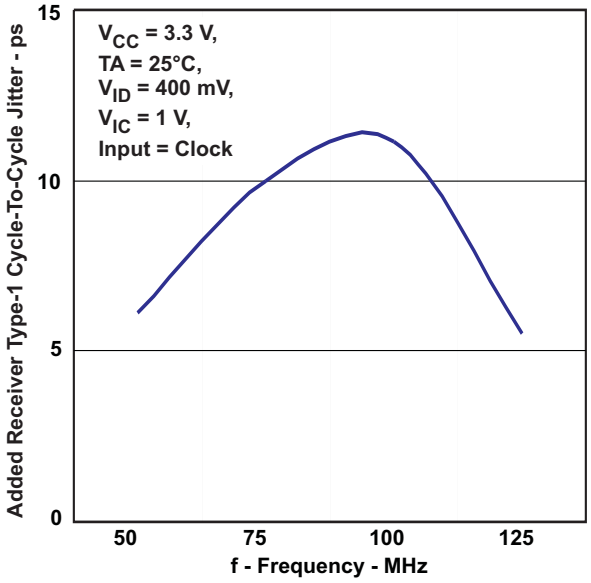


Figure 27.

ADDED RECEIVER TYPE-2 CYCLE-TO-CYCLE JITTER
vs
FREQUENCY

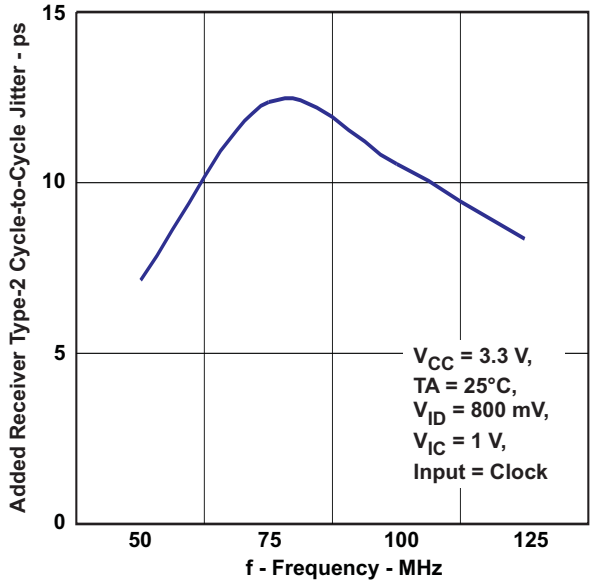


Figure 28.

ADDED DRIVER CYCLE-TO-CYCLE JITTER
vs
FREQUENCY

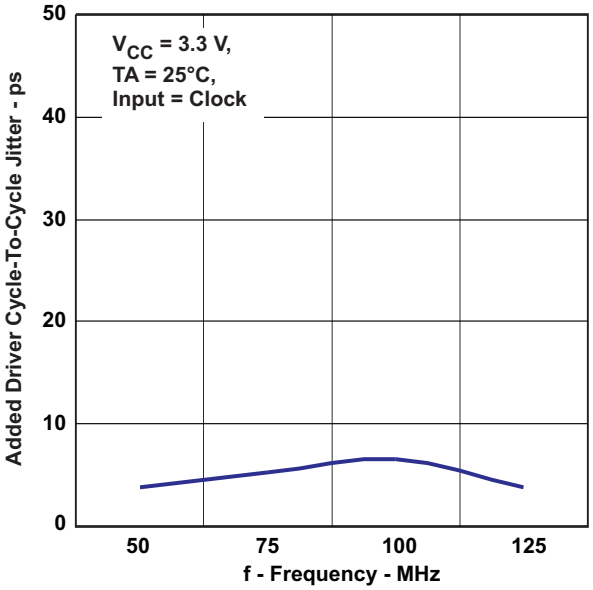


Figure 29.

ADDED RECEIVER TYPE-1 DETERMINISTIC JITTER
vs
DATA RATE

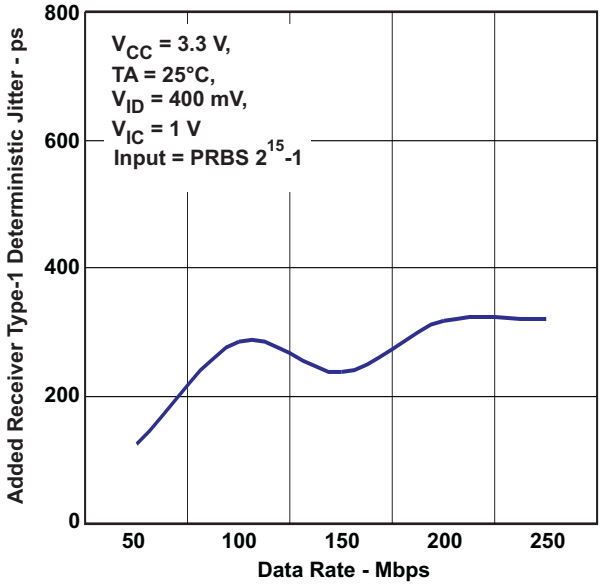


Figure 30.

TYPICAL CHARACTERISTICS (continued)

ADDED RECEIVER TYPE-2 DETERMINISTIC JITTER vs DATA RATE

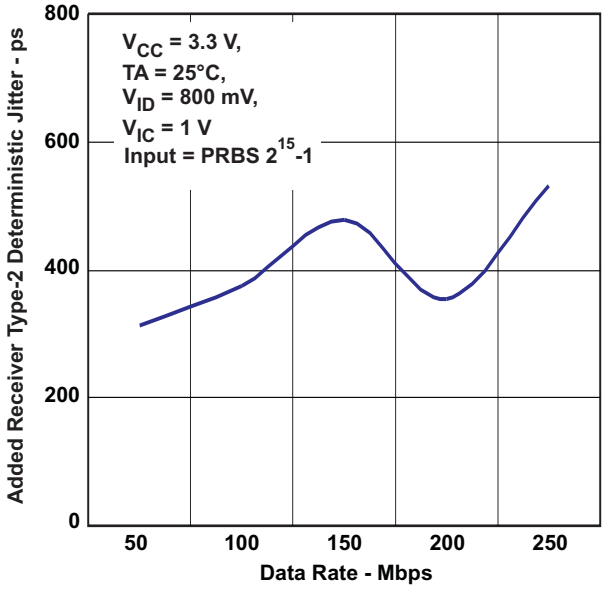


Figure 31.

DRIVER OUTPUT EYE PATTERN 250 Mbps, 2^{15}–1 PRBS, V_{CC} = 3.3 V

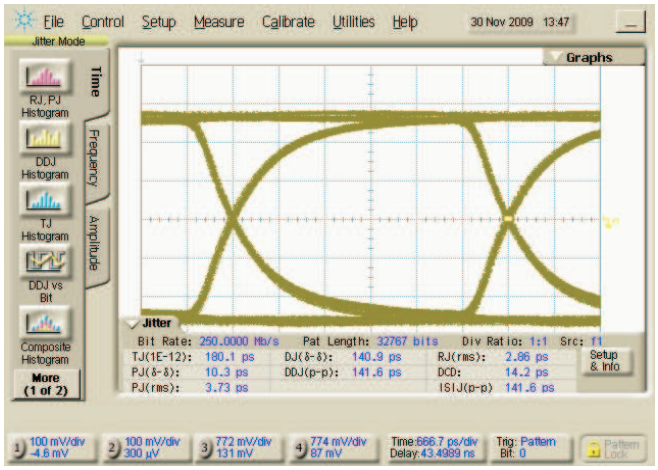


Figure 32.

RECEIVER OUTPUT EYE PATTERN 250 Mbps, 2^{15}–1 PRBS, V_{CC} = 3.3 V $|V_{ID}|$ = 400 mV_{PP}, V_{IC} = 1 V

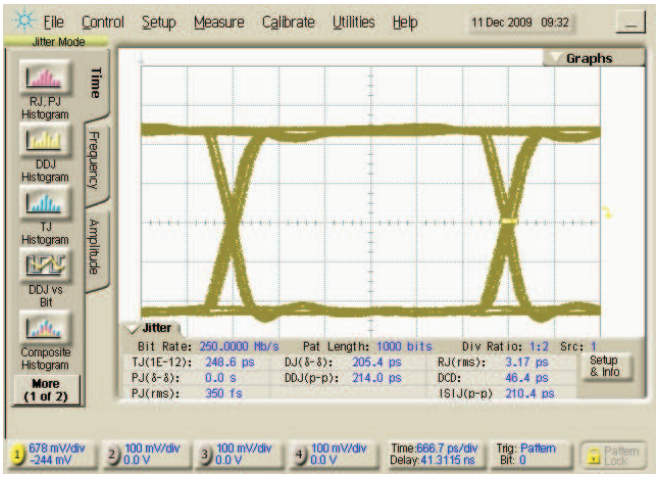


Figure 33.

RECEIVER OUTPUT EYE PATTERN 250 Mbps, 2^{15}–1 PRBS, V_{CC} = 3.3 V $|V_{ID}|$ = 800 mV_{PP}, V_{IC} = 1 V

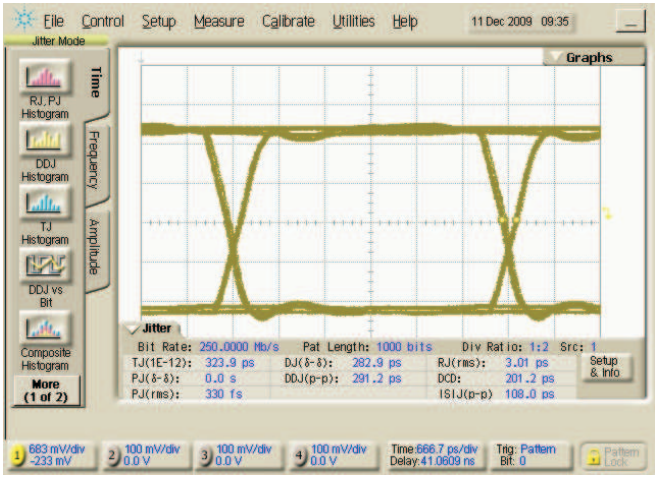


Figure 34.

APPLICATION INFORMATION

Source Synchronous System Clock (SSSC)

There are two approaches to transmit data in a synchronous system: centralized synchronous system clock (CSSC) and source synchronous system clock (SSSC). CSSC systems synchronize data transmission between different modules using a clock signal from a centralized source. The key requirement for a CSSC system is for data transmission and reception to complete during a single clock cycle. The maximum operating frequency is the inverse of the shortest clock cycle for which valid data transmission and reception can be ensured. SSSC systems achieve higher operating frequencies by sending clock and data signals together to eliminate the flight time on the transmission media, backplane, or cables. In SSSC systems, the maximum operating frequency is limited by the cumulated skews that can exist between clock and data. The absolute flight time of data on the backplane does not provide a limitation on the operating frequency as it does with CSSC.

The SN65MLVD082 can be designed for interfacing the data and clock to support source synchronous system clock (SSSC) operation. It is specified for transmitting data up to 250 Mbps and clock frequencies up to 125 MHz. Figure 35 shows an example of a SSSC architecture supported by M-LVDS transceivers. The SN65MLVD206, a single channel transceiver, transmits the main system clock between modules. A retiming unit is then applied to the main system clock to generate a local clock for subsystem synchronization processing. System operating data (or control) and subsystem clock signals are generated from the data processing unit, such as a microprocessor, FPGA, or ASIC, on module 1, and sent to slave modules through the SN65MLVD082. Such design configurations are common while transmitting parallel control data over the backplane with a higher SSSC subsystem clock frequency. The subsystem clock frequency is aligned with the operating frequencies of the data processing unit to synchronize data transmission between different units.

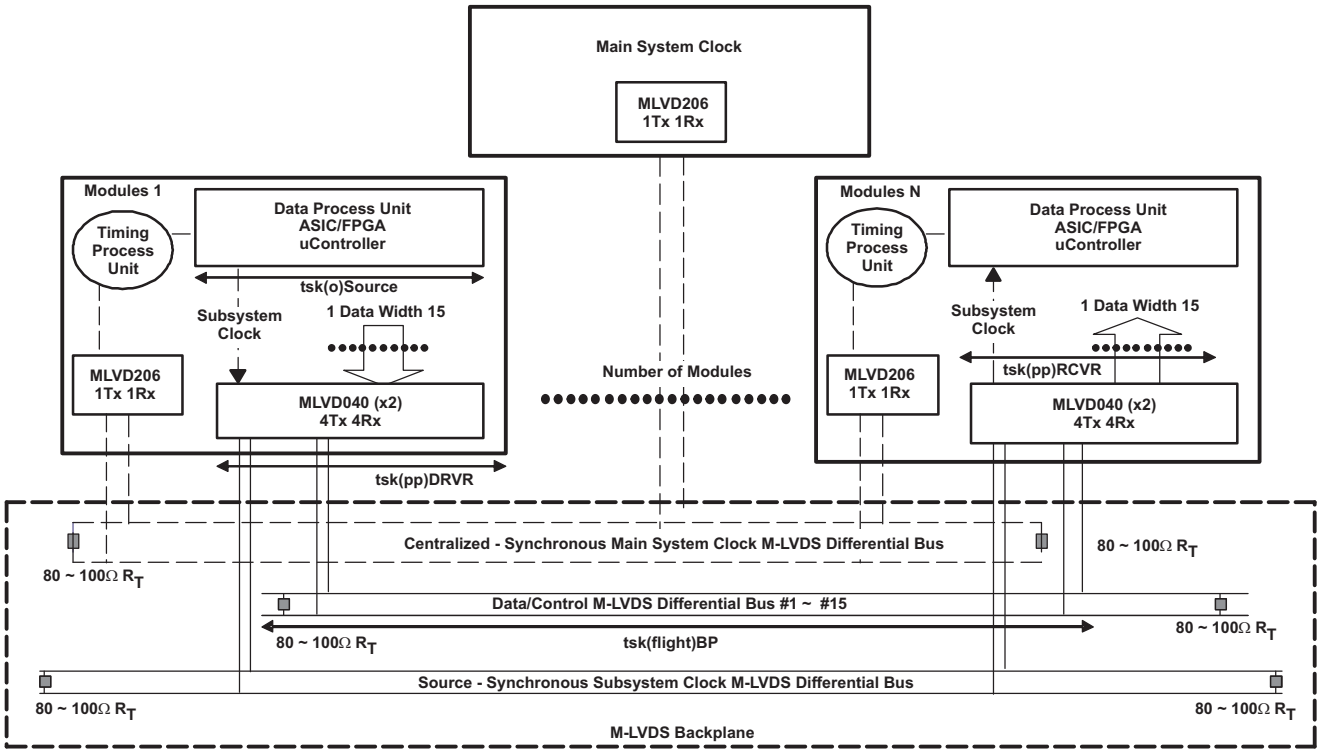


Figure 35. Using Differential M-LVDS to Perform Source Synchronous System Clock Distribution

The maximum SSSC frequencies in a transparent mode can be calculated with Equation 1:

$$f_{max(clk)} < 1/[\ t_{sk(o)Source} + t_{sk(pp)DRVR} + t_{sk(flight)BP} + t_{sk(pp)RCVR} \quad (1)$$

Setup time and hold time on the receiver side are decided by the data processing unit, FPGA, or ASIC in this example. By considering data passes through the transceiver only, the general calculation result is 238 MHz when using the following data:

$t_{sk(o)Source}$ = 2 ns – Output skew of data processing unit; any skew between data bits, or clock and data bits

$t_{sk(pp)DRVR}$ = 0.6 ns – Driver part-to-part skew of the SN65MLVD040

$t_{sk(flight)BP}$ = 0.4 ns – Skew of propagation delay on the backplane between data and clock

$t_{sk(pp)RCVR}$ = 1 ns – Receiver part-to-part skew of the SN65MLVD040

The 238-MHz maximum operating speed calculated above was determined based on data and clock skews only. Another important consideration when calculating the maximum operating speed is output transition time. Transition-time-limited operating speed is calculated from Equation 2:

$$f = 45\% \times \frac{1}{2 \times t_{transition}} \quad (2)$$

Using the typical transition time of the SN65MLVD040 of 1.4 ns, a transition-time-limited operating frequency of 170 MHz can be supported.

In addition to the high operating frequencies of SSSC that can be ensured, the SN65MLVD040 presents other benefits as other M-LVDS bus transceivers can provide:

- Robust system operation due to common mode noise cancellation using a low voltage differential receiver
- Low EMI radiation noise due to differential signaling improves signal integrity through the backplane
- A singly terminated transmission line is easy to design and implement
- Low power consumption in both active and idle modes minimizes thermal concerns on each module

In dense backplane design, these benefits are important for improving the performance of the whole system.

LIVE INSERTION/GLITCH-FREE POWER UP/DOWN

The SN65MLVD040 family of products offered by Texas Instruments provides a glitch-free powerup/down feature that prevents the M-LVDS outputs of the device from turning on during a powerup or powerdown event. This is especially important in live insertion applications, when a device is physically connected to an M-LVDS multipoint bus and V_{CC} is ramping.

While the M-LVDS interface for these devices is glitch free on powerup/down, the receiver output structure is not. Figure 36 shows the performance of the receiver output pin, R (CHANNEL 2), as V_{CC} (CHANNEL 1) is ramped.

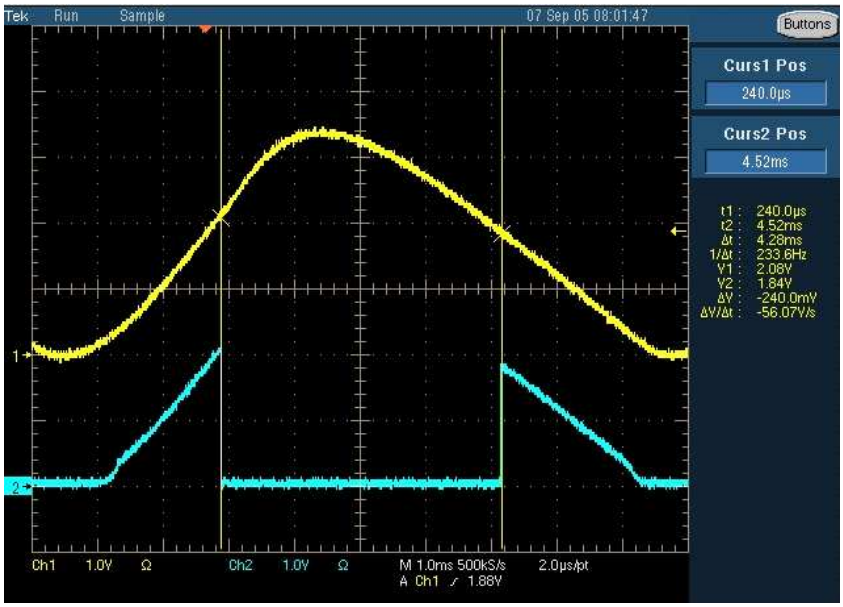


Figure 36. M-LVDS Receiver Output: V_{CC} (CHANNEL 1), R Pin (CHANNEL 2)

The glitch on the R pin is independent of the $\overline{RE}$ voltage. Any complications or issues from this glitch are resolved in power sequencing or system requirements that suspend operation until V_{CC} has reached a steady state value.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65MLVD040RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	MLVD040	Samples
SN65MLVD040RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	MLVD040	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

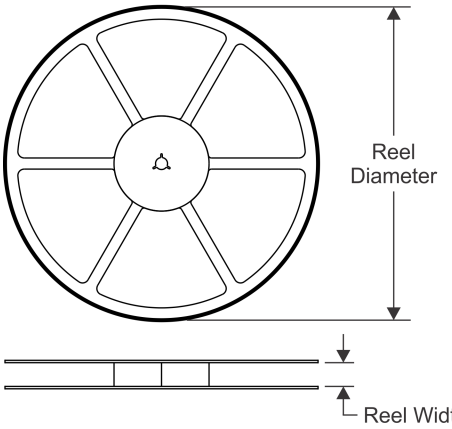
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

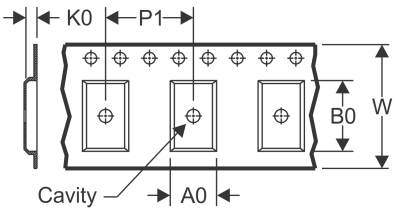
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

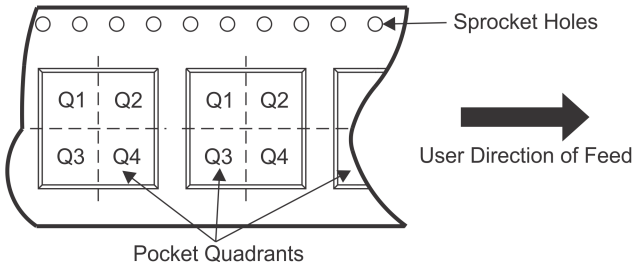


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

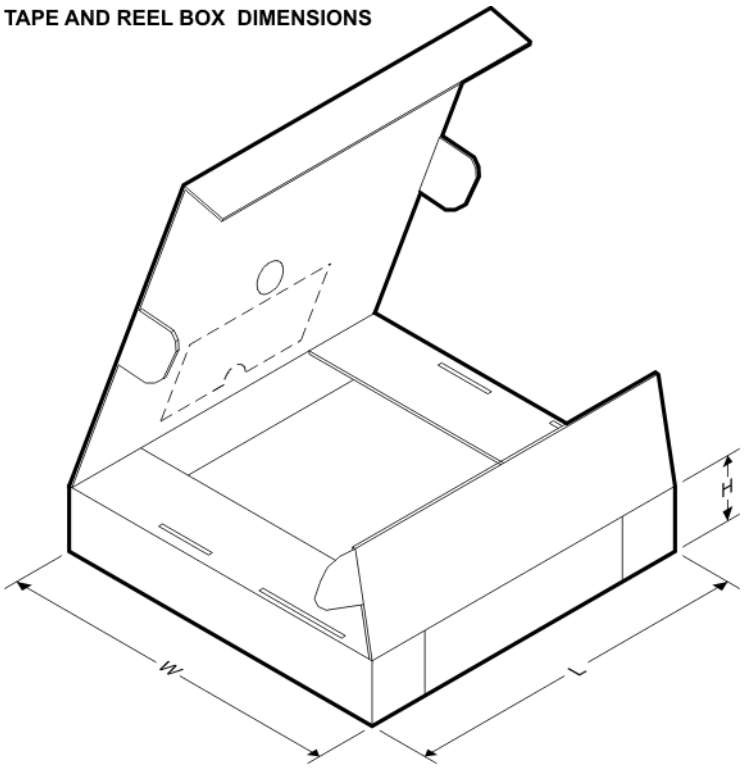
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD040RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN65MLVD040RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

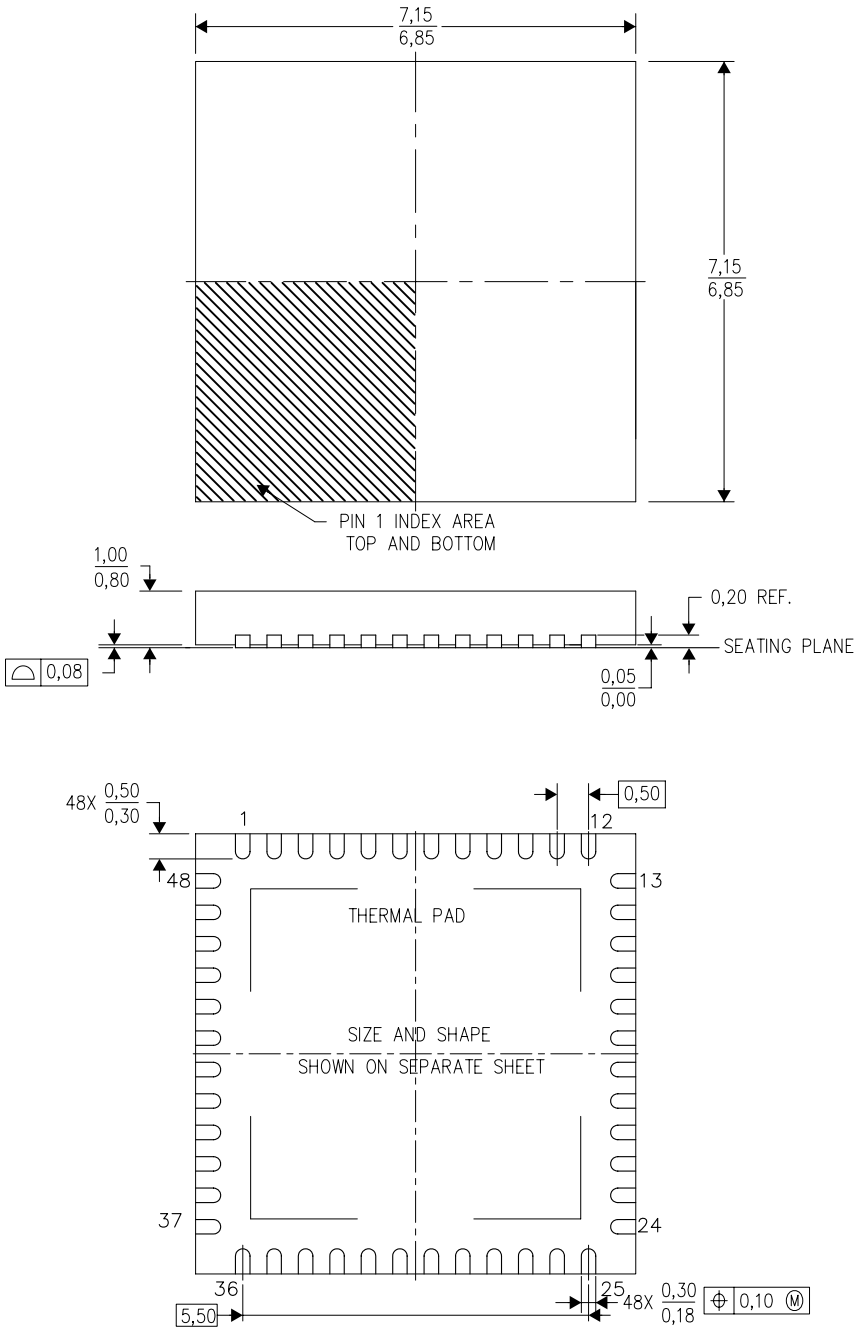
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD040RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
SN65MLVD040RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

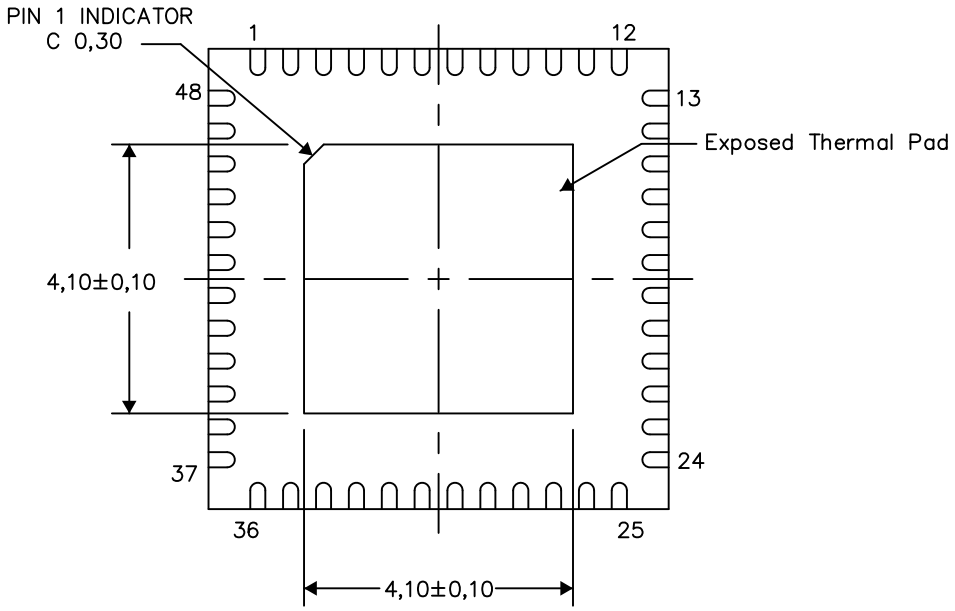
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



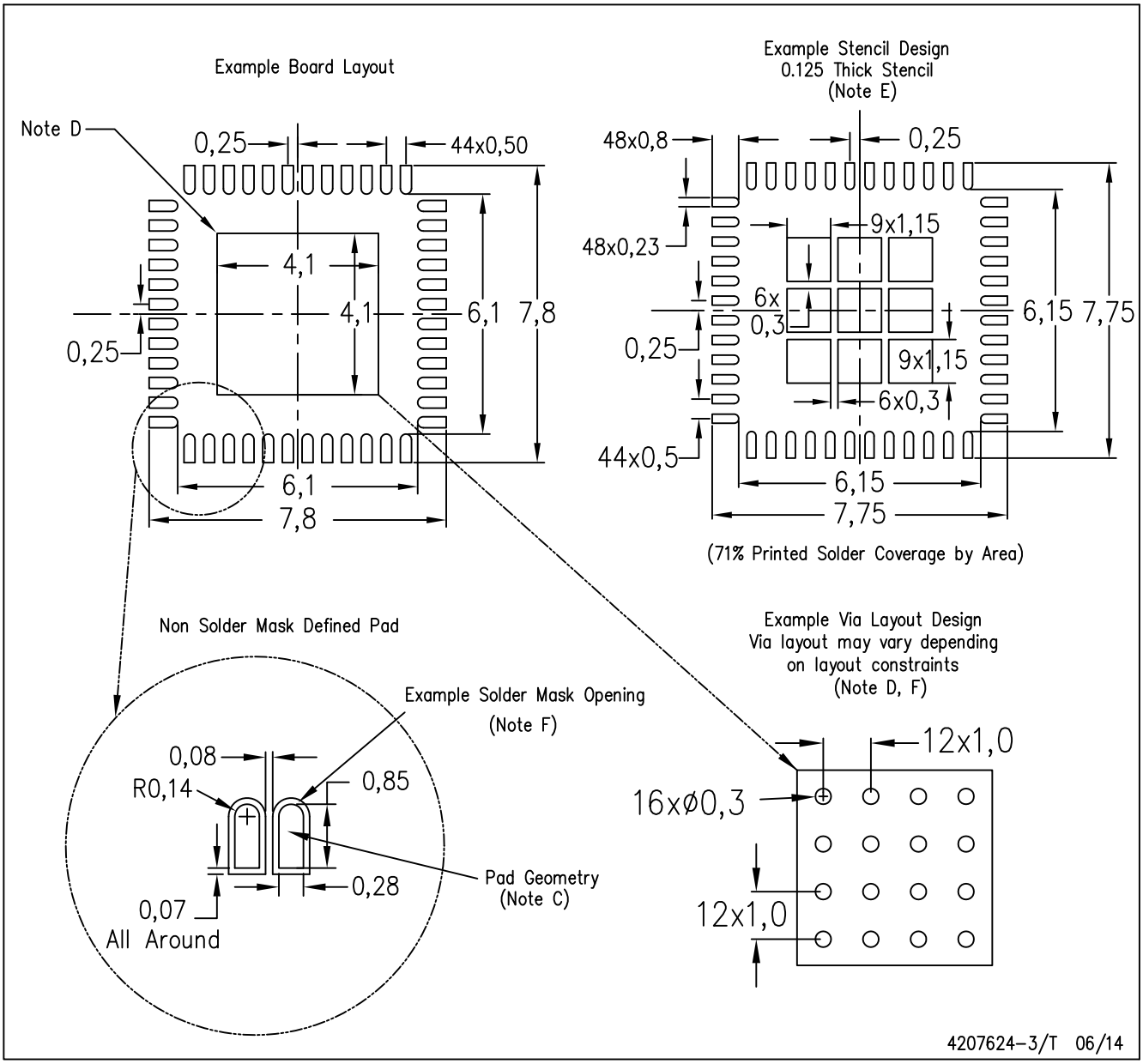
Bottom View

Exposed Thermal Pad Dimensions

4206354–3/Z 03/15

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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