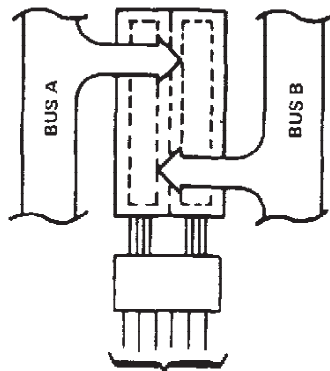


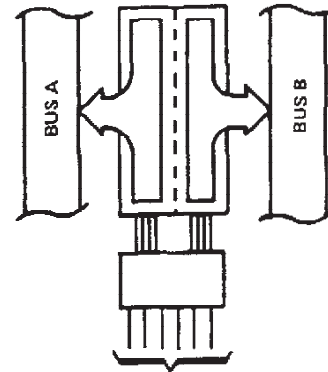
SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

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(21)	(3)	(1)	(23)	(2)	(22)
\bar{G}	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21)	(3)	(1)	(23)	(2)	(22)
\bar{G}	DIR	CAB	CBA	SAB	SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

TRANSFER
STORED DATA
TO A OR B

Enable (\bar{G}) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable \bar{G} is active (low). In the isolation mode (control \bar{G} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0° to 70°C .

FUNCTION TABLE

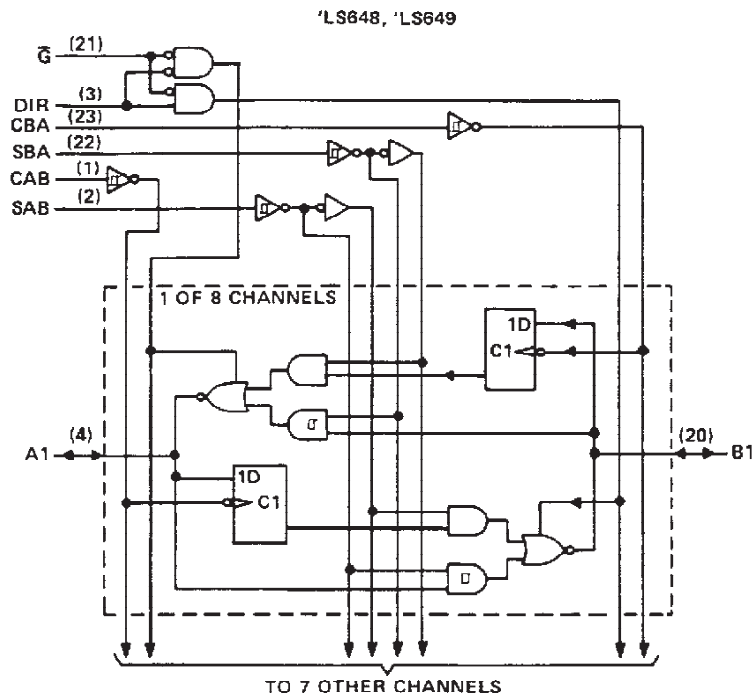
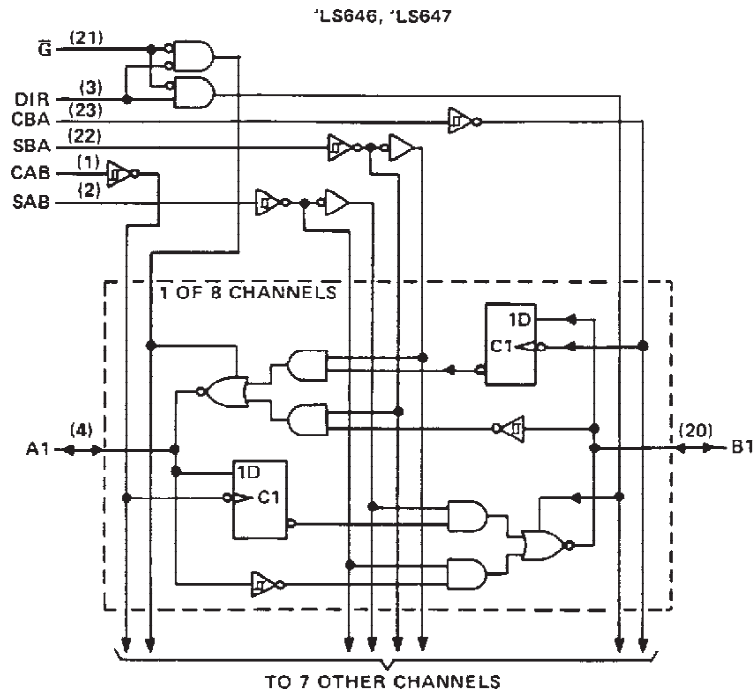
INPUTS						DATA I/O†		OPERATION OR FUNCTION	
\bar{G}	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	LS646, LS647	LS648, LS649
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time \bar{B} Data to A Bus
L	L	X	HorL	X	H	Output	Input	Stored B Data to A Bus	Stored \bar{B} Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time \bar{A} Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus	Stored \bar{A} Data to B Bus

† The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

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logic diagrams (positive logic)



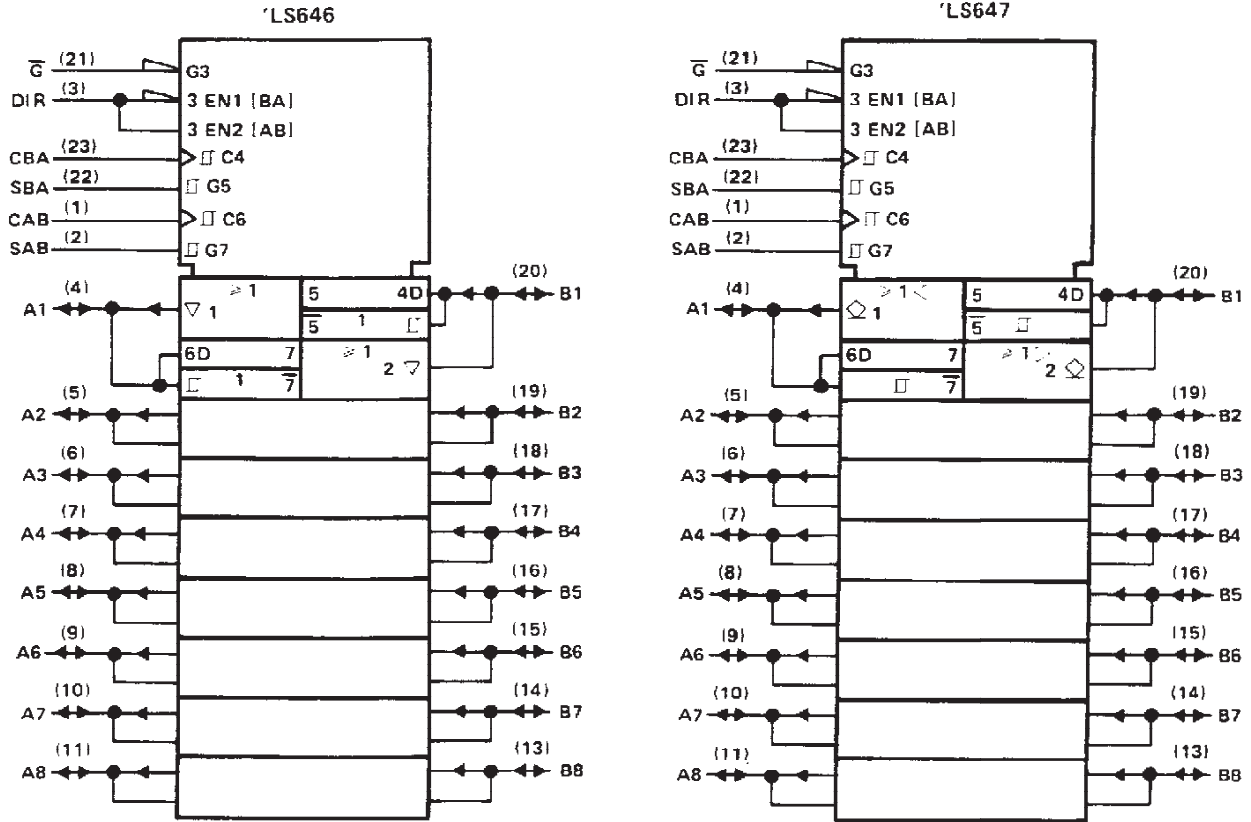
Pin numbers shown are for DW, JT, and NT packages.

SN54LS646, SN54LS647, SN74LS646, SN74LS647

OCTAL BUS TRANSCEIVERS AND REGISTERS

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logic symbols †

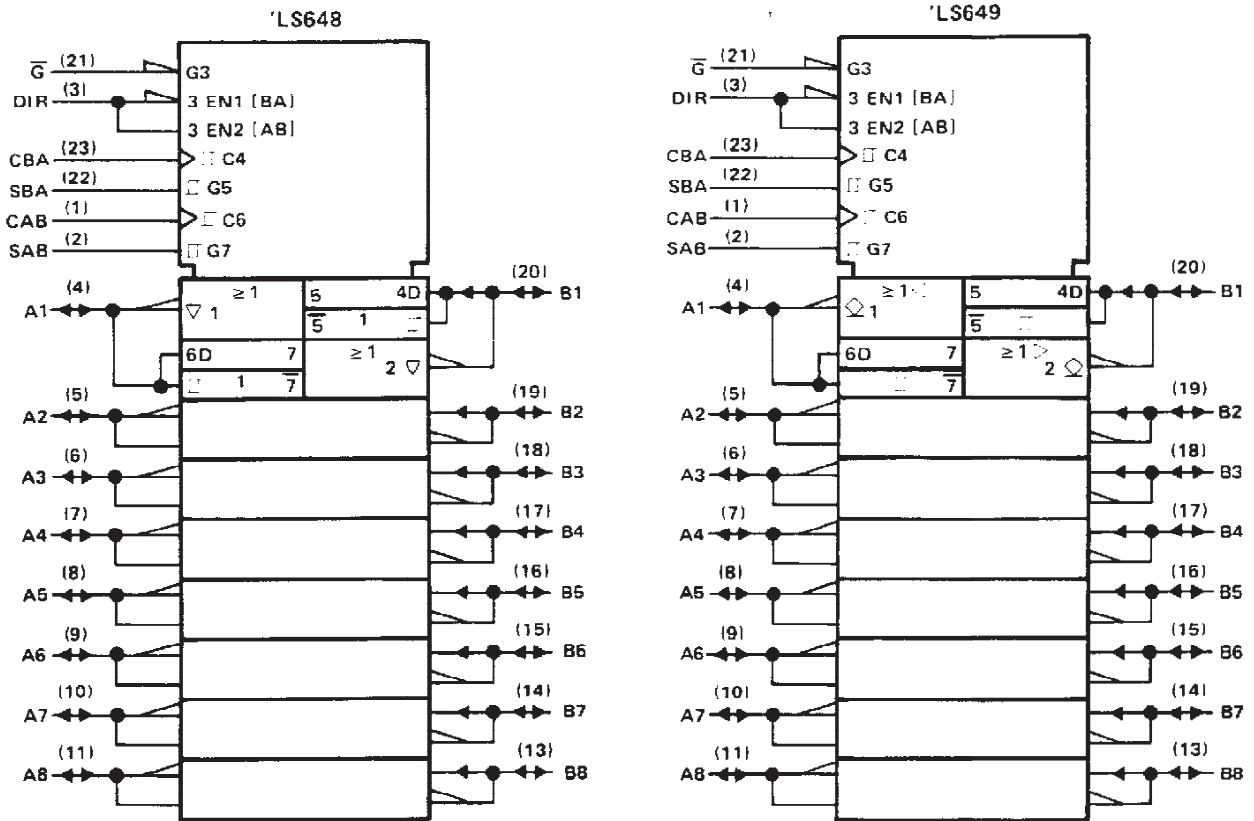


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

SN54LS648, SN54LS649, SN74LS648, SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

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logic symbols† (continued)

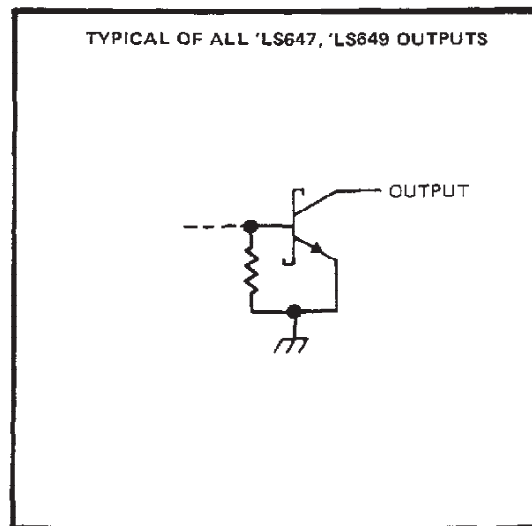
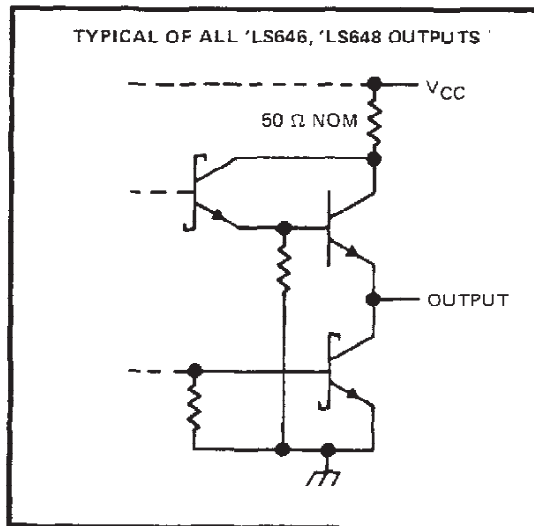
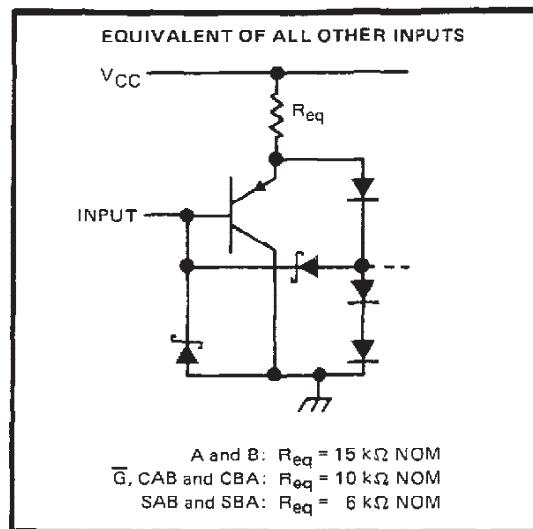
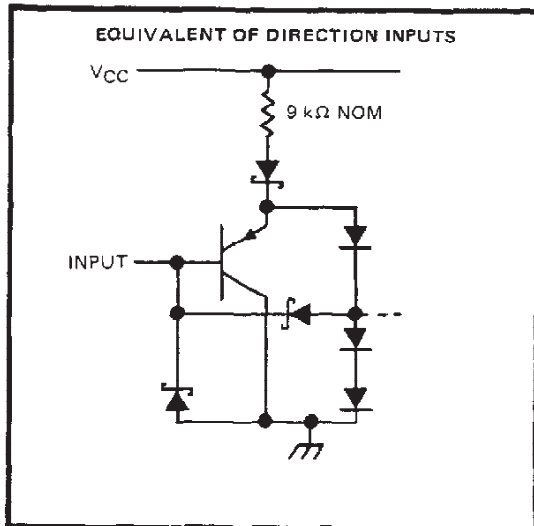


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

SN54LS646 THRU SN54LS649
SN74LS646 THRU SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS

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schematics of inputs and outputs



SN54LS646, SN54LS648, SN74LS646, SN74LS648

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS646			'LS648			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CAB or CBA	A or B	$R_L = 667\ \Omega$, $C_L = 45\ \text{pF}$, See Note 2	15	25		15	25	ns	
t_{PHL}				23	35		24	40	ns	
t_{PLH}	A or B	B or A		12	18		12	18	ns	
t_{PHL}				13	20		15	25	ns	
t_{PLH}	SAB or SBA [†] with Bus input high	A or B		26	40		37	55	ns	
t_{PHL}				21	35		24	40	ns	
t_{PLH}	SAB or SBA [†] with Bus input low	A or B		33	50		26	40	ns	
t_{PHL}				14	25		23	40	ns	
t_{PZH}	\overline{G}	A or B		33	55		30	50	ns	
t_{PZL}				42	65		37	55	ns	
t_{PZH}	DIR	A or B	28	45		23	40	ns		
t_{PZL}			39	60		30	45	ns		
t_{PHZ}	\overline{G}	A or B	23	35		28	45	ns		
t_{PLZ}			22	35		22	35	ns		
t_{PHZ}	DIR	A or B	20	30		24	35	ns		
t_{PLZ}			19	30		19	30	ns		

[†] These parameters are measured with the internal output state of the storage register opposite to that of the input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN54LS647, SN54LS649, SN74LS647, SN74LS649

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (control inputs)	7 V
Off-state output voltage (A and B ports)	5.5 V
Operating free-air temperature range: SN54LS647, SN54LS649	– 55°C to 125°C
SN74LS647, SN74LS649	– 0°C to 70°C
Storage temperature range	– 65°C to 150°C

recommended operating conditions

		SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.5			0.6	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output voltage			12			24	mA
t_w	Pulse duration	CBA or CAB high		15	15			ns
		CBA or CAB low		30	30			
		Data high or low		30	30			
t_{su}	Setup time before CAB † or CBA †	A or B		15	15		ns	
t_h	Hold time after CAB † or CBA †	A or B		0	0		ns	
T_A	Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			– 1.5			– 1.5	V
Hysteresis ($V_{T+} - V_{T-}$)	A or B input	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4		V
I_{OH}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$			0.1			0.1	mA
V_{OL}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$			0.25	0.4	0.25	0.4	V
I_I	A or B	$V_{CC} = \text{MAX}$			0.1			0.1	mA
	All others		$V_I = 5.5 \text{ V}$			0.1		0.1	
I_{IH}		$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}		$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			– 0.4			– 0.4	mA
I_{CC}	'LS647	$V_{CC} = \text{MAX}, \text{Outputs open}$	Outputs high	79	130		79	130	mA
			Outputs low	94	150		94	150	
	'LS649	$V_{CC} = \text{MAX}, \text{Outputs open}$	Outputs high	79	130		79	130	
			Outputs low	94	150		94	150	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.



SN54LS647, SN54LS649, SN74LS647, SN74LS649

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

SDLS190A – DECEMBER 1982 – REVISED MAY 2004

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS647			'LS649			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CAB or CBA	A or B	$R_L = 667\ \Omega$, $C_L = 45\ \text{pF}$, See Note 2	22		35	17		30	ns
t_{PHL}				28		45	28		45	ns
t_{PLH}	A or B	B or A		17		26	15		25	ns
t_{PHL}				18		27	20		30	ns
t_{PLH}	SAB or SBA† with Bus input high	A or B		33		50	37		55	ns
t_{PHL}				29		45	28		45	ns
t_{PLH}	SAB or SBA† with Bus input low			39		60	30		45	ns
t_{PHL}				19		30	26		40	ns
t_{PLH}	G	A or B		25		40	21		40	ns
t_{PHL}				33		50	34		50	ns
t_{PLH}	DIR		23		35	19		30	ns	
t_{PHL}			25		40	27		45	ns	

† These parameters are measured with the internal outputs state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS646DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	0 to 70	LS646	Samples
SN74LS646NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74LS647DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
SN74LS647NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74LS649NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

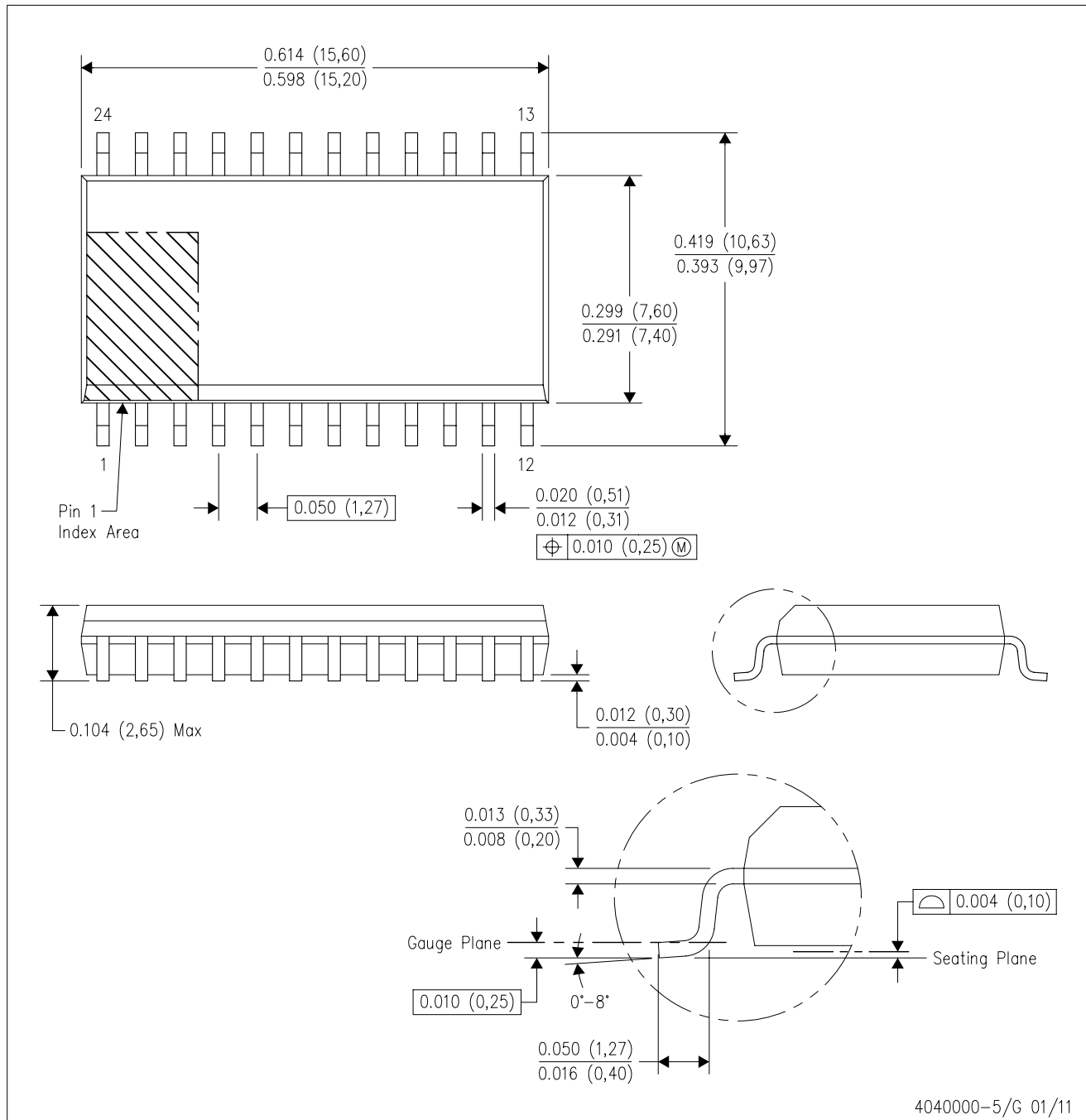
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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