

SN74ALS29863 9-BIT TRANSCEIVER WITH 3-STATE OUTPUTS

SDAS096C – JANUARY 1986 – REVISED JANUARY 1995

- Functionally Equivalent to AMD's AM29863
- Power-Up High-Impedance State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

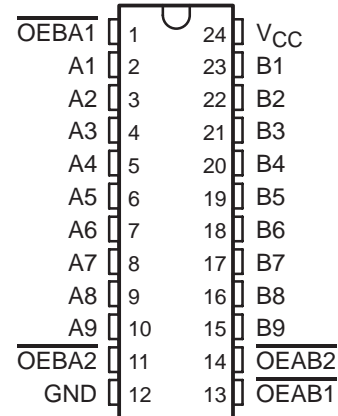
description

This 9-bit transceiver is designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable ($\overline{OEAB1}$, $\overline{OEAB2}$, $\overline{OEBA1}$, and $\overline{OEBA2}$) inputs.

The SN74ALS29863 is characterized for operation from 0°C to 70°C.

DW OR NT PACKAGE
(TOP VIEW)



FUNCTION TABLE

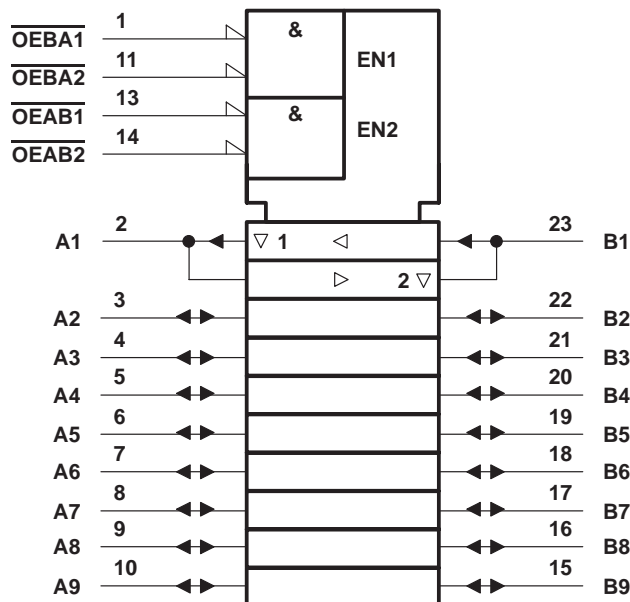
| INPUTS | | | | OPERATION |
|--------------------|--------------------|--------------------|--------------------|---------------|
| $\overline{OEAB1}$ | $\overline{OEAB2}$ | $\overline{OEBA1}$ | $\overline{OEBA2}$ | |
| L | L | L | L | Latch A and B |
| L | L | H | X | A to B |
| L | L | X | H | |
| H | X | L | L | B to A |
| X | H | L | L | |
| H | X | H | X | Isolation |
| H | X | X | H | |
| X | H | X | H | |
| X | H | H | X | |

SN74ALS29863

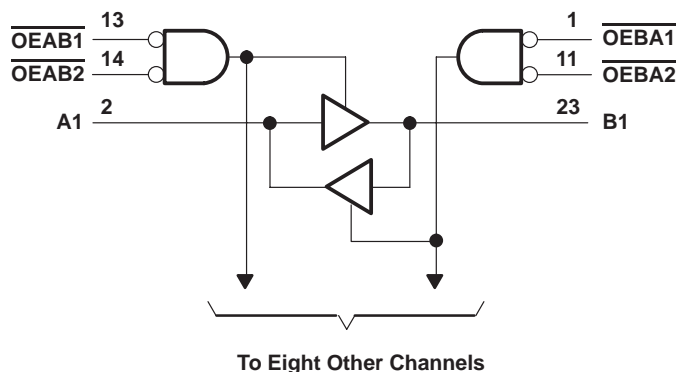
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I (all inputs and I/O ports) | 5.5 V |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--------------------------------------|------|-----|------|------|
| V_{CC} Supply voltage | 4.75 | 5 | 5.25 | V |
| V_{IH} High-level input voltage | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.8 | V |
| I_{OH} High-level output current | | | -24 | mA |
| I_{OL} Low-level output current | | | 48 | mA |
| T_A Operating free-air temperature | 0 | | 70 | °C |

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-------------------|----------------|---|--------------------------|------|------|------|
| V _{IK} | | V _{CC} = 4.75 V, I _I = -18 mA | | | -1.2 | V |
| V _{OH} | | V _{CC} = 4.75 V | I _{OH} = -15 mA | | 2.4 | V |
| | | | I _{OH} = -24 mA | | 2 | |
| V _{OL} | | V _{CC} = 4.75 V, I _{OL} = 48 mA | | 0.35 | 0.5 | V |
| I _I | | V _{CC} = 5.25 V, V _I = 5.5 V | | | 0.1 | mA |
| I _{IH} | Control inputs | V _{CC} = 5.25 V, V _I = 2.7 V | | | 20 | μA |
| | A or B ports‡ | | | | 20 | |
| I _{IL} | Control inputs | V _{CC} = 5.25 V, V _I = 0.4 V | | | -0.1 | mA |
| | A or B ports‡ | | | | -0.1 | |
| I _{OS} § | | V _{CC} = 5.25 V, V _O = 0 | -75 | | -250 | mA |
| I _{CC} | | V _{CC} = 5.25 V | | 40 | 65 | mA |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

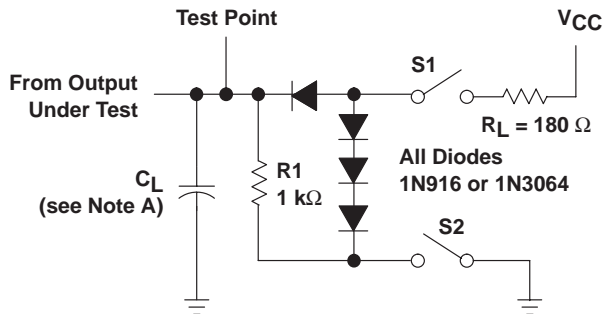
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC} = 4.75 V to 5.25 V | | UNIT |
|------------------|--|-------------|-------------------------|------------------------------------|-----|------|
| | | | | MIN | MAX | |
| t _{PLH} | A or B | B or A | C _L = 300 pF | | | ns |
| t _{PHL} | | | | | | |
| t _{PLH} | A or B | B or A | C _L = 50 pF | | | ns |
| t _{PHL} | | | | | | |
| t _{PZH} | \overline{OEAB} or \overline{OEBA} | A or B | C _L = 300 pF | | | ns |
| t _{PZL} | | | | | | |
| t _{PZH} | \overline{OEAB} or \overline{OEBA} | A or B | C _L = 50 pF | | | ns |
| t _{PZL} | | | | | | |
| t _{PHZ} | \overline{OEAB} or \overline{OEBA} | A or B | C _L = 50 pF | | | ns |
| t _{PLZ} | | | | | | |
| t _{PHZ} | \overline{OEAB} or \overline{OEBA} | A or B | C _L = 5 pF | | | ns |
| t _{PLZ} | | | | | | |



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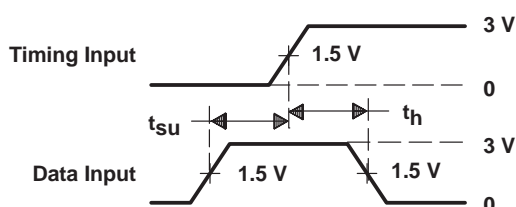
PARAMETER MEASUREMENT INFORMATION



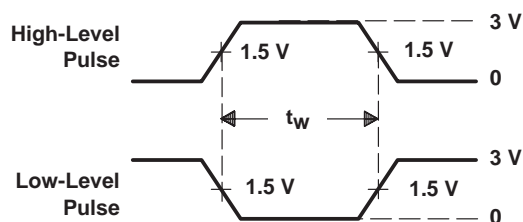
LOAD CIRCUIT

SWITCH POSITION TABLE

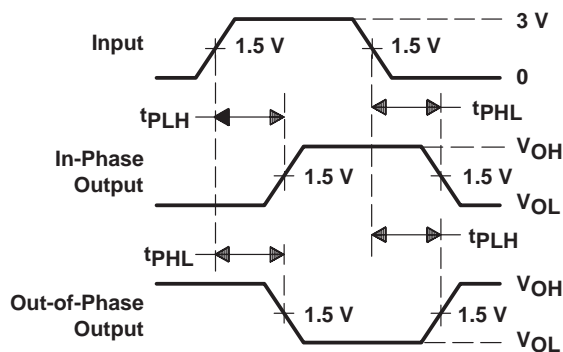
| TEST | S1 | S2 |
|-----------|--------|--------|
| t_{PLH} | Closed | Closed |
| t_{PHL} | Closed | Closed |
| t_{PZH} | Open | Closed |
| t_{PZL} | Closed | Open |
| t_{PHZ} | Closed | Closed |
| t_{PLZ} | Closed | Closed |



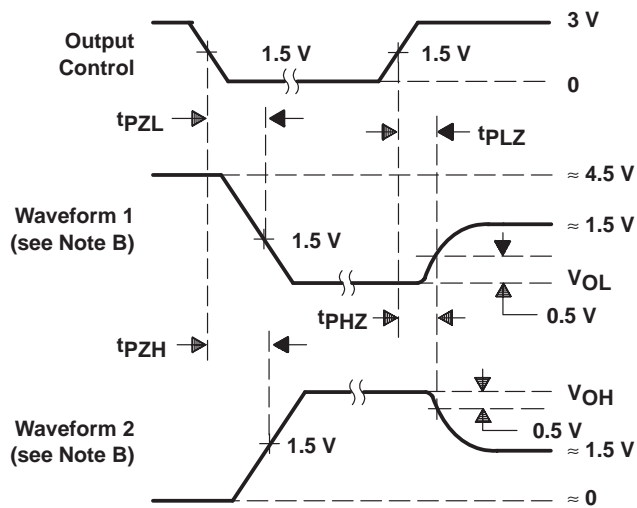
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74ALS29863DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS29863 | Samples |
| SN74ALS29863DWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS29863 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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