

## SNx4LV126A Quadruple Bus Buffer Gates With 3-State Outputs

### 1 Features

- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 6.5 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Ioff Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Servers
- Network Switch
- Electronic Point of Sales
- TV
- Set-Top-Box

### 3 Description

The 'LV126A quadruple bus buffer gates are designed for 2-V to 5.5-V  $V_{CC}$  operation.

These quadruple bus buffer gates are designed for 2-V to 5.5-V  $V_{CC}$  operation.

The 'LV126A devices feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

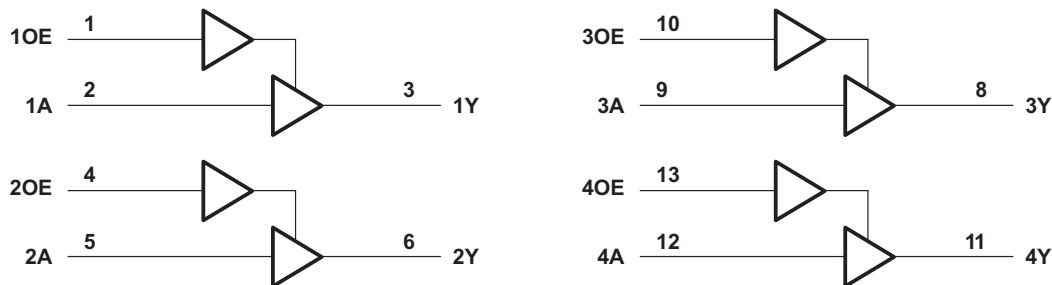
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)    |
|-------------|------------|--------------------|
| SN74LV126A  | SOIC (14)  | 3.91 mm × 8.65 mm  |
|             | SOP (14)   | 5.30 mm × 10.30 mm |
|             | SSOP (14)  | 5.30 mm × 6.20 mm  |
|             | TSSOP (14) | 4.40 mm × 5.00 mm  |
|             | TVSOP (14) | 4.40 mm × 3.60 mm  |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



## Table of Contents

|   |          |  |           |
|---|----------|--|-----------|
| <b>1 Features</b> .....   | <b>1</b> | <b>8 Detailed Description</b> .....                              | <b>9</b>  |
| <b>2 Applications</b> .....   | <b>1</b> | 8.1 Overview .....   | 9         |
| <b>3 Description</b> .....  | <b>1</b> | 8.2 Functional Block Diagram .....                               | 9         |
| <b>4 Revision History</b> .....   | <b>2</b> | 8.3 Feature Description .....                                    | 9         |
| <b>5 Pin Configuration and Functions</b> .....                                | <b>3</b> | 8.4 Device Functional Modes .....                                | 9         |
| <b>6 Specifications</b> .....   | <b>4</b> | <b>9 Application and Implementation</b> .....                    | <b>10</b> |
| 6.1 Absolute Maximum Ratings .....  | 4        | 9.1 Application Information .....                                | 10        |
| 6.2 ESD Ratings .....   | 4        | 9.2 Typical Application .....                                    | 10        |
| 6.3 Recommended Operating Conditions .....                                    | 4        | <b>10 Power Supply Recommendations</b> .....                     | <b>11</b> |
| 6.4 Thermal Information .....   | 5        | <b>11 Layout</b> .....   | <b>11</b> |
| 6.5 Electrical Characteristics .....  | 5        | 11.1 Layout Guidelines .....                                     | 11        |
| 6.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ ..... | 6        | 11.2 Layout Example .....  | 11        |
| 6.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ..... | 6        | <b>12 Device and Documentation Support</b> .....                 | <b>12</b> |
| 6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....   | 6        | 12.1 Related Links .....   | 12        |
| 6.9 Noise Characteristics for SN74LV126A .....                                | 7        | 12.2 Trademarks .....  | 12        |
| 6.10 Operating Characteristics .....  | 7        | 12.3 Electrostatic Discharge Caution .....                       | 12        |
| 6.11 Typical Characteristics .....  | 7        | 12.4 Glossary .....  | 12        |
| <b>7 Parameter Measurement Information</b> .....                              | <b>8</b> | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | <b>12</b> |

## 4 Revision History

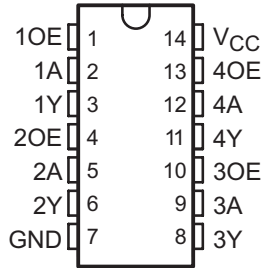
### Changes from Revision H (April 2005) to Revision I

Page

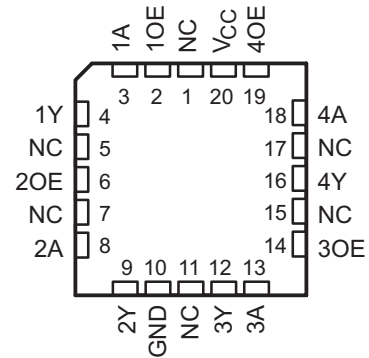
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section .....
- Updated operating free-air temperature maximum from 85°C to 125°C for SN74LV126A .....

## 5 Pin Configuration and Functions

SN54LV126A: J or W Package  
SN74LV126A: D, DB, DGV, NS, or PW Package  
(Top View)



SN54LV126A: FK Package  
(Top View)



A. NC – No internal connection

### Pin Functions

| PIN | I/O             | DESCRIPTION     |
|-----|-----------------|-----------------|
| 1   | 1OE             | Enable pin      |
| 2   | 1A              | Input 1         |
| 3   | 1Y              | Output 1        |
| 4   | 2OE             | Enable 2        |
| 5   | 2A              | Input 2         |
| 6   | 2Y              | Output 2        |
| 7   | GND             | GND             |
| 8   | 3Y              | Output 3        |
| 9   | 3A              | Input 3         |
| 10  | 3OE             | Enable 3        |
| 11  | 4Y              | Output 4        |
| 12  | 4A              | Input 4         |
| 13  | 4OE             | Enable 4        |
| 14  | V <sub>CC</sub> | V <sub>CC</sub> |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|           |   | MIN  | MAX              | UNIT |
|-----------|---|------|------------------|------|
| $V_{CC}$  | Supply voltage  | -0.5 | 7                | V    |
| $V_I$     | Input voltage <sup>(2)</sup>  | -0.5 | 7                | V    |
| $V_O$     | Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup> | -0.5 | 7                | V    |
| $V_O$     | Output voltage <sup>(2)(3)</sup>  | -0.5 | $V_{CC} + 0.5$ V | V    |
| $I_{IK}$  | Input clamp current, $V_I < 0$  |      | -20              | mA   |
| $I_{OK}$  | Output clamp current, $V_O < 0$   |      | -50              | mA   |
| $I_O$     | Continuous output current, $V_O = 0$ to $V_{CC}$                                      | -35  | 35               | mA   |
|           | Continuous current through $V_{CC}$ or GND  | -70  | 70               | mA   |
| $T_{stg}$ | Storage temperature   | -65  | 150              | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 5.5-V maximum.

### 6.2 ESD Ratings

|             |                         | VALUE  | UNIT |
|-------------|-------------------------|--|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | 2000 |
|             |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | 1000 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

 see <sup>(1)</sup>

|          |                           | MIN                     | MAX                 | UNIT     |
|----------|---------------------------|-------------------------|---------------------|----------|
| $V_{CC}$ | Supply voltage            | 2                       | 5.5                 | V        |
| $V_{IH}$ | High-level input voltage  | $V_{CC} = 2$ V          | 1.5                 | V        |
|          |                           | $V_{CC} = 2.3$ to 2.7 V | $V_{CC} \times 0.7$ |          |
|          |                           | $V_{CC} = 3$ to 3.6 V   | $V_{CC} \times 0.7$ |          |
|          |                           | $V_{CC} = 4.5$ to 5.5 V | $V_{CC} \times 0.7$ |          |
| $V_{IL}$ | Low-level input voltage   | $V_{CC} = 2$ V          | 0.5                 | V        |
|          |                           | $V_{CC} = 2.3$ to 2.7 V | $V_{CC} \times 0.3$ |          |
|          |                           | $V_{CC} = 3$ to 3.6 V   | $V_{CC} \times 0.3$ |          |
|          |                           | $V_{CC} = 4.5$ to 5.5 V | $V_{CC} \times 0.3$ |          |
| $V_I$    | Input voltage             | 0                       | 5.5                 | V        |
| $V_O$    | Output voltage            | High or low state       | 0                   | $V_{CC}$ |
|          |                           | 3-state                 | 0                   | 5.5      |
| $I_{OH}$ | High-level output current | $V_{CC} = 2$ V          | -50                 | µA       |
|          |                           | $V_{CC} = 2.3$ to 2.7 V | -2                  | mA       |
|          |                           | $V_{CC} = 3$ to 3.6 V   | -8                  |          |
|          |                           | $V_{CC} = 4.5$ to 5.5 V | -16                 |          |

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

## Recommended Operating Conditions (continued)

 see <sup>(1)</sup>

|                     |                                    | MIN                                   | MAX | UNIT          |                    |
|---------------------|------------------------------------|---------------------------------------|-----|---------------|--------------------|
| $I_{OL}$            | Low-level output current           | $V_{CC} = 2\text{ V}$                 | 50  | $\mu\text{A}$ |                    |
|                     |                                    | $V_{CC} = 2.3\text{ to }2.7\text{ V}$ | 2   | mA            |                    |
|                     |                                    | $V_{CC} = 3\text{ to }3.6\text{ V}$   | 8   |               |                    |
|                     |                                    | $V_{CC} = 4.5\text{ to }5.5\text{ V}$ | 16  |               |                    |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 2.3\text{ to }2.7\text{ V}$ | 200 | ns/V          |                    |
|                     |                                    | $V_{CC} = 3\text{ to }3.6\text{ V}$   | 100 |               |                    |
|                     |                                    | $V_{CC} = 4.5\text{ to }5.5\text{ V}$ | 20  |               |                    |
| $T_A$               | Operating free-air temperature     | SN54LV126A                            | –55 | 125           | $^{\circ}\text{C}$ |
|                     |                                    | SN74LV126A                            | –40 | 125           |                    |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | D   | DB   | DGV   | NS    | PW   | UNIT  |                             |
|-------------------------------|---|------|-------|-------|------|-------|-----------------------------|
|                               | 14 PINS   |      |       |       |      |       |                             |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance <sup>(2)</sup> | 92.7 | 105.0 | 127.6 | 89.6 | 119.8 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta JC(\text{top})}$   | Junction-to-case (top) thermal resistance             | 54.1 | 57.5  | 50.7  | 47.2 | 48.6  |                             |
| $R_{\theta JB}$               | Junction-to-board thermal resistance                  | 47.0 | 52.3  | 60.5  | 48.4 | 61.5  |                             |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter            | 18.9 | 19.1  | 6.1   | 14.0 | 5.7   |                             |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter          | 46.7 | 51.8  | 59.8  | 48.1 | 61.0  |                             |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                  | $V_{CC}$   | MIN            | TYP | MAX           | UNIT |
|-----------|----------------------------------|------------|----------------|-----|---------------|------|
| $V_{OH}$  | $I_{OH} = -50\ \mu\text{A}$      | 2 to 5.5 V | $V_{CC} - 0.1$ |     | V             |      |
|           | $I_{OH} = -2\ \text{mA}$         | 2.3 V      | 2              |     |               |      |
|           | $I_{OH} = -8\ \text{mA}$         | 3 V        | 2.48           |     |               |      |
|           | $I_{OH} = -16\ \text{mA}$        | 4.5 V      | 3.8            |     |               |      |
| $V_{OL}$  | $I_{OL} = 50\ \mu\text{A}$       | 2 to 5.5 V | 0.1            |     | V             |      |
|           | $I_{OL} = 2\ \text{mA}$          | 2.3 V      | 0.4            |     |               |      |
|           | $I_{OL} = 8\ \text{mA}$          | 3 V        | 0.44           |     |               |      |
|           | $I_{OL} = 16\ \text{mA}$         | 4.5 V      | 0.55           |     |               |      |
| $I_I$     | $V_I = 5.5\ \text{V}$ or GND     | 0 to 5.5 V | $\pm 1$        |     | $\mu\text{A}$ |      |
| $I_{OZ}$  | $V_O = V_{CC}$ or GND            | 5.5 V      | $\pm 5$        |     | $\mu\text{A}$ |      |
| $I_{CC}$  | $V_I = V_{CC}$ or GND, $I_O = 0$ | 5.5 V      | 20             |     | $\mu\text{A}$ |      |
| $I_{off}$ | $V_I$ or $V_O = 0$ to 5.5 V      | 0          | 5              |     | $\mu\text{A}$ |      |
| $C_i$     | $V_I = V_{CC}$ or GND            | 3.3 V      | 1.6            |     | pF            |      |

## 6.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER   | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |                     |                  | MIN                 | MAX | UNIT |
|-------------|--------------|-------------|----------------------|--------------------------|---------------------|------------------|---------------------|-----|------|
|             |              |             |                      | MIN                      | TYP                 | MAX              |                     |     |      |
| $t_{pd}$    | A            | Y           | $C_L = 15\text{ pF}$ | 7.1 <sup>(1)</sup>       | 13 <sup>(1)</sup>   | 1 <sup>(2)</sup> | 15.5 <sup>(2)</sup> | ns  |      |
| $t_{en}$    | OE           |             |                      | 7.4 <sup>(1)</sup>       | 13 <sup>(1)</sup>   | 1 <sup>(2)</sup> | 15.5 <sup>(2)</sup> |     |      |
| $t_{dis}$   | OE           |             |                      | 5.7 <sup>(1)</sup>       | 14.7 <sup>(1)</sup> | 1 <sup>(2)</sup> | 17 <sup>(2)</sup>   |     |      |
| $t_{pd}$    | A            | Y           | $C_L = 50\text{ pF}$ | 9.2                      | 16.5                | 1                | 18.5                | ns  |      |
| $t_{en}$    | OE           |             |                      | 9.5                      | 16.5                | 1                | 18.5                |     |      |
| $t_{dis}$   | OE           |             |                      | 8.1                      | 18.2                | 15               | 20.5                |     |      |
| $t_{sk(o)}$ |              |             |                      |                          | 2                   |                  | 2 <sup>(3)</sup>    |     |      |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) This note applies to SN54LV126A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) Value applies for SN74LV126A only

## 6.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER   | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |                    |                  | MIN                 | MAX | UNIT |
|-------------|--------------|-------------|----------------------|--------------------------|--------------------|------------------|---------------------|-----|------|
|             |              |             |                      | MIN                      | TYP                | MAX              |                     |     |      |
| $t_{pd}$    | A            | Y           | $C_L = 15\text{ pF}$ | 5 <sup>(1)</sup>         | 8 <sup>(1)</sup>   | 1 <sup>(2)</sup> | 9.5 <sup>(2)</sup>  | ns  |      |
| $t_{en}$    | OE           |             |                      | 5.1 <sup>(1)</sup>       | 8 <sup>(1)</sup>   | 1 <sup>(2)</sup> | 9.5 <sup>(2)</sup>  |     |      |
| $t_{dis}$   | OE           |             |                      | 4.4 <sup>(1)</sup>       | 9.7 <sup>(1)</sup> | 1 <sup>(2)</sup> | 11.5 <sup>(2)</sup> |     |      |
| $t_{pd}$    | A            | Y           | $C_L = 50\text{ pF}$ | 6.4                      | 11.5               | 1                | 13                  | ns  |      |
| $t_{en}$    | OE           |             |                      | 6.6                      | 11.5               | 1                | 13                  |     |      |
| $t_{dis}$   | OE           |             |                      | 6.1                      | 13.2               | 1                | 15                  |     |      |
| $t_{sk(o)}$ |              |             |                      |                          | 1.5                |                  | 1.5 <sup>(3)</sup>  |     |      |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) This note applies to SN54LV126A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) Value applies for SN74LV126A only

## 6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER   | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |                    |                  | MIN                | MAX | UNIT |
|-------------|--------------|-------------|----------------------|--------------------------|--------------------|------------------|--------------------|-----|------|
|             |              |             |                      | MIN                      | TYP                | MAX              |                    |     |      |
| $t_{pd}$    | A            | Y           | $C_L = 15\text{ pF}$ | 3.5 <sup>(1)</sup>       | 5.5 <sup>(1)</sup> | 1 <sup>(2)</sup> | 6.5 <sup>(2)</sup> | ns  |      |
| $t_{en}$    | OE           |             |                      | 3.6 <sup>(1)</sup>       | 5.1 <sup>(1)</sup> | 1 <sup>(2)</sup> | 6 <sup>(2)</sup>   |     |      |
| $t_{dis}$   | OE           |             |                      | 3.3 <sup>(1)</sup>       | 6.8 <sup>(1)</sup> | 1 <sup>(2)</sup> | 8 <sup>(2)</sup>   |     |      |
| $t_{pd}$    | A            | Y           | $C_L = 50\text{ pF}$ | 4.6                      | 7.5                | 1                | 8.5                | ns  |      |
| $t_{en}$    | OE           |             |                      | 4.6                      | 7.1                | 1                | 8                  |     |      |
| $t_{dis}$   | OE           |             |                      | 4.3                      | 8.8                | 1                | 10                 |     |      |
| $t_{sk(o)}$ |              |             |                      |                          | 1                  |                  | 1 <sup>(3)</sup>   |     |      |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) This note applies to SN54LV126A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) This values applies for SN74LV126A only

### 6.9 Noise Characteristics for SN74LV126A

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see <sup>(1)</sup>)

| PARAMETER   |  | MIN  | TYP  | MAX  | UNIT |
|-------------|--|------|------|------|------|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ |      | 0.3  | 0.8  | V    |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ |      | -0.2 | -0.8 |      |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ |      | 3.1  |      |      |
| $V_{IH(D)}$ | High-level dynamic input voltage       | 2.31 |      |      |      |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |      |      | 0.97 |      |

(1) Characteristics are for surface-mount packages only.

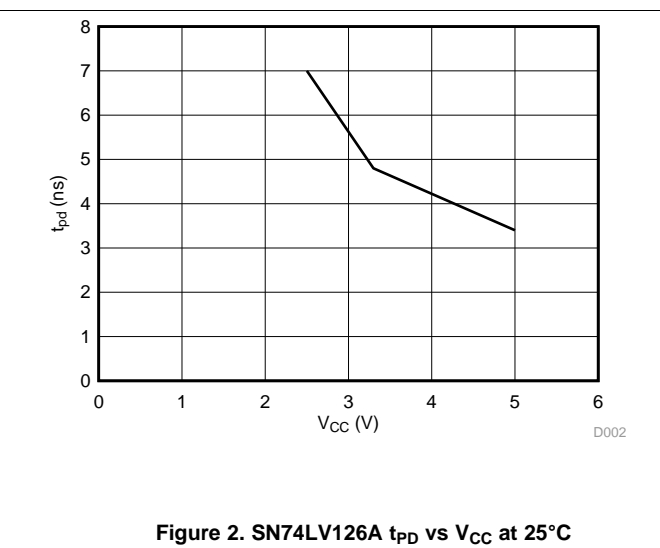
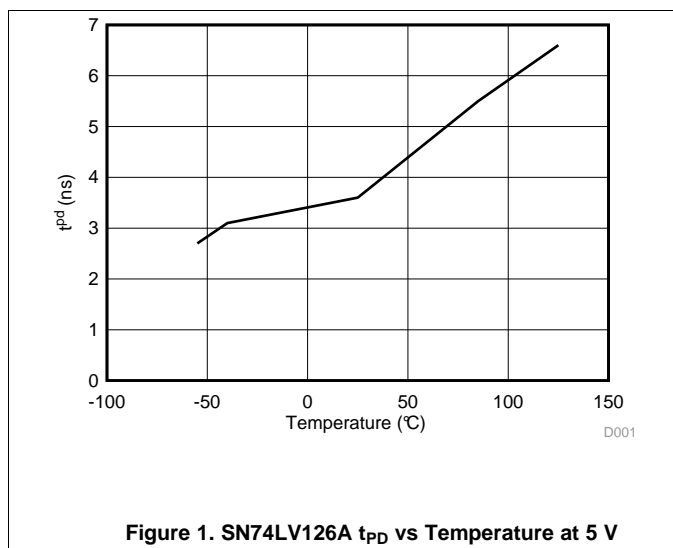
### 6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

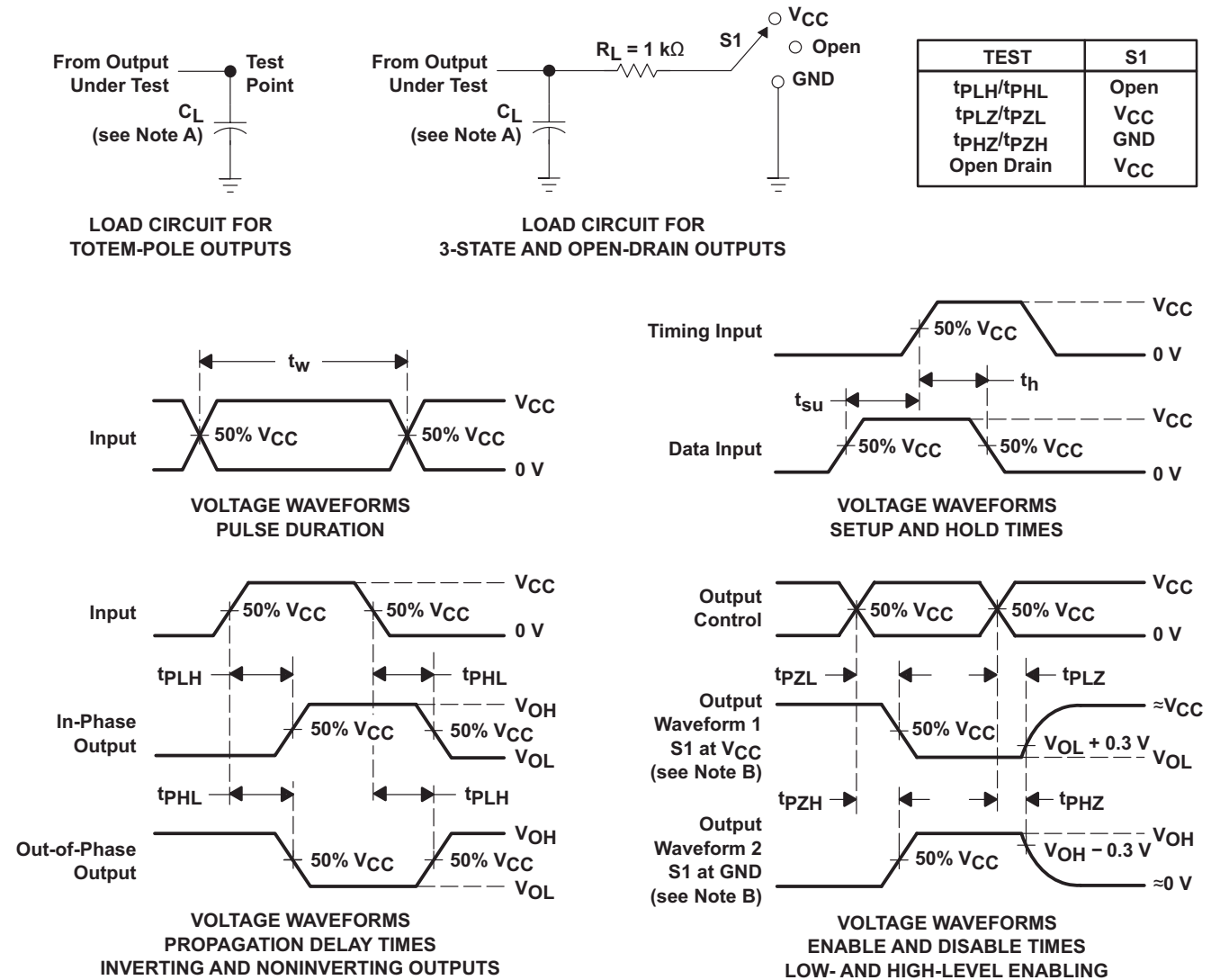
| PARAMETER |                               | TEST CONDITIONS  | $V_{CC}$ | TYP  | UNIT |
|-----------|-------------------------------|--|----------|------|------|
| $C_{pd}$  | Power dissipation capacitance | Outputs enable; $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$ | 3.3 V    | 14.4 | pF   |
|           |                               |  | 5 V      | 15.9 |      |

### 6.11 Typical Characteristics

TBD



## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

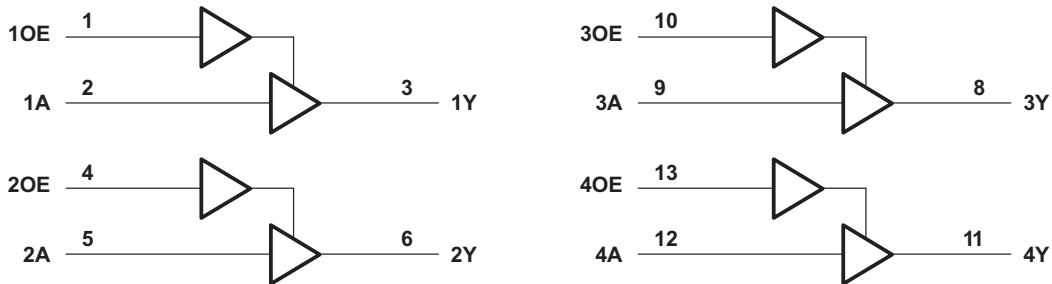


## 8 Detailed Description

### 8.1 Overview

The SN74LV126A devices are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### 8.2 Functional Block Diagram



A. Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

**Figure 4. Logic Diagram (Positive Logic)**

### 8.3 Feature Description

- Wide operating voltage range, operates from 2 to 5.5 V
- Allows down voltage translation, inputs accept voltages to 5.5 V
- Ioff supports live insertion, partial power down mode, and back drive protection

### 8.4 Device Functional Modes

**Table 1. Function Table  
(Each Buffer)**

| INPUTS                 |   | OUTPUT<br>Y |
|------------------------|---|-------------|
| $\overline{\text{OE}}$ | A |             |
| L                      | H | H           |
| L                      | L | L           |
| H                      | X | Z           |

## 9 Application and Implementation

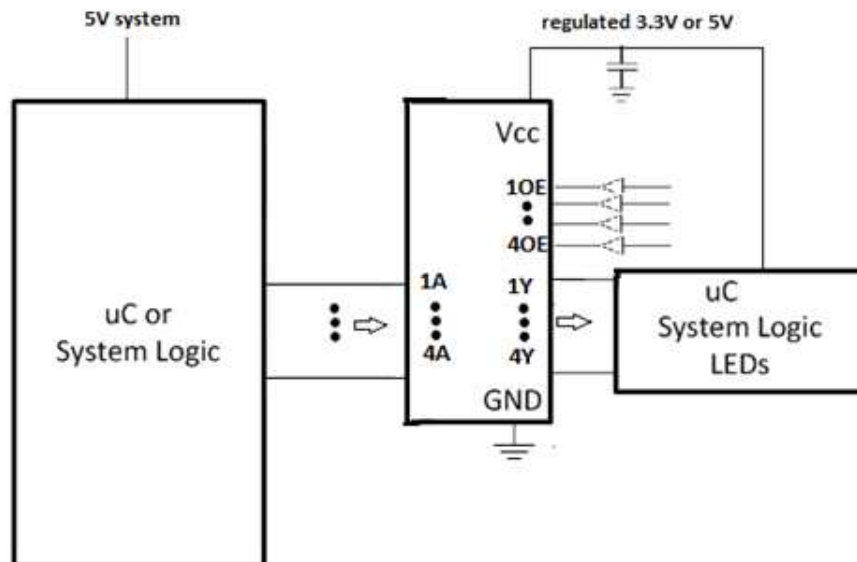
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LV126A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates minimize overshoot and undershoot on the outputs. The inputs are 5.5-V tolerant at any valid  $V_{CC}$  making Ideal for translating down to  $V_{CC}$ .

### 9.2 Typical Application



**Figure 5. Typical Application Schematic**

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

1. Recommended input conditions
  - Rise time and fall time specs see  $(\Delta t/\Delta V)$  in [Recommended Operating Conditions](#).
  - Specified High and low levels. See  $(V_{IH}$  and  $V_{IL})$  in [Recommended Operating Conditions](#).
2. Recommend output conditions
  - Load currents should not exceed 35 mA per output and 70 mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

## Typical Application (continued)

### 9.2.3 Application Curve

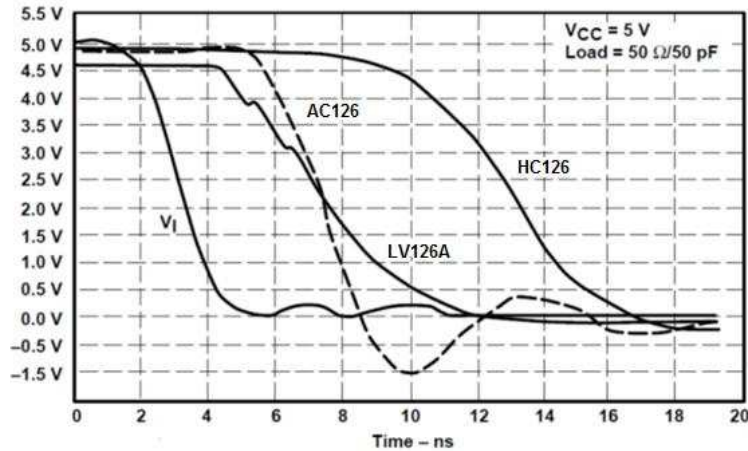


Figure 6. Switching Characteristics Comparison

## 10 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in [Recommended Operating Conditions](#). Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended and if there are multiple  $V_{CC}$  terminals then .01 or .022  $\mu\text{F}$  is recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they also cannot float when disabled.

### 11.2 Layout Example

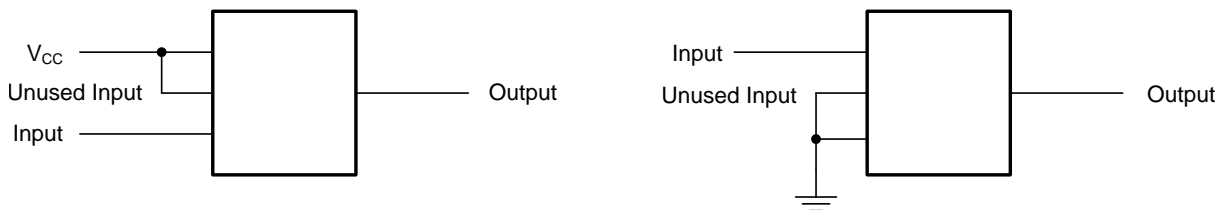


Figure 7. Layout Recommendation

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS      | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54LV126A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| SN74LV126A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12.2 Trademarks

All trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LV126AD      | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV126A                  | <a href="#">Samples</a> |
| SN74LV126ADBR    | ACTIVE        | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV126A                  | <a href="#">Samples</a> |
| SN74LV126ADG4    | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV126A                  | <a href="#">Samples</a> |
| SN74LV126ADGVR   | ACTIVE        | TVSOP        | DGV             | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV126A                  | <a href="#">Samples</a> |
| SN74LV126ADR     | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV126A                  | <a href="#">Samples</a> |
| SN74LV126ADRG4   | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV126A                  | <a href="#">Samples</a> |
| SN74LV126ANSR    | ACTIVE        | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | 74LV126A                | <a href="#">Samples</a> |
| SN74LV126APW     | ACTIVE        | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV126A                  | <a href="#">Samples</a> |
| SN74LV126APWR    | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV126A                  | <a href="#">Samples</a> |
| SN74LV126APWRG4  | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV126A                  | <a href="#">Samples</a> |
| SN74LV126APWT    | ACTIVE        | TSSOP        | PW              | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV126A                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV126ADBR  | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 6.6     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV126ADGVR | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV126ADR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LV126ANSR  | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV126APWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV126APWT  | TSSOP        | PW              | 14   | 250  | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV126ADBR  | SSOP         | DB              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LV126ADGVR | TVSOP        | DGV             | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74LV126ADR   | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74LV126ANSR  | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LV126APWR  | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74LV126APWT  | TSSOP        | PW              | 14   | 250  | 367.0       | 367.0      | 35.0        |



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

|                              |  |
|------------------------------|--|
| Audio                        | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                               |
| Amplifiers                   | <a href="http://amplifier.ti.com">amplifier.ti.com</a>                               |
| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>   |
| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>   |
| Clocks and Timers            | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                        | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt                   | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers             | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |  |
|-------------------------------|--|
| Automotive and Transportation | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| Communications and Telecom    | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| Space, Avionics and Defense   | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| Video and Imaging             | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)