SN74LV4052A Dual 4-Channel Analog Multiplexers and Demultiplexers

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Fast Switching
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Extremely Low Input Current
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22:
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Telecomunications
- Infotainment
- Signal Gating and Isolation
- Home Appliances
- Programmable Logic Circuits
- Modulation and Demodulation

3 Description

The SN74LV4052A device is a dual, 4-channel CMOS analog multiplexer and demultiplexer that is designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV4052A device handles both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV4052AD	SOIC (16)	9.90 mm × 3.91 mm
SN74LV4052ADB	SSOP (16)	6.20 mm × 5.30 mm
SN74LV4052ADGV	TVSOP (16)	3.60 mm × 4.40 mm
SN74LV4052ANS	SO (16)	10.30 mm × 5.30 mm
SN74LV4052AN	PDIP (16)	19.30 mm × 6.35 mm
SN74LV4052APW	TSSOP (16)	5.00 mm × 4.40 mm
SN74LV4052ARGY	VQFN (16)	4.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

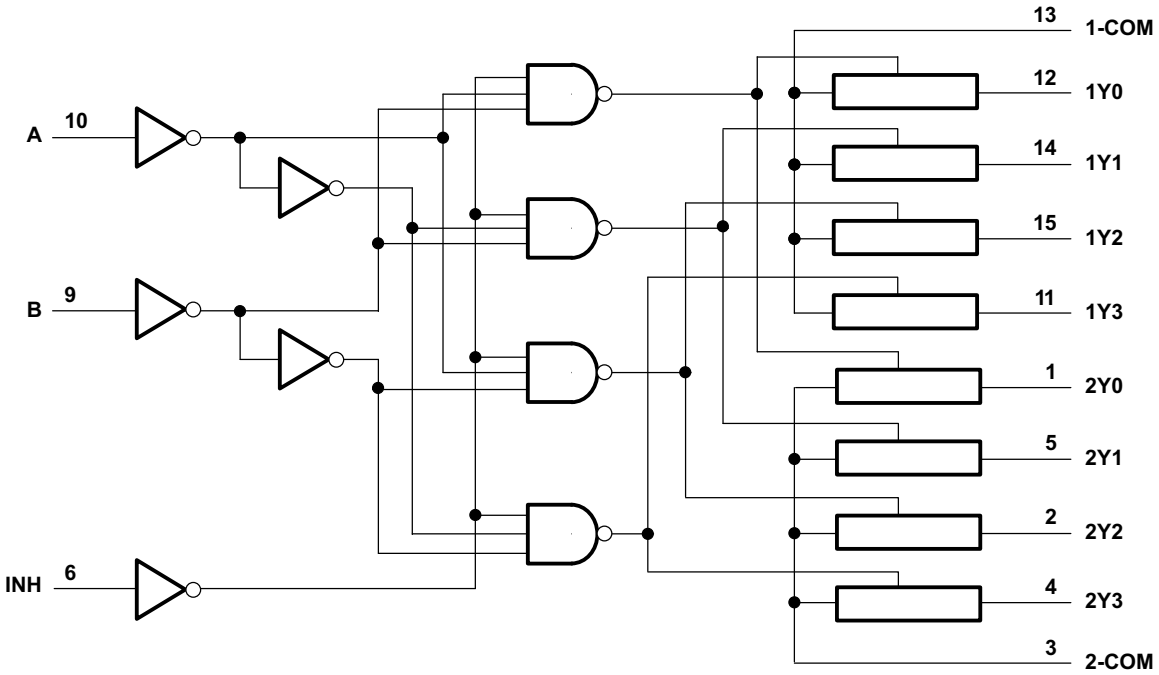


Table of Contents

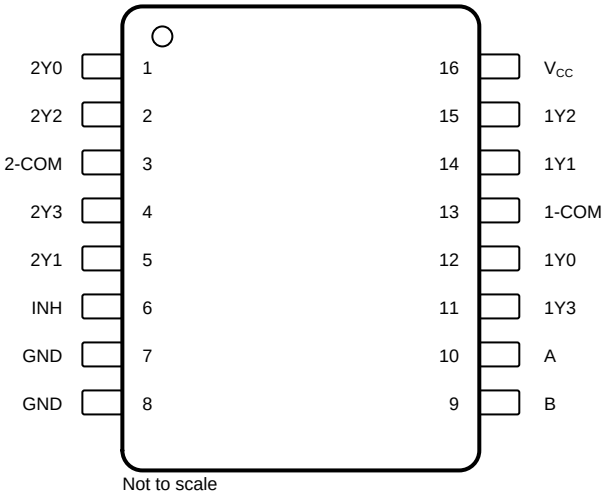
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (October 2012) to Revision K	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet	1
• Deleted SN54LV4052A from data sheet	1
• Changed Package thermal impedance, $R_{\theta JA}$, values in the *Thermal Information* table From: 73 To: 90.9 (D), From: 82 To: 102.8 (DB), From: 120 To: 125.7 (DGV), From: 67 To: 54.8 (N), From: 64 To: 89.7 (NS), From: 108 To: 113.2 (PW), and From: 39 To: 48.9 (RGY)	5

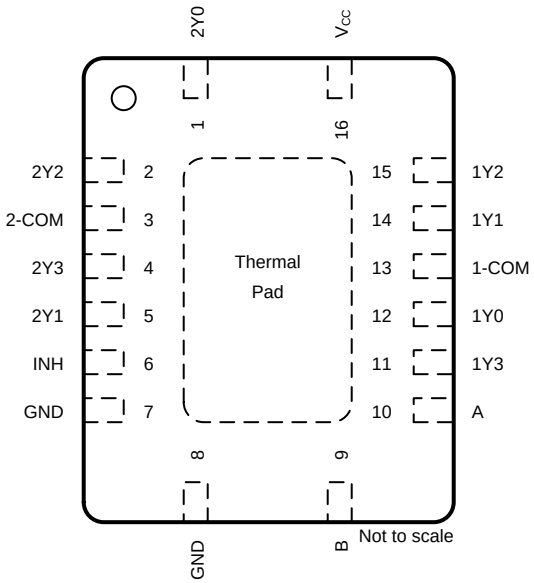
5 Pin Configuration and Functions

D, DB, DGV, N, NS, or PW Package
16-Pin SOIC, SSOP, TVSOP, SO, PDIP, or TSSOP
Top View



Not to scale

RGY Package
16-Pin VQFN With Thermal Pad
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	2Y0	I/O	Port 2 channel 0
2	2Y2	I/O	Port 2 channel 2
3	2-COM	I/O	Port 2 common channel
4	2Y3	I/O	Port 2 channel 3
5	2Y1	I/O	Port 2 channel 1
6	INH	I	Inhibit input
7	GND	—	Device ground
8	GND	—	Device ground
9	B	I	Logic input selector B
10	A	I	Logic input selector A
11	1Y3	I/O	Port 1 channel 3
12	1Y0	I/O	Port 1 channel 0
13	1-COM	I/O	Port 1 common channel
14	1Y1	I/O	Port 1 channel 1
15	1Y2	I/O	Port 1 channel 2
16	V_{CC}	—	Device power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	7	V
Input voltage, V_I(2)		–0.5	7	V
Switch I/O voltage, V_{IO}(2)(3)		–0.5	V_{CC} + 0.5	V
Input clamp current, I_{IK}	V_I < 0		–20	mA
I/O diode current, I_{IOK}	V_{IO} < 0 and V_{IO} > V_{CC}		50	mA
Switch through current, I_T	V_{IO} = 0 to V_{CC}		±25	mA
Continuous current through V_{CC} or GND			±50	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Tested on D package

6.3 Recommended Operating Conditions

see(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2(2)	5.5	V
V_{IH}	High-level input voltage (control inputs)	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage (control inputs)	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Control input voltage		0	5.5	V
V_{IO}	Input or output voltage		0	V_{CC}	V
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs* (SCBA004).
(2) With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. TI recommends that only digital signals be transmitted at these low supply voltages.

6.4 Thermal Information

THERMAL METRIC[1]		SN74LV4052A							UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.9	102.8	125.7	54.8	89.7	113.2	48.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	53.3	50.9	42.1	48.1	48.2	46.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48	53.4	57.5	34.8	50.1	58.3	25	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.6	16.5	5.6	26.9	16.7	6.3	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.8	52.9	57	34.7	49.8	57.8	25	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	11.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
r_{on}	On-state switch resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL} (see Figure 2)	V_{CC} = 2.3 V	T_A = 25°C		43	180	Ω
				T_A = –40 to 85°C			225	
			V_{CC} = 3 V	T_A = 25°C		34	150	
				T_A = –40 to 85°C			190	
			V_{CC} = 4.5 V	T_A = 25°C		25	75	
				T_A = –40 to 85°C			100	
$r_{on(p)}$	Peak on-state resistance	I_T = 2 mA, V_I = V_{CC} to GND, V_{INH} = V_{IL}	V_{CC} = 2.3 V	T_A = 25°C		133	500	Ω
				T_A = –40 to 85°C			600	
			V_{CC} = 3 V	T_A = 25°C		63	180	
				T_A = –40 to 85°C			225	
			V_{CC} = 4.5 V	T_A = 25°C		35	100	
				T_A = –40 to 85°C			125	
Δr_{on}	Difference in on-state resistance between switches	I_T = 2 mA, V_I = V_{CC} to GND, V_{INH} = V_{IL}	V_{CC} = 2.3 V	T_A = 25°C		1.5	30	Ω
				T_A = –40 to 85°C			40	
			V_{CC} = 3 V	T_A = 25°C		1.1	20	
				T_A = –40 to 85°C			30	
			V_{CC} = 4.5 V	T_A = 25°C		0.7	15	
				T_A = –40 to 85°C			20	
I_I	Control input current	V_I = 5.5 V or GND, and V_{CC} = 0 to 5.5 V		T_A = 25°C			±0.1	µA
				T_A = –40 to 85°C			±1	
$I_{S(off)}$	OFF-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_{INH} = V_{IH} , and V_{CC} = 5.5 V (see Figure 3)		T_A = 25°C			±0.1	µA
				T_A = –40 to 85°C			±1	
$I_{S(on)}$	ON-state switch leakage current	V_I = V_{CC} or GND, V_{INH} = V_{IL}, and V_{CC} = 5.5 V (see Figure 4)		T_A = 25°C			±0.1	µA
				T_A = –40 to 85°C			±1	
I_{CC}	Supply current	V_I = V_{CC} or GND, V_{CC} = 5.5 V, and T_A = –40 to 85°C					20	µA
C_{IC}	Control input capacitance	f = 10 MHz, V_{CC} = 3.3 V, and T_A = 25°C				2.1		pF
C_{IS}	Common terminal capacitance	V_{CC} = 3.3 V and T_A = 25°C				13.1		pF
C_{OS}	Switch terminal capacitance	V_{CC} = 3.3 V and T_A = 25°C				5.6		pF
C_F	Feedthrough capacitance	V_{CC} = 3.3 V and T_A = 25°C				0.5		pF

6.6 Switching Characteristics: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range and V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 15 pF (see Figure 5)	T_A = 25°C		1.9	10	ns
					T_A = –40 to 85°C			16	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 15 pF (seeFigure 6)	T_A = 25°C		8	18	ns
					T_A = –40 to 85°C			23	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 15 pF (see Figure 6)	T_A = 25°C		8.3	18	ns
					T_A = –40 to 85°C			23	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 50 pF (see Figure 5)	T_A = 25°C		3.8	12	ns
					T_A = –40 to 85°C			18	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		9.4	28	ns
					T_A = –40 to 85°C			35	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		12.4	28	ns
					T_A = –40 to 85°C			35	

6.7 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range and V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 15 pF (see Figure 5)	T_A = 25°C		1.2	6	ns
					T_A = –40 to 85°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 15 pF (seeFigure 6)	T_A = 25°C		5.7	12	ns
					T_A = –40 to 85°C			15	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 15 pF (see Figure 6)	T_A = 25°C		6.6	12	ns
					T_A = –40 to 85°C			15	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 50 pF (see Figure 5)	T_A = 25°C		2.5	9	ns
					T_A = –40 to 85°C			12	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		6.7	20	ns
					T_A = –40 to 85°C			25	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		9.5	20	ns
					T_A = –40 to 85°C			25	

6.8 Switching Characteristics: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range and V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 15 pF (see Figure 5)	T_A = 25°C		0.7	4	ns
					T_A = –40 to 85°C			7	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 15 pF (seeFigure 6)	T_A = 25°C		4	8	ns
					T_A = –40 to 85°C			10	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 15 pF (see Figure 6)	T_A = 25°C		5	8	ns
					T_A = –40 to 85°C			10	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 50 pF (see Figure 5)	T_A = 25°C		1.5	6	ns
					T_A = –40 to 85°C			8	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		4.7	14	ns
					T_A = –40 to 85°C			18	

Switching Characteristics: V_{CC} = 5 V ± 0.5 V (continued)

over recommended operating free-air temperature range and V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		6.9	14	ns
					T_A = –40 to 85°C			18	

6.9 Switching Characteristics: Analog

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)(1)	V_{CC} = 2.3 V		30		MHz
				V_{CC} = 3 V		35		
				V_{CC} = 4.5 V		50		
Crosstalk (between any switches)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 8)(2)	V_{CC} = 2.3 V		–45		dB
				V_{CC} = 3 V		–45		
				V_{CC} = 4.5 V		–45		
Crosstalk (control input to signal output)	INH	COM or Y	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	V_{CC} = 2.3 V		20		mV
				V_{CC} = 3 V		35		
				V_{CC} = 4.5 V		65		
Feedthrough attenuation (switch off)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 10)(2)	V_{CC} = 2.3 V		–45		dB
				V_{CC} = 3 V		–45		
				V_{CC} = 4.5 V		–45		
Sine-wave distortion	COM or Y	Y or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 11)	V_I = 2 V_{p-p} and V_{CC} = 2.3 V		0.1%		
				V_I = 2.5 V_{p-p} and V_{CC} = 3 V		0.1%		
				V_I = 4 V_{p-p} and V_{CC} = 4.5 V		0.1%		

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase fin frequency until dB meter reads –3 dB.
(2) Adjust f_{in} voltage to obtain 0 dBm at input.

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF and f = 10 MHz	11.8	pF

6.11 Typical Characteristics

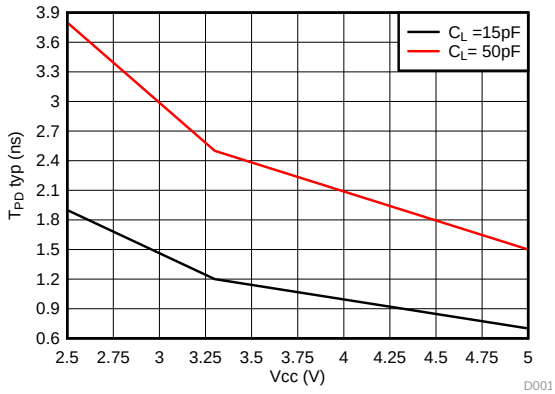


Figure 1. Typical Propagation Delay vs V_{cc}

7 Parameter Measurement Information

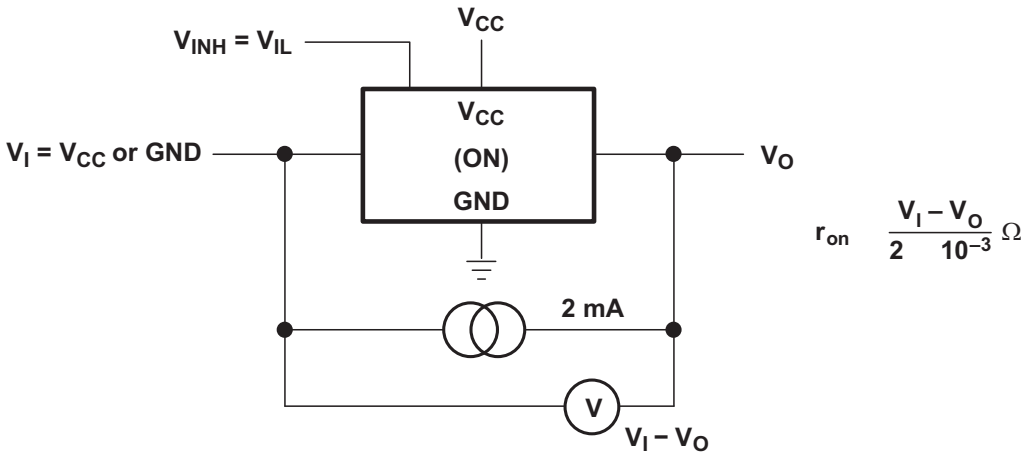
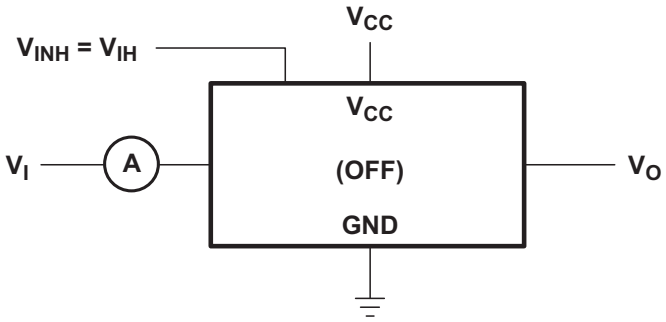
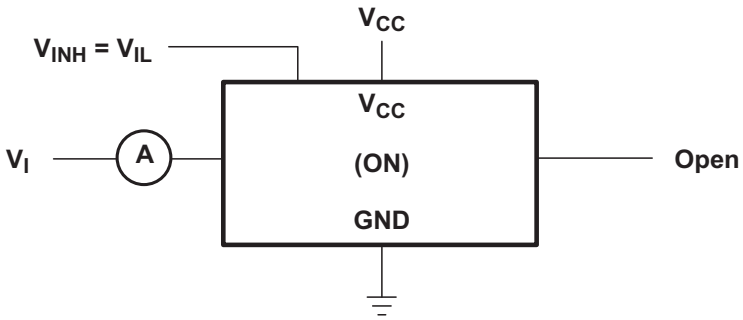


Figure 2. ON-State Resistance Test Circuit



Condition 1: V_I = 0, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = 0

Figure 3. OFF-State Switch Leakage-Current Test Circuit



$V_I = V_{CC}$ or GND

Figure 4. ON-State Switch Leakage-Current Test Circuit

Parameter Measurement Information (continued)

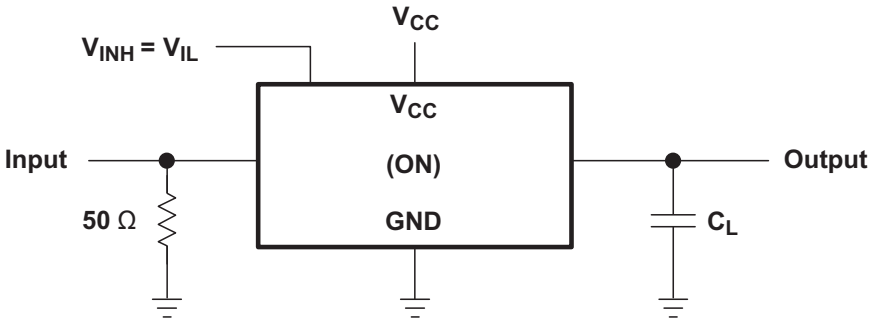
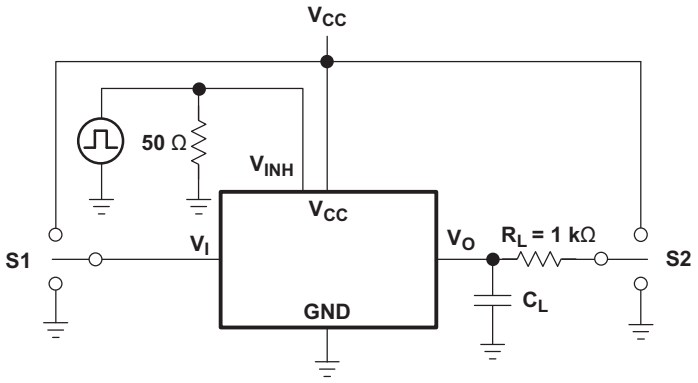
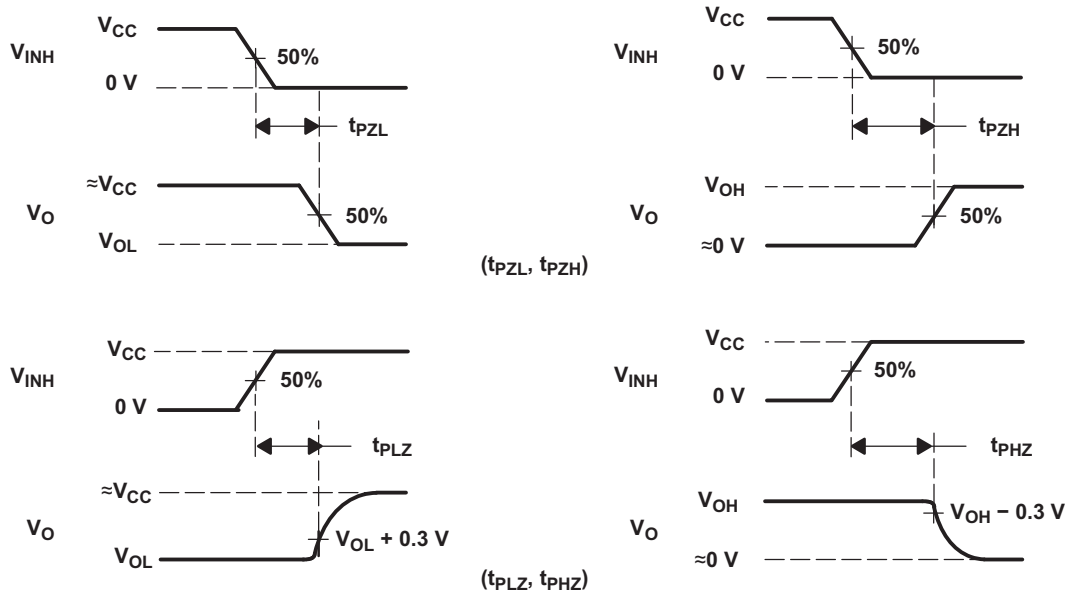


Figure 5. Propagation Delay Time, Signal Input to Signal Output



TEST	S1	S2
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	GND V_{CC}	V_{CC} GND

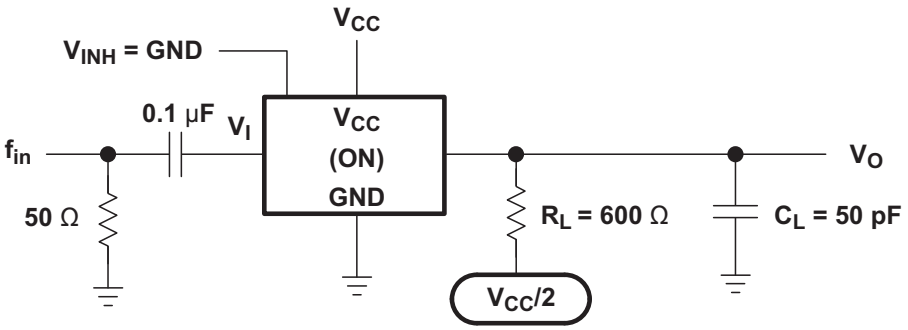
TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 6. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

Parameter Measurement Information (continued)



NOTE A: f_{in} is a sine wave.

Figure 7. Frequency Response (Switch ON)

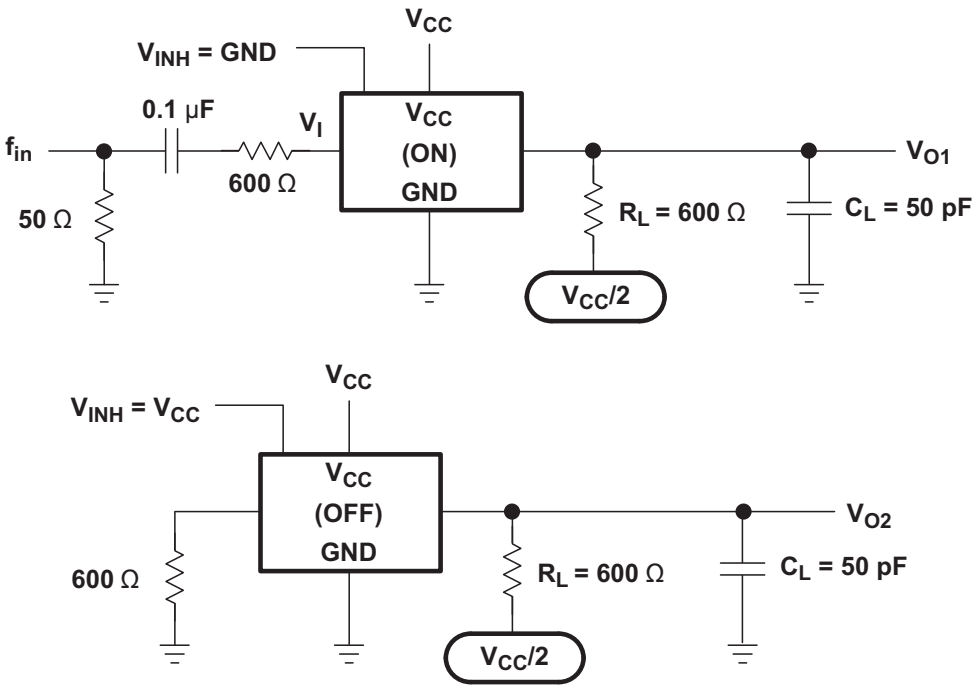


Figure 8. Crosstalk Between Any Two Switches

Parameter Measurement Information (continued)

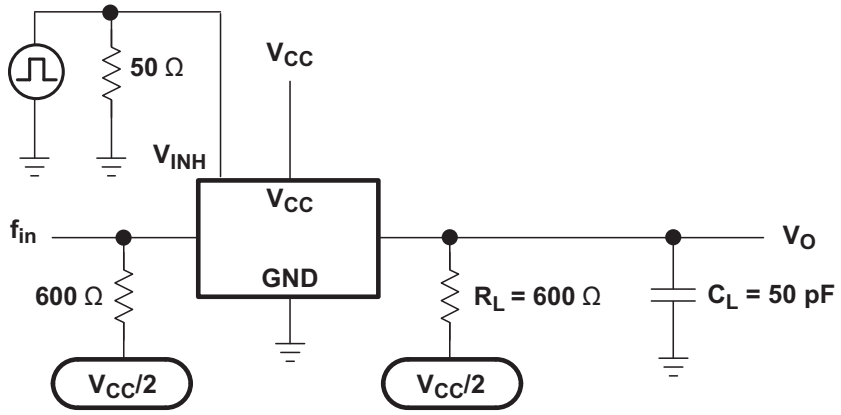


Figure 9. Crosstalk Between Control Input and Switch Output

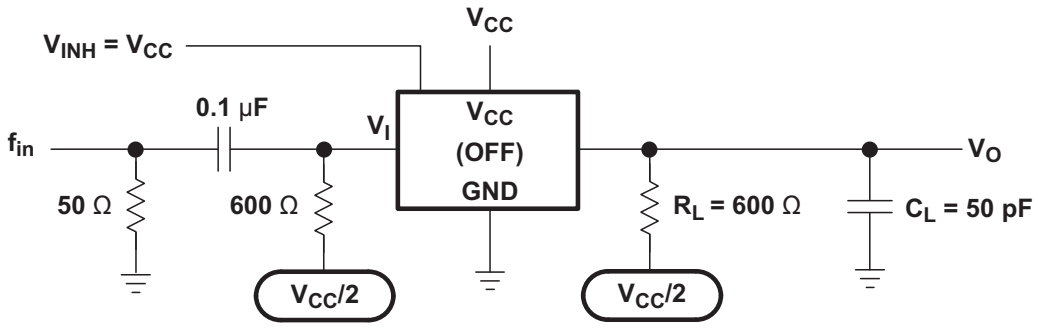


Figure 10. Feedthrough Attenuation (Switch OFF)

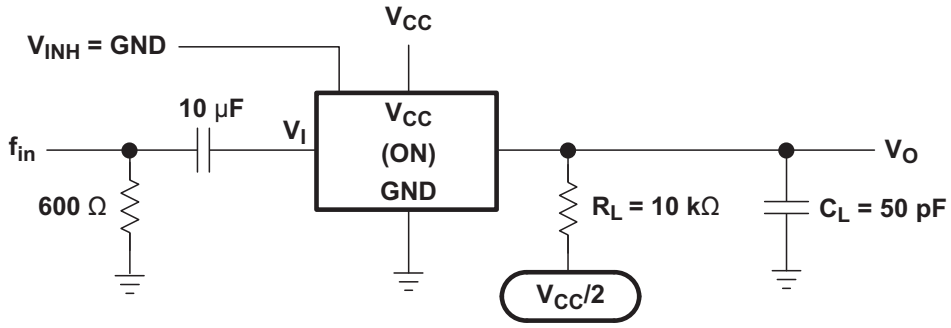


Figure 11. Sine-Wave Distortion

8 Detailed Description

8.1 Overview

The SN74LV4052A device is a dual, 4-channel CMOS analog multiplexer and demultiplexer that is designed for 2-V to 5.5-V V_{CC} operation. It has low input current consumption at the digital input pins and low crosstalk between switches. The active low Inhibit (INH) tri-state all the channels when high and when low, depending on the A and B inputs, one of the four independent input/outputs (nY0 - nY3) connects to the COM channel. The SN74LV4052A is available in multiple package options including TSSOP (PW) and QFN (RGY).

8.2 Functional Block Diagram

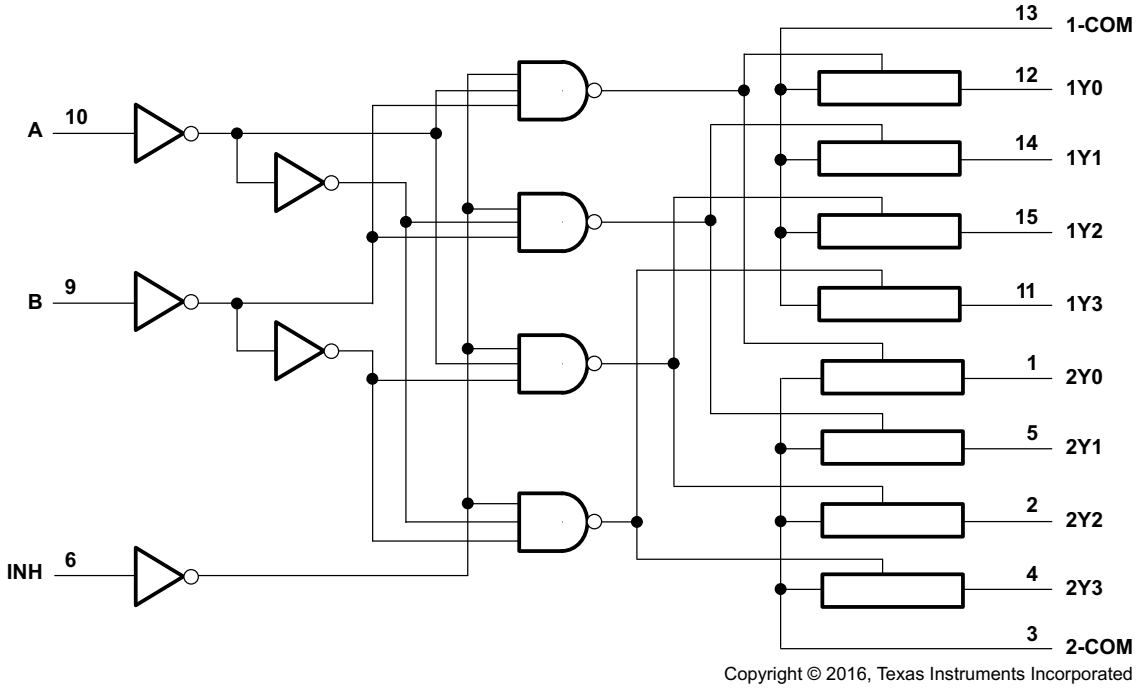


Figure 12. Logic Diagram (Positive Logic)

8.3 Feature Description

- The SN74LV4052A operates from 2-V to 5.5-V V_{CC} with extremely low input current consumption at the CMOS input pins of A, B and INH.
- The SN74LV4052A enables fast switching with low crosstalk between the switches. 5.5 V peak level bidirectional transmission allowed with the either analog or digital signals.

8.4 Device Functional Modes

Table 1 lists the functional modes of SN74LV4052A.

Table 1. Function Table

INPUTS			ON CHANNELS
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Typical applications for the SN74LV4052A include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

9.2 Typical Application

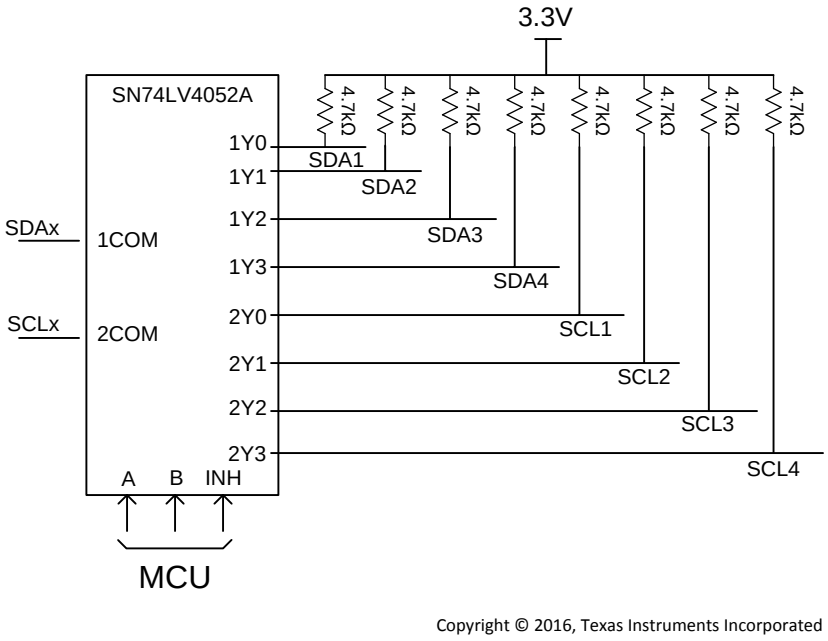


Figure 13. Typical I^2C Multiplexing Application

9.2.1 Design Requirements

Designing with the SN74LV4052A device requires a stable input voltage between 2 V and 5.5 V (see *Recommended Operating Conditions* for details). Another important design consideration are the characteristics of the signal being multiplexed which ensures no important information is lost due to timing or incompatibility with this device.

9.2.2 Detailed Design Procedure

The SN74LV4052A dual 1- to 4-channel multiplexer is ideal for I^2C selection. The I^2C data and clock lines are selected using A,B select lines from the MCU. The pullup resistors are selected based on the capability of the driver. Low pullup resistor results in faster rise time; however, it generates additional current during the low state into the driver. See to the *Recommended Operating Conditions* of the datasheet for the input transition rates (V_{IH} and V_{IL}) of the CMOS inputs.

Typical Application (continued)

9.2.3 Application Curve

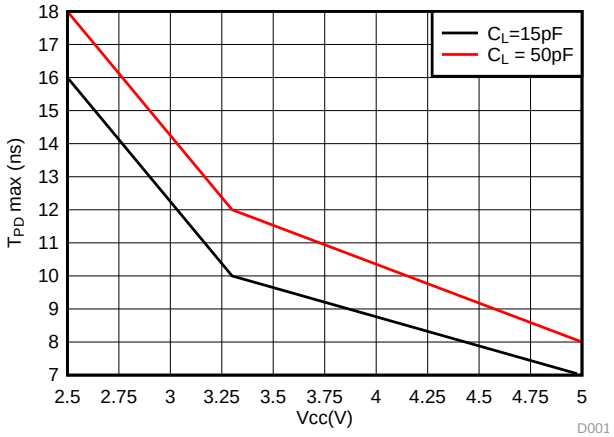


Figure 14. Maximum Propagation Delay vs V_{cc}

10 Power Supply Recommendations

Most systems have a common 3.3-V or 5-V rail that can supply the V_{CC} pin of this device. If this rail is not available, a switched-mode power supply (SMPS) or a low dropout regulator (LDO) can supply this device from a higher-voltage rail.

See the *Recommended Operating Conditions* for operating voltage range for this device. Having bypass capacitors of 0.1 µF is highly recommended.

11 Layout

11.1 Layout Guidelines

TI recommends keeping the signal lines as short and as straight as possible (see Figure 15). Incorporation of microstrip or stripline techniques are also recommended when signal lines are more than 1 in. long. These traces must be designed with a characteristic impedance of either 50-Ω or 75-Ω as required by the application. Do not place this device too close to high-voltage switching components because they may cause interference. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 16 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

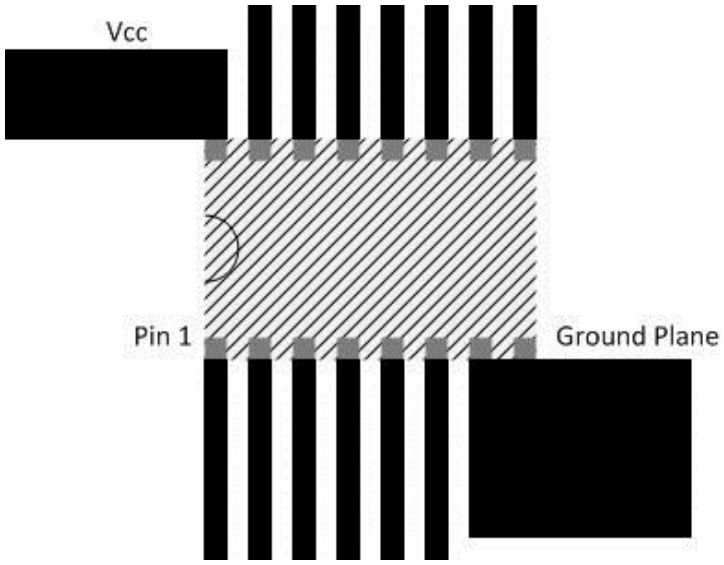


Figure 15. Layout Schematic

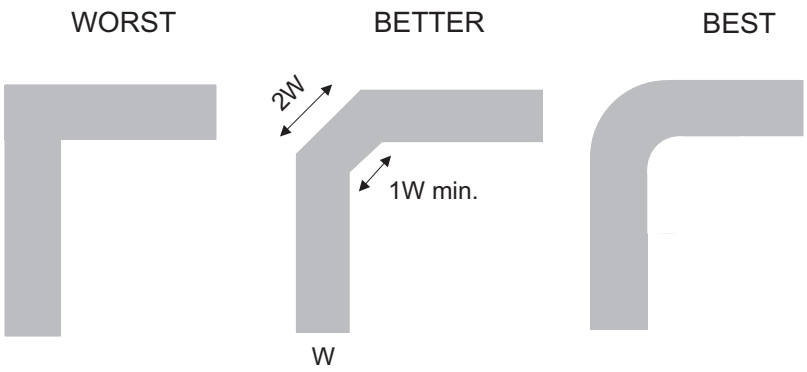


Figure 16. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265