

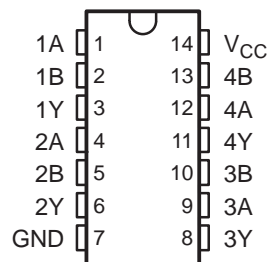
FEATURES

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -40°C to 125°C and -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree ⁽¹⁾
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operates From 2 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.3 ns at 3.3 V

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$

D OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74LVC00A quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The device performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION⁽¹⁾

| T_A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|--|------------------------|--------------|-----------------------|------------------|
| -40°C to 125°C | SOIC – D | Reel of 2500 | SN74LVC00AQDREP | LVC00AE |
| | TSSOP – PW | Reel of 2000 | SN74LVC00AQPWREP | LVC00AE |
| -55°C to 125°C | TSSOP – PW | Reel of 2000 | SN74LVC00AMPWREP | LVC00AM |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (EACH GATE)

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | H | L |
| L | X | H |
| X | L | H |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LVC00A-EP QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCAS729B–NOVEMBER 2003–REVISED MARCH 2007

LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|---|----------------------|-----------------------|----------|
| V _{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V _O | Output voltage range ⁽²⁾⁽³⁾ | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 V | | -50 mA |
| I _{OK} | Output clamp current | V _O < 0 V | | -50 mA |
| I _O | Continuous output current | | | ±50 mA |
| | Continuous current through V _{CC} or GND | | | ±100 mA |
| θ _{JA} | Package thermal impedance ⁽⁴⁾ | D package | | 86 °C/W |
| | | PW package | | 113 °C/W |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------------|--------------------------------|----------------------------------|-----|-----------------|------|
| V _{CC} | Supply voltage | Operating | 2 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 2.7 V to 3.6 V | 2 | | V |
| V _{IL} | Low-level input voltage | V _{CC} = 2.7 V to 3.6 V | | 0.8 | V |
| V _I | Input voltage | | 0 | 5.5 | V |
| V _O | Output voltage | | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 2.7 V | | -12 | mA |
| | | V _{CC} = 3 V | | -24 | |
| I _{OL} | Low-level output current | V _{CC} = 2.7 V | | 12 | mA |
| | | V _{CC} = 3 V | | 24 | |
| T _A | Operating free-air temperature | M suffix | -55 | 125 | °C |
| | | Q suffix | -40 | 125 | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|--|-----------------|-----------------------|--------------------|------|------|
| V _{OH} | I _{OH} = -100 μA | 2.7 V to 3.6 V | V _{CC} - 0.2 | | | V |
| | I _{OH} = -12 mA | 2.7 V | 2.2 | | | |
| | | 3 V | 2.4 | | | |
| | I _{OH} = -24 mA | 3 V | 2.2 | | | |
| V _{OL} | I _{OL} = 100 μA | 2.7 V to 3.6 V | | | 0.2 | V |
| | I _{OL} = 12 mA | 2.7 V | | | 0.4 | |
| | I _{OL} = 24 mA | 3 V | | | 0.55 | |
| I _I | V _I = 5.5 V or GND | 3.6 V | | | ±5 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | | | 10 | μA |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | | | 500 | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | | 5 | | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25 °C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

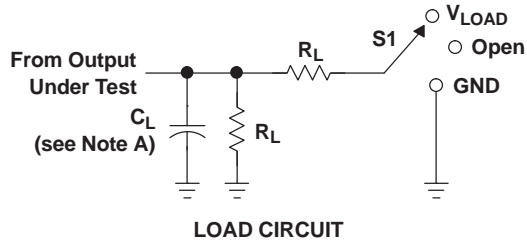
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|-----------------|--------------|-------------|-------------------------|-----|---------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | | 5.1 | 1 | 4.3 | ns |

Operating Characteristics

T_A = 25 °C

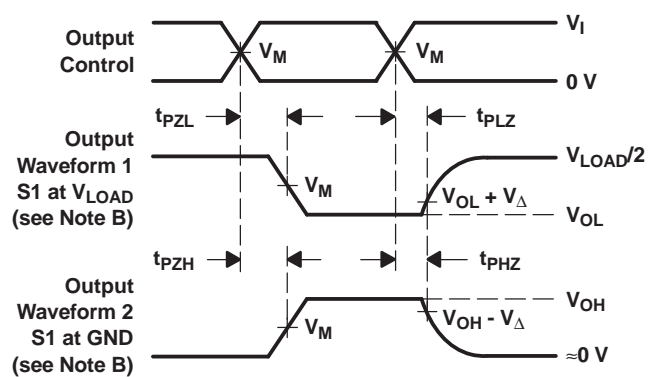
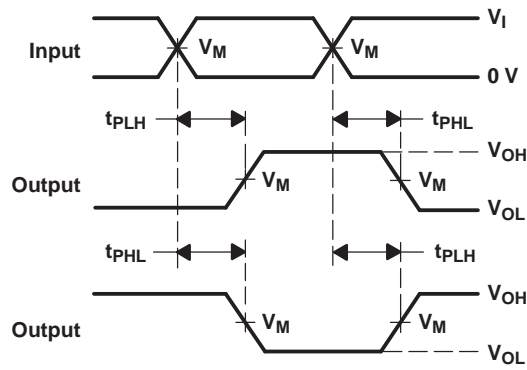
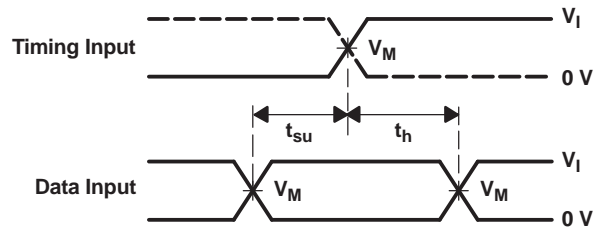
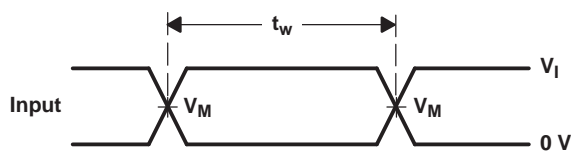
| PARAMETER | TEST CONDITIONS | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT |
|--|-----------------|-------------------------|-------------------------|------|
| | | TYP | TYP | |
| C _{pd} Power dissipation capacitance per gate | f = 10 MHz | 18 | 19 | pF |

PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|-------------------|--------|---------------|-------|------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V \pm 0.3 V | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC00AMPWREP | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | LVC00AM | Samples |
| SN74LVC00AMPWREPG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | LVC00AM | Samples |
| SN74LVC00AQDREP | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00AE | Samples |
| SN74LVC00AQPWREP | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00AE | Samples |
| V62/04652-01XE | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00AE | Samples |
| V62/04652-01YE | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00AE | Samples |
| V62/04652-02YE | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | LVC00AM | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC00A-EP :

- Catalog: [SN74LVC00A](#)

- Automotive: [SN74LVC00A-Q1](#)

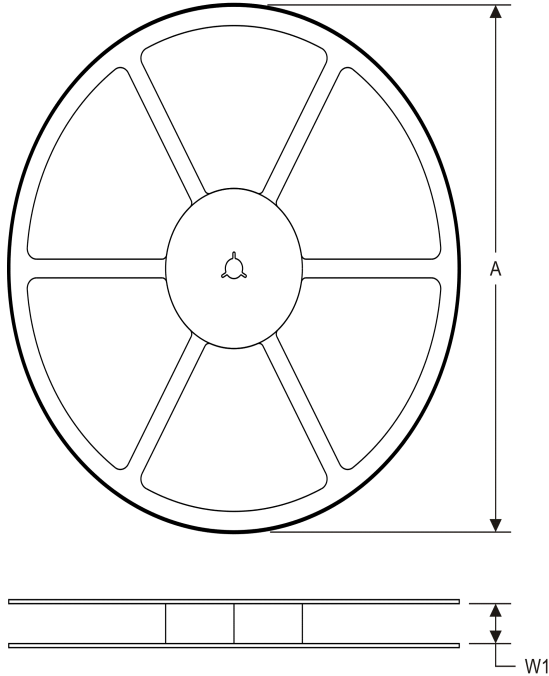
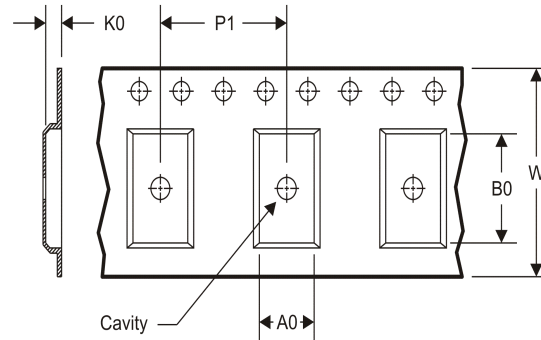
- Military: [SN54LVC00A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC00AMPWREP | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC00AQDREP | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC00AQPWREP | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC00AMPWREP | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LVC00AQDREP | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LVC00AQPWREP | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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