SN74LVTH16373-EP 3.3-V ABT 16-Bit Transparent D-Type Latch With Tri-State Outputs

1 Features

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree [(1)]
- Member of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up Tri-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 4000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)

2 Applications

- Data Buffer
- Bus Driver
- Display Driver

3 Description

The SN74LVTH16373 is a 16-bit transparent D-type latch with tri-state outputs designed for low-voltage (3.3 V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

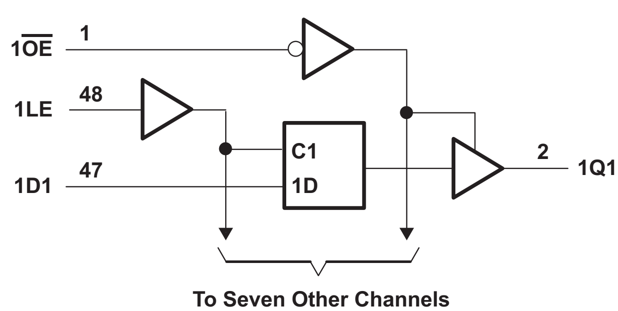
Device Information[(2)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVTH16373-EP	TSSOP (48)	12.50 mm × 6.10 mm
	SSOP (48)	15.88 mm × 7.49 mm
	BGA MICROSTAR JUNIOR (56)	4.50 mm × 7.00 mm

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

(2) For all available packages, see the orderable addendum at the end of the data sheet.

SN74LVTH16373-EP Single Channel Block Diagram



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4 Revision History

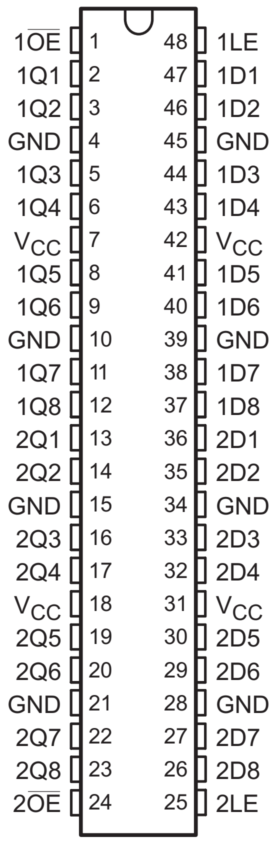
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2004) to Revision B **Page**

- Added *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics* section, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Corrected table notes for *Absolute Maximum Ratings* table 4
- Added new device temperature range to *Recommended Operating Conditions* table 5
- Added new device specifications in Timing Requirements (M Version) and Switching Characteristics (M Version) tables.. 8
- Added Figure 1 to *Specifications* section 9

5 Pin Configuration and Functions

DGG or DL Package
48-Pin TSSOP or SSOP
Top View



GQL Package
56-Pin BGA MICROSTAR JUNIOR
Top View

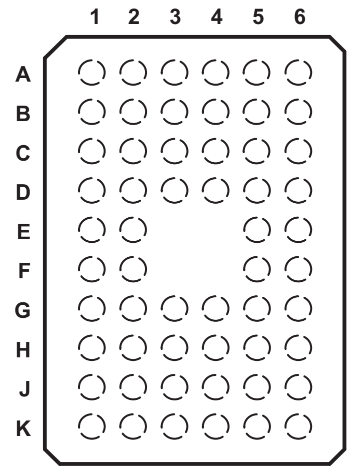


Table 1. Pin Assignments(1)

	1	2	3	4	5	6
A	1$\overline{OE}$	NC	NC	NC	NC	1LE
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	VCC	VCC	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	VCC	VCC	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2$\overline{OE}$	NC	NC	NC	NC	2LE

(1) NC − No internal connection.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1Dn[1]	37, 38, 49, 41, 43, 44, 46, 47	I	Data input pins
1LE	48	I	Latch enable pin to control 1Qn output states
1$\overline{OE}$	1	I	Active low enable pin for 1Qn pins
1Qn[1]	2, 3, 5, 6, 8, 9, 11, 12	O	Output pins
2Dn[1]	26, 27, 29, 30, 32, 33, 35, 36	I	Data input pins
2LE	25	I	Latch enable pin to control 2Qn output states
2Qn[1]	13, 14, 16, 17, 19, 20, 22, 23	O	Output pins
2$\overline{OE}$	24	I	Active low enable pin for 2Qn pins
GND	4, 10, 15, 21, 28, 34, 39, 45	—	Ground
VCC	7, 18, 31, 42	I	Power supply input for internal circuits

(1) "n" denotes numbering (1 to 8) for data input and output pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	4.6	V
V_I	Input voltage[2]	–0.5	7	V
V_O	Voltage applied to any output in the high-impedance or power-off state[2]	–0.5	7	V
V_O	Voltage applied to any output in the high state[2]	–0.5	V_{CC} + 0.5 V	V
I_O	Current into any output in the low state		128	mA
I_O	Current into any output in the high state[3]		64	mA
I_{IK}	Input clamp current (V_I < 0)	–50		mA
I_{OK}	Output clamp current (V_O < 0)	–50		mA
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per A114-A	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[1]	±3000	V
		Machine model (MM), per A115-A	200	V

(1) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage			5.5	V
I_{OH}	High-level output current			–32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate, outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		µs/V
T_A	Operating ambient temperature	I version	–40	85	°C
		M version	–55	125	°C

(1) All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)(2)		SN74LVTH16373-EP			UNIT
		DGG (TSSOP)	DL (SSOP)	GQL (BGA MICROSTAR JUNIOR)	
		48 PINS	48 PINS	56 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.9	60.3	62.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.6	31	24.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.8	32.1	28.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	9.3	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.5	31.8	28	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted); all typical values are at V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}		V_{CC} = 2.7 V,	I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = –100 µA	V_{CC} – 0.2			V
		V_{CC} = 2.7 V,	I_{OH} = –8 mA	2.4			V
		V_{CC} = 3 V,	I_{OH} = –32 mA	2			V
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 24 mA			0.5	V
		V_{CC} = 3 V,	I_{OL} = 16 mA			0.4	V
			I_{OL} = 32 mA			0.5	V
			I_{OL} = 64 mA			0.55	V
I_I	Control inputs	V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10	µA
		V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	µA
	Data inputs	V_{CC} = 3.6 V	V_I = V_{CC}			1	µA
			V_I = 0			–5	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			±100	µA
$I_{I(hold)}$	Data inputs	V_{CC} = 3 V	V_I = 0.8 V	75			µA
			V_I = 2 V	–75			µA
		V_{CC} = 3.6 V[1],	V_I = 0 to 3.6 V			±650	µA
I_{OZH}		V_{CC} = 3.6 V,	V_O = 3 V			5	µA
I_{OZL}		V_{CC} = 3.6 V,	V_O = 0.5 V			–5	µA
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 to 3 V, $\overline{OE}$ = don't care				±100	µA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 to 3 V, $\overline{OE}$ = don't care				±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19	mA
			Outputs low			5	mA
			Outputs disabled			0.19	mA
ΔI_{CC}[2]		V_{CC} = 3 to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2	mA
C_i		V_I = 3 V or 0			3		pF
C_o		V_O = 3 V or 0			9		pF

(1) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(2) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

6.6 Timing Requirements (I Version)

over recommended operating conditions (unless otherwise noted); T_A = –40°C to 85°C

			MIN	MAX	UNIT
t_w	Pulse duration, LE high	V_{CC} = 3.3 V ± 0.3 V	3		ns
		V_{CC} = 2.7 V	3		ns
t_{su}	Setup time, data before LE↓	V_{CC} = 3.3 V ± 0.3 V	1		ns
		V_{CC} = 2.7 V	0.6		ns
t_h	Hold time, data after LE↓	V_{CC} = 3.3 V ± 0.3 V	1		ns
		V_{CC} = 2.7 V	1.1		ns

6.7 Switching Characteristics (I Version)

over recommended operating conditions (unless otherwise noted); T_A = –40°C to 85°C; all typical values are at V_{CC} = 3.3 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	V_{CC} = 3.3 V ± 0.3 V	1.5	2.7	3.8	ns
			V_{CC} = 2.7 V			4.2	ns
t_{PHL}	D	Q	V_{CC} = 3.3 V ± 0.3 V	1.5	2.5	3.6	ns
			V_{CC} = 2.7 V			4	ns
t_{PLH}	LE	Q	V_{CC} = 3.3 V ± 0.3 V	2.1	3	4.3	ns
			V_{CC} = 2.7 V			4.8	ns
t_{PHL}	LE	Q	V_{CC} = 3.3 V ± 0.3 V	2.1	2.9	4	ns
			V_{CC} = 2.7 V			4	ns
t_{PZH}	$\overline{OE}$	Q	V_{CC} = 3.3 V ± 0.3 V	1.5	2.8	4.3	ns
			V_{CC} = 2.7 V			5.1	ns
t_{PZL}	$\overline{OE}$	Q	V_{CC} = 3.3 V ± 0.3 V	1.5	2.8	4.3	ns
			V_{CC} = 2.7 V			4.7	ns
t_{PHZ}	$\overline{OE}$	Q	V_{CC} = 3.3 V ± 0.3 V	2.4	3.5	5	ns
			V_{CC} = 2.7 V			5.4	ns
t_{PLZ}	$\overline{OE}$	Q	V_{CC} = 3.3 V ± 0.3 V	2	3.2	4.7	ns
			V_{CC} = 2.7 V			4.8	ns
$t_{sk(o)}$			V_{CC} = 3.3 V ± 0.3 V	0.5			ns

6.8 Timing Requirements (M Version)

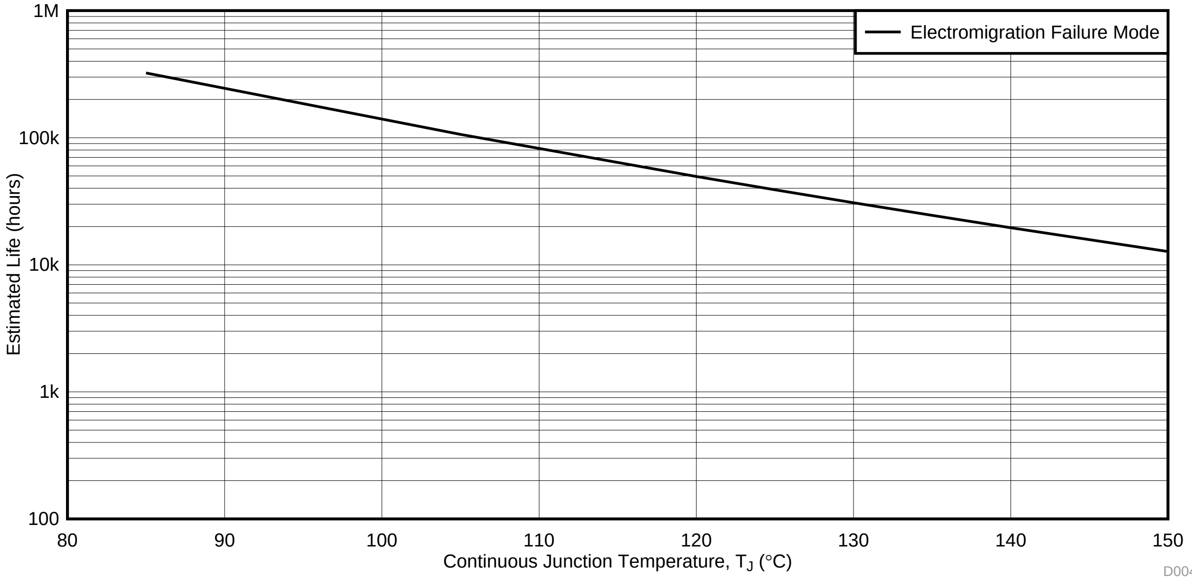
over recommended operating conditions (unless otherwise noted); T_A = –55°C to 125°C

			MIN	MAX	UNIT
t_w	Pulse duration, LE high	V_{CC} = 3.3 V ± 0.3 V	3		ns
		V_{CC} = 2.7 V	3		ns
t_{su}	Setup time, data before LE↓	V_{CC} = 3.3 V ± 0.3 V	1.6		ns
		V_{CC} = 2.7 V	1		ns
t_h	Hold time, data after LE↓	V_{CC} = 3.3 V ± 0.3 V	1.4		ns
		V_{CC} = 2.7 V	1.5		ns

6.9 Switching Characteristics (M Version)

over recommended operating conditions (unless otherwise noted); T_A = –55°C to 125°C; all typical values are at V_{CC} = 3.3 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	V_{CC} = 3.3 V ± 0.3 V	1.5	2.7	5	ns
			V_{CC} = 2.7 V			5.5	ns
t_{PHL}	D	Q	V_{CC} = 3.3 V ± 0.3 V	1.5	2.5	4.8	ns
			V_{CC} = 2.7 V			5.3	ns
t_{PLH}	LE	Q	V_{CC} = 3.3 V ± 0.3 V	2.1	3	5.4	ns
			V_{CC} = 2.7 V			5.9	ns
t_{PHL}	LE	Q	V_{CC} = 3.3 V ± 0.3 V	2.1	2.9	4.9	ns
			V_{CC} = 2.7 V			4.9	ns
t_{PZH}	$\overline{OE}$	Q	V_{CC} = 3.3 V ± 0.3 V	1.5	2.8	7	ns
			V_{CC} = 2.7 V			7.9	ns
t_{PZL}	$\overline{OE}$	Q	V_{CC} = 3.3 V ± 0.3 V	1.5	2.8	6.2	ns
			V_{CC} = 2.7 V			7.2	ns
t_{PHZ}	$\overline{OE}$	Q	V_{CC} = 3.3 V ± 0.3 V	1.8	3.5	7.2	ns
			V_{CC} = 2.7 V			7.9	ns
t_{PLZ}	$\overline{OE}$	Q	V_{CC} = 3.3 V ± 0.3 V	2	3.2	5.2	ns
			V_{CC} = 2.7 V			5.4	ns
$t_{sk(o)}$			V_{CC} = 3.3 V ± 0.3 V	0.5			ns



(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

Figure 1. Derating Chart for SN74LVTH16373-EP

6.10 Typical Characteristics

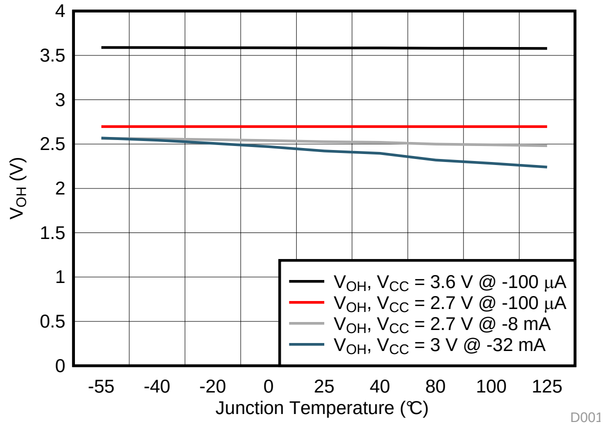


Figure 2. V_{OH} vs Temperature

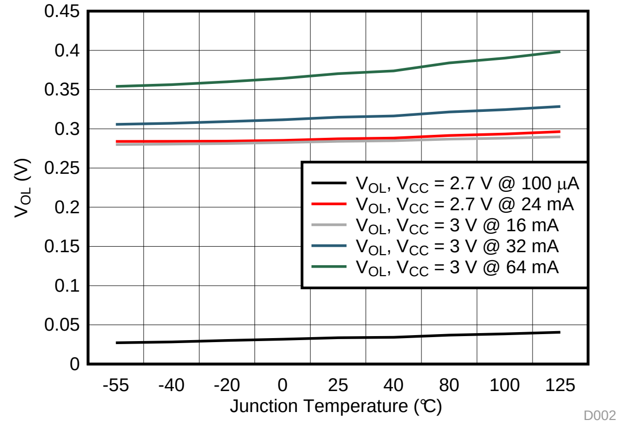
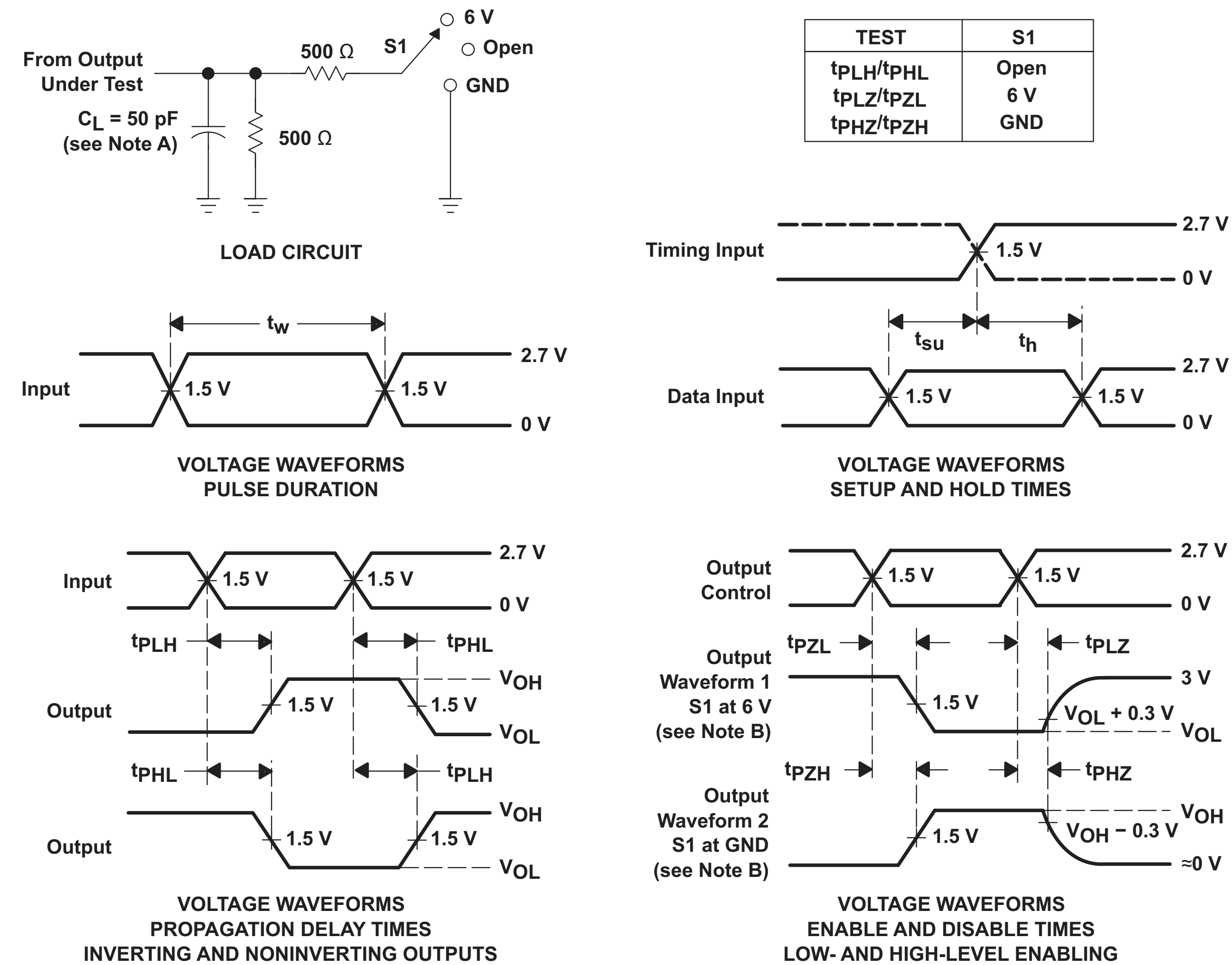


Figure 3. V_{OL} vs Temperature

7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time, with one transition per measurement.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVTH16373 is a 16-bit transparent D-type latch with tri-state outputs designed for low-voltage (3.3-V) VCC operation, but with the capability to provide a TTL interface to a 5-V system environment. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one 16-bit latch. When the latchenable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components. OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

8.2 Functional Block Diagram

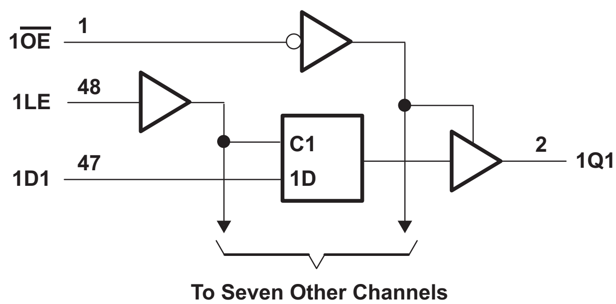


Figure 5. Logic Diagram (Positive Logic)

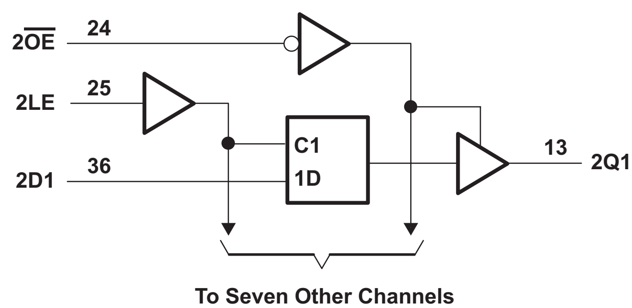


Figure 6. Logic Diagram (Positive Logic)

8.3 Feature Description

The SN74LVTH16373 included active bus-hold circuitry that holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. Additionally, it features power up three state that will keep the outputs in high-impedance state during power up or power down when VCC is between 0 and 1.5 V. This prevents driver conflict during power up.

To ensure the high-impedance state above 1.5 V, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up tri-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Table 2. Function Table (Each 8-Bit Section)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

8.4 Device Functional Modes

Device functions as tristatable 8 or 16-bit latch per function table defined in Table 2.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The specially designed 3-V LVTH family uses the 0.8-µ BiCMOS process technology for bus-interface functions. Like its 5-V ABT counterpart, LVHT provides up to 64 mA of drive, low propagation delays. The bus-hold feature eliminates requirements for external pullup resistors and I/Os that can handle up to 7 V, which allows them to act as 5-V/3-V translators.

9.2 Typical Application

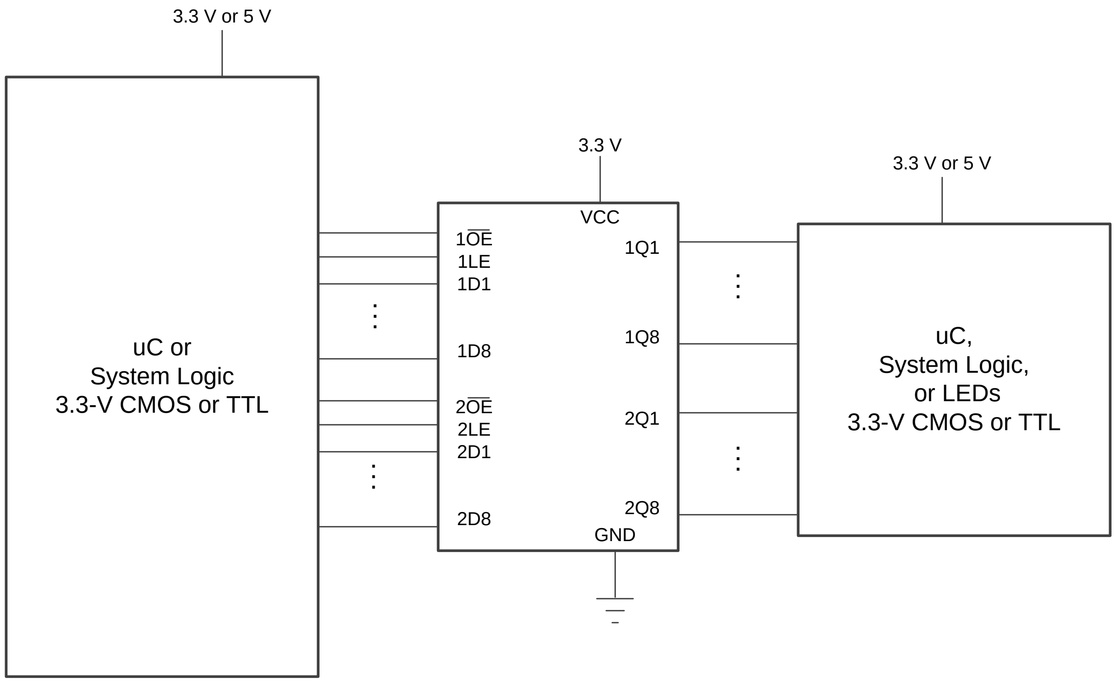


Figure 7. Application Diagram

9.2.1 Design Requirements

The SN54LVTH16373 utilizes BiCMOS technology with high-drive currents. Care must be taken to avoid bus contention that can disrupt system functionality and/or cause violation of absolute maximum ratings.

9.2.2 Detailed Design Procedure

- Recommended input conditions
  - Rise time and fall time specifications. See Δt/ΔV in Recommended Operating Conditions.
  - Specified high and low levels. See V_{IH} and V_{IL} in Recommended Operating Conditions.
  - Inputs are overvoltage tolerant, which allows them to go as high as 5.5 V independent of V_{CC}.
- Recommend output conditions
  - Avoid buss contention.
  - Do not exceed I_{OH} and I_{OL} current limits in Recommended Operating Conditions.
  - Outputs that are being driven high may not be pulled above V_{CC} by more they 0.5 V.

Typical Application (continued)

9.2.3 Application Curves

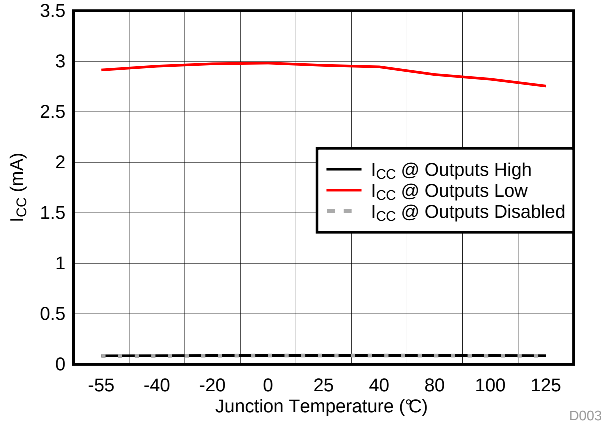


Figure 8. I_{CC} vs Temperature

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 9 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

11.2 Layout Example

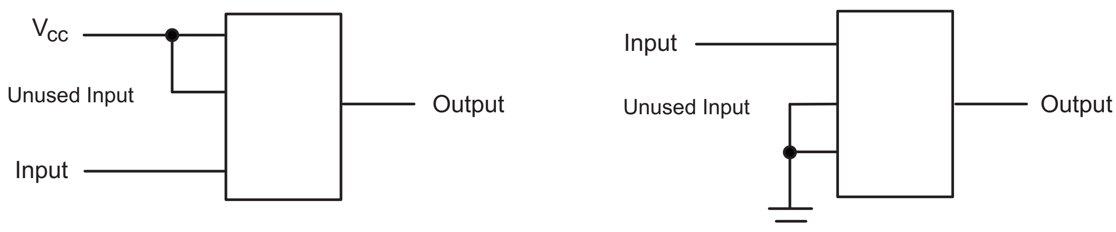


Figure 9. Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

Widebus, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLVTH16373IDGGREP	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH16373EP	Samples
CLVTH16373IDLREP	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH16373EP	Samples
CLVTH16373MGQLREP	ACTIVE	BGA MICROSTAR JUNIOR	GQL	56	2000	TBD	SNPB	Level-1-235C-UNLIM	-55 to 125	H16373MEP	Samples
V62/04712-01XE	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH16373EP	Samples
V62/04712-01YE	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH16373EP	Samples
V62/04712-02ZA	ACTIVE	BGA MICROSTAR JUNIOR	GQL	56	2000	TBD	SNPB	Level-1-235C-UNLIM	-55 to 125	H16373MEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVTH16373-EP :

- Catalog: SN74LVTH16373

- Military: SN54LVTH16373

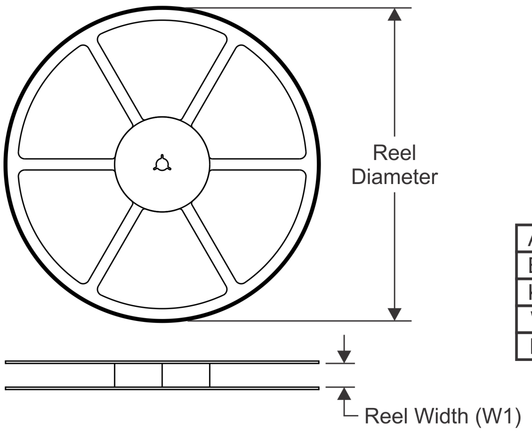
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

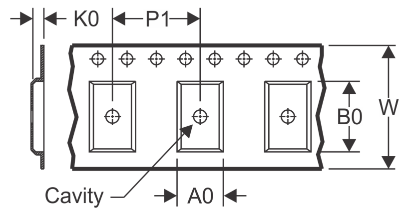
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

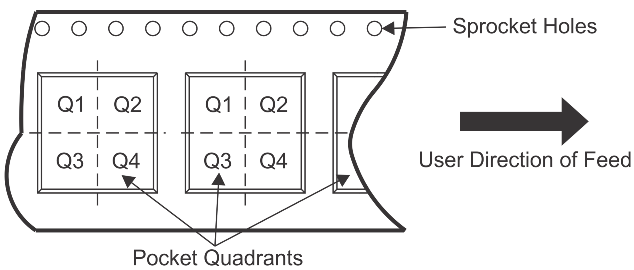


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

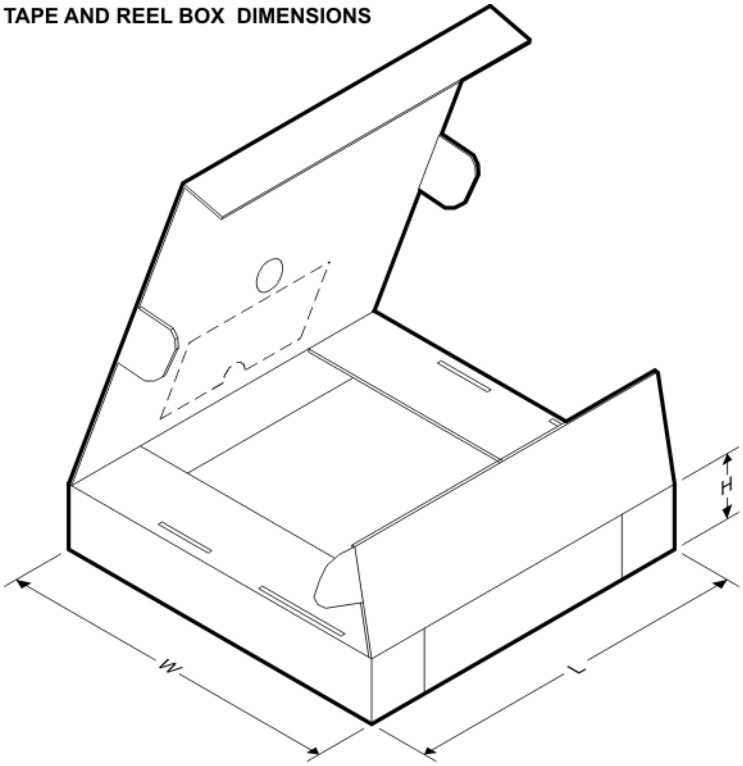
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVTH16373IDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
CLVTH16373IDLREP	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CLVTH16373MGQLREP	BGA MI CROSTA R JUNI OR	GQL	56	2000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

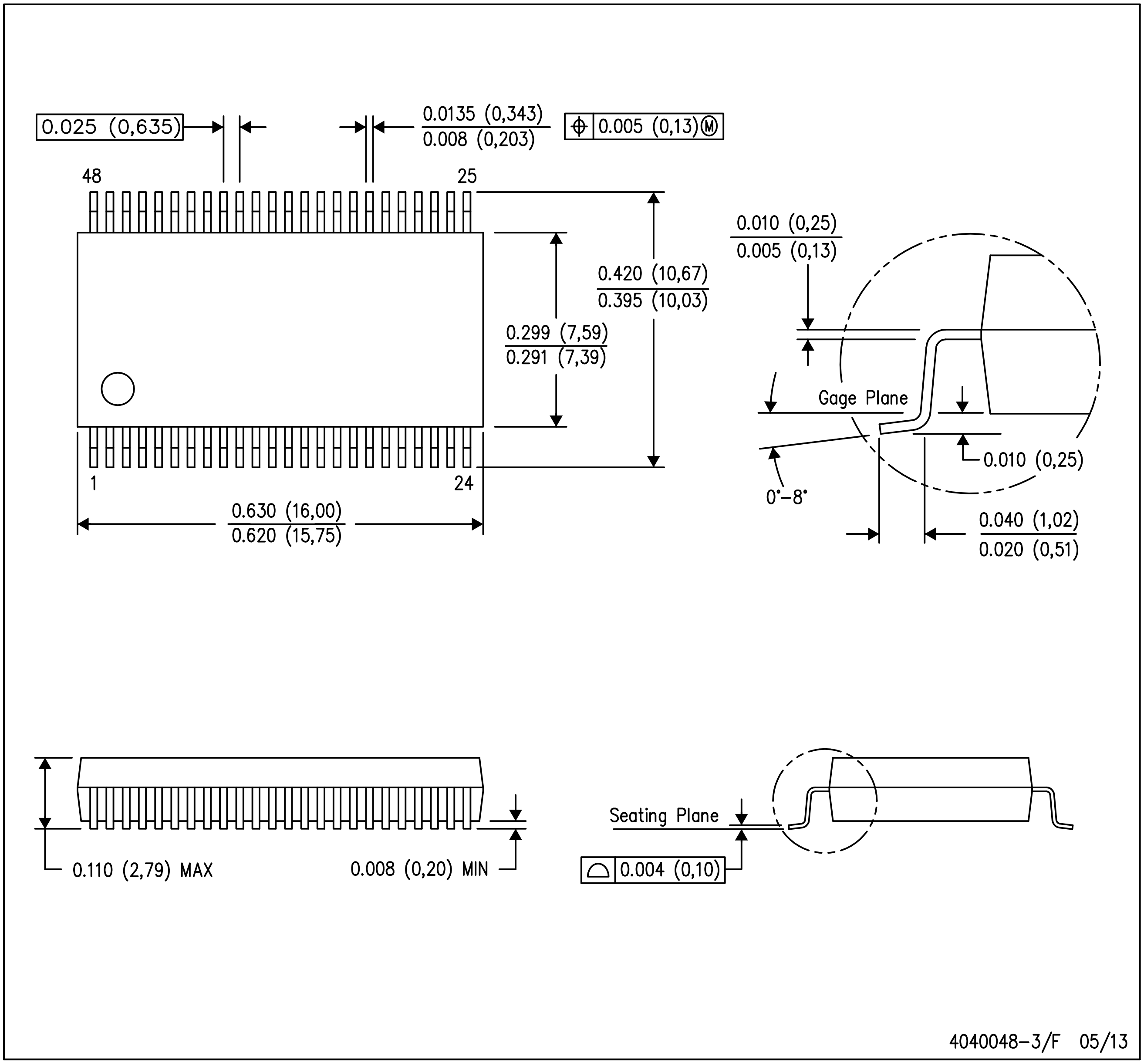
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVTH16373IDGGREP	TSSOP	DGG	48	2000	367.0	367.0	45.0
CLVTH16373IDLREP	SSOP	DL	48	1000	367.0	367.0	55.0
CLVTH16373MGQLREP	BGA MICROSTAR JUNIOR	GQL	56	2000	336.6	336.6	28.6

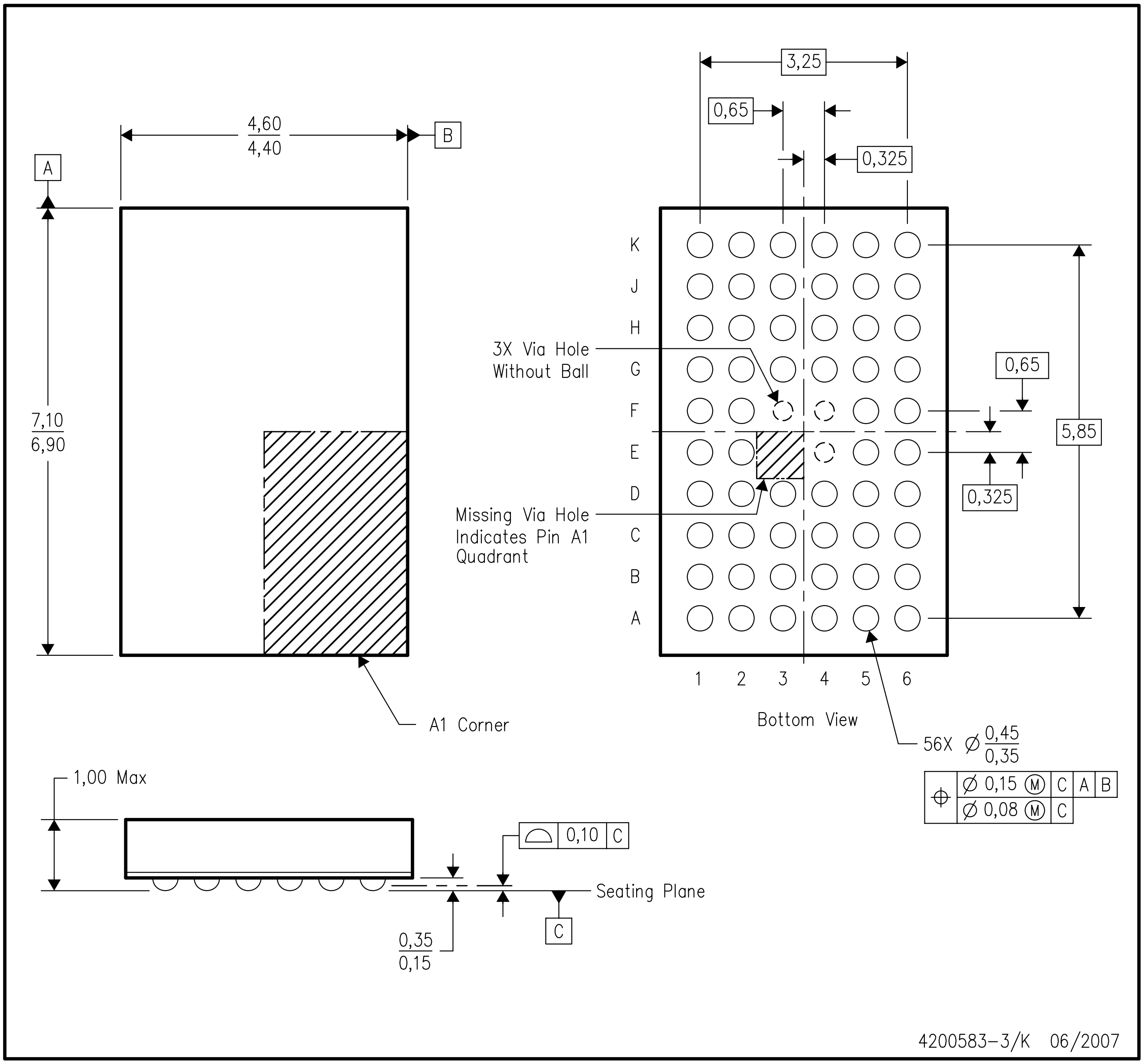
DL (R-PDSO-G48) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

PowerPAD is a trademark of Texas Instruments.

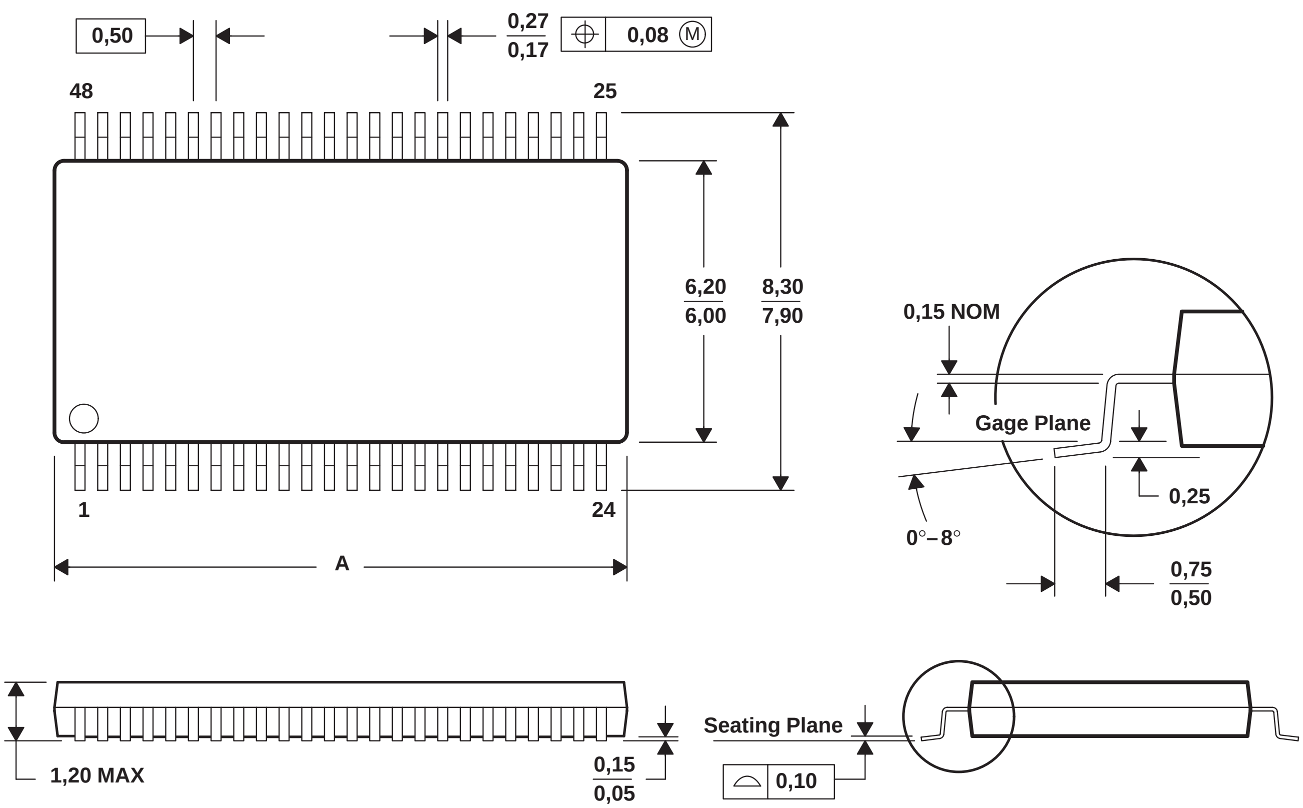
GQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–285 variation BA–2.
D. This package is tin–lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead–free.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153