SN54LVTH16646, SN74LVTH16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS SCBS698G - JULY 1997 - REVISED MAY 2004

 Members of the Texas Instruments Widebus™ Family 	SN74LVTH16646		D PACKAGE DR DL PACKAGE
 State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation 	1DIR [1CLKAB [1SAB [1 56 2 55	10E 1CLKBA 1SBA
 Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC}) 	GND [1A1 [1A2 [4 53 5 52 6 51	GND 1B1 1B2
 Support Unregulated Battery Operation Down to 2.7 V 	V _{CC} [1A3 [8 49	V _{CC} 1B3
 Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1A4 [1A5 [GND [10 47	1B4 1B5 GND
 I_{off} and Power-Up 3-State Support Hot Insertion 	1A6 [1A7 [12 45	1B6 1B7
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	1A8 [2A1 [2A2 [14 43 15 42	1B8 2B1 2B2
 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	2A3 [GND [17 40	2B2 2B3 GND
 Flowthrough Architecture Optimizes PCB Layout 	2A4 [2A5 [20 37	2B4 2B5
 Latch-Up Performance Exceeds 500 mA Per JESD 17 	2A6 V _{CC}	22 35	2B6 V _{CC}
 ESD Protection Exceeds JESD 22 2000-V Human-Body Model (A114-A) 200-V Machine Model (A115-A) 	2A7 [2A8 [GND [2SAB [24 33 25 32	2B7 2B8 GND 2SBA
description/ordering information	2CLKAB 2DIR	27 30	2011 2011 2011 2011

The 'LVTH16646 devices are 16-bit bus transceivers and registers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
		Tube	SN74LVTH16646DL	1)/71/40040
–40°C to 85°C	SSOP – DL	Tape and reel	SN74LVTH16646DLR	LVTH16646
	TSSOP – DGG	Tape and reel	SN74LVTH16646DGGR	LVTH16646
–55°C to 125°C	CFP – WD	Tube	SNJ54LVTH16646WD	SNJ54LVTH16646WD

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54LVTH16646, SN74LVTH16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS698G - JULY 1997 - REVISED MAY 2004

description/ordering information (continued)

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH16646 devices.

Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

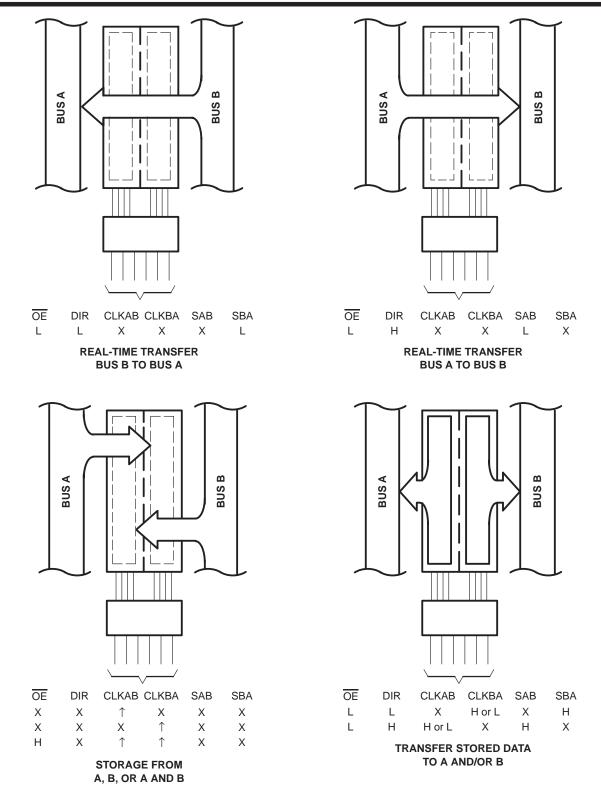
INPUTS						DAT	A I/O	
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8 B1-B8		OPERATION OR FUNCTION
Х	Х	\uparrow	Х	Х	Х	Input	Unspecified [†]	Store A, B unspecified [†]
Х	Х	Х	\uparrow	Х	Х	Unspecified [†]	Input	Store B, A unspecified [†]
Н	Х	\uparrow	\uparrow	Х	Х	Input	Input	Store A and B data
Н	Х	H or L	H or L	Х	Х	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus
L	L	Х	H or L	Х	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B Bus
L	Н	H or L	Х	Н	Х	Input	Output	Stored A data to bus

ELINCTION TABLE

[†] The data-output functions can be enabled or disabled by various signals at OE or DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.



SCBS698G - JULY 1997 - REVISED MAY 2004

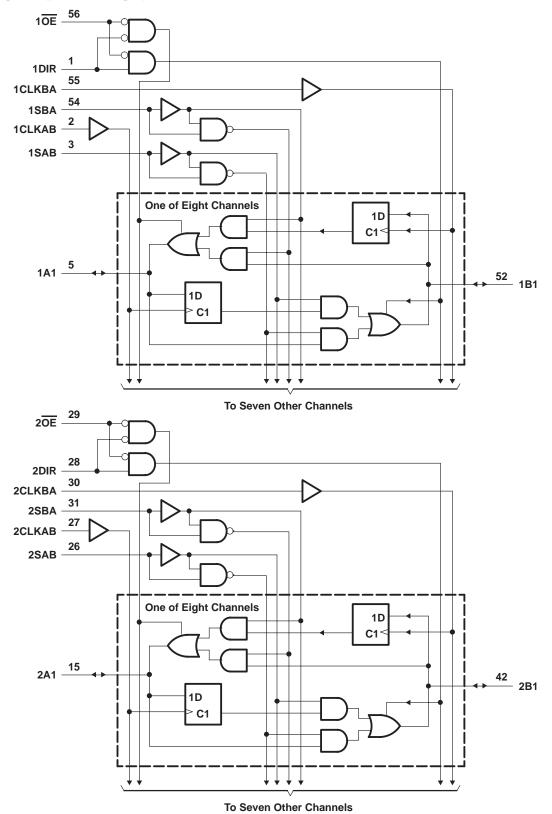






SCBS698G - JULY 1997 - REVISED MAY 2004

logic diagram (positive logic)





SCBS698G - JULY 1997 - REVISED MAY 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}
or power-off state, V_O (see Note 1) -0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I _O : SN54LVTH16646
SN74LVTH16646
Current into any output in the high state, I _O (see Note 2): SN54LVTH16646
SN74LVTH16646
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I_{OK} ($V_O < 0$)
Package thermal impedance, θ _{JA} (see Note 3): DGG package
DL package
Storage temperature range, T _{stg} 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LVT	H16646	SN74LVT	H16646	
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	Ň	2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current		1	-24		-32	mA
IOL	Low-level output current		200	48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled	0	10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCBS698G - JULY 1997 - REVISED MAY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				SN5	4LVTH1	6646	SN74	LVTH1	6646	
PAI	RAMETER	TEST C	ONDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 2.7 V,	lı = -18 mA			-1.2	-1.2			V
		$V_{CC} = 2.7 V \text{ to } 3.6 V,$	I _{OH} = -100 μA	V _{CC} -0	.2		V _{CC} -0	2		
		V _{CC} = 2.7 V,	IOH = -8 mA	2.4			2.4			
VOH			I _{OH} = -24 mA	2						V
		$V_{CC} = 3 V$	$I_{OH} = -32 \text{ mA}$				2			
			I _{OL} = 100 μA			0.2			0.2	
		$V_{CC} = 2.7 V$	I _{OL} = 24 mA			0.5			0.5	
			I _{OL} = 16 mA			0.4			0.4	V
VOL			I _{OL} = 32 mA			0.5			0.5	V
		V _{CC} = 3 V	I _{OL} = 48 mA			0.55				
			I _{OL} = 64 mA			N			0.55	
	Control inputo	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GND		1	±1			±1	
	Control inputs	$V_{CC} = 0 \text{ or } 3.6 \text{ V},$	V _I = 5.5 V		A.	10			10	
lj –		V _I = 5.5 V		K	20			20	μA	
	A or B ports‡	V _{CC} = 3.6 V	$V_I = V_{CC}$		2	1			1	
			$V_{I} = 0$	C C	5	-5			-5	
loff		$V_{CC} = 0,$	V_{I} or V_{O} = 0 to 4.5 V	Q					±100	μA
		V _{CC} = 3 V	VI = 0.8 V	75			75			
ll(hold)	A or B ports		V _I = 2 V	-75			-75			μA
		V _{CC} = 3.6 V§,	V _I = 0 to 3.6 V						±500	
IOZPU		$\frac{V_{CC}}{OE} = 0 \text{ to } 1.5 \text{ V}, \text{ V}_{O} = 0$	= 0.5 V to 3 V,			±100*			±100	μΑ
IOZPD		$\frac{V_{CC}}{OE}$ = 1.5 V to 0, V _O = OE = don't care	= 0.5 V to 3 V,			±100*			±100	μA
			Outputs high			0.19			0.19	
		$V_{CC} = 3.6 \text{ V}, I_O = 0,$ $V_I = V_{CC} \text{ or GND}$	Outputs low			5			5	mA
			Outputs disabled			0.19			0.19	
∆ICC¶		$V_{CC} = 3 V$ to 3.6 V, On Other inputs at V_{CC} or	ie input at V _{CC} – 0.6 V, GND			0.2			0.2	mA
Ci		V _I = 3 V or 0			4			4		pF
C _{io}				10			10		pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. [‡] Unused pins at V_{CC} or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

I This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



SCBS698G - JULY 1997 - REVISED MAY 2004

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

			5	SN54LV	TH16646		5	SN74LV	TH16646		
			×CC = ± 0.		V _{CC} =	2.7 V	= V _{CC} ± 0.		V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	ock frequency		150		150		150		150	MHz
tw	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
	Setup time,	Data high	1.2	-0	1.5		1.2		1.5		
tsu	A or B before CLKAB↑ or CLKBA↑	Data low	2	24	2.8		2		2.8		ns
4.	Hold time,	Data high	0.5	.67.	0		0.5		0		
th	A or B after CLKAB↑ or CLKBA↑		0.5		0.5		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 2)

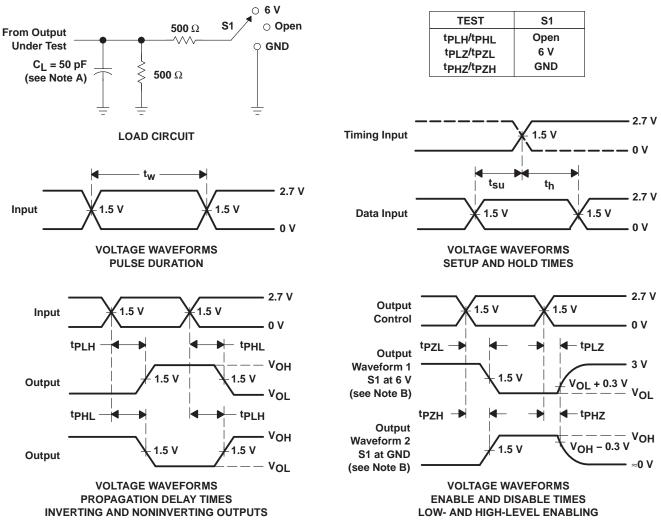
			9	SN54LV	ГН16646			SN74	LVTH1	6646		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	۷ _{CC} = ± 0.1		V _{CC} =	2.7 V		CC = 3.3 ± 0.3 V	V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
fmax			150		150		150			150		MHz
^t PLH	CLKBA or	A or P	1.3	4.5		5	1.3	2.8	4.2		4.7	20
^t PHL	CLKAB	A or B	1.3	4.5		5	1.3	2.8	4.2		4.7	ns
^t PLH	A	D or A	1	3.6		4.1	1	2.4	3.4		3.9	
^t PHL	A or B	B or A	1	3.6	η_{\pm}	4.1	1	2.1	3.4		3.9	ns
^t PLH	SBA or SAB‡	A	1	4.7	M:	5.6	1	2.8	4.5		5.4	
^t PHL	SDA UI SAD+	A or B	1	4.7		5.6	1	3	4.5		5.4	ns
^t PZH	OE	A or D	1	4.5	a.	5.4	1	2.5	4.3		5.2	20
^t PZL	ÛE	A or B	1	4.5		5.4	1	2.6	4.3		5.2	ns
^t PHZ	OE	A	2	5.8		6.3	2	4	5.6		6.1	
^t PLZ	ÛE	A or B	2	× 5.6		6.3	2	3.6	5.4		6.1	ns
^t PZH		A an D	1	4.6		5.5	1	3	4.4		5.3	
^t PZL	DIR	A or B	1	4.6		5.5	1	3	4.4		5.3	ns
^t PHZ	DID	A an D	1.5	6		7.1	1.5	3.9	5.7		6.8	
^t PLZ	DIR	A or B	1.5	5.5		6	1.5	3.6	5.2		5.7	ns

[†] All typical values are at V_{CC} = 3.3 V, $T_A = 25^{\circ}C$.

[‡]These parameters are measured with the internal output state of the storage register opposite that of the bus input.



SCBS698G - JULY 1997 - REVISED MAY 2004



PARAMETER MEASUREMENT INFORMATION

NOTES: A. C₁ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



TEXAS

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74LVTH16646DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVTH16646DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH16646DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH16646DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH16646DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH16646DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVTH16646 :

Enhanced Product: SN74LVTH16646-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH16646DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74LVTH16646DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH16646DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74LVTH16646DLR	SSOP	DL	56	1000	346.0	346.0	49.0

MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G**)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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