

TCA6507 Low-Voltage 7-Bit I²C and SMBus LED Driver With Intensity Control and Shutdown

1 Features

- Seven LED Driver Outputs: ON, OFF, Blinking, Fading at Programmable Rates
- Open-Drain Outputs Directly Drive LEDs to 40-mA Maximum
- Two Independent Banks of LED Drivers
- Widely Programmable Blink Rates, Fade-ON and Fade-OFF Rates and Maximum Intensity
- Outputs Not Used as LED Drivers Can Be Used as Regular General-Purpose Open-Drain Outputs
- 16 Steps of Maximum Intensity Control from Fully-OFF to Fully-ON States
- Smooth Perceived Transitions for Fade-ON and Fade-OFF
- Operating Power-Supply Voltage Range of 1.65-V to 3.6-V
- 5.5-V Tolerant Open-Drain Outputs
- Low Standby Current With Shutdown Capability for Additional Power Savings
- Internal Oscillator Requires No External Components
- Programmed Through I²C Bus Interface Logic Compatible With SMBus
- No Glitch on Power Up
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Mobile Phones
- Desktop and Laptop Computers
- Human Machine Interface

3 Description

This 7-bit LED dimmer for the two-line bidirectional bus (I²C) is designed to control (or dim) LEDs through the I²C interface. Without this device, the microcontroller must be actively involved in turning on and off the LEDs (per the required dimming rate), which uses valuable processor time. The TCA6507 alleviates this issue by limiting the number of operations required by the processor in blinking LEDs and helps to create a more efficient system. The TCA6507 handles all pulse width modulation (PWM) logic, allowing the processor to use its cycles for more important tasks.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA6507	TSSOP (14)	5.00 mm x 4.40 mm
	BGA MICROSTAR JUNIOR (12)	2.00 mm x 2.50 mm
	X2QFN (12)	2.00 mm x 1.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

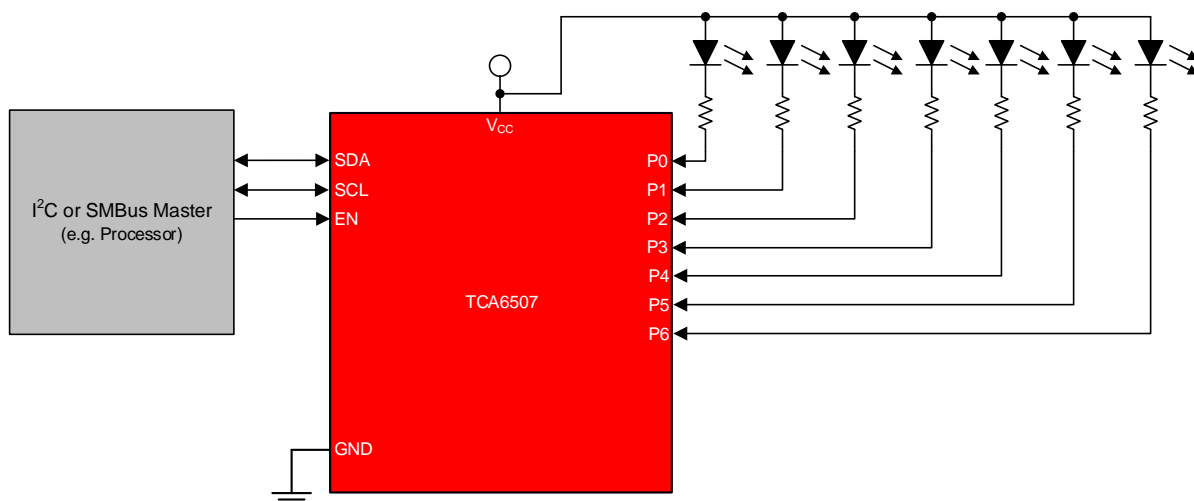


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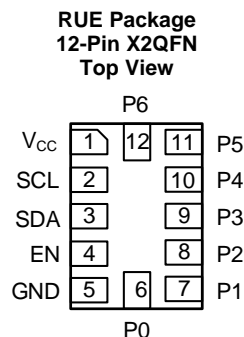
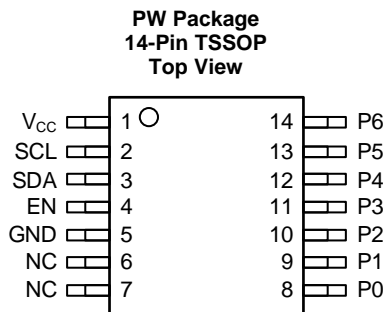
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2007) to Revision C	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

5 Pin Configuration and Functions



Pin Functions –TSSOP and X2QFN

NAME	PIN		TYPE	DESCRIPTION
	TSSOP	X2QFN		
EN	4	4	I	Enable input. If set to low, it puts the TCA6507 in shutdown mode and resets the internal registers and I ² C/SMBus state machine to their default states.
GND	5	5	—	Ground.
P0	8	6	O	P-port output 0. Open-drain design structure.
P1	9	7	O	P-port output 1. Open-drain design structure.
P2	10	8	O	P-port output 2. Open-drain design structure.
P3	11	9	O	P-port output 3. Open-drain design structure.
P4	12	10	O	P-port output 4. Open-drain design structure.
P5	13	11	O	P-port output 5. Open-drain design structure.
P6	14	12	O	P-port output 6. Open-drain design structure.
SDA	3	3	I/O	Serial data bus. Connect to V _{CC} through a pullup resistor.
SCL	2	2	I	Serial clock bus. Connect to V _{CC} through a pullup resistor.
V _{CC}	1	1	—	Supply voltage of I ² C registers, oscillator, and control logic. Connect directly to V _{CC} of the external I ² C master. Provides voltage-level translation.

ZXU Package
12-Pin BGA MICROSTAR JUNIOR
Top View

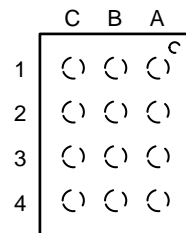


Table 1. ZXU Package Terminal Assignments

	C	B	A
1	P1	P2	GND
2	P3	EN	SDA
3	P4	P0	SCL
4	P5	P6	V _{CC}

Pin Functions –BGA Microstar Junior

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	GND	—	Ground.
A2	SDA	I/O	Serial data bus. Connect to V _{CC} through a pullup resistor.
A3	SCL	I	Serial clock bus. Connect to V _{CC} through a pullup resistor.
A4	V _{CC}	—	Supply voltage of I ² C registers, oscillator, and control logic. Connect directly to V _{CC} of the external I ² C master. Provides voltage-level translation.
B1	P2	O	P-port output 2. Open-drain design structure.
B2	EN	I	Enable input. If set to low, it puts the TCA6507 in shutdown mode and resets the internal registers and I ² C/SMBus state machine to their default states.
B3	P0	O	P-port output 0. Open-drain design structure.
B4	P6	O	P-port output 6. Open-drain design structure.
C1	P1	O	P-port output 1. Open-drain design structure.
C2	P3	O	P-port output 3. Open-drain design structure.
C3	P4	O	P-port output 4. Open-drain design structure.
C4	P5	O	P-port output 5. Open-drain design structure.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

				MIN	MAX	UNIT
V _{CC}	Supply voltage			-0.5	4.6	V
V _I	Input voltage ⁽²⁾			-0.5	6.5	V
V _O	Output voltage ⁽²⁾				6.5	V
I _{IK}	Input clamp current	V _I < 0	SCL, EN		±20	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}	P port, SDA		±20	mA
I _{OL}	Continuous output low current	V _O = 0 to V _{CC}	P port		50	mA
			SDA		25	
I _{CC}	Continuous current through GND				250	mA
	Continuous current through V _{CC}				20	
T _{stg}	Storage temperature			-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage of I ² C registers, oscillator, and control logic			1.65		3.6	V
V _{IH}	High-level input voltage	SCL, SDA, EN	1.65 V ≤ V _{CC} ≤ 1.95 V	1.3		3.6	V
			1.96 V ≤ V _{CC} ≤ 3.6 V	0.7 × V _{CC}		3.6	
V _{IL}	Low-level input voltage	SCL, SDA, EN	1.65 V ≤ V _{CC} ≤ 1.95 V	-0.5		0.3	V
			1.96 V ≤ V _{CC} ≤ 3.6 V	-0.5		0.3 × V _{CC}	
V _O	Output voltage			0		5.5	V
I _{OL}	Low-level output current ⁽¹⁾					40	mA
T _A	Operating free-air temperature			-40		85	°C

- (1) The total current sourced by the P port must be limited to 200 mA.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TCA6507			UNIT
		PW (TSSOP)	ZXU (BGA MICROSTAR JUNIOR)	RUE (X2QFN)	
		14 PINS	12 PINS	12 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	127.2	155.2	181.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	55.8	99.4	80.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	38.9	91.5	95.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	9.3	6.8	3.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	68.3	92.1	95.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

GND = 0 V, T_A = –40°C to 85°

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
f _{INT}	Intensity control clock frequency	Operating mode	1.65 V to 3.6 V	23	32	43	kHz
V _{IK}	Input diode clamp voltage	I _I = –18 mA	1.65 V to 3.6 V	–1.2			V
V _{POR}	Power-on reset voltage	V _I = V _{CC} or GND, I _O = 0	1.65 V to 3.6 V		1.4		V
V _{OL}	SDA	I _{OL} = 6 mA	1.65 V to 3.6 V		0.2	0.6	V
I _{OL}	SDA		1.65 V to 3.6 V	3	13.2		mA
	P port ⁽²⁾	V _{OL} = 0.5 V	1.65 V	25	59.7		mA
		V _{OL} = 0.6 V	1.8 V to 3.6 V	40	68		mA
I _I	SCL, SDA, EN	V _I = V _{CC} or GND	1.65 V to 3.6 V			±0.1	μA
I _{CC}	Standby current	EN disabled, P port idle, Intensity control disabled, SCL = V _{CC} , SDA = V _{CC} , I _O = 0, f _{SCL} = 0	1.65 V to 1.95 V		2	12	μA
			1.96 V to 3.6 V		3	15	
	Operating mode	P port running, Intensity control enabled, SCL = V _{CC} , SDA = V _{CC} , I _O = 0, f _{SCL} = 0	1.65 V to 1.95 V		9.7	17	μA
			1.96 V to 3.6 V		10.4	20	
		P port running, Intensity control enabled, SDA = V _{CC} , I _O = 0, f _{SCL} = 400 kHz	1.65 V to 1.95 V		10.2	18	μA
			1.96 V to 3.6 V		11.4	25	
C _i	SCL		1.65 V to 3.6 V			7	pF
C _{io}	SDA	V _{IO} = V _{CC} or GND	1.65 V to 3.6 V			8	pF
C _o	P port	V _O = V _{CC} or GND	1.65 V to 3.6 V			10	pF

(1) All typical values are at T_A = 25°C.

(2) The total current sourced by the P port must be limited to 200 mA.

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 8)

		STANDARD MODE I ² C BUS		FAST MODE I ² C BUS		UNIT
		MIN	MAX	MIN	MAX	
t _{scl}	I ² C clock frequency	0	100	0	400	kHz
t _{sch}	I ² C clock high time	4		0.6		μs
t _{scl}	I ² C clock low time	4.7		1.3		μs
t _{sp}	I ² C spike time		50		50	ns
t _{sds}	I ² C serial-data setup time	250		100		ns
t _{sdh}	I ² C serial-data hold time	0		0		ns
t _{icr}	I ² C input rise time		1000	20 + 0.1C _b ⁽¹⁾	300	ns
t _{icf}	I ² C input fall time		300	20 + 0.1C _b ⁽¹⁾	300	ns
t _{ocf}	I ² C output fall time	10-pF to 400-pF bus	300	20 + 0.1C _b ⁽¹⁾	250	ns
t _{buf}	I ² C bus free time between STOP and START conditions	4.7		1.3		μs
t _{sts}	I ² C START or repeated START condition setup	4.7		0.6		μs
t _{sth}	I ² C START or repeated START condition hold	4		0.6		μs
t _{sps}	I ² C STOP condition setup	4		0.6		μs
t _{vd(data)}	Valid-data time	SCL low to SDA output valid	1		1	μs
t _{vd(ack)}	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low	1		1	μs
C _b	I ² C bus capacitive load	0	400	0	400	pF

(1) C_b = total capacitance of one bus line in pF.

6.7 Oscillator Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		STANDARD MODE I ² C BUS		FAST MODE I ² C BUS		UNIT
		MIN	MAX	MIN	MAX	
t _{osc}	Oscillator start-up time from power-down or shutdown mode to fully on at 32 kHz	5		5		ms

6.8 Switching Characteristics

over recommended operating free-air temperature range, C_L ≤ 100 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I ² C BUS		FAST MODE I ² C BUS		UNIT
			MIN	MAX	MIN	MAX	
t _{pv}	Output data valid (in general-purpose output mode)	SCL	P port	400		400	ns
t _{ps}	Shutdown data valid	EN (low)	P port (high)	60		60	μs
t _w	EN pulse duration			60		60	μs

6.9 Typical Characteristics

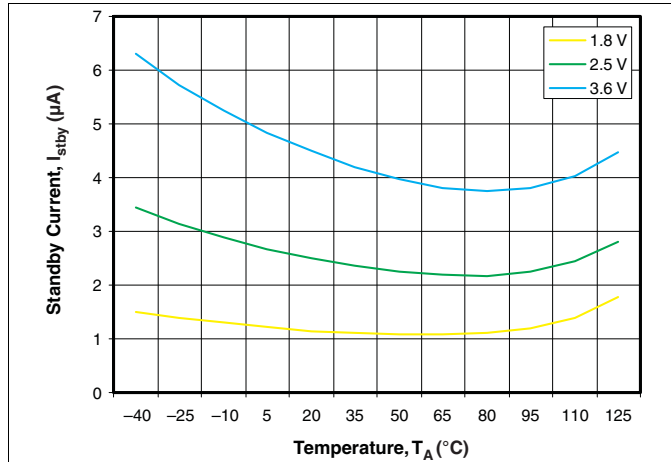


Figure 1. Standby Current vs Temperature
[EN is Low (PWM Disabled), f_{SCL} = 0]

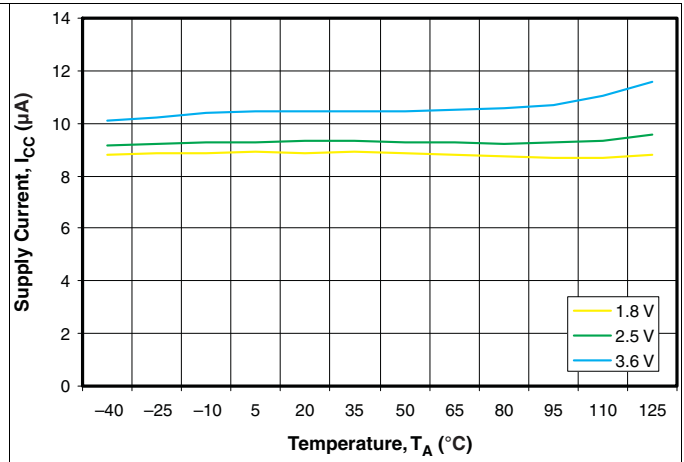


Figure 2. Supply Current vs Temperature
[EN is High (PWM Enabled), f_{SCL} = 0]

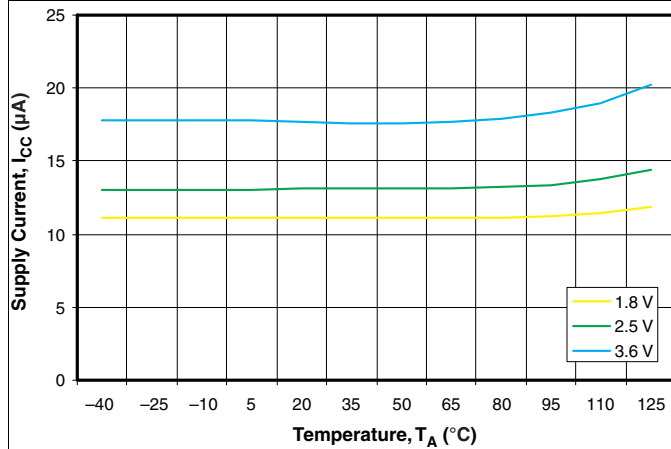


Figure 3. Supply Current vs Temperature
[EN is High (PWM Enabled), f_{SCL} = 400 kHz]

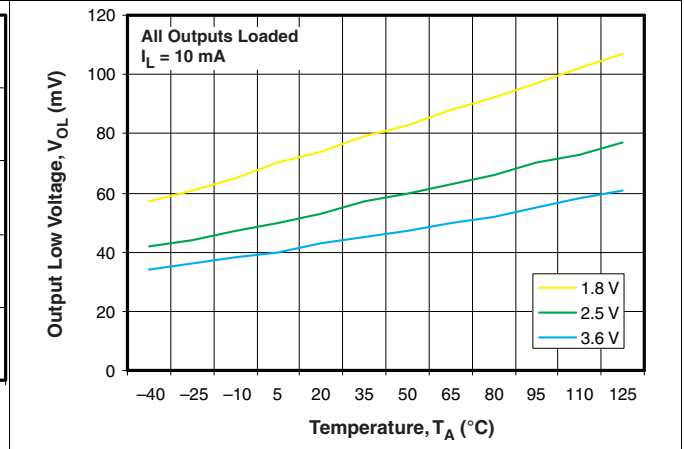


Figure 4. Port Output Low Voltage vs Temperature

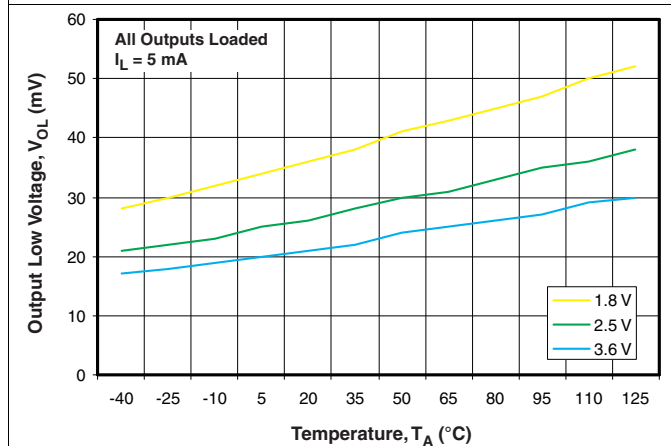


Figure 5. Port Output Low Voltage vs Temperature

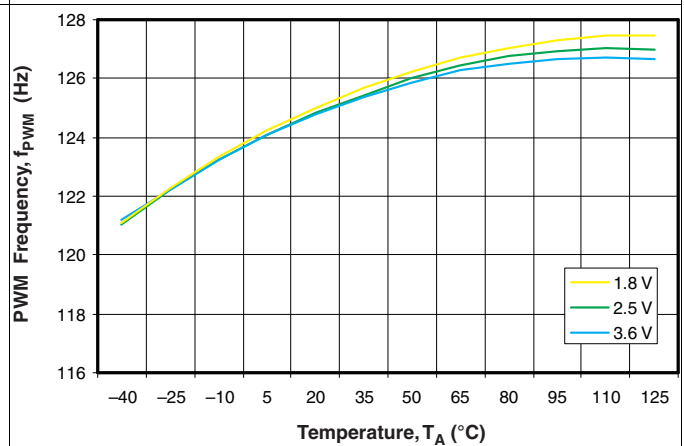


Figure 6. PWM Frequency vs Temperature

Typical Characteristics (continued)

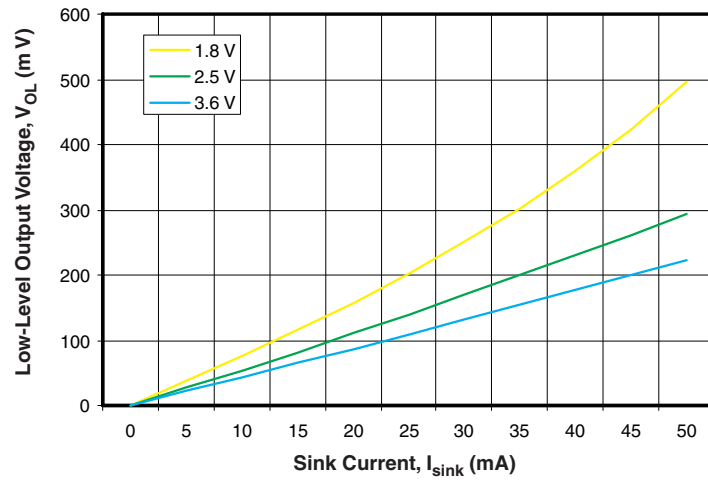
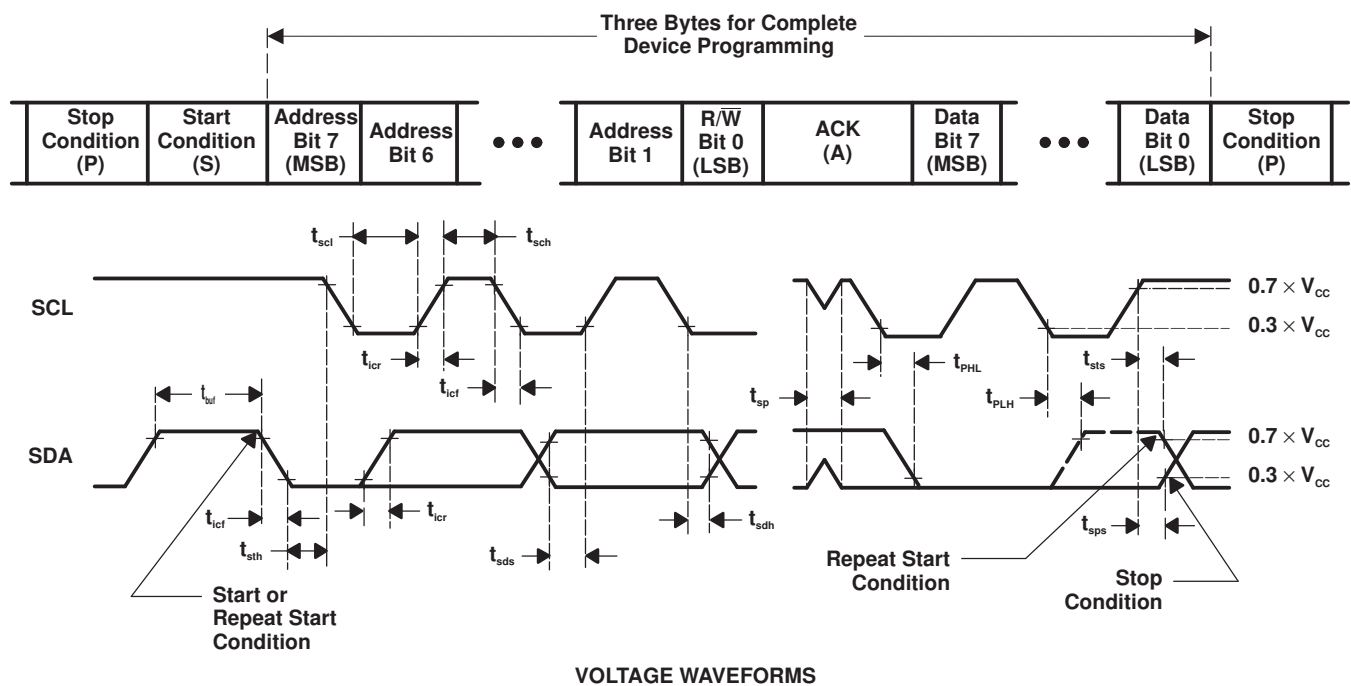
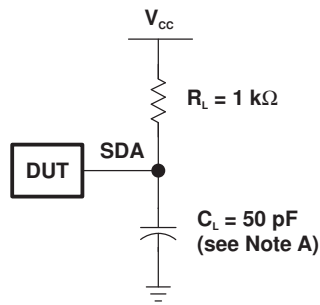


Figure 7. Output Low Voltage vs Sink Current

7 Parameter Measurement Information

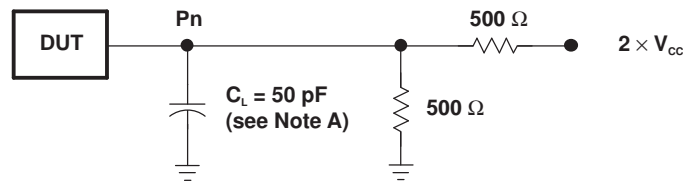


BYTE	DESCRIPTION
1	I ² C address
2	Command
3	P-port data

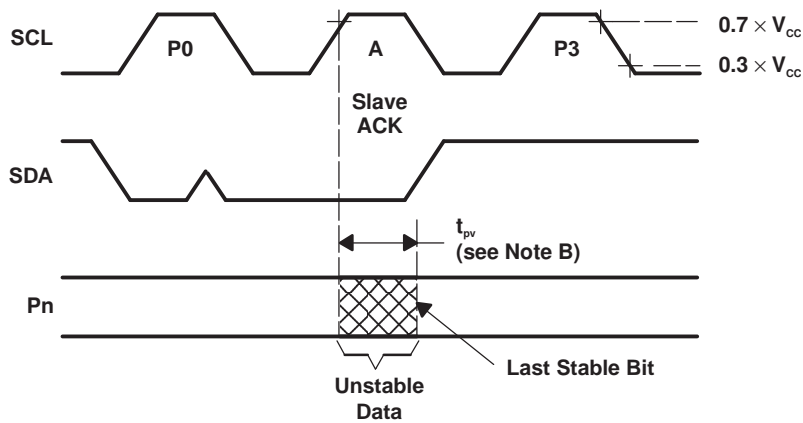
- A. C_L includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 8. I²C Interface Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE ($R/\bar{W} = 0$)

- A. C_L includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. All parameters and waveforms are not applicable to all devices.

Figure 9. P-Port Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TCA6507 can be used for driving LEDs and for general-purpose parallel output expansion. The TCA6507 has three select registers (Select0, Select1, and Select2), which can be used to configure each LED output into one of seven different operating modes. At power on, the outputs are in high impedance.

When used to drive LEDs, the seven outputs can be configured into two banks of outputs (BANK0 and BANK1). Each bank of outputs can be independently controlled for dimming rate and intensity through the I²C bus. The dimming and blink rates are fully programmable. The intensity of each bank of LEDs is controlled by dynamically varying the duty cycle of the signal, which has a period of approximately 8 ms and a pulse rate of 125 times per second, driving the outputs. The TCA6507 has two independent dimming/blinking modules—PWM0 and PWM1—driven by a single internal oscillator that supports these features. PWM0 determines the characteristics of BANK0, and PWM1 determines the characteristics of BANK1.

The TCA6507 has a master intensity level known as the ambient light detection (ALD) value. The associated pulse width modulation (PWM) signal for this value is PWMALD. The TCA6507 can be programmed such that PWMALD overrides PWM0 or PWM1, so selected LEDs are on steadily at the master intensity level. Further, the TCA6507 can be programmed such that the ALD value can override the maximum intensity values for PWM0 and PWM1. Thus, the ALD value can control the brightness of all LEDs, whether they are on steadily, or controlled by one of the dimming modules. The ALD value is stored in the lower four bits of the One-Shot / Master Intensity register.

When the I²C bus is idle, and intensity control is not used, the TCA6507 can be put into shutdown mode by setting the enable (EN) pin low. This mode provides additional power savings, as it is a low-power mode where the LEDs are off. A low signal on the EN pin also resets the registers and I²C/SMBus state machine in the TCA6507 to their default state.

An initial setup command must be sent from the I²C master to the TCA6507 to program the dimming rate and intensity (and intensity ramp if needed) for each bank of outputs. From then on, only one command from the bus master is required to turn each individual output ON, OFF, or to cycle at the programmed dimming rate. The default value for all time parameters is 256 ms, so the default blink rate is approximately one per second.

The TCA6507 is optimized for 1.65 V to 3.6 V on the SDA/SCL side, but the LEDs can be driven by any voltage up to 5.5 V. This allows the TCA6507 to interface with next-generation microprocessors and microcontrollers, where supply levels are dropping down to conserve power.

This LED dimmer supports hot insertion.

8.2 Functional Block Diagram

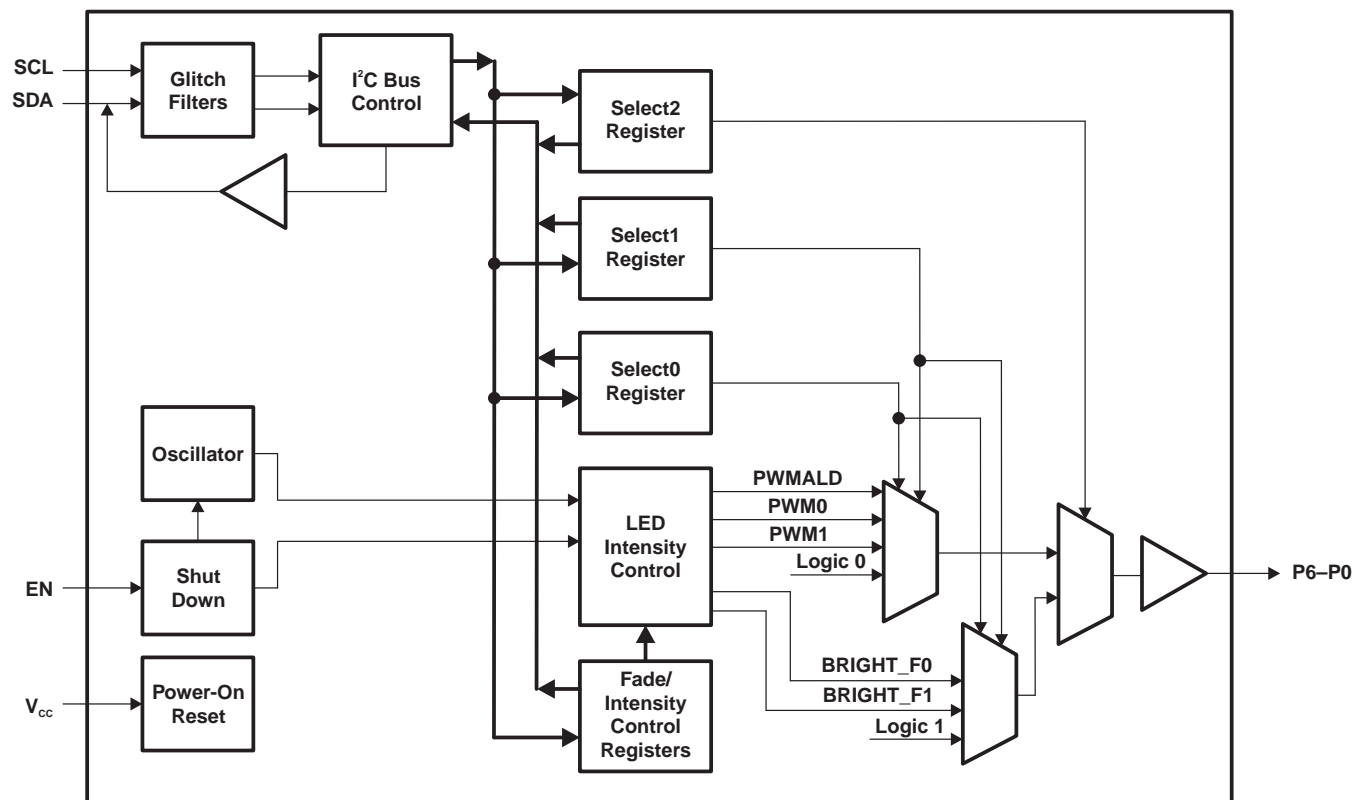
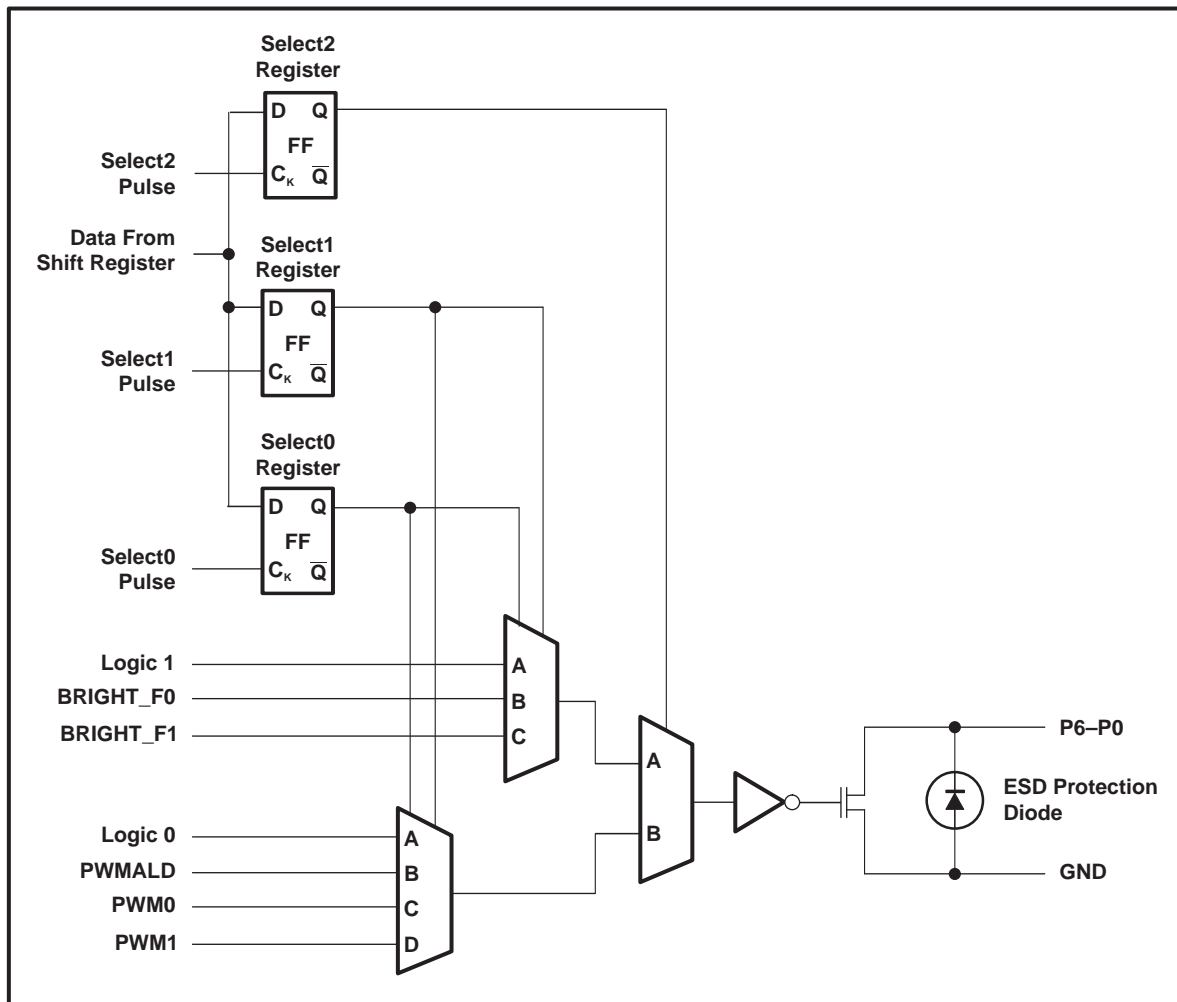


Figure 10. TCA6507 Functional Block Diagram

Functional Block Diagram (continued)

Figure 11. Output Port Simplified Schematic

8.3 Feature Description

8.3.1 Seven LED Driver Outputs

The TCA6507 features 7 outputs that can be controlled with multiple modes: ON, OFF, blinking (one of the two separate banks), and fading at a programmable rate (one of the two separate banks).

8.3.2 Open-Drain Outputs Directly Drive LEDs

The TCA6507 has open-drain outputs (see [Figure 11](#)) that are capable of sinking current up to 40 mA for LEDs.

8.3.3 Widely Programmable

The TCA6507 has two separate banks, which can be programmed to do a wide variety of blink rates, fade-ON and fade-OFF rates, as well as maximum intensity (brightness).

8.4 Device Functional Modes

8.4.1 Power-On Reset

When power (from 0 V) is applied to V_{CC} , an internal power-on reset holds the TCA6507 in a reset condition until V_{CC} has reached V_{POR} . At that point, the reset condition is released, and the TCA6507 registers and I²C/SMBus state machine initialize to their default states.

After the initial power-up phase, V_{CC} must be lowered to below 0.2 V, and then back up to the operating voltage (V_{CC}) for a power-reset cycle.

8.4.2 Enable and Reset

If the enable (EN) input is set to low, the TCA6507 is put in the standby or shutdown mode. In this mode, the oscillator is turned off, the registers are returned to their default state, and the I²C/SMBus state machine is initialized. This mode is useful for low-power consumption. An internal filtering circuit prevents negative glitches from accidentally shutting down the device. EN must be low for a minimum of approximately 60 μ s to ensure a shutdown state.

The system master can reset the TCA6507 in the event of a timeout or other improper operation by setting EN low for a minimum of approximately 60 μ s. This has the same effect as a power-on reset without powering-down the TCA6507.

The oscillator start up time (t_{OSC}) is measured from the point when EN is set high.

8.5 Programming

8.5.1 I²C Interface

The TCA6507 has a standard bidirectional I²C interface that is controlled by a master device to be configured or read the status of this device. Each slave on the I²C bus has a specific device address to differentiate between other slave devices that are on the same I²C bus. Many slave devices require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one, or multiple registers where data is stored, written, or read.

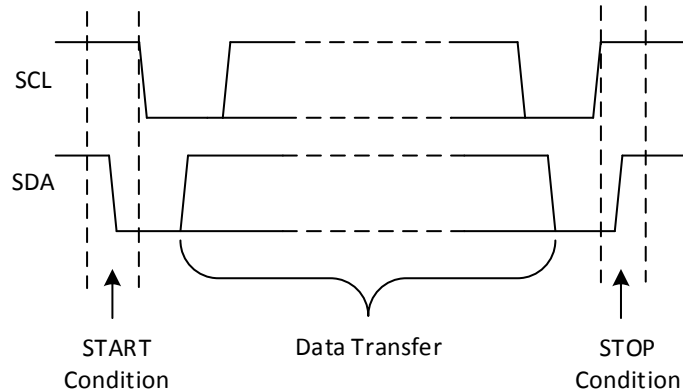
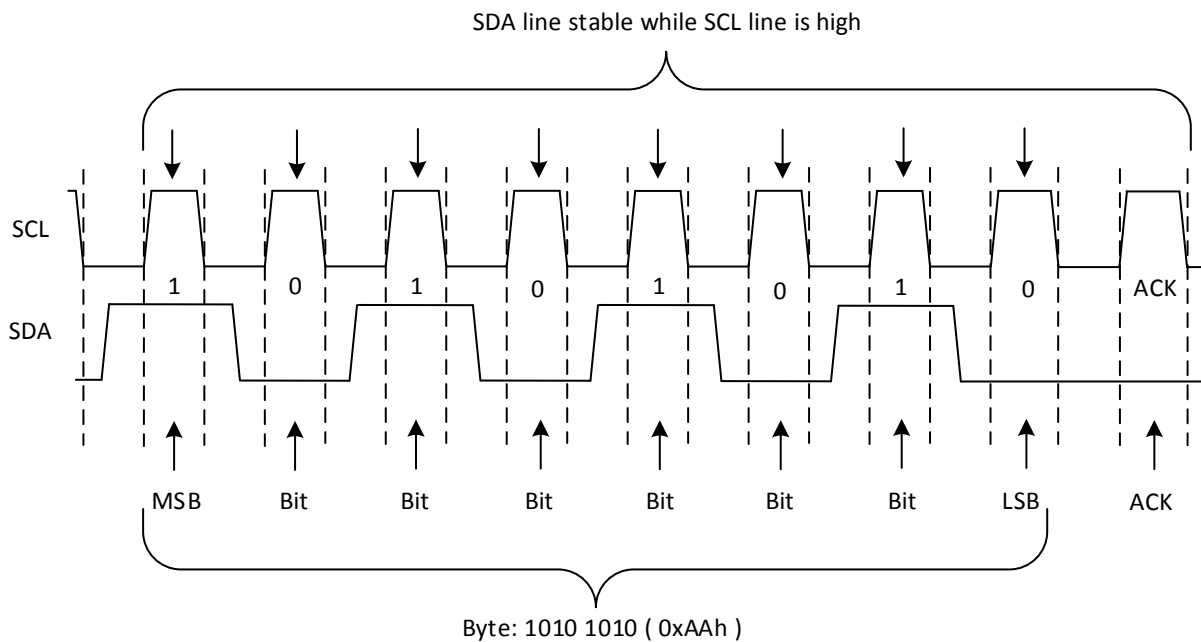
The physical I²C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V_{CC} through a pullup resistor. The size of the pullup resistor is determined by the amount of capacitance on the I²C lines. (For further details, refer to *I²C Pullup Resistor Calculation (SLVA689)*.) Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition.

The following is the general procedure for a master to access a slave device:

1. If a master wants to send data to a slave:
 - Master-transmitter sends a START condition and addresses the slave-receiver
 - Master-transmitter sends data to slave-receiver
 - Master-transmitter terminates the transfer with a STOP condition
2. If a master wants to receive or read data from a slave:
 - Master-receiver sends a START condition and addresses the slave-transmitter
 - Master-receiver sends the requested register to read to slave-transmitter
 - Master-receiver receives data from the slave-transmitter

Programming (continued)

- Master-receiver terminates the transfer with a STOP condition


Figure 12. Definition of START and STOP Conditions

Figure 13. Bit Transfer
8.5.2 Bus Transactions

Data must be sent to and received from the slave devices, and this is accomplished by reading from or writing to registers in the slave device.

Registers are locations in the memory of the slave that contain information, whether it be the configuration information, or some sampled data to send back to the master. The master must write information to these registers to instruct the slave device to perform a task.

Programming (continued)

8.5.2.1 Writes

To write on the I²C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/W bit) set to 0, which signifies a write. After the slave sends the acknowledge bit, the master then sends the register address of the register to which it wishes to write. The slave acknowledges again, letting the master know it is ready. After this, the master starts sending the register data to the slave until the master has sent all the data necessary (which can be only a single byte), and the master terminates the transmission with a STOP condition.

Figure 14 shows an example of writing a single byte to a register.

- Master controls SDA line
- Slave controls SDA line

Write to one register in a device

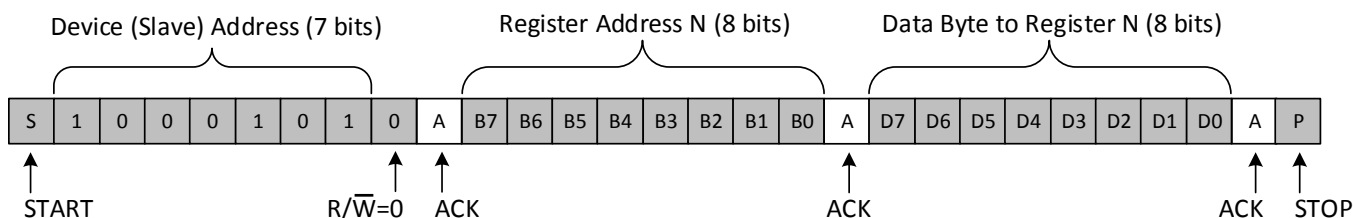


Figure 14. Write to Register

- Master controls SDA line
- Slave controls SDA line

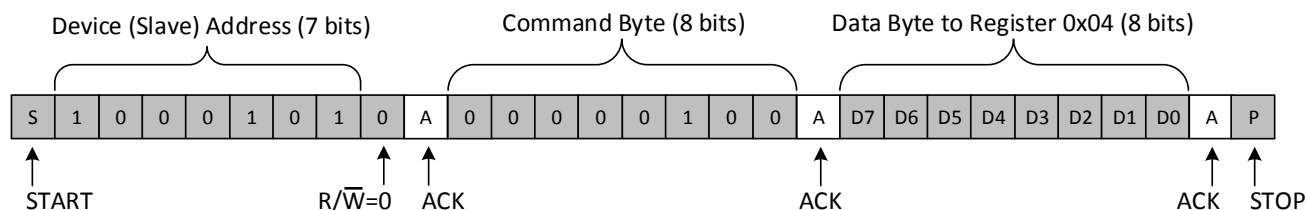


Figure 15. Write to the Fully On Register (0x04)

Programming (continued)

8.5.2.2 Reads

Reading from a slave is very similar to writing, but requires some additional steps. To read from a slave, the master must first instruct the slave which register it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/W bit equal to 0 (signifying a write), followed by the register address it wishes to read from. Once the slave acknowledges this register address, the master sends a START condition again, followed by the slave address with the R/W bit set to 1 (signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus, but continues supplying the clock to the slave. During this part of the transaction, the master becomes the master-receiver, and the slave becomes the slave-transmitter.

The master continues to send out the clock pulses, but releases the SDA line so that the slave can transmit data. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data. Once the master has received the number of bytes it is expecting, it sends a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

Figure 16 shows an example of reading a single byte from a slave register.

- Master controls SDA line
- Slave controls SDA line

Read from one register in a device

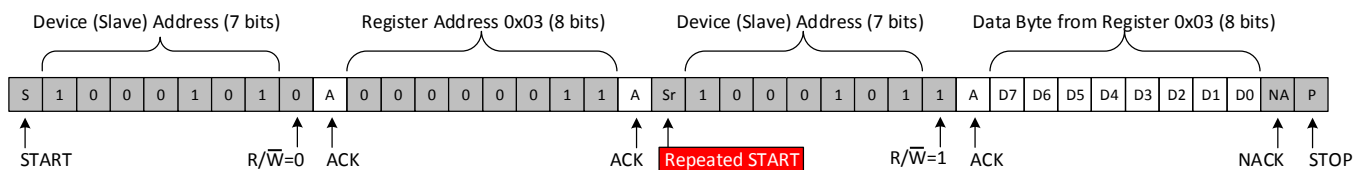


Figure 16. Read From Register Example

8.5.3 Device Address

The address of the TCA6507 is shown in Figure 17.



Figure 17. TCA6507 Address

The last bit of the slave address defines the operation (read or write) to be performed. High (1) selects a read operation, and low (0) selects a write operation.

Table 2. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I ² C slave address	1	0	0	0	1	0	1	R/W
Px I/O data bus	X ⁽¹⁾	P6	P5	P4	P3	P2	P1	P0

(1) X = Don't care.

8.5.4 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the control register. The last four bits (B0, B1, B2 and B3) of this command byte determine the internal registers (Select0, Select1, Select2, Fade-ON Time, Fully-ON Time, Fade-OFF Time, First Fully-OFF Time, Second Fully-OFF Time, Maximum Intensity and Initialization) that are affected. The command byte is sent only during a write transmission.

After the command byte is received, the I²C master starts sending data bytes. The first data byte goes into the internal register defined by the command byte. Bit B4 in the command byte is used to determine the programming mode. If B4 is low, all data bytes are written to the register defined by B0, B1, B2, and B3. If B4 is high, the last four bits of the command byte are automatically incremented after the byte is written, and the next data byte is stored in the corresponding register. Registers are written in the sequence shown in [Table 6](#). Once the Initialization register (register 0x0A) is written to, the command byte returns to 0 (Select0 register).

The upper three bits (B7–B5) of the command byte must be programmed as zeroes for proper operation.

If a STOP condition occurs after the command byte is received, the TCA6507 stores the command byte and then remains idle until the I²C master sends the next operation.

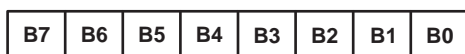


Figure 18. Control Register Bits

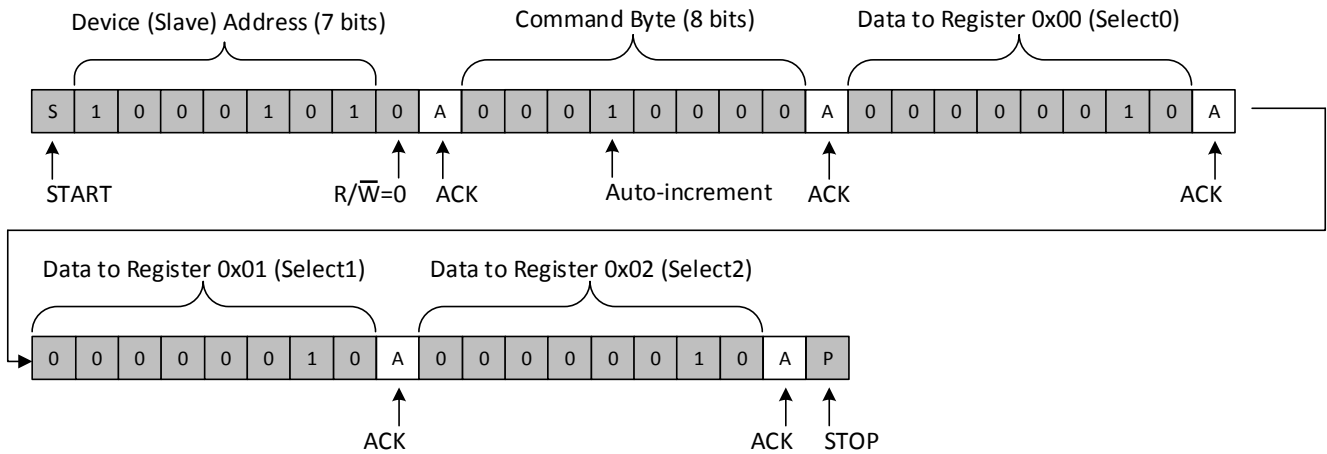
Table 3. Command Byte

BIT	FUNCTION
B7	Reserved. Must be programmed as 0.
B6	Reserved. Must be programmed as 0.
B5	Reserved. Must be programmed as 0.
B4	Auto increment. 1 = Auto increment enabled. 0 = Auto increment disabled.
B3	Register address 3.
B2	Register address 2.
B1	Register address 1.
B0	Register address 0.

8.5.5 Auto-Increment Mode

In auto-increment mode, the last four bits of the command byte are automatically incremented after the byte is written, and the next data byte is stored in the corresponding register.

- Master controls SDA line
- Slave controls SDA line



The registers are written to in the order shown in [Table 6](#).

8.5.6 LED Operation

For LED states, see [Figure 10](#) and [Table 8](#).

It is the combination of Select2, Select1, and Select0 registers that gives the state of the LED or Px.

Bit 0 from the Select0 register, bit = 0 from Select1 register, and bit=0 from the Select2 register provide the state for P0, or the first LED. Similarly, bit = 1 from the Select0 register, bit 1 from Select1 register, and bit = 1 from the Select2 register provide the state for P1, or the second LED (see [Table 4](#)).

Table 4. LED Operation

	MSB							LSB
Select0	X	0	0	0	0	0	0	0
Select1	X	0	0	0	0	0	0	0
Select2	X	0	0	0	0	0	0	0
Output or LED affected	X	P6 7th LED	P5 6th LED	P4 5th LED	P3 4th LED	P2 3rd LED	P1 2nd LED	P0 1st LED

8.5.7 Blinking Pattern Control

The Fade-ON time, Fully-ON time, Fade-OFF time, First Fully-OFF time, and Second Fully-OFF time registers must be written to for basic blink control. Each of these registers has eight bits – top four bits for BANK1 (or PWM1), and bottom four bits for BANK0 (or PWM0) (see [Table 20](#)).

Each BANK or PWM has a default value of 4 (4b0100), which translates to a time of 256 ms. The largest value for each BANK or PWM is 15 (4b1111), which translates to a time of 16320 ms (see [Figure 19](#) and [Table 5](#)).

Table 5. Intensity Parameters (see [Figure 19](#))

REGION	PARAMETER NAME	PARAMETER RANGE	REGISTER RANGE	REGISTER NAME	REGISTER
A1, A2	Fade-ON time	0 to 16320 ms (exponential trend)	0 to 15	Fade-ON time	0x03

Table 5. Intensity Parameters (see Figure 19) (continued)

REGION	PARAMETER NAME	PARAMETER RANGE	REGISTER RANGE	REGISTER NAME	REGISTER
B1, B2	Fully-ON time	0 to 16320 ms (exponential trend)	0 to 15	Fully-ON time	0x04
C1, C2	Fade-OFF time	0 to 16320 ms (exponential trend)	0 to 15	Fade-OFF time	0x05
D	First fully-OFF time	0 to 16320 ms (exponential trend)	0 to 15	First fully-OFF time	0x06
E	Second fully-OFF time	0 to 16320 ms (exponential trend)	0 to 15	Second fully-OFF time	0x07
F	Maximum intensity	0 to 100%	0 to 15	Maximum intensity	0x08

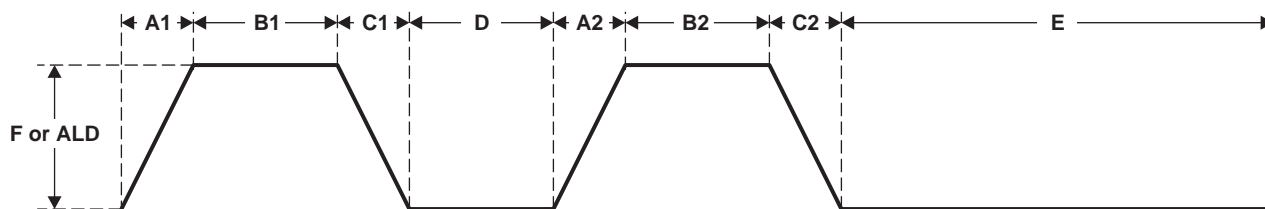


Figure 19. LED Pattern Sections Per Bank

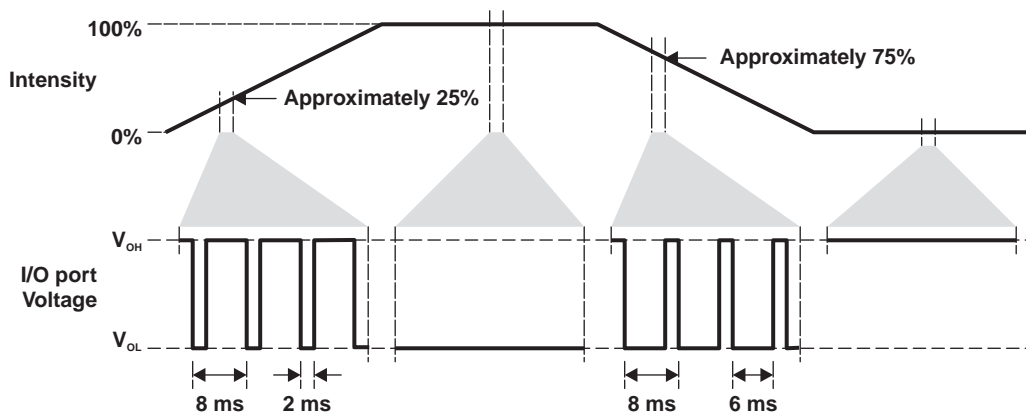


Figure 20. Output Port Voltage vs LED Intensity, Maximum Intensity = 100%

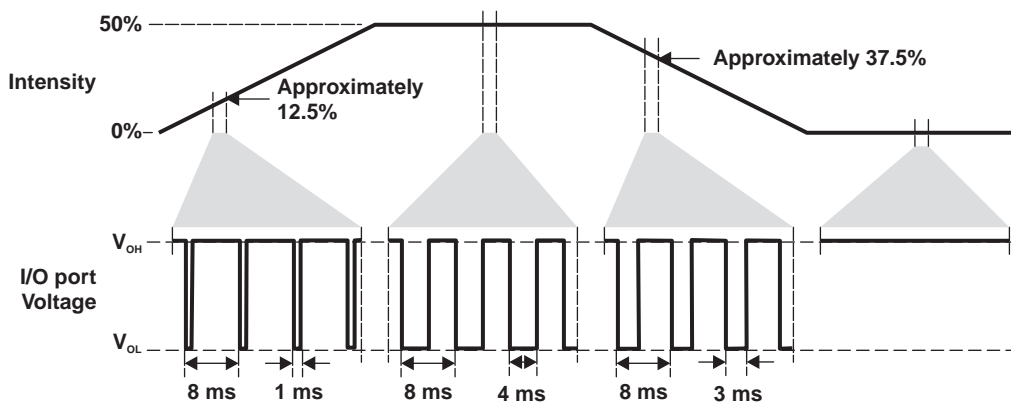


Figure 21. Output Port Voltage vs LED Intensity, Maximum Intensity = 50%

8.5.8 Intensity Control

The Maximum Intensity registers must be written to for setting the intensity of the LED. This register has eight bits – top four bits for BANK1 (or PWM1), and bottom four bits for BANK0 (or PWM0). This register can be written to after sending data to the Second Fully-OFF Time register (see [Table 20](#)).

The Maximum Intensity register has a default value of 15 (1111), which translates to 100% brightness (see [Figure 19](#) and [Table 5](#)).

8.6 Register Maps

Table 6. Control Register Description

CONTROL REGISTER BITS				COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT (BINARY)
B3	B2	B1	B0				
0	0	0	0	0x00	Select0	Read/write byte	0000 0000
0	0	0	1	0x01	Select1	Read/write byte	0000 0000
0	0	1	0	0x02	Select2	Read/write byte	0000 0000
0	0	1	1	0x03	Fade-ON Time	Read/write byte	0100 0100
0	1	0	0	0x04	Fully-ON Time	Read/write byte	0100 0100
0	1	0	1	0x05	Fade-OFF Time	Read/write byte	0100 0100
0	1	1	0	0x06	First Fully-OFF Time	Read/write byte	0100 0100
0	1	1	1	0x07	Second Fully-OFF Time	Read/write byte	0100 0100
1	0	0	0	0x08	Maximum Intensity	Read/write byte	1111 1111
1	0	0	1	0x09	One Shot / Master Intensity	Read/write byte	0000 1111
1	0	1	0	0x0A	Initialization	Write byte	N/A

The Select0 register (register 0x00), Select1 (register 0x01), and Select2 register (register 0x02) configure the state of each of the outputs (see [Table 8](#)).

Registers that define time periods have a range of 0 to 16320 ms, as defined in [Table 7](#).

Table 7. Time Parameters

CODE (DECIMAL)	TIME (ms)
0	0
1	64
2	128
3	192
4 (default)	256
5	384
6	512
7	768
8	1024
9	1536
10	2048
11	3072
12	4096
13	5760
14	8128
15	16320

8.6.1 Registers 0x00 - 0x02 (Select Registers)

Table 8. Select2, Select1, and Select0 Register States

SELECT2	SELECT1	SELECT0	STATE
0	0	0	LED off (high impedance).
0	0	1	LED off (high impedance).
0	1	0	LED on with maximum intensity value of PWM0 (ALD value or BRIGHT_F0 value, depending on One Shot / Master Intensity Register setting).
0	1	1	LED on with maximum intensity value of PWM1 (ALD value or BRIGHT_F1 value, depending on One Shot / Master Intensity Register setting).
1	0	0	LED fully on (output low). Can be used as general-purpose output.
1	0	1	LED on at brightness set by One Shot / Master Intensity register.
1	1	0	LED blinking with intensity characteristics of BANK0 (PWM0).
1	1	1	LED blinking with intensity characteristics of BANK1 (PWM1).

Table 9. Register 0x00 (Select0 Register)

BIT	S0-7	S0-6	S0-5	S0-4	S0-3	S0-2	S0-1	S0-0
DEFAULT	X ⁽¹⁾	0	0	0	0	0	0	0

(1) X = Don't care.

Table 10. Register 0x01 (Select1 Register)

BIT	S1-7	S1-6	S1-5	S1-4	S1-3	S1-2	S1-1	S1-0
DEFAULT	X ⁽¹⁾	0	0	0	0	0	0	0

(1) X = Don't care.

Table 11. Register 0x02 (Select2 Register)

BIT	S2-7	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1	S2-0
DEFAULT	X ⁽¹⁾	0	0	0	0	0	0	0

(1) X = Don't care.

To use a P port as a general-purpose output, Select1 and Select0 registers must be set low (or 0), and then the inverse of the data written to the Select2 bit appears on the open-drain output.

The intensity of each bank of LEDs can be customized by programming six registers: Fade-ON Time, Fully-ON Time, Fade-OFF Time, First Fully-OFF Time, Second Fully-OFF Time, and Maximum Intensity registers. Each bank is designed to produce two identical intensity pulses per blink cycle. Both pulses have the same fade-ON, fully-ON and fade-OFF times, but independent fully-OFF times to achieve a double-blink effect when desired.

The Fade-ON Time register (register 0x03) defines the time from the fully-OFF state to the fully-ON state for the LED per region A in [Figure 19](#). The first four bits (C7–C4) in this register set the fade-ON time for BANK1, and the next four bits (C3–C0) set the fade-ON time for BANK0. The data for each bank is a binary number between 0 and 15. For BANK1, the MSB is bit C7, while the least significant bit (LSB) is bit C4. For BANK0, the MSB is bit C3 while the LSB is bit C0. See [Table 7](#) for more information.

8.6.2 Register 0x03 (Fade-ON Time)

Table 12. Register 0x03 (Fade-ON Time Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	0	1	0	0	0	1	0	0

The Fully-ON Time register (register 4) defines the time spent at maximum intensity between the fade-ON state and fade-OFF state for the LED per region B in [Figure 19](#). The first four bits (C7–C4) in this register set the fully-ON time for BANK1, and the next four bits (C3–C0) set the fully-ON time for BANK0. The data for each bank is a binary number between 0 and 15. For BANK1, the MSB is bit C7, while the LSB is bit C4. For BANK0, the most significant bit (MSB) is bit C3, while the LSB is bit C0.

See [Table 7](#) for more information on the possible time values.

8.6.3 Register 0x04 (Fully-ON Time)

Table 13. Register 0x04 (Fully-ON Time Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	0	1	0	0	0	1	0	0

The Fade-OFF Time register (register 5) defines the time from the fully-ON state to the fully-OFF state for the LED per region C in [Figure 19](#). The first four bits (C7–C4) in this register set the fade-OFF time for BANK1, and the next four bits (C3–C0) set the fade-OFF time for BANK0. The data for each bank is a binary number between 0 and 15. For BANK1, the MSB is bit C7, while the LSB is bit C4. For BANK0, the MSB is bit C3, while the least significant bit (LSB) is bit C0.

See [Table 7](#) for more information on the possible time values.

8.6.4 Register 0x05 (Fade-OFF Time)

Table 14. Register 0x05 (Fade-OFF Time Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	0	1	0	0	0	1	0	0

The first and second Fully-OFF Time registers (registers 6 and 7) define the time spent at zero intensity (in the fully-OFF state of the LED) per region D and E, respectively, in [Figure 19](#). The first four bits (C7–C4) in this register set the fully-OFF time for BANK1, and the next four bits (C3–C0) set the fully-OFF time for BANK0. The data for each bank is a binary number between 0 and 15. For BANK1, the MSB is bit C7, while the LSB is bit C4. For BANK0, the MSB is bit C3, while the LSB is bit C0.

See [Table 7](#) for more information on the possible time values.

8.6.5 Register 0x06 - 0x07 (Fully-OFF Time)

Table 15. Register 0x06 (First Fully-OFF Time Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	0	1	0	0	0	1	0	0

Table 16. Register 0x07 (Second Fully-OFF Time Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	0	1	0	0	0	1	0	0

The Maximum Intensity register defines the duty cycle of the waveform driving the LED in its fully-ON state per region F in [Figure 19](#). The first four bits (C7–C4) in this register set the duty cycle for BANK1 and the next four bits (C3–C0) set the duty cycle for BANK0. The data for each bank is a binary number between 0 and 15. For BANK1, the MSB is bit C7, while the LSB is bit C4. For BANK0, the MSB is bit C3, while the LSB is bit C0. The values in this register also define the LED intensity indicated by the BRIGHT_F0 or BRIGHT_F1 modes. The intensity of each LED is updated 125 times per second (every 8 ms with a 32-kHz clock).

See [Table 7](#) for more information on the possible time values.

8.6.6 Register 0x08 (Maximum Intensity per Bank)

Table 17. Register 0x08 (Maximum Intensity Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

The Maximum Intensity register defines the maximum intensity per PWM bank. The values in this register are used if the One-Shot / Master Intensity Register bits are set to 0 for the corresponding bank. If they are set to 1 (ALD value), then the maximum brightness is defined by the ALD value.

The values for each value are shown in [Table 18](#).

Table 18. Brightness Register Values

Code		Brightness
Decimal	Nibble (Hex)	
0	0x0	0 %
1	0x1	6.66%
2	0x2	13.32%
3	0x3	19.98%
4	0x4	26.64 %
5	0x5	33.33 %
6	0x6	39.96 %
7	0x7	46.62 %
8	0x8	53.28 %
9	0x9	59.94 %
10	0xA	66.66 %
11	0xB	73.26 %
12	0xC	79.92 %
13	0xD	86.58 %
14	0xE	93.24 %
15	0xF	100 %

8.6.7 Register 0x09 (One-Shot / Master Intensity)

The One-Shot / Master Intensity register (register 9) (see [Table 19](#)) is an 8-bit register with three functions.

Bits 0–3 set the master intensity value (ALD). It is a binary number between 0 and 15.

Bits 4–5 determine whether the maximum intensity of PWM0 and PWM1 is set by the programmed F value (BRIGHT_F0 or BRIGHT_F1) or the master ALD value. The default value for these bits is 0. Bit 4 supports PWM0 and bit 5 is for PWM1. If bit 4 (or bit 5) is 0, the maximum intensity value for PWM0 (or PWM1) is set by the F value. If bit 4 (or bit 5) is 1, the maximum intensity value for PWM0 (or PWM1) is set by the master ALD value. This allows the user to vary the brightness of all LEDs by changing a single register.

Bits 6–7 determine whether each PWM operates in normal or one-shot mode. Bit 6 supports PWM0 and bit 7 is for PWM1. If bit 6 (or bit 7) is 0, PWM0 (or PWM1) operates in the normal mode where the LEDs goes through the full intensity cycle defined by [Table 5](#) and [Figure 19](#). If bit 6 (or bit 7) is 1, PWM0 (or PWM1) operate in the one-shot mode. In this mode, the LEDs can be used to create a single-shot lighting effect where the LED intensity is valid for a particular segment of the cycle shown in [Table 5](#) and [Figure 19](#).

Table 19. One-Shot / Master Intensity Register

BIT	DESCRIPTION
0–3	Master intensity (ALD) value. Valid values are 0 to 15. See Table 18 for more information

Table 19. One-Shot / Master Intensity Register (continued)

BIT	DESCRIPTION
4	Determines whether maximum intensity of PWM0 is set by the programmed F value or the master ALD value 0 = F value 1 = ALD value
5	Determines whether maximum intensity of PWM1 is set by the programmed F value or the master ALD value 0 = F value defined in Maximum Intensity per Bank Register (0x08) 1 = ALD value
6	Determines if PWM0 operates in normal or one-shot mode 0 = Normal mode 1 = One-shot mode
7	Determines if PWM1 operates in normal or one-shot mode 0 = Normal mode 1 = One-shot mode

8.6.8 Register 0x0A (Initialization Register)

The Initialization register (register 0x0A) determines whether to initialize each PWM and, if so, provides the starting point of the LED intensity cycle for each bank. Bits 0–3 (C0–C3) are for BANK0 and bits 4–7 (C4–C7) are for BANK1.

Bits 0–2 provide the starting point for PWM0. If bit 3 is high (or 1), it initializes PWM0.

Bits 4–6 provide the starting point for PWM1. If bit 7 is high (or 1), it initialized PWM1.

In the one-shot mode for BANK0, the LEDs start at the beginning of the region defined by C2, C1, and C0 in the Initialization register and, when it reaches the end of that region, the LED stays at that intensity level defined at the end of the region. When the stop point is reached, all P ports attached to PWM0 disconnect from PWM0, and stay at either the maximum intensity level for PWM0 (BRIGHT_F0 or ALD value), or the OFF state. The bits in the Select2 and Select1 registers change to reflect the final state of the LED at that time. PWM0 continues running, and is free to be used by other LEDs. The one-shot mode works similarly for BANK1.

Upon writing to this register, each bank is initialized to the state listed in [Table 21](#) and [Table 22](#).

Table 20. Register 0x0A (Initialization Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0

Table 21. Bank 1 Initialization Register

C7	C6	C5	C4	INTENSITY CYCLE
1	0	0	0	Beginning at region A1 in Table 5 and Figure 18
1	0	0	1	Beginning at region B1 in Table 5 and Figure 18
1	0	1	0	Beginning at region C1 in Table 5 and Figure 18
1	0	1	1	Beginning at region D in Table 5 and Figure 18
1	1	0	0	Beginning at region A2 in Table 5 and Figure 18
1	1	0	1	Beginning at region B2 in Table 5 and Figure 18
1	1	1	0	Beginning at region C2 in Table 5 and Figure 18
1	1	1	1	Beginning at region E in Table 5 and Figure 18

Table 22. Bank 0 Initialization Register

C3	C2	C1	C0	STARTING POINT OF INTENSITY CYCLE
1	0	0	0	Beginning at region A1 in Table 5 and Figure 18
1	0	0	1	Beginning at region B1 in Table 5 and Figure 18
1	0	1	0	Beginning at region C1 in Table 5 and Figure 18
1	0	1	1	Beginning at region D in Table 5 and Figure 18
1	1	0	0	Beginning at region A2 in Table 5 and Figure 18
1	1	0	1	Beginning at region B2 in Table 5 and Figure 18
1	1	1	0	Beginning at region C2 in Table 5 and Figure 18
1	1	1	1	Beginning at region E in Table 5 and Figure 18

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

9.1 Application Information

Applications of the TCA6507 contains an I²C (or SMBus) master device. The TCA6507 is used to control the blinking pattern of LEDs or as a general purpose output.

9.2 Typical Application

Figure 22 shows a general application in which the TCA6507 can be used. Each LED output is driving one LED. Figure 25 highlights another application where the TPS61052 boost converter and high-power LED driver and TCA6507 7-bit LED driver can be used in combination for applications requiring flashlight functionality and/or high-brightness indicator/backlight LEDs.

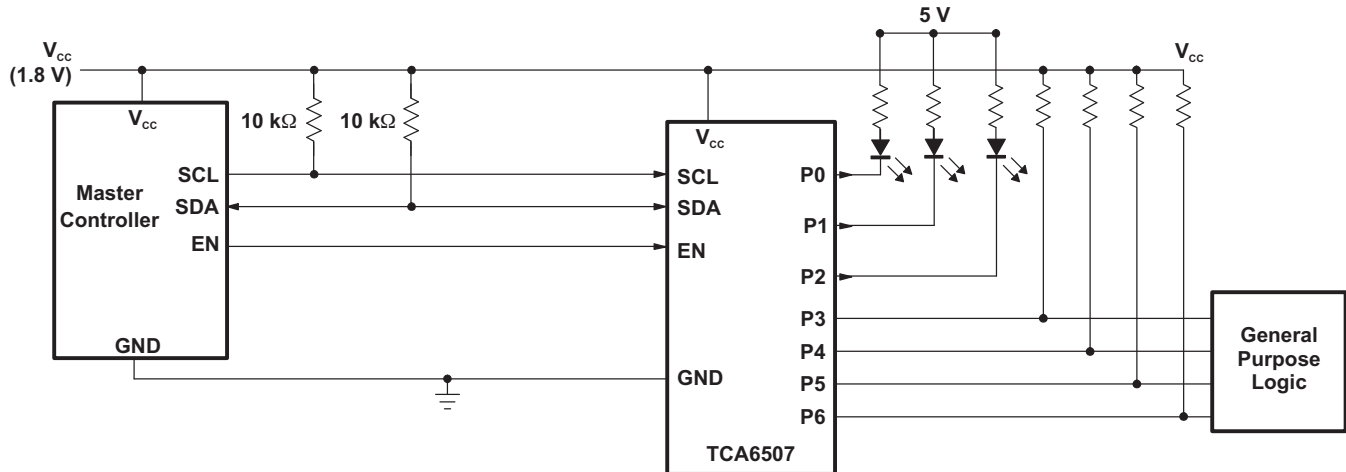


Figure 22. Typical Application

9.2.1 Design Requirements

For the typical application example, the TCA6507 is set up to blink the P0 with Bank0 pattern, P1 fully on, and P2 with Bank1 blinking pattern. The banks is setup to the flashing pattern defined in Figure 23. The options for lengths of time for each section can be seen in Table 7.

Typical Application (continued)

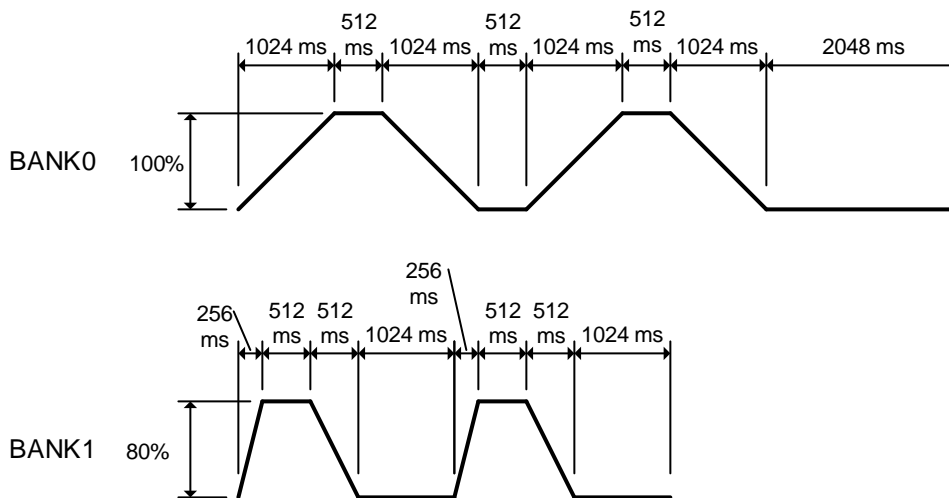


Figure 23. Blinking Pattern for the Two Banks

9.2.2 Detailed Design Procedure

For the typical application blinking pattern seen in Figure 23, the desired values are listed in Table 23, with the corresponding registers and values.

Table 23. LED Pattern

SECTION	BANK1 VALUE	BANK0 VALUE	UNIT	REGISTER	BANK1 NIBBLE (HEX)	BANK0 NIBBLE (HEX)	REGISTER VALUE (HEX)
Fade-ON time	256	1024	ms	0x03	0x4	0x8	0x48
Fully-ON time	512	512	ms	0x04	0x6	0x6	0x66
Fade-OFF time	512	1024	ms	0x05	0x6	0x8	0x68
First fully-OFF time	1024	512	ms	0x06	0x8	0x6	0x86
Second fully-OFF time	1024	2048	ms	0x07	0x8	0xA	0x8A
Maximum brightness	62.5	100	%	0x08	0x9	0xF	0x9F

The select register values are shown in Table 24.

Table 24. Select Registers

REGISTER		VALUE (BINARY)	VALUE (HEX)
NAME	ADDRESS		
SELECT0	0x00	8b0000 0100	0x04
SELECT1	0x01	8b0000 0101	0x05
SELECT2	0x02	8b0000 0111	0x07

With the above values for the appropriate registers, the next step must be to write the values to the device. This can be accomplished very easily with the auto-increment feature (see *Auto-Increment Mode* for more information).

Table 25. Writing to Registers

BYTE #	BYTE	DESCRIPTION
1	0x89	Address and write bit
2	0x10	Command byte with auto-increment
3	0x04	Write to SELECT0 register
4	0x05	Write to SELECT1 register
5	0x06	Write to SELECT2 register
6	0x48	Write to Fade-ON Time register
7	0x66	Write to Fully-ON Time register
8	0x68	Write to Fade-OFF Time register
9	0x86	Write to First Fully-OFF Time register
10	0x8A	Write to Second Fully-OFF Time register
11	0x9F	Write to Maximum Brightness register

After the above bytes are written to the device, the LEDs blinks according to the defined pattern.

9.2.3 Application Curve

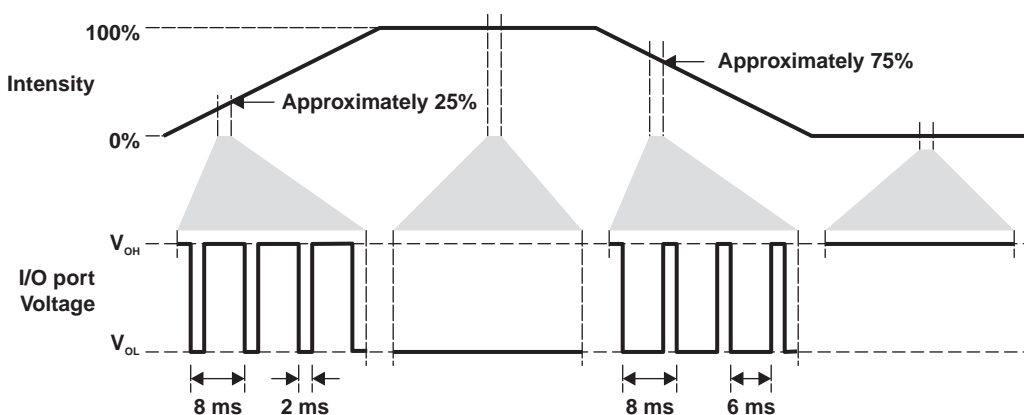


Figure 24. Output Port Voltage vs LED Intensity, Maximum Intensity = 100%

9.3 System Example

Figure 25 highlights another application where the TPS61052 boost converter and high-power LED driver and TCA6507 7-bit LED driver can be used in combination for applications requiring flashlight functionality, high-brightness indicator and backlight LEDs, or both.

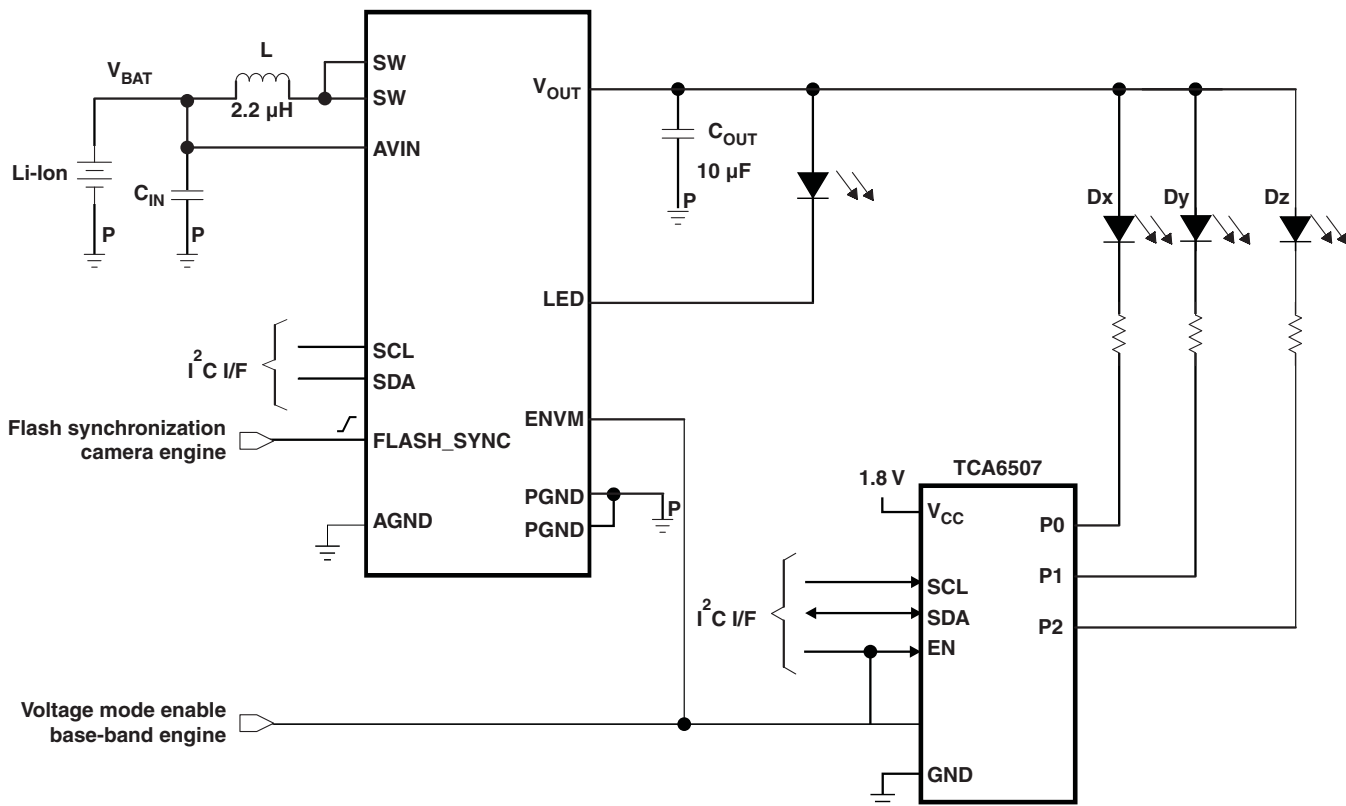


Figure 25. White LED Flashlight Driver and High-Brightness LED Indicator/Backlight Power Supply

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA6507 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 26](#) and [Figure 27](#).

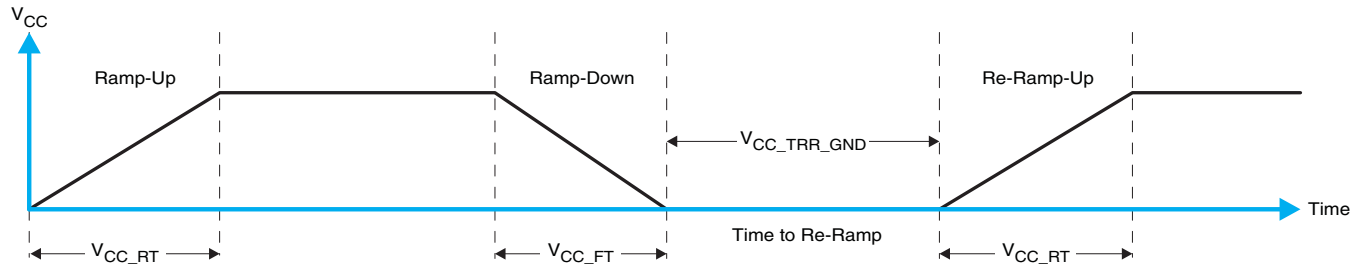


Figure 26. V_{CC} Is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}

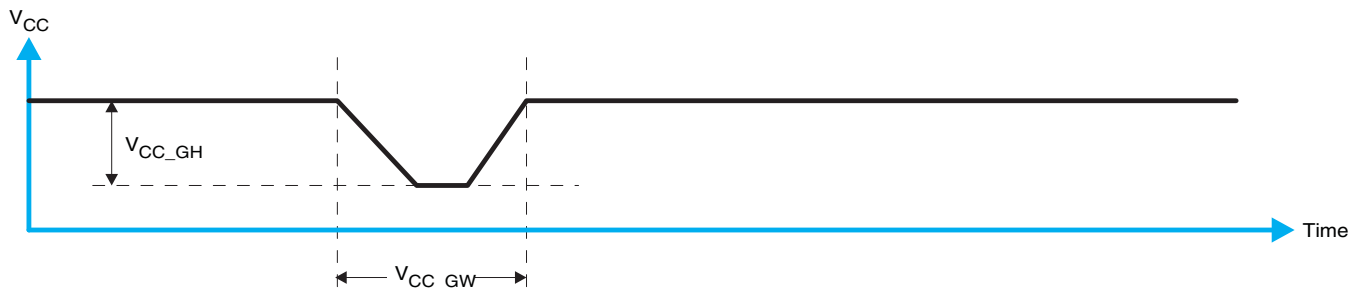


Figure 27. V_{CC} Is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

[Recommended Supply Sequencing and Ramp Rates](#) specifies the performance of the power-on reset feature for TCA6507 for both types of power-on reset.

10.1.1 Recommended Supply Sequencing and Ramp Rates

$T_A = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 26	1	100	ms
V_{CC_RT}	Rise rate	See Figure 26	0.01	100	ms
$V_{CC_TRR_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See Figure 26	0.001		ms
$V_{CC_TRR_POR50}$	Time to re-ramp (when V_{CC} drops to $V_{POR_MIN} - 50\text{ mV}$)	See Figure 27	0.001		ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when $V_{CCX_GW} = 1\ \mu\text{s}$	See Figure 28		1.2	V
V_{CC_GW}	Glitch width that does not cause a functional disruption when $V_{CCX_GH} = 0.5 \times V_{CCX}$	See Figure 28			μs
V_{PORF}	Voltage trip point of POR on falling V_{CC}	0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}	1.033		1.428	V

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}), and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 28](#) and [Recommended Supply Sequencing and Ramp Rates](#) provide more information on how to measure these specifications.

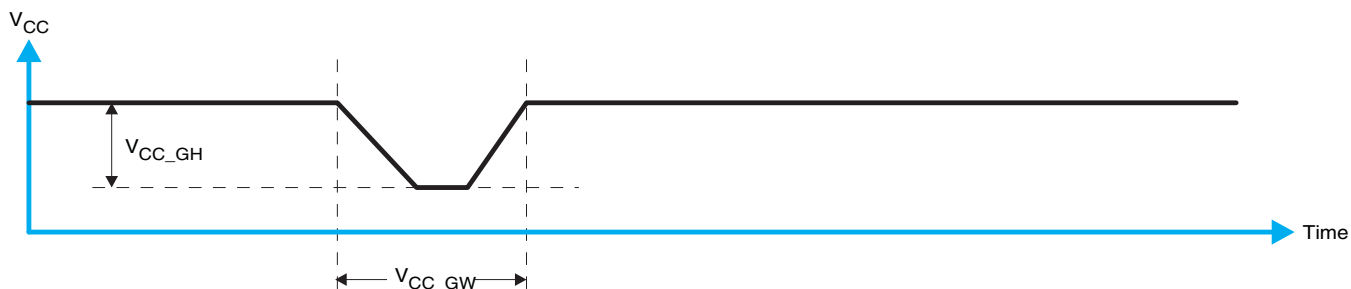


Figure 28. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. [Figure 29](#) and [Recommended Supply Sequencing and Ramp Rates](#) provide more details on this specification.

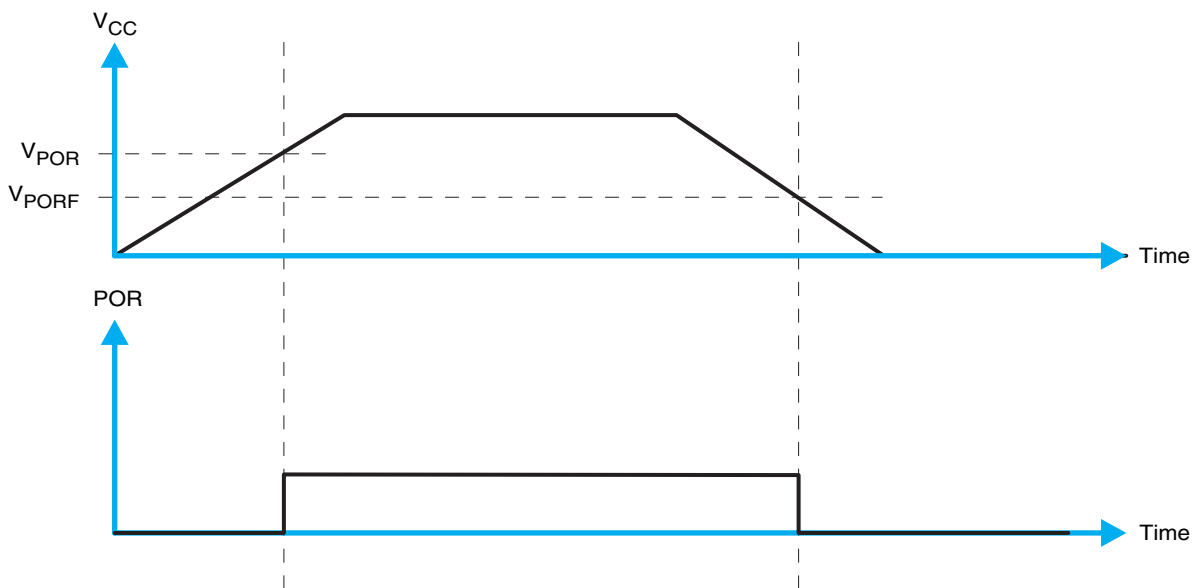


Figure 29. V_{POR}

11 Layout

11.1 Layout Guidelines

For PCB layout of the TCA6507, common PCB layout practices must be followed, but additional concerns related to high-speed data transfer, such as matched impedances and differential pairs, are not a concern for I²C signals speeds. It is common to have a dedicated ground plane on an inner layer of the board, and pins that are connected to ground must have a low-impedance path to the ground plane in the form of wide polygon pours, and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch, and a smaller capacitor to filter out high-frequency ripple.

11.2 Layout Example

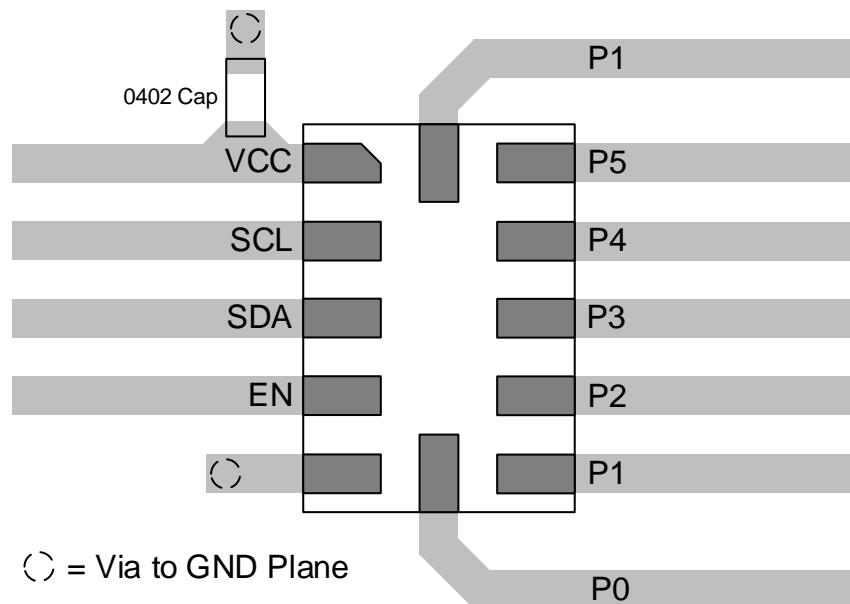


Figure 30. RUE Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *I2C Bus Pullup Resistor Calculation*, [SLVA689](#)
- *Introduction to Logic*, [SLVA700](#)
- *Maximum Clock Frequency of I2C Bus Using Repeaters*, [SLVA695](#)
- *Programming Fun Lights With the TI TCA6507*, [SCPA043](#)
- *Understanding the I2C Bus*, [SLVA704](#)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA6507PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH507	Samples
TCA6507PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH507	Samples
TCA6507PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH507	Samples
TCA6507PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH507	Samples
TCA6507RUER	ACTIVE	X2QFN	RUE	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2M	Samples
TCA6507ZXUR	ACTIVE	BGA MICROSTAR JUNIOR	ZXU	12	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	PH507	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA6507PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TCA6507RUEP	X2QFN	RUE	12	3000	179.0	8.4	1.6	2.2	0.55	4.0	8.0	Q1
TCA6507ZXUR	BGA MICROSTAR JUNIOR	ZXU	12	2500	330.0	8.4	2.3	2.8	1.0	4.0	8.0	Q2

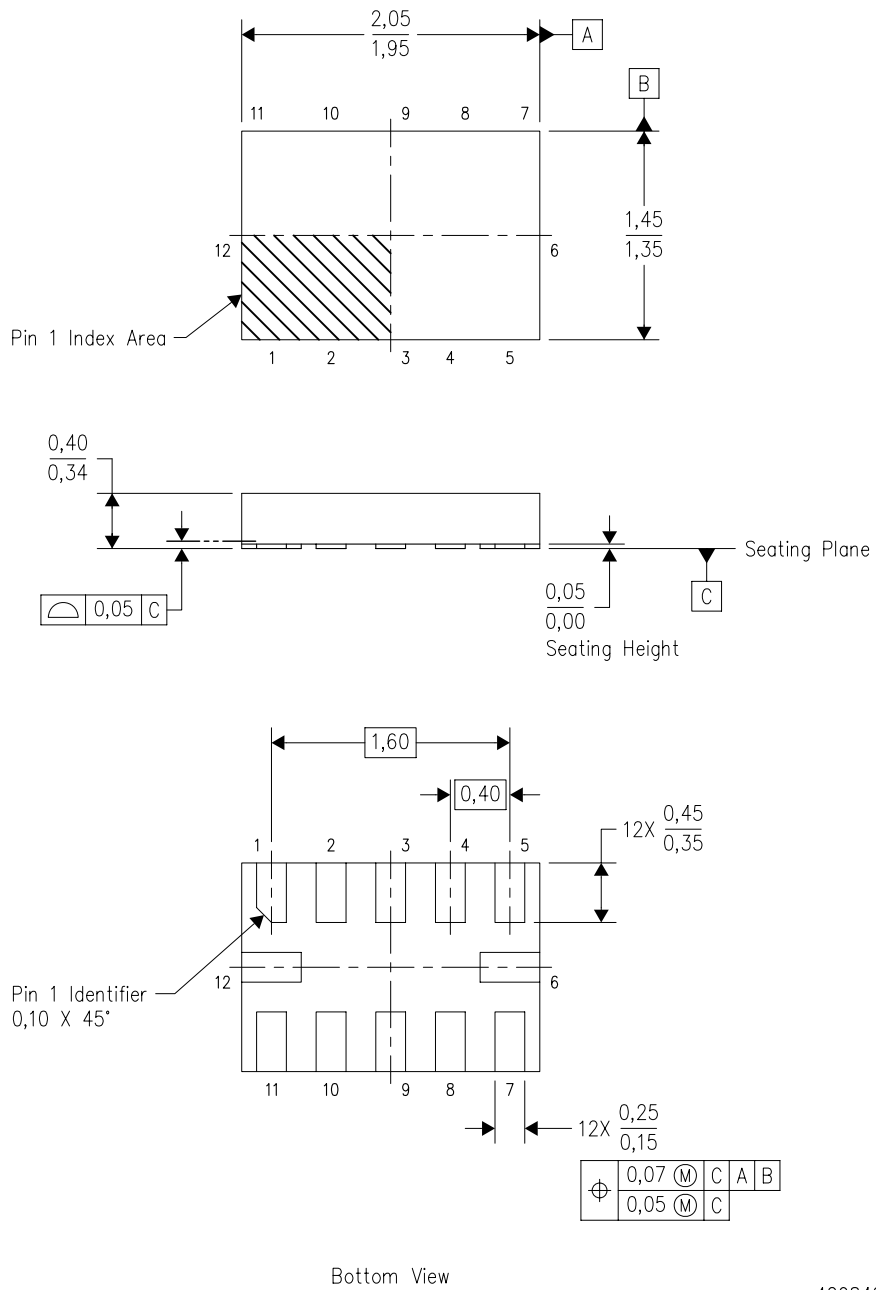
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA6507PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TCA6507RUER	X2QFN	RUE	12	3000	203.0	203.0	35.0
TCA6507ZXUR	BGA MICROSTAR JUNIOR	ZXU	12	2500	336.6	336.6	28.6

RUE (R-PX2QFN-N12)

PLASTIC QUAD FLATPACK NO-LEAD

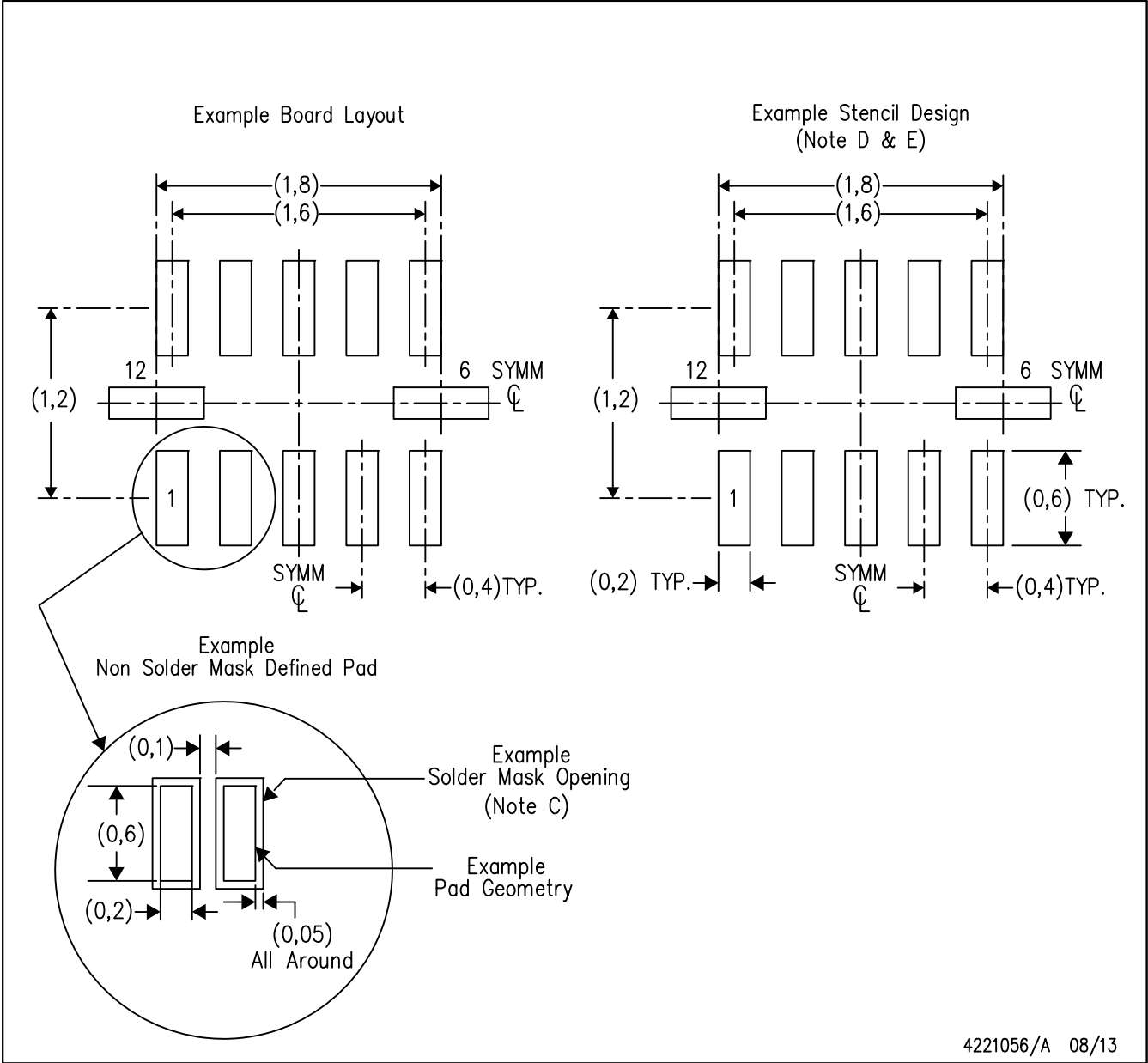


4208463/C 07/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation X2DFE.

RUE (R-PX2QFN-N12)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - D. Maximum stencil thickness 0,1 mm (4 mils).
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

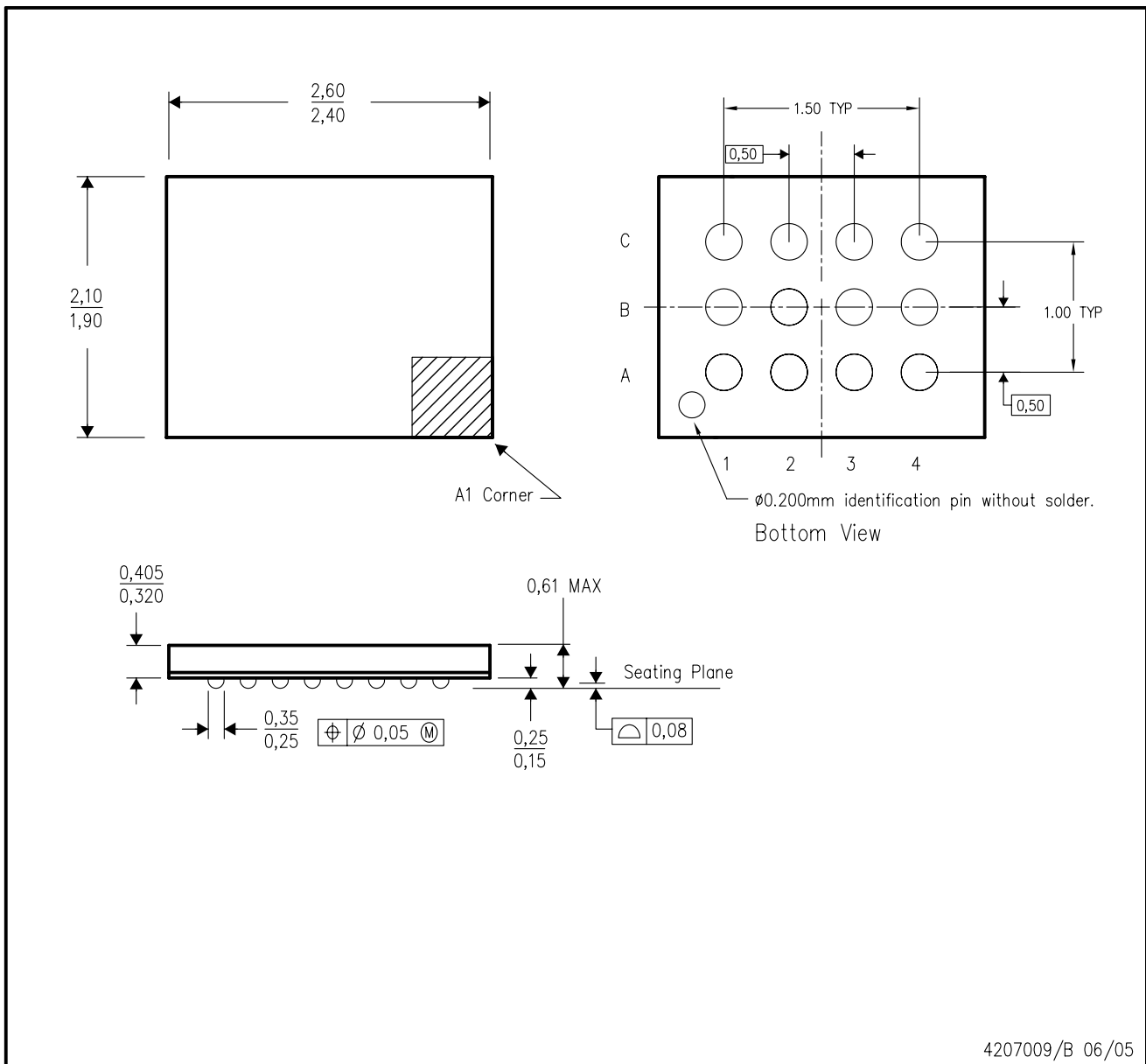


4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

ZXU (S-PBGA-N12)

PLASTIC BALL GRID ARRAY



4207009/B 06/05

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. This package is a lead-free solder ball design.

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