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SCLS713A - MARCH 2009 - REVISED JULY 2015

# TLC59212 8-Bit Open-Collector Sink Driver with Latch

Technical

Documents

### 1 Features

- LBC3S (Lin BiCMOS) Process
- High Voltage Output (V<sub>OUT</sub> = 24 V)
- Output Current (I<sub>OL</sub> Maximum = 40 mA)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged Device Model (C101)

# 2 Applications

- Lamps and Displays (LED)
- Hammers
- Relay

# 3 Description

Tools &

Software

The TLC59212 device is an 8-bit open-collector driver with latch designed for 5-V  $V_{CC}$  operation.

Support &

Community

2.2

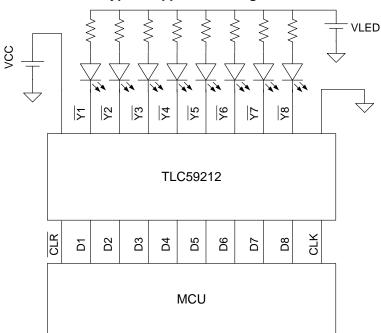
These circuits are positive-edge-triggered D-type flipflops with a direct clear (CLR) input. Information at the data (D) input meeting the setup time requirements is transferred to the  $\overline{Y}$  output on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D-input has no effect at the output.

The TLC59212 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)			
TI 050212	PDIP (20)	24.33 mm × 6.35 mm			
TLC59212	TSSOP (20)	6.50 mm × 4.40 mm			

(1) For all available packages, see the orderable addendum at the end of the data sheet.



#### **Typical Application Diagram**

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# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

#### Changes from Original (March 2009) to Revision A

Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ..... 1

#### EXAS ISTRUMENTS

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Page



# 5 Pin Configuration and Functions

N or PW Package 20-Pin PDIP or TSSOP Top View						
	1	U	20	Vcc		
D1 [	2		19	] <u>71</u>		
D2 [	3		18	] <u>72</u>		
D3 [	4		17	<u>] 73</u>		
D4 🗌	5		16	] <u>Y4</u>		
D5 🗌	6		15	] <u>Y5</u>		
D6 🗌	7		14	<u> </u>		
D7 [	8		13	] <u>7</u> 7		
D8 🗌	9		12	] <u>78</u>		
CLK [	10		11	GND		

#### **Pin Functions**

PIN		I/O	DESCRIPTION		
NAME	NO.	1/0	DESCRIPTION		
CLR	1	I	Direct clear of output		
D1	2	I	Input control to the current sink driver		
D2	3	I	Input control to the current sink driver		
D3	4	Ι	Input control to the current sink driver		
D4	5	I	Input control to the current sink driver		
D5	6	I	Input control to the current sink driver		
D6	7	I	Input control to the current sink driver		
D7	8	I	Input control to the current sink driver		
D8	9	Ι	Input control to the current sink driver		
CLK	10	I	Clock to positive edge triggered D flipflops		
GND	11	_	Ground		
<u>Y8</u>	12	0	Output to load		
<u>Y7</u>	13	0	Output to load		
<u>Y6</u>	14	0	Output to load		
<u>Y5</u>	15	0	Output to load		
<u>¥4</u>	16	0	Output to load		
<u>Y3</u>	17	0	Output to load		
<u>Y2</u>	18	0	Output to load		
<u>Y1</u>	19	0	Output to load		
V <sub>cc</sub>	20	I	Supply voltage		

# 6 Specifications

#### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	7	V
D	Input voltage	D, CLK, CLR	-0.5	7	V
Vo	Output voltage	H output	-0.5	30	V
Io	Output current	1 bit for output low		40	mA
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0 V		-20	mA
T <sub>A</sub>	Operating free-air temperature		-40	85	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### 6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 $^{\left(2\right)}$	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

#### 6.3 Recommended Operating Conditions

 $V_{CC}$  = 4.5 V to 5.5 V. Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> × 0.7	V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage	0	$V_{CC} \times 0.3$	V
Vo	Output voltage	0	24	V
Io	Output current, Duty cycle < 100%	0	40	mA
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

#### 6.4 Thermal Information

		TLC5		
	THERMAL METRIC <sup>(1)</sup>	N (PDIP)	PW (TSSOP)	UNIT
		20 PINS	20 PINS	
$R_{\thetaJA}$	Junction-to-ambient thermal resistance	55.8	96.0	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	47.4	29.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.8	47.3	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	24.3	1.8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	36.6	46.7	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	_	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

#### 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST COND	TIONS	MIN	TYP	MAX	UNIT
V <sub>t+</sub>	Positive-going input threshold	D, CLR, CLK				3.5	V
V <sub>t-</sub>	Negative-going input threshold	D, CLR, CLK		1.5			V
Vt	Hysteresis	D, CLR, CLK		0.5		2	V
V <sub>O(off)</sub>	Output tr sustain voltage	I <sub>ce</sub> = 1 mA		24			V
I <sub>OZ</sub>	Output tr leakage current	V <sub>O</sub> = 24 V			0	5	μA
IIH	High-level input current	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 5.5 V			0	1	μA
IIL	Low-level input current	$V_{CC} = 5.5 V, V_{I} = 0 V$			0	-1	μA
l <sub>off</sub>	Leakage current	$V_{I} = 0$ to 5 V, $V_{O} = 0$ to 30 V,	$V_{\rm CC} = 0$		0	5	μA
	Cumply current	$V_1 = 0$ to 5 V, $V_0 = 0$ to 30 V,	Output = all OFF		0	5	۵
I <sub>CC</sub>	Supply current	$V_{CC} = 0$	Output = all ON		8 20	μA	
V <sub>OL</sub>	Low-level output voltage	$V_{CC} = 4.5 \text{ V}, \text{ I}_{O} = 40 \text{ mA}$			0.32	0.55	V
r <sub>ON</sub>	ON-state resistance	V <sub>CC</sub> = 4.5 V, I <sub>O</sub> = 10 mA			8	13	Ω
Ci	Input capacitance	$V_{I} = V_{CC}$ or GND			5		pF

#### 6.6 Timing Requirements

over  $T_{A}$  = –40°C to 85°C,  $V_{CC}$  = 4.5 V to 5.5 V, O/C to Y (unless otherwise noted)

				MIN	MAX	UNIT
t <sub>su</sub>	Setup time	CLK	$V_{DD} = 4.5 V$ to 5.5 V	5		ns
t <sub>h</sub>	Hold time	CLK	$V_{DD} = 4.5 V$ to 5.5 V	15		ns
tw	Pulse width	CLK, CLR	$V_{DD} = 4.5 \text{ V} \text{ to } 5.5 \text{ V}$	20		ns

### 6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), see Figure 2

PARAMETER	TEST	LOAD	т	<sub>A</sub> = 25°C		T <sub>A</sub> = -40°C to 8	85°C	UNIT
PARAMETER	CONDITIONS	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNIT
t <sub>TLH</sub>	Output = low to high	$C_L = 50 \text{ pF}, \text{ R}_L = 500 \Omega$		60	185		185	ns
t <sub>THL</sub>	Output = high to low	$C_L = 50 \text{ pF}, \text{ R}_L = 500 \Omega$		10	185		185	ns
t <sub>PLH</sub>	Output = low to high	$C_L = 50 \text{ pF}, \text{ R}_L = 500 \Omega$		70	210		250	ns
t <sub>PHL</sub>	Output = high to low	$C_L = 50 \text{ pF}, \text{ R}_L = 500 \Omega$		45	210		250	ns
t <sub>PHLR</sub>	CLR-Y	$C_L = 50 \text{ pF}, \text{ R}_L = 500 \Omega$		70	210		250	ns



# 6.8 Typical Characteristics

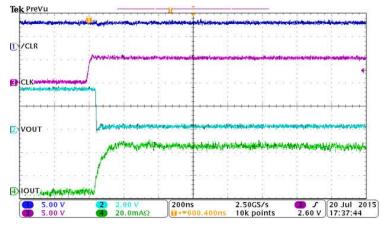
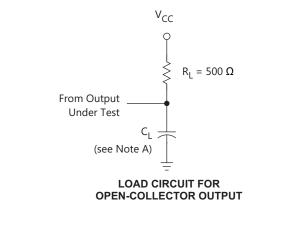
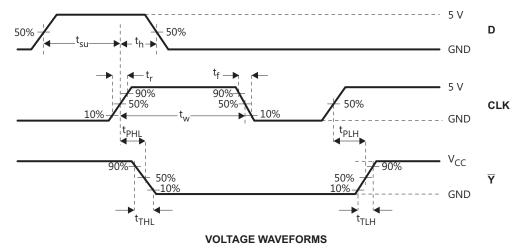


Figure 1. Output Voltage and Current Response



### 7 Parameter Measurement Information





- A. C<sub>L</sub> includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  3 ns, and t<sub>f</sub>  $\leq$  3 ns.
- C. The outputs are measured one at a time with one transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

#### Figure 2. Test Circuit and Voltage Waveforms

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### 8 Detailed Description

#### 8.1 Overview

The TLC59212 device is an 8-bit open-collector driver with latch designed for 5-V V<sub>CC</sub> operation.

#### 8.2 Functional Block Diagram

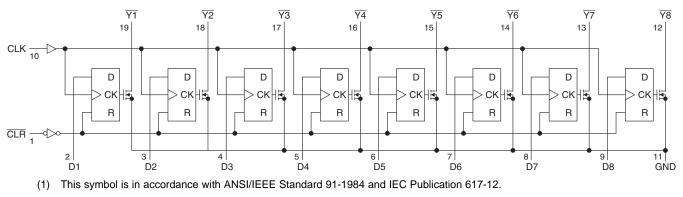


Figure 3. Logic Symbol

#### 8.3 Feature Description

Each of the 8 channels is controlled by its input (Dn), a direct clear ( $\overline{CLR}$ ), and clock (CLK) through a positiveedge-triggered D-type flip-flops. Information at the data (D) input meeting the setup time requirements is transferred to the output (Y) on the positive-going edge of the clock (CLK) pulse. When CLK is at either the high or low level, the D-input has no effect at the output. When  $\overline{CLR}$  is at low level, the D-input has no effect at the output.

#### 8.4 Device Functional Modes

Table 1 lists the functional modes of the TLC59212.

	INPUTS				
CLR	CLK	D	Y		
L	Х	Х	H*		
Н	↑ (	L	H*		
Н	↑ (	Н	L		
Н	L	Х	Y <sub>0</sub>		
Н	Ļ	Х	Y <sub>0</sub>		

Table 1. Function Table (Each Latch)<sup>(1)</sup>

(1) L: Low-level

H: High-level H\*: with pullup resistor

X: Irrelevant

↑: Rising edge

↓: Falling edge

Ž : High-impedance (OFF)



#### 9 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 9.1 Application Information

In LED display application, TLC59212 is used to drive the current sink for 8 LEDs in parallel. LED display pattern can be created by providing different bit pattern. At every positive clock edge, new bit pattern will be transferred to LED display.

#### 9.2 Typical Application

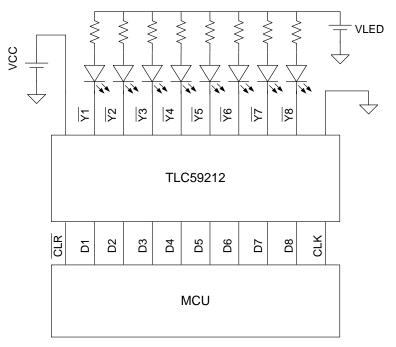


Figure 4. Typical Application Diagram

#### 9.2.1 Design Requirements

For LED display application, LED is selected based on the application. The current level is determined by the required brightness. Given the available LED supply, the resistor value could be determined. The TCL59212 has a maximum current requirement less than 40mA for constant on application.

#### 9.2.2 Detailed Design Procedure

The selection of supply voltage (VLED), LED, and resistor sets the current of the LED.

$$VR + VL + VOL = VLED$$
(1)  
I = (VLED - VL - VOL) /R (2)

VR is the voltage drop across the resistor, VL is the voltage drop across the LED when LED is on, VOL is the output voltage at the collector when the driver is enabled. For example, when VLED = 5 V, VL = 2.4 V, and VOL = 0.35 V, a 55- $\Omega$  resistor is used to obtain output current 40 mA.



# **Typical Application (continued)**

# 9.2.3 Application Curve

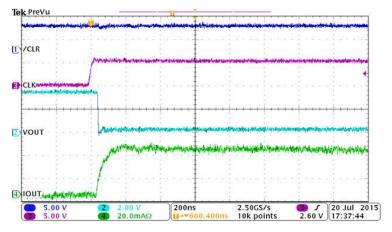


Figure 5. Output Voltage and Current Response

# **10** Power Supply Recommendations

The supply voltage to TLC59212 is from 4.5 V to 5.5 V. The voltage at output can be up to 24 V.

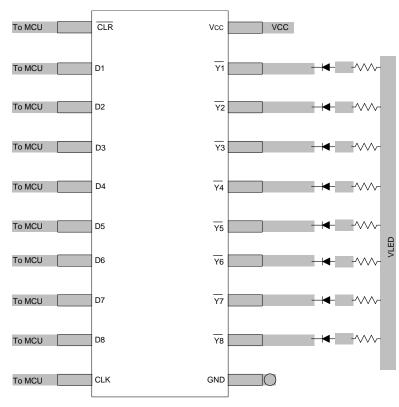


# 11 Layout

### 11.1 Layout Guidelines

The traces that carry current from the LED cathodes to the output pins must be wide enough to support the current (up to 40 mA).

## 11.2 Layout Example



◯ VIA to GND

Figure 6. Layout Recommendation



# **12 Device and Documentation Support**

#### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**Design Support TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 12.2 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

#### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

### 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



4-Mar-2016

# PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TLC59212IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59212	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(<sup>6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE OPTION ADDENDUM

4-Mar-2016

# PACKAGE MATERIALS INFORMATION

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# TAPE AND REEL INFORMATION





# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions a	are nominal
-------------------	-------------

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59212IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TEXAS INSTRUMENTS

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# PACKAGE MATERIALS INFORMATION

19-Jun-2015



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59212IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  $\beta$ . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



# LAND PATTERN DATA



NOTES: Α. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
  C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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