TPS53114 Single Synchronous Step-down Controller for Low Voltage Power Rails

1 Features

- D-CAP2™ Mode Control
  - Fast Transient Response
  - No External Parts Required For Loop Compensation
  - Compatible with Ceramic Output Capacitors
- High Initial Reference Accuracy (±1%)
- Low Output Ripple
- Wide Input Voltage Range: 4.5 V to 24 V
- Output Voltage Range: 0.76 V to 5.5 V
- Low-Side $R_{DS(on)}$ Loss-Less Current Sensing
- Adaptive Gate Drivers with Integrated Boost Diode
- Adjustable Soft Start
- Pre-Biased Soft Start
- Selectable Switching Frequency 350 kHz / 700 kHz
- Cycle-By-Cycle Over Current Limiting Control
- Thermally Compensated OCP by 4000 ppm/°C at I_{TRIP}

2 Applications

- Point-of-Load Regulation in Low Power Systems for Wide Range of Applications
  - Digital TV Power Supply
  - Networking Home Terminal
  - Digital Set Top Box (STB)
  - DVD Player / Recorder
  - Gaming Consoles

3 Description

The TPS53114 is a single, adaptive on-time D-CAP2™ mode synchronous buck controller. The TPS53114 enables system designers to complete the suite of various end equipment's power bus regulators with cost effective low external component count and low standby current solution. The main control loop for the TPS53114 uses the D-CAP2™ mode control which provides a very fast transient response with no external components. The TPS53114 also has a circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP and ultra-low ESR ceramic capacitors. The device provides convenient and efficient operation with input voltages from 4.5 V to 24 V and output voltage from 0.76 V to 5.5 V.

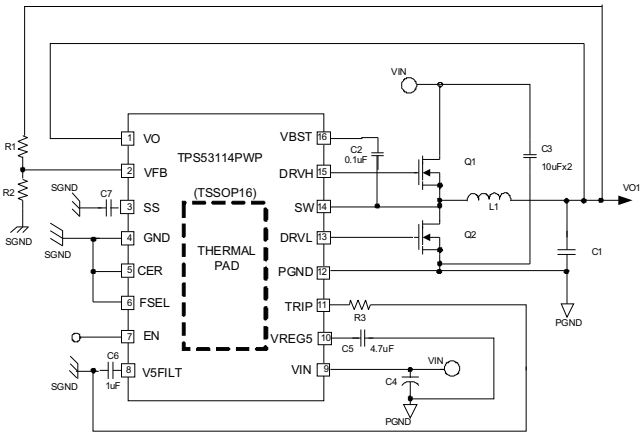
The TPS53114 is available in the 16-pin TSSOP and HTSSOP packages, and is specified from –40°C to 85°C ambient temperature range.

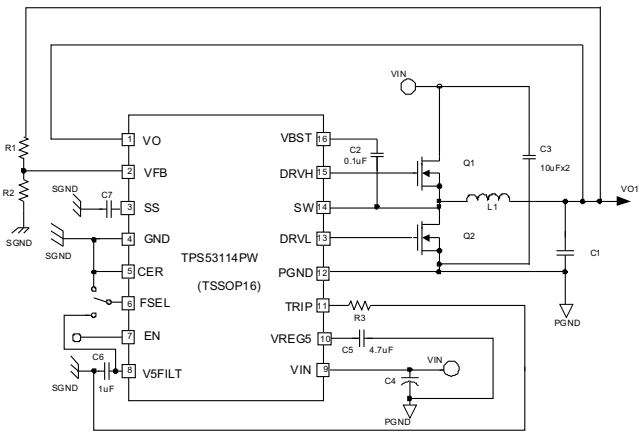
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS53114	TSSOP (16)	5.00 mm x 4.40 mm
TPS53114	HTSSOP 916)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematics





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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2010) to Revision C — **Page**

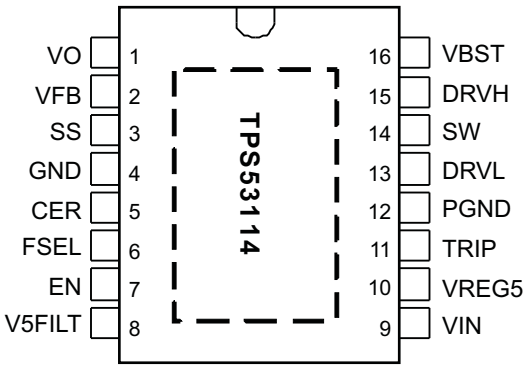
- Changed the datasheet to the new TI standard format ... 1
- Added Thermal PWP information ... 5
- Changed from 4.8 V to 4.6 V. ... 5
- Changed from 8 to 12 Ω. ... 5
- Added Figures 8 and 9 ... 8
- Added "The TPS53114 enables system designers to complete the suite of various end equipment power bus regulators with cost effective, low external component count and low standby current solution." ... 9
- Changed Equation 1 ... 11

Changes from Revision A (August 2009) to Revision B — **Page**

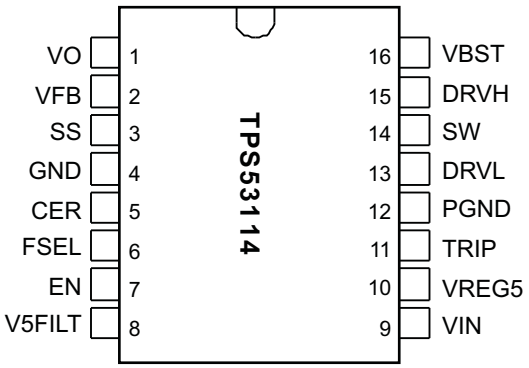
- Changed From: I_{OCL} + To: I_{OCL} - ... 14
- Added minus V_{OCLoff} ... 14

6 Pin Configurations and Functions

16-Pin HTSSOP
PWP Package
(Top View)



16-Pin TSSOP
PW Package
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
VBST	16	I	Supply input for high-side NFET driver. Bypass to SW with a high-quality 0.1-µF ceramic capacitor. An external schottky diode can be added from VREG5 if forward drop is critical to drive the high-side FET.
EN	7	I	Enable. Pull High to enable SMPS.
SS	3	O	Soft start programming pin. Connect capacitor from SS pin to GND to program soft start time.
VO	1	I	Output voltage input for on-time adjustment and output discharge. Connect directory to the output voltage.
VFB	2	I	D-CAP2 feedback input. Connect to output voltage with resistor divider.
GND	4	I	Signal ground pin. Connect to PGND and system ground at a single point.
DRVH	15	O	High-side N-channel MOSFET gate driver output. SW referenced driver switches between SW(OFF) and VBST(ON).
SW	14	I/O	Switch node connections for both the high-side driver and over current comparator.
DRVL	13	O	Low-side N-Channel MOSFET gate driver output. PGND referenced driver switches between PGND(OFF) and VREG5(ON).
PGND	12	I/O	Power ground connection for both the low-side driver and over current comparator. Connect PGND and GND strongly together near the IC.
TRIP	11	I	over current threshold programming pin. Connect to GND with a resister to set threshold for low-side $R_{DS(on)}$ current limit.
VIN	9	I	Supply Input for 5-V linear regulator. Bypass to GND with a minimum high-quality 0.1-µF ceramic capacitor.
V5FILT	8	I	5-V supply input for the control circuitry except the MOSFET drivers. Bypass to GND with a minimum high-quality 1.0-µF ceramic capacitor. V5FILT is connected to VREG5 via internal 10-Ω resistor.
VREG5	10	O	Output of 5-V linear regulator and supply for MOSFET driver. Bypass to GND with a minimum high-quality 4.7-µF ceramic capacitor. VREG5 is connected to V5FILT via internal 10-Ω resistor.
CER	5	I	Output capacitor select pin. Connect to GND for ceramic output capacitors. Connect to V5FILT for conductive polymer electrolyte type output capacitors (SP-CAP, POS-CAP, PXE).
FSEL	6	I	Switching frequency selection pin. Connect to GND for low switching frequency or connect to V5FILT for high switching frequency.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Input voltage range	VIN, EN	–0.3	26	V
		VBST	–0.3	32	
		VBST - SW	–0.3	6	
		V5FILT, VFB, TRIP, VO, FSEL, CER	–0.3	6	
	Output voltage range	DRVH	–1	32	V
		DRVH - SW	–0.3	6	
		SW	–2	26	
		DRVL, VREG5, SS	–0.3	6	
		PGND	–0.3	0.3	
T_A	Operating ambient temperature range		–40	85	°C
T_J	Junction temperature range		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	-2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	-500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Supply input voltage	VIN	4.5	24	V
		V5FILT	4.5	5.5	
	Input voltage	VBST	–0.1	30	V
		VBST - SW	–0.1	5.5	
		VFB, VO, FSEL, CER	–0.1	5.5	
		TRIP	–0.1	0.3	
		EN	–0.1	24	
	Output voltage	DRVH	–0.1	30	V
		VBST - SW	–0.1	5.5	
		SW	1.8	24	
		DRVL, VREG5, SS	–0.1	5.5	
		PGND	–0.1	0.1	
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS53114		UNIT
		PWP (16 PINS)	PW (16 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.2	109.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.4	31.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	28.3	54.7	
ψ_{JT}	Junction-to-top characterization parameter	1.4	0.9	
ψ_{JB}	Junction-to-board characterization parameter	28.1	54.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.9	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	VIN supply current	VIN current, T_A = 25°C, VREG5 tied to V5FLT, EN = 5V, VFB = 0.8V, SW = 0.5V		350	600	µA
I_{VINSDN}	VIN shutdown current	VIN current, T_A = 25°C, No Load , EN = 0V, VREG5 = ON		28	60	µA
VFB VOLTAGE and DISCHARGE RESISTANCE						
V_{BG}	Bandgap Initial regulation accuracy	T_A = 25°C	–1.0%		1.0%	
V_{VFBTHL}	VFB threshold voltage	T_A = 25°C , FSEL = 0 V, CER = V5FILT	755	765	775	mV
		T_A = –40°C to 85°C, FSEL = 0V, CER = V5FILT	752		778	
V_{VFBTHH}	VFB threshold voltage	T_A = 25°C , FSEL = CER = V5FILT	748	758	768	mV
		T_A = –40°C to 85°C, FSEL = CER = V5FILT	745		771	
I_{VFB}	VFB input current	VFB = 0.8V, T_A = 25°C	–100	–10	100	nA
R_{Dischg}	Vo discharge resistance	EN = 0V, VO = 0.5V, T_A = 25°C		40	80	Ω
VREG5 OUTPUT						
V_{VREG5}	VREG5 output voltage	T_A=25°C, 5.5V < VIN < 24V, 0 < I_{VREG5} < 10mA	4.6	5.0	5.2	V
V_{LN5}	Line regulation	5.5V < VIN < 24V, I_{VREG5} = 10mA			20	mV
V_{LD5}	Load regulation	1mA < I_{VREG5} < 10mA			40	mV
I_{VREG5}	Output current	VIN = 5.5V, V_{VREG5} = 4.0V, T_A = 25°C		170		mA
OUTPUT: N-CHANNEL MOSFET GATE DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = –100mA		5.5	11	Ω
		Sink, I_{DRVH} = 100mA		2.5	5	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = –100mA		4	12	Ω
		Sink, I_{DRVL} = 100mA		2	4	
INTERNAL BST DIODE						
V_{FBST}	Forward voltage	$V_{VREG5-VBST}$, IF = 10mA, T_A = 25°C	0.7	0.8	0.9	V
I_{VBSTLK}	VBST leakage current	VBST = 29V, SW = 24V, T_A = 25°C		0.1	1	µA
SOFT START						
I_{ssc}	SS charge current	VSS = 0V , SOURCE CURRENT	1.4	2.0	2.6	µA
I_{ssd}	SS discharge current	VSS = 0.5V , SINK CURRRENT	100	150		µA
UVLO						
$V_{UV5VFILT}$	V5FILT UVLO threshold	V5FILT rising	3.7	4.0	4.3	V
		Hysteresis	0.2	0.3	0.4	

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD						
V_{ENH}	EN H-level threshold voltage	EN	2.0			V
V_{ENL}	EN L-level threshold voltage	EN			0.3	V
CURRENT SENSE						
I_{TRIP}	TRIP source current	VTRIP = 0.1V, T_A = 25°C	8.5	10	11.5	µA
TC_{ITRIP}	I_{TRIP} temperature coefficient	on the basis of 25°C		4000		ppm/°C
V_{OCLoff}	OCP compensation offset	($V_{TRIP-GND}$-$V_{PGND-SW}$) voltage, $V_{TRIP-GND}$ = 60mV, T_A = 25°C	–10	0	10	mV
		($V_{TRIP-GND}$-$V_{PGND-SW}$) voltage, VTRIP-GND = 60mV	–15		15	
V_{Rtrip}	Current limit threshold setting range	$V_{TRIP-GND}$ voltage	30		200	
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	110%	115%	120%	
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis (recovery <20µs)		10%		
THERMAL						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(1)		150		°C
		Hysteresis(1)		20		

(1) Specified by design. Not production tested.

7.6 Timing Requirements

PARAMETER			MIN	TYP	MAX	UNIT
OUTPUT: N-CHANNEL MOSFET GATE DRIVERS						
t_D	Dead time	DRVH-low to DRVL-on	20	50	80	ns
		DRVL-low to DRVH-on	20	40	80	
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
t_{OVPDEL}	Output OVP prop delay			1.5		µs
t_{UVPDEL}	Output UVP delay		17	30	40	µs
t_{UVPEN}	Output UVP enable delay	UVP enable delay / soft start time	X1.4	X1.7	X2.0	

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ONL}	On time	SW = 12V, VO = 1.8V, FSEL = 0V		390		ns
t_{ONH}	On time	SW = 12V, VO = 1.8V, FSEL = V5FILT		139		ns
t_{OFFL}	Min off time	SW = 0.7V, T_A = 25°C, VFB = 0.7V, FSEL = 0V		285		ns
t_{OFFH}	Min off time	SW = 0.7V, T_A = 25°C, VFB = 0.7V, FSEL = V5FILT		216		ns

7.8 Typical Characteristics

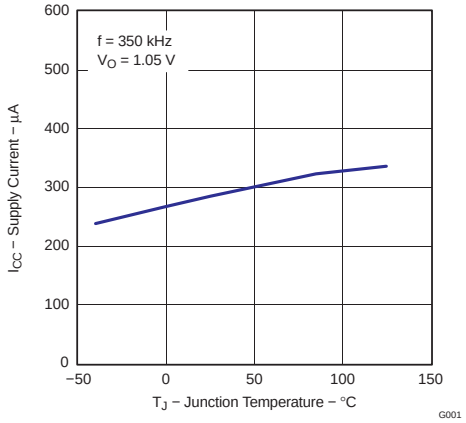


Figure 1. VIN Supply Current vs Junction Temperature

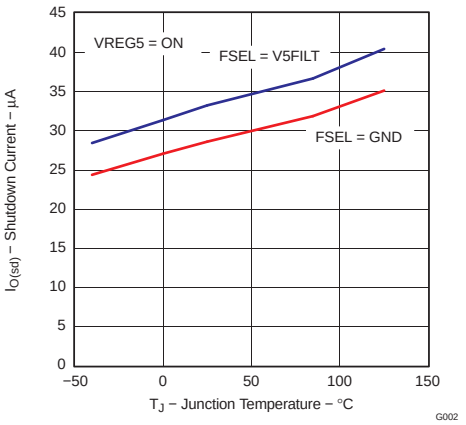


Figure 2. VIN Shutdown Current vs Junction Temperature

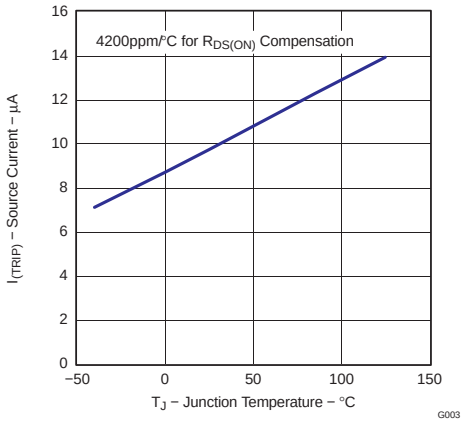


Figure 3. Trip Source Current vs Junction Temperature

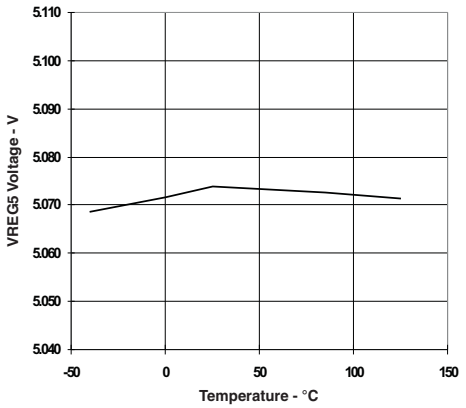


Figure 4. VREG5 Voltage

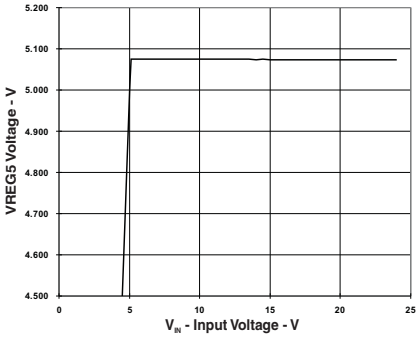
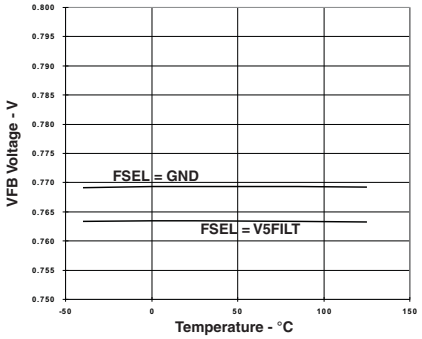


Figure 5. VREG5 Voltage vs Input Voltage



V_O = 1.05 V, I_O = 4 A

Figure 6. VFB Voltage vs Temperature

Typical Characteristics (continued)

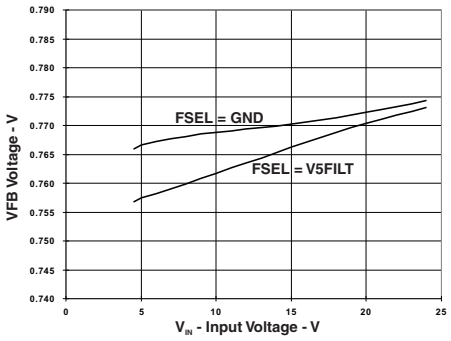


Figure 7. VFB Voltage vs Input Voltage

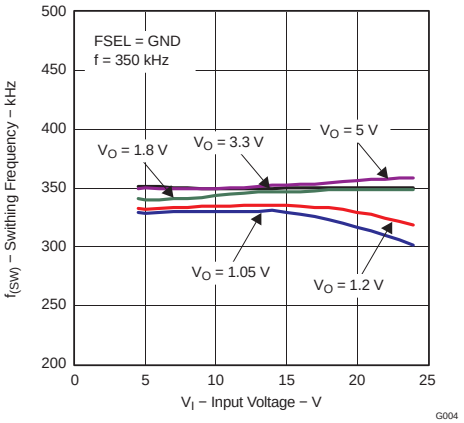


Figure 8. Switching Frequency (I_O = 1 A) vs. Input Voltage

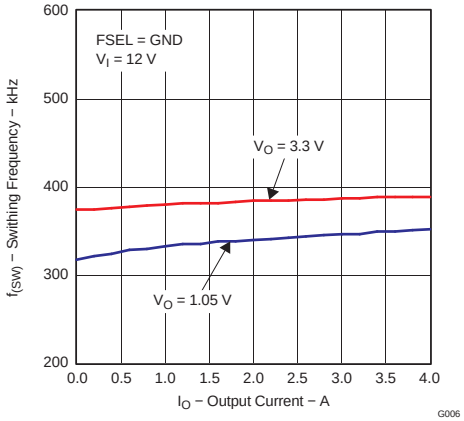


Figure 9. Switching Frequency vs. Output Current

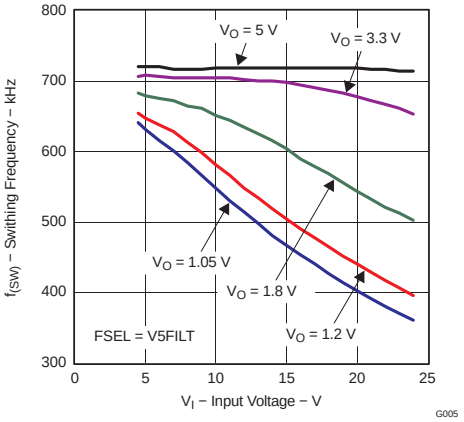


Figure 10. Switching Frequency vs. Input Voltage

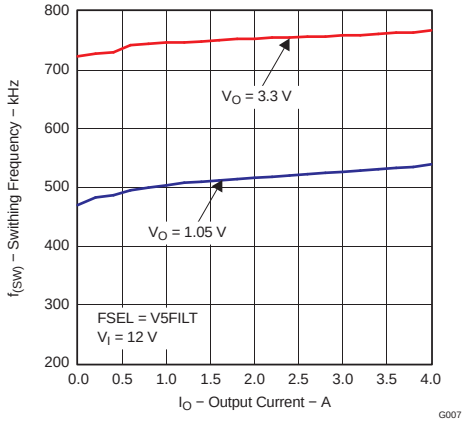


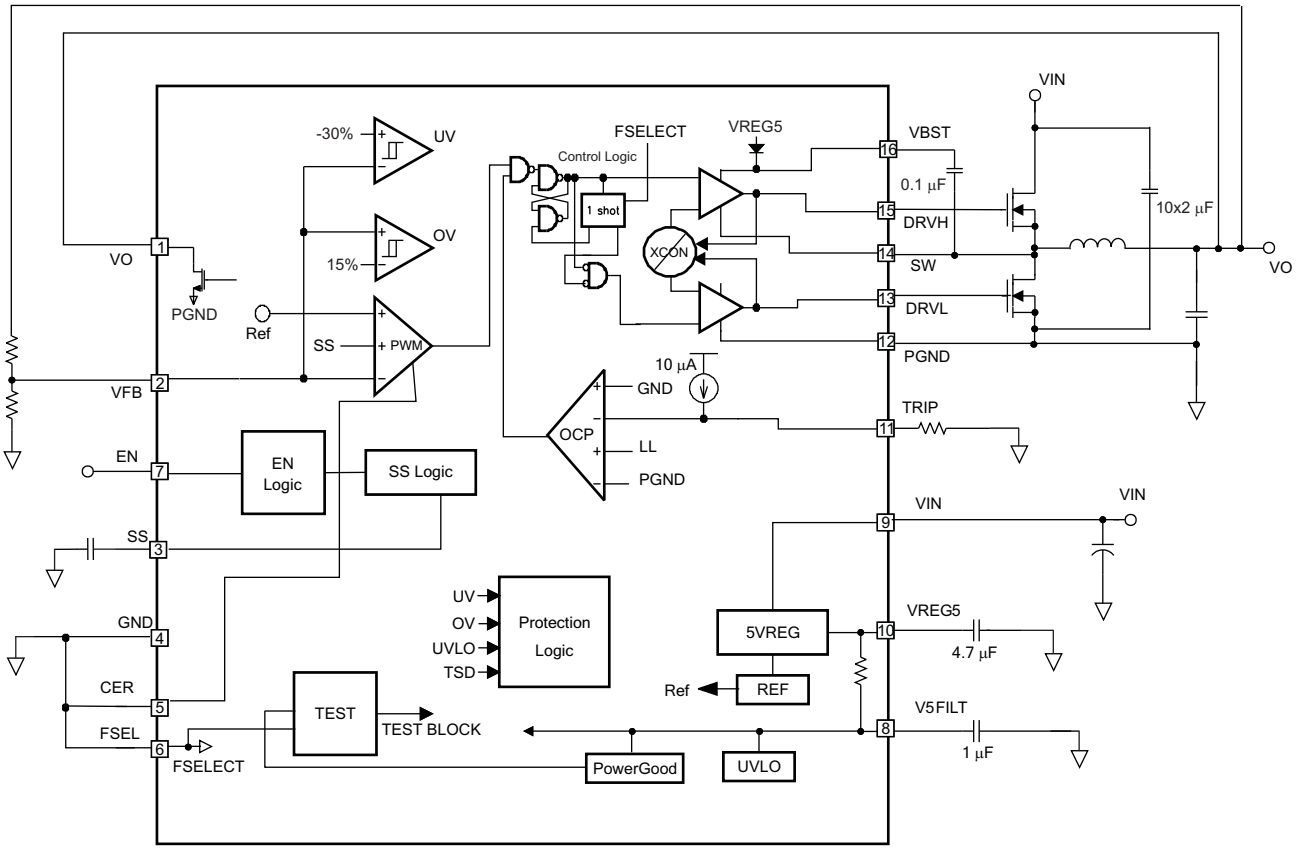
Figure 11. Switching Frequency vs. Output Current

8 Detailed Description

8.1 Overview

The TPS53114 is a single, adaptive on-time D-CAP2™ mode synchronous buck controller. The TPS53114 enables system designers to complete the suite of various end equipment power bus regulators with cost effective, low external component count and low standby current solution. The main control loop for the TPS53114 uses the D-CAP2™ mode control which provides a very fast transient response with no external compensation components. The TPS53114 also has a circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP and ultra-low ESR ceramic capacitors. The device provides convenient and efficient operation with input voltages from 4.5 V to 24 V and output voltage from 0.76 V to 5.5 V.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 PWM Operation

The main control loop of the TPS53114 is an adaptive on-time pulse width modulation (PWM) controller using a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. After an internal one-shot timer expires, this MOSFET is turned off. The one-shot timer is reset and the high-side MOSFET is turned back on when the feedback voltage falls below the reference voltage. The one shot is set by the converter input voltage VIN, and the output voltage VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP mode control.

Feature Description (continued)

8.3.2 Drivers

The TPS53114 contains two high-current resistive MOSFET gate drivers. The low-side driver is a ground referenced, VREG5 powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET whose source is connected to PGND. The high-side driver is a floating SW referenced VBST powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET. To maintain the VBST voltage during the high-side driver ON time, a capacitor is placed from SW to VBST. Each driver draws average current equal to gate charge (Q_g at V_{gs} = 5 V) times switching frequency (f_{SW}).

To prevent cross-conduction, there is a narrow dead-time when both high-side and low-side drivers are OFF between each driver transition. During this time the inductor current is carried by one of the MOSFET's body diodes.

8.3.3 PWM Frequency and Adaptive On-time Control

TPS53114 employs adaptive on-time control scheme and does not have a dedicated on board oscillator. TPS53114 runs with pseudo-constant frequency by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. Therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

8.3.4 5-Volt Regulator

The TPS53114 has an internal 5-V low-dropout (LDO) Regulator to provide a regulated voltage for all both drivers and the IC's internal logic. A high-quality 4.7-µF or greater ceramic capacitor from VREG5 to GND is required to stabilize the internal regular. An internal 10-Ω resistor from VREG5 filters the regulator output to the IC's analog and logic input voltage, V5FILT. An additional high-quality 1.0-µF ceramic capacitor is required from V5FILT to GND to filter switching noise from VREG5.

8.3.5 Soft Start

The TPS53114 has a programmable soft start . When the EN pin becomes high, 2.0-µA current begins charging the capacitor which is connected SS pin to GND. Smooth control of the output voltage is maintained during start up.

8.3.6 Pre-bias Support

The TPS53114 supports pre-bias start-up without sinking current from the output capacitor. When enabled, the low-side driver is held off until the soft start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage (VFB)), then the TPS53114 slowly activates synchronous rectification by limiting the first DRVL pulses with a narrow on-time. This limited on-time is then incremented on a cycle-by-cycle basis until it coincides with the full 1-D off-time. This scheme prevents the initial sinking of current from the pre-bias output, and ensure that the output voltage (V_{OUT}) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

8.3.7 Switching Frequency Selection

The TPS53114 allows the user to select from two different switching frequencies by connecting the FSEL pin to either GND or V5FILT. Connect FSEL to GND for a switching frequency (f_{sw}) of 350 KHz. Connect FSEL to V5FILT for a switching frequency of 700 KHz.

8.3.8 Output Discharge Control

The TPS53114 discharges the outputs when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). The device discharges output using an internal 40-Ω MOSFET which is connected to VO and PGND. The external low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output. This discharge ensures that, on start, the regulated voltage always initializes from 0 V.

Feature Description (continued)

8.3.9 Over Current Protection

TPS53114 has a cycle-by-cycle over current limit feature. The over current limits the inductor valley current by monitoring the voltage drop across the low-side MOSFET $R_{DS(on)}$ during the low-side driver on-time. If the inductor current is larger than the over current limit (OCL), the TPS53114 delays the start of the next switching cycle until the sensed inductor current falls below the OCL current. MOSFET $R_{DS(on)}$ current sensing is used to provide an accuracy and cost effective solution without external devices. To program the OCL, the TRIP pin should be connected to GND through a trip voltage setting resistor, according to Equation 1 and Equation 2.

$$V_{TRIP} = \left(I_{OCL} - \frac{(V_{IN} - V_O)}{2 \bullet L1 \bullet f_{sw}} \bullet \frac{V_O}{V_{IN}} \right) \bullet R_{DS(ON)} \quad (1)$$

$$R_{TRIP}(k\Omega) = \frac{V_{TRIP}(mV)}{I_{TRIP}(\mu A)} \quad (2)$$

The trip voltage should be between 30 mV to 200 mV over all operational temperature, including the 4000 ppm/°C temperature slope compensation for the temperature dependency of the $R_{DS(on)}$. If the load current exceeds the over current limit, the voltage will begin to drop. If the over current conditions continues, the output voltage will fall below the under voltage protection threshold and the TPS53114 will shut down.

8.3.10 Over/under Voltage Protection

TPS53114 monitors a resistor divided feedback voltage to detect over and under voltage. If the feedback voltage is higher than 115% of the reference voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver OFF and the low-side MOSFET driver ON. When the feedback voltage is lower than 70% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 30 µs, TPS53114 latches OFF both top and bottom MOSFET drivers. This function is enabled approximately 1.7x T_{SS} after power-on. The OVP and UVP latch off is reset when EN goes low level.

8.3.11 UVLO Protection

TPS53114 has V5FILT under voltage lock out protection (UVLO) that monitors the voltage of V5FILT pin. When the V5FILT voltage is lower than UVLO threshold voltage, the device is shut off. All output drivers are OFF and output discharge is ON. The UVLO is non-latch protection.

8.3.12 Thermal Shutdown

The TPS53114 includes an over temperature protection shut-down feature. If the TPS53114 die temperature exceeds the OTP threshold (typically 150°C), both the high-side and low-side drivers are shut off, the output voltage discharge function is enabled and then the device is shut off until the die temperature drops. Thermal shutdown is a non-latch protection.

8.4 Device Functional Modes

8.4.1 Operation

The TPS53114 has two operating modes. The TPS53114 is in shut down mode when the EN pin is low. When the EN pin is pulled high, the TPS53114 enters the normal operating mode.

9 Application and Implementation

9.1 Application Information

9.2 350-kHz Operation Application

The schematic of Figure 12 shows a typical 350-kHz application schematic. The 350 kHz switching frequency is selected by connecting FSEL to the GND pin. The input voltage is 12 V and the output voltage is 1.05 V.

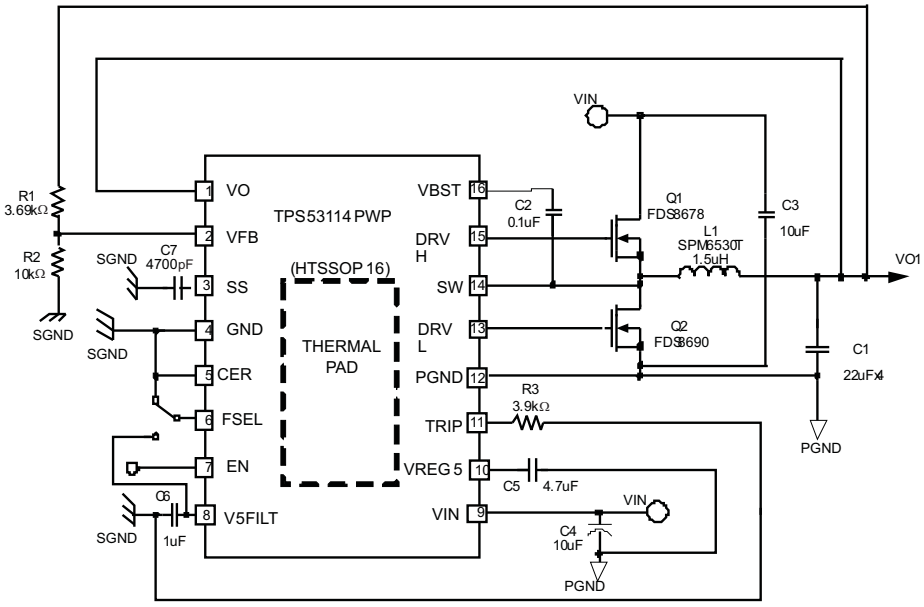


Figure 12. Typical Application Circuit at 350-kHz Switching Frequency Selection (FSEL pin = GND)

9.2.1 Design Requirements

Table 1. Design Parameters

PARAMETERS	EXAMPLE VALUES
Input voltage	12 V
Output voltage	1.05 V
Output current	4 A
Switching frequency	350 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Choose Inductor

The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improve S/N ratio and contribute to stable operation. L1 can be calculated using Equation 3.

$$L1 = \frac{(V_{IN(max)} - V_O1)}{I_{L1(ripple)} \bullet f_{SW}} \bullet \frac{V_O1}{V_{IN(max)}} = \frac{3 \bullet (V_{IN(max)} - V_O1)}{I_O1 \bullet f_{SW}} \bullet \frac{V_O1}{V_{IN(max)}} \quad (3)$$

The inductors current ratings needs to support both the RMS (thermal) current and the peak (saturation) current. The RMS and peak inductor current can be estimated as follows:

$$I_{L1(ripple)} = \frac{V_{IN(max)} - V_O1}{L1 \bullet f_{SW}} \bullet \frac{V_O1}{V_{IN(max)}} \quad (4)$$

$$I_{L1(peak)} = \frac{V_{TRIP}}{R_{DS(ON)}} + I_{L1(ripple)} \quad (5)$$

$$I_{L1(RMS)} = \sqrt{I_O 1^2 + \frac{1}{12}(I_{L1(ripple)})^2} \quad (6)$$

Note:

The calculation above shall serve as a general reference. To further improve transient response, the output inductance could be reduced further. This needs to be considered along with the selection of the output capacitor.

9.2.2.2 Choose Output Capacitor

The capacitor value and ESR determines the amount of output voltage ripple and load transient response. Recommend to use ceramic output capacitor.

$$C1 = \frac{\Delta I_{load}^{\ 2} \bullet L1}{2 \bullet V_O 1 \bullet \Delta V_{OS}} \quad (7)$$

$$C1 = \frac{\Delta I_{load}^{\ 2} \bullet L1}{2 \bullet K \bullet \Delta V_{US}} \quad (8)$$

Where:

$$K = (V_{IN} - V_O 1) \bullet \frac{T_{on} 1}{T_{ON} 1 + T_{min(off)}} \quad (9)$$

$$C1 = \frac{I_{L1(ripple)}}{8 \bullet V_O 1_{(ripple)}} \bullet \frac{1}{f_{SW}} \quad (10)$$

Select the capacitance value greater than the largest value calculated from Equation 7, Equation 8 and Equation 10. The capacitance for C1 should be greater than 66 µF.

Where:

ΔV_{OS} = The allowable amount of overshoot voltage in load transition

ΔV_{US} = The allowable amount of undershoot voltage in load transition

$T_{min(off)}$ = Minimum off time

9.2.2.3 Choose Input Capacitor

The TPS53114 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10-µF high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage.

9.2.2.4 Choose Bootstrap Capacitor

The TPS53114 requires a bootstrap capacitor from SW to VBST to provide the floating supply for the high-side drivers. A minimum 0.1-µF high-quality ceramic capacitor is recommended. The voltage rating should be greater than 10.0 V.

9.2.2.5 Choose VREG5 and V5FILT Capacitors

The TPS53114 requires both the VREG5 regulator and V5FILT input are bypassed. A minimum 4.7-µF high-quality ceramic capacitor must be connected between the VREG5 and GND for proper operation. A minimum 1.0-µF high-quality ceramic capacitor must be connected between the V5FILT and GND for proper operation. Both of these capacitors' voltage ratings should be greater than 10 V.

9.2.2.6 Choose Output Voltage Set Point Resistors

The output voltage is set with a resistor divider from output voltage node to the VFBx pin. It is recommended to use 1% tolerance or better resistors. Select R2 between 10 kΩ and 100 kΩ and use Equation 11 or Equation 12 to calculate R1.

$$R1 = \left(\frac{V_O 1}{0.765 + \frac{VFB1_{(ripple)}}{2}} - 1 \right) \bullet R2 \qquad (FSEL = GND) \tag{11}$$

$$R1 = \left(\frac{V_O 1}{0.758 + \frac{VFB1_{(ripple)}}{2}} - 1 \right) \bullet R2 \qquad (FSEL = V5FILT) \tag{12}$$

Where:

$VFB1_{(ripple)}$ = Ripple voltage at VFB1

9.2.2.7 Choose Over Current Set Point Resistor

$$V_{TRIP} = \left(I_{OCL} - \frac{(V_{IN} - V_O)}{2 \bullet L1 \bullet f_{sw}} \bullet \frac{V_O}{V_{IN}} \right) \bullet R_{DS(ON)} \tag{13}$$

$$R_{TRIP}\ (k\Omega) = \frac{V_{TRIP}\ (mV) - V_{OCLoff}}{I_{TRIP}\ (\mu A)} \tag{14}$$

Where:

$R_{DS(ON)}$ = Low side FET on-resistance
I_{TRIP} = TRIP pin source current (≒ 10 µA)
V_{OCLoff} = Minimum over current limit offset voltage (-20 mV)
I_{OCL} = over current limit

9.2.2.8 Choose Soft Start Capacitor

Soft start timing equations are as follows:

$$T_{SS} = \frac{C_7 \bullet 0.765}{2e^{-6}}(s) \qquad (FSEL = GND) \tag{15}$$

$$T_{SS} = \frac{C_7 \bullet 0.758}{2e^{-6}}(s) \qquad (FSEL = V5FILT) \tag{16}$$

9.2.2.9 Choose Package Option

TPS53114 power dissipation:

$$P_d = f_{SW} \bullet (CiH + CiL) \bullet VREG5 \bullet V_{in(max)} \tag{17}$$

Where:

C_{iH} = Input capacitor of high side MOSFET
C_{iL} = Input capacitor of low side MOSFET

Choose package considering the Dissipation Rating table.

9.2.3 350 kHz Application Curves

The application curves of Figure 13 and Figure 14 apply to both the circuits of 700 kHz Operation Application and 350-kHz Operation Application .

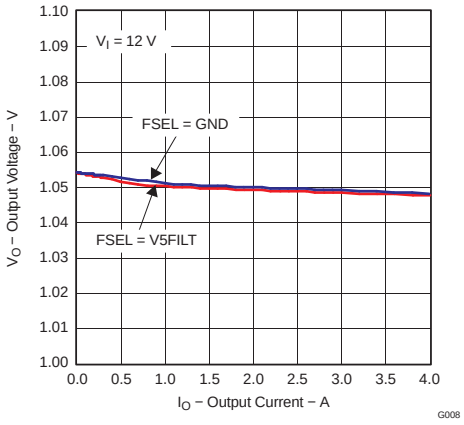


Figure 13. 1.05-V Output Voltage vs. Output Current

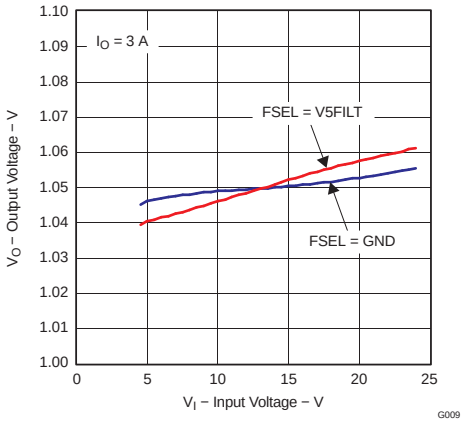


Figure 14. 1.05-V Output Voltage vs. Input Voltage

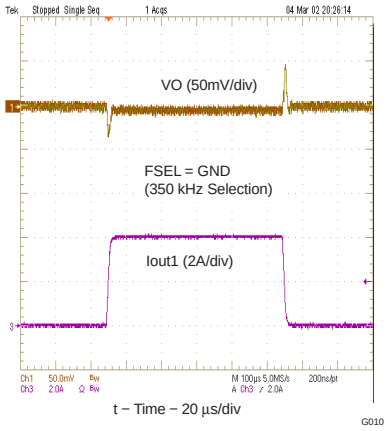


Figure 15. 1.05-V Load Transient Response

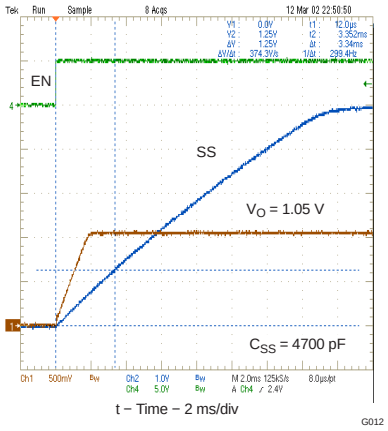


Figure 16. Startup Waveform

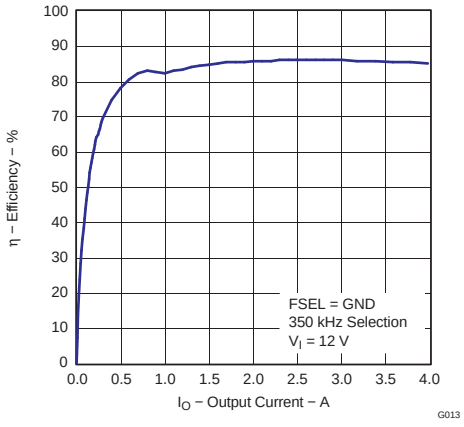


Figure 17. 1.05-V Efficiency vs. Output Current

9.3 700 kHz Operation Application

The schematic of Figure 18 shows a typical 700 kHz application schematic. The 700 kHz switching frequency is selected by connecting FSEL to the V5FILT pin. The input voltage is 12 V and the output voltage is 1.05 V.

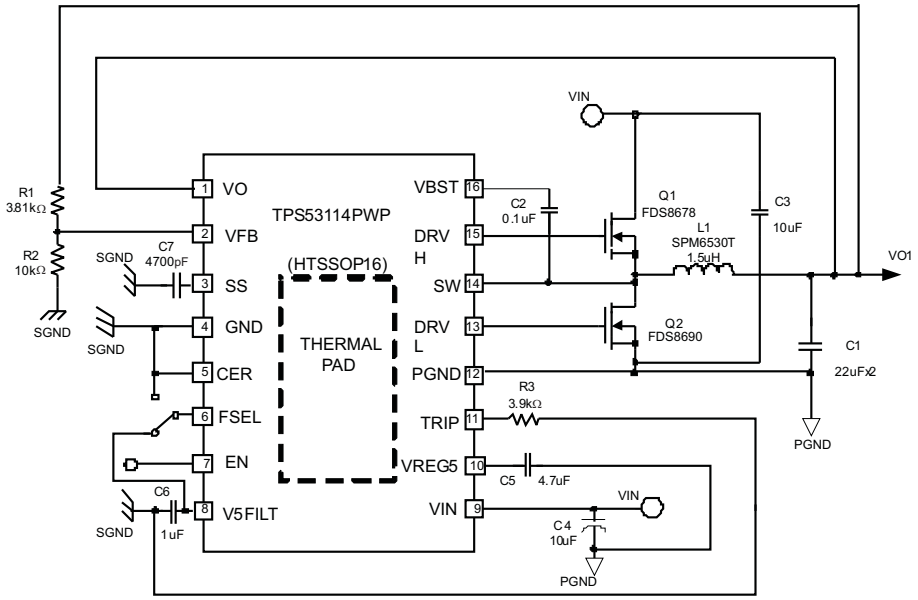


Figure 18. Typical Application Circuit at 700-kHz Switching Frequency Selection (FSEL pin = V5FILT)

9.3.1 Design Requirements

Table 2. Design Parameters

PARAMETERS	EXAMPLE VALUES
Input voltage	12 V
Output voltage	1.05 V
Output current	4 A
Switching frequency	700 kHz

9.3.2 Detailed Design Procedure

For the Detailed Design Procedure, refer to Detailed Design Procedure.

9.3.3 700 kHz Application Curves

The application curves of Figure 13 and Figure 14 apply to both the circuits of 700 kHz Operation Application and 350-kHz Operation Application .

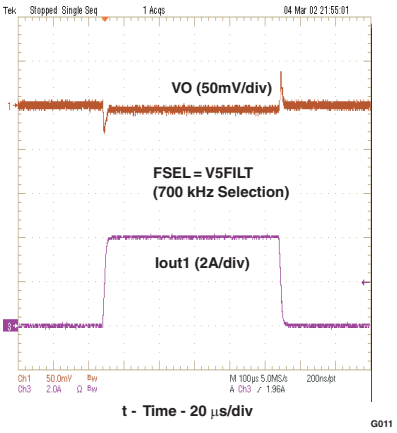


Figure 19. 1.05-V Load Transient Response

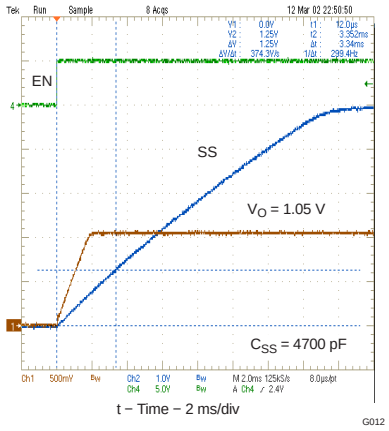


Figure 20. Startup Waveform

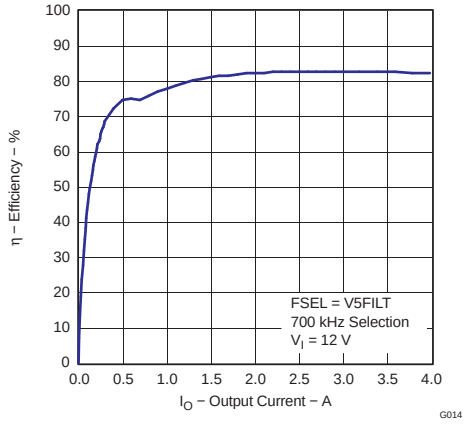


Figure 21. 1.05-V Efficiency vs. Output Current

10 Power Supply Recommendations

The TPS53114 is designed to operate from an input voltage supply range between 4.5 V and 24 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS53114 device additional 0.1 µF ceramic capacitance may be required in addition to the ceramic bypass capacitors, 10 µF.

11 Layout

11.1 Layout Guidelines

- Keep the input switching current loop as small as possible.
- Place the input capacitor (C3) close to the top switching FET.
- Place the input capacitor (C4) close to the IC VIN pin.
- The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions.
- Independent connections should be brought from the output to the feedback pin (VFB) and VO pin of the device.
- Keep analog and non-switching components away from switching components.
- Terminate the feedback resistor divider (R2), slow start capacitor C7), CER pin, V5FILT capacitor (C6) and TRIP resistor (R3) to signal ground (SGND).
- Connect the signal ground (SGND) copper area to the GND pin at the GND pin.
- Make a single point connection from the signal ground to power ground directly under the IC as shown.
- Do not allow switching current to flow under the device.

11.2 Layout Example

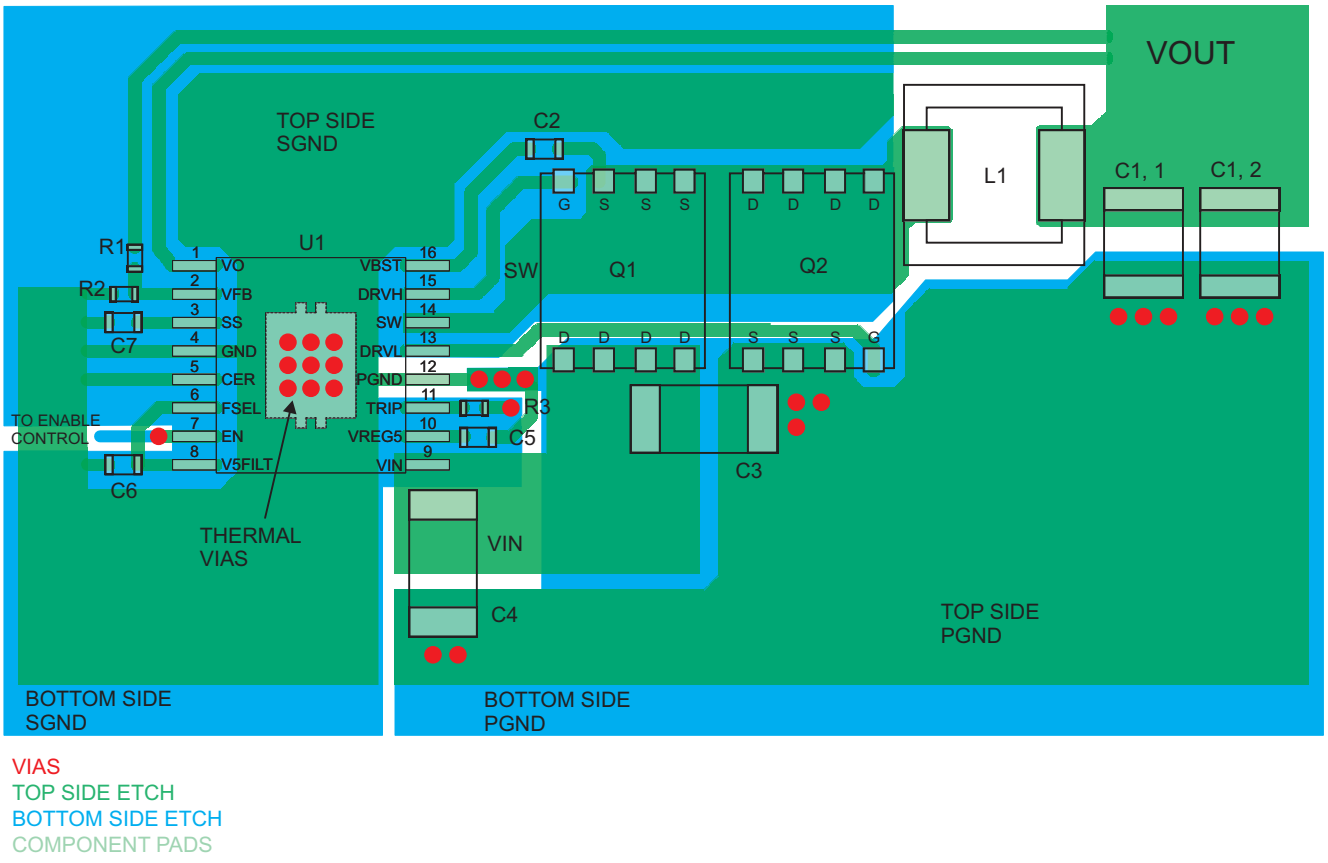


Figure 22. Typical TPS53114 Layout

12 Device and Documentation Support

12.1 Trademarks

D-CAP2 is a trademark of Texas Instruments.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS53114PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS53114	Samples
TPS53114PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS53114	Samples
TPS53114PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS53114	Samples
TPS53114PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS53114	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

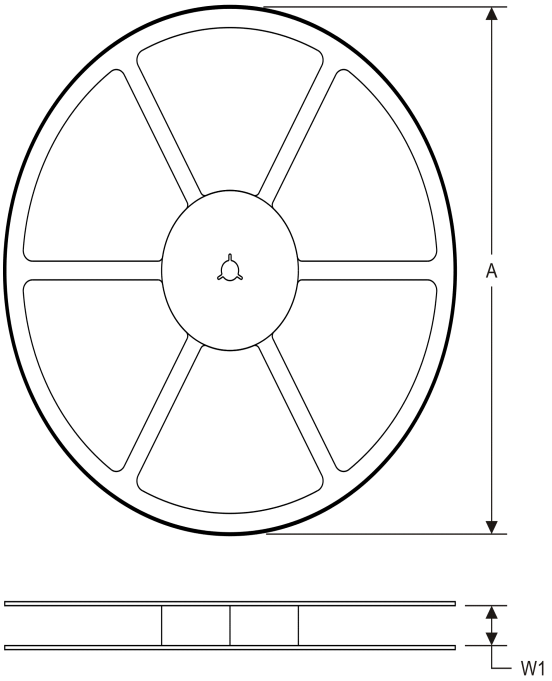
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

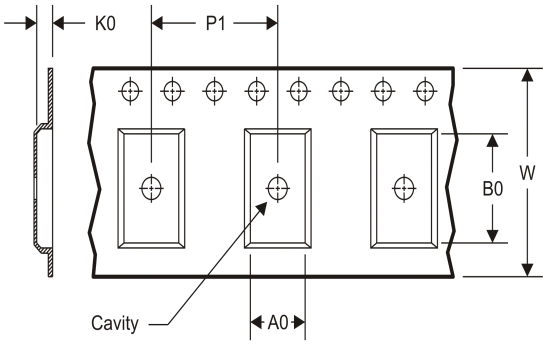
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



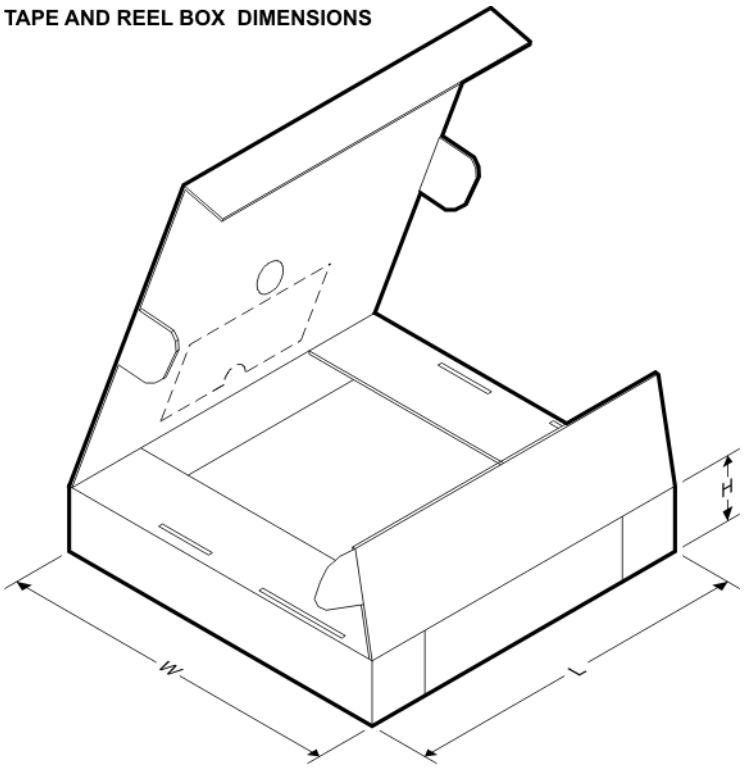
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53114PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS53114PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

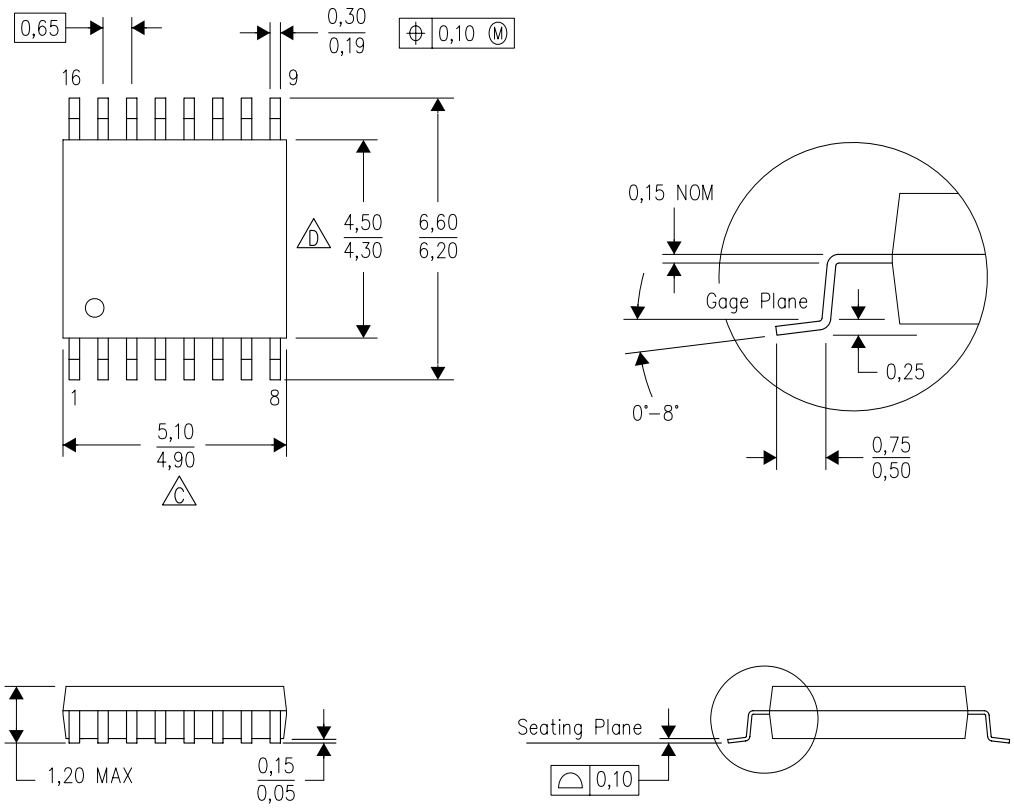
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53114PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0
TPS53114PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

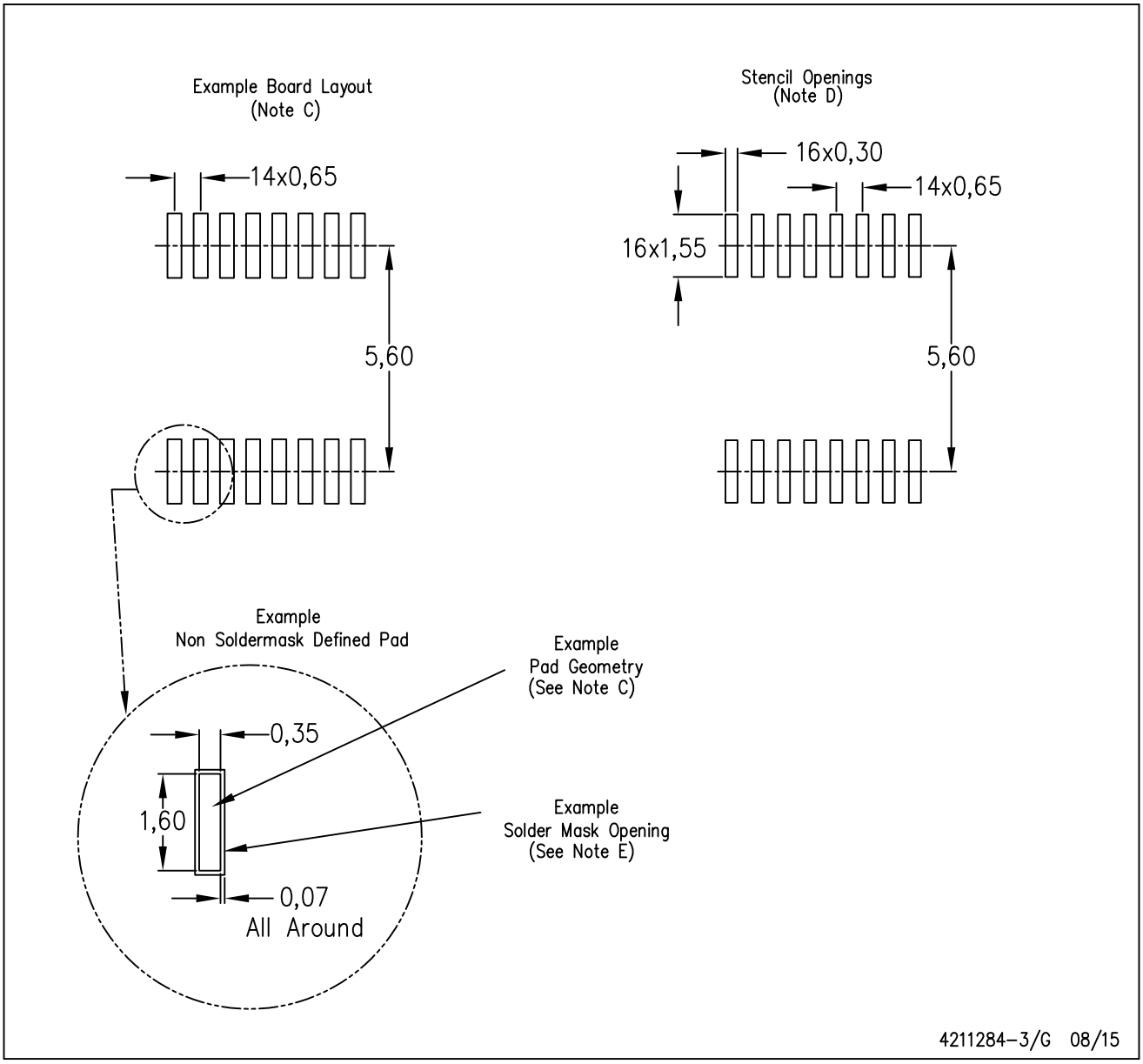
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

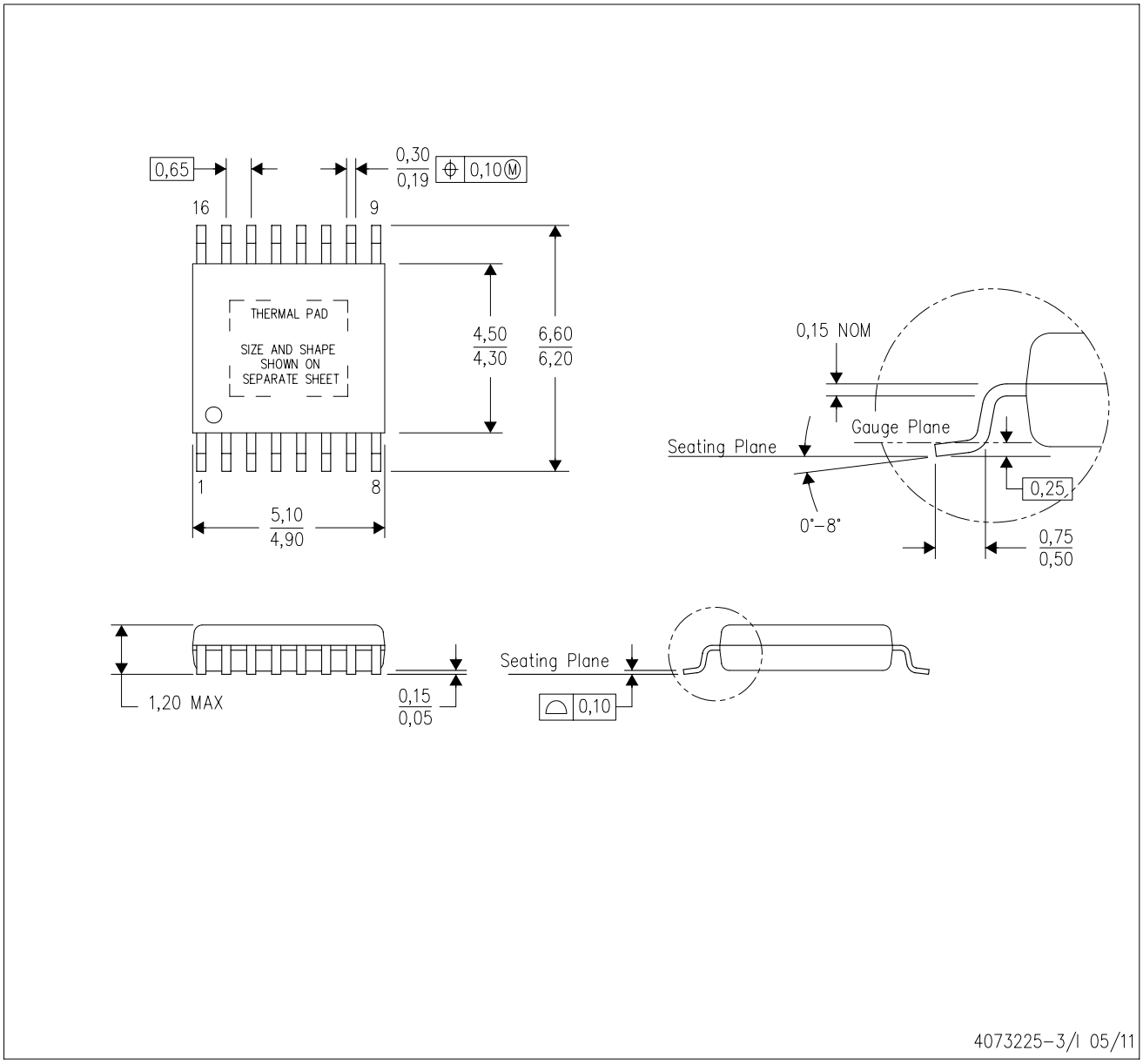
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

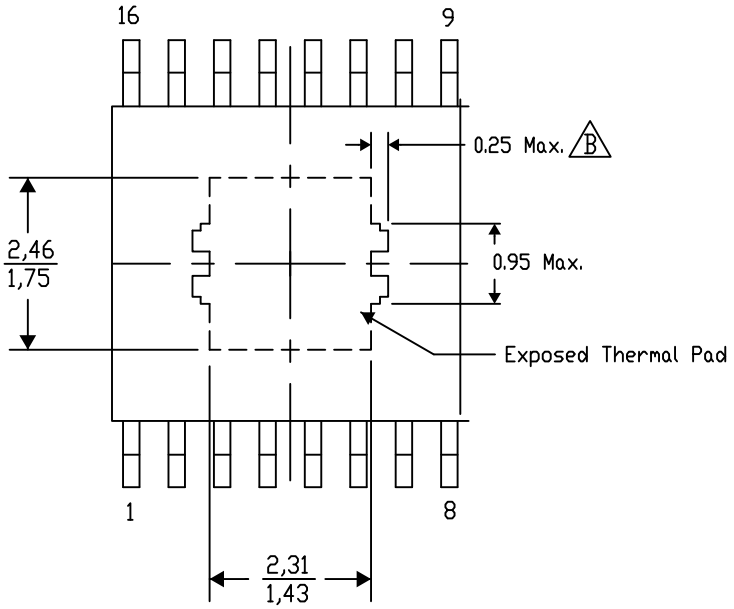
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

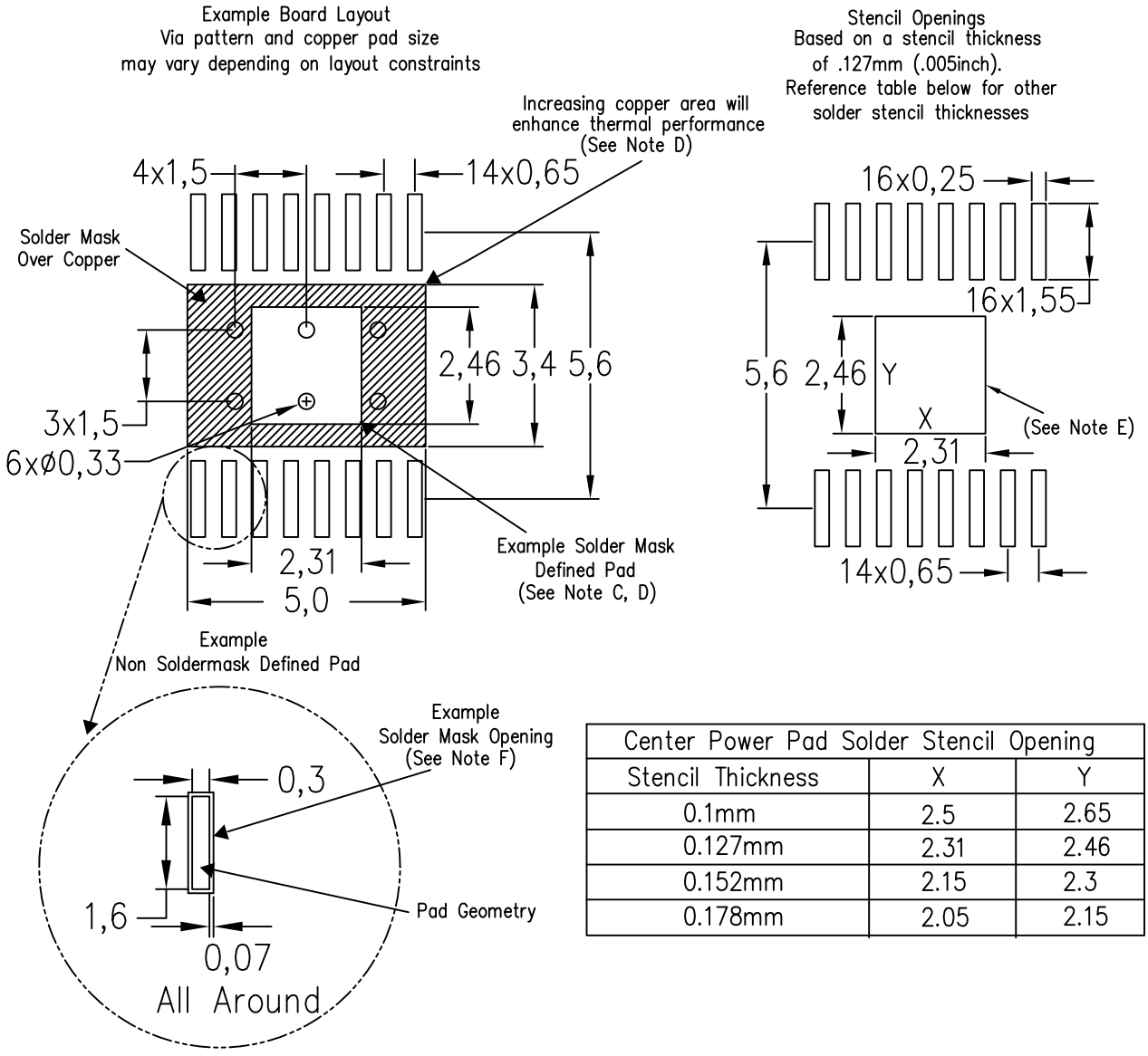
4206332–6/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–3/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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