

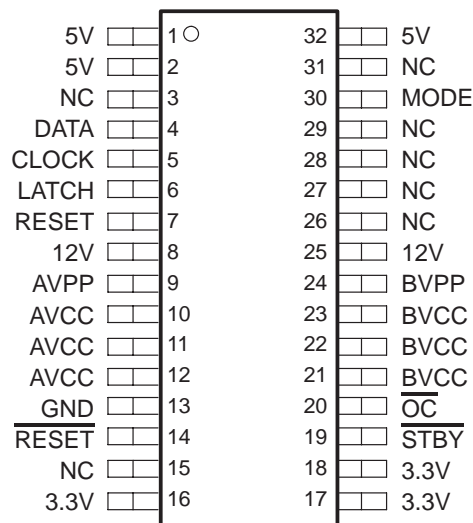
TPS2216

DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

- Fully Integrated xVCC and xVPP Switching
- xVPP Programmed Independent of xVCC
- 3.3-V, 5-V, and/or 12-V Power Distribution
- Low $r_{DS(on)}$ (60-m Ω xVCC Switch Typical)
- Short Circuit and Thermal Protection
- 150- μ A (Maximum) Quiescent Current
- Standby Mode: 50-mA Current Limit (Typ)
- 12-V Supply Can Be Disabled
- 3.3-V Low-Voltage Mode
- Meets PC Card™ Standards
- TTL-Logic Compatible Inputs
- Available in 30-Pin SSOP (DB) and 32-Pin TSSOP (DAP) Packages
- Break-Before-Make Switching
- Internal Power-On Reset

**DAP PACKAGE†
(TOP VIEW)**



description

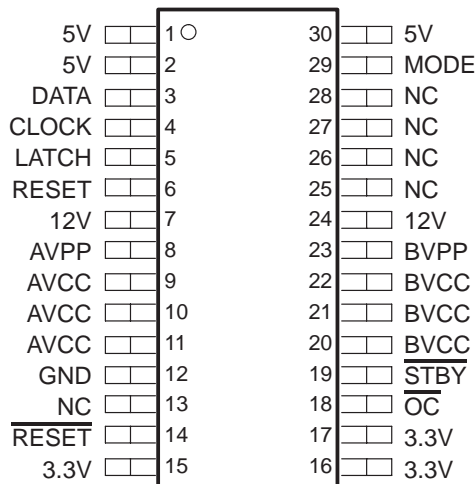
The TPS2216 PC Card power-interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit. This device allows the distribution of 3.3-V, 5-V, and/or 12-V power to the card. The current-limiting feature eliminates the need for fuses. Current-limit reporting can help the user isolate a system fault.

The TPS2216 features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5-V power. This feature facilitates low-power system designs such as sleep modes where only 3.3 V is available. This device also has the ability to program the xVPP outputs independent of the xVCC outputs. A standby mode that changes all output-current limits to 50 mA (typical) has been incorporated.

End-equipment applications for the TPS2216 include: notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, and bar-code scanners.

The TPS2216 is backward-compatible with the TPS2202A and TPS2206.

**DB PACKAGE†
(TOP VIEW)**



† The TPS2216 is identical to the TPS2214 in all respects except packaging and pin assignments.

NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PC Card is a trademark of PCMCIA (Personal Computer Memory Card International Association).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TPS2216 DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

AVAILABLE OPTIONS

| T _J | PACKAGED DEVICES† | |
|----------------|----------------------------|---------------------------------------|
| | PLASTIC SMALL OUTLINE (DB) | PowerPAD PLASTIC SMALL OUTLINE™ (DAP) |
| -40°C to 125°C | TPS2216DB(R) | TPS2216DAP(R) |

† The DB and DAP packages are available in tubes and left-end taped and reeled. Add R suffix to device type (e.g., TPS2216DBR) for taped and reeled.

Terminal Functions

| NAME | TERMINAL NO. | | I/O | DESCRIPTION |
|---------------------------|--------------------|---------------------------|-----|--|
| | DB | DAP | | |
| | 3.3V | 15, 16, 17 | | |
| 5V | 1, 2, 30 | 1, 2, 32 | I | 5-V input for card power and/or chip power |
| 12V | 7, 24 | 8, 25 | I | 12-V V _{pp} input card power |
| AVCC | 9, 10, 11 | 10, 11, 12 | O | VCC output: 3.3-V, 5-V, GND or high impedance to card |
| AVPP | 8 | 9 | O | VPP output: 3.3-V, 5-V, 12-V, GND or high impedance to card |
| BVCC | 20, 21, 22 | 21, 22, 23 | O | VCC output: 3.3-V, 5-V, GND or high impedance to card |
| BVPP | 23 | 24 | O | VPP output: 3.3-V, 5-V, 12-V, GND or high impedance to card |
| GND | 12 | 13 | | Ground |
| MODE | 29 | 30 | I | TPS2206 operation when floating or pulled low; must be pulled high externally for TPS2216 operation. MODE is internally pulled low with a 150-kΩ pulldown resistor. |
| $\overline{\text{OC}}$ | 18 | 20 | O | Logic-level output that goes low when an overcurrent or overtemperature condition exists. |
| RESET | 6 | 7 | I | Logic-level reset input active high. Do not connect if $\overline{\text{RESET}}$ pin is used. RESET is internally pulled low with a 150-kΩ pulldown resistor. |
| $\overline{\text{RESET}}$ | 14 | 14 | I | Logic-level reset input active low. Do not connect if RESET pin is used. The pin is internally pulled high with a 150-kΩ pullup resistor. |
| $\overline{\text{STBY}}$ | 19 | 19 | I | Logic-level active low input sets the TPS2216 to standby mode and sets all current limits to 50 mA. The pin is internally pulled high with a 150-kΩ pullup resistor. |
| CLOCK | 4 | 5 | I | Logic-level clock for serial data word |
| DATA | 3 | 4 | I | Logic-level serial data word |
| LATCH | 5 | 6 | I | Logic-level latch for serial data word |
| NC | 13, 25, 26, 27, 28 | 3, 15, 26, 27, 28, 29, 31 | | No internal connection |

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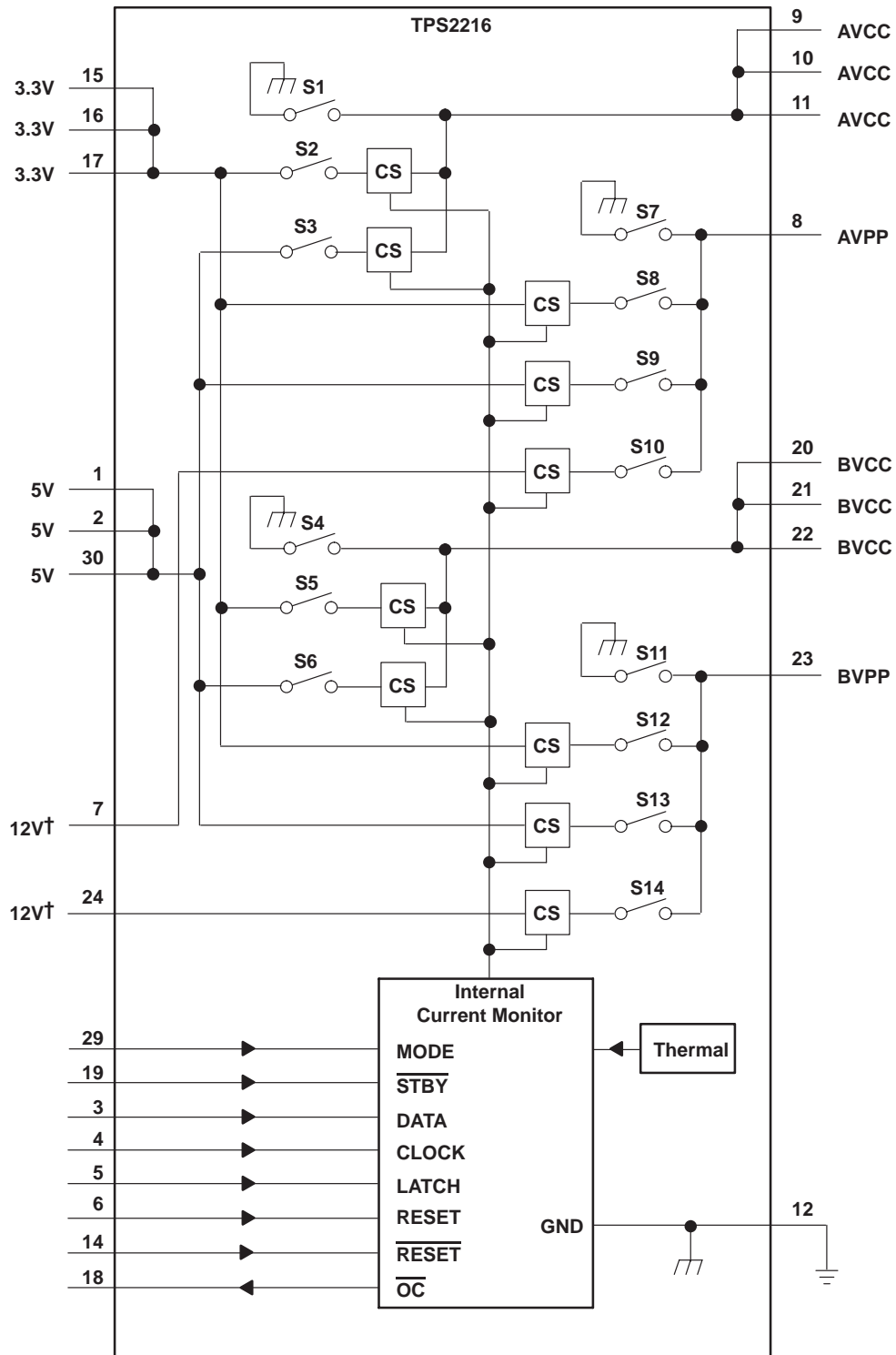


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TPS2216 DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

functional block diagram (pin numbers refer to DB package)



† Both 12V pins must be connected together.

TPS2216 DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

absolute maximum ratings over operating virtual free-air temperature (unless otherwise noted)†

| | |
|--|------------------------------|
| Input voltage range for card power: $V_I(3.3V)$ | -0.3 V to 6 V |
| $V_I(5V)$ | -0.3 V to 6 V |
| $V_I(12V)$ | -0.3 V to 14 V |
| Logic input voltage | -0.3 V to 6 V |
| Output voltage range: $V_O(xVCC)$ | -0.3 V to 6 V |
| $V_O(xVPP)$ | -0.3 V to 14 V |
| Continuous total power dissipation | See Dissipation Rating Table |
| Output current: $I_O(xVCC)$ | Internally limited |
| $I_O(xVPP)$ | Internally limited |
| Operating virtual junction temperature range, T_J | -40°C to 125°C |
| Storage temperature range, T_{stg} | -55°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR‡ ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|---|--|--|--|
| DB | 1095 mW | 10.99 mW/°C | 602 mW | 438 mW |
| DAP | 4255 mW | 42.55 mW/°C | 2340 mW | 1702 mW |

‡ These devices are mounted on an JEDEC low-k board (2 oz. traces on surface), 1-W power applied.

recommended operating conditions

| | | MIN | MAX | UNIT |
|---|--|-----|------|------|
| Input voltage, V_I | $V_I(3.3V)$ | 2.7 | 5.25 | V |
| | $V_I(5V)$ | 2.7 | 5.25 | V |
| | $V_I(12V)$ | 2.7 | 13.5 | V |
| Output current, I_O | $I_O(VCC)$ at $T_A = 70^\circ\text{C}$ | | 1 | A |
| | $I_O(VPP)$ at $T_A = 70^\circ\text{C}$ | | 200 | mA |
| Clock frequency | | | 2.5 | MHz |
| Pulse duration | Data | 200 | | ns |
| | Latch | 250 | | |
| | Clock | 100 | | |
| Data hold time§ | | 100 | | ns |
| Data setup time§ | | 100 | | ns |
| Latch delay time§ | | 100 | | ns |
| Clock delay time§ | | 250 | | ns |
| Operating virtual junction temperature, T_J | | -40 | 125 | °C |

§ Refer to Figures 2 and 3.



TPS2216

DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

electrical characteristics, $T_J = 25^\circ\text{C}$, $V_{I(5V)} = 5\text{ V}$, $V_{I(3.3V)} = 3.3\text{ V}$, $V_{I(12V)} = 12\text{ V}$, $\overline{\text{STBY}}$ floating, all outputs unloaded (unless otherwise noted)

power switch

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|--|--|---|-------|-----|------------------|----------|
| Switch resistance [†] | 3.3 V to xVCC, with one switch on | $T_J = 25^\circ\text{C}$, $I_O = 1\text{ A}$ | | 60 | 85 | m Ω | |
| | | $T_J = 125^\circ\text{C}$, $I_O = 1\text{ A}$ | | 90 | 120 | | |
| | | $T_J = 25^\circ\text{C}$, $V_{I(5V)} = 0$, $I_O = 1\text{ A}$ | | 65 | 85 | | |
| | | $T_J = 125^\circ\text{C}$, $V_{I(5V)} = 0$, $I_O = 1\text{ A}$ | | 90 | 130 | | |
| | 5 V to xVCC, with one switch on | $T_J = 25^\circ\text{C}$, $I_O = 1\text{ A}$ | | 60 | 85 | | |
| | | $T_J = 125^\circ\text{C}$, $I_O = 1\text{ A}$ | | 90 | 120 | | |
| | 3.3 V to xVCC, with two switches on | $T_J = 25^\circ\text{C}$, $I_O = 1\text{ A each}$ | | 65 | 105 | | |
| | | $T_J = 125^\circ\text{C}$, $I_O = 1\text{ A each}$ | | 95 | 140 | | |
| | | $T_J = 25^\circ\text{C}$, $V_{I(5V)} = 0$, $I_O = 1\text{ A each}$ | | 70 | 105 | | |
| | | $T_J = 125^\circ\text{C}$, $V_{I(5V)} = 0$, $I_O = 1\text{ A each}$ | | 100 | 140 | | |
| | 5 V to xVCC, with two switches on | $T_J = 25^\circ\text{C}$, $I_O = 1\text{ A each}$ | | 70 | 105 | | |
| | | $T_J = 125^\circ\text{C}$, $I_O = 1\text{ A each}$ | | 100 | 140 | | |
| | 3.3 V/5 V/12 V to xVPP | $T_J = 25^\circ\text{C}$, $I_O = 50\text{ mA}$ | | 0.7 | 1 | | Ω |
| | | $T_J = 125^\circ\text{C}$, $I_O = 50\text{ mA}$ | | 1.4 | 2.5 | | |
| 3.3 V/5 V to xVCC | $T_J = 25^\circ\text{C}$, $\overline{\text{STBY}} = \text{low}$, $I_O = 30\text{ mA}$ | | 1.4 | 2 | | | |
| | $T_J = 125^\circ\text{C}$, $\overline{\text{STBY}} = \text{low}$, $I_O = 30\text{ mA}$ | | 2 | 3 | | | |
| 3.3 V/5 V/12 V to xVPP | $T_J = 25^\circ\text{C}$, $\overline{\text{STBY}} = \text{low}$, $I_O = 30\text{ mA}$ | | 5 | 7 | | | |
| | $T_J = 125^\circ\text{C}$, $\overline{\text{STBY}} = \text{low}$, $I_O = 30\text{ mA}$ | | 10 | 16 | | | |
| Clamp low voltage | $V_{O(xVCC)}$ | $I_{O(xVCC)}$ at 10 mA, After reset | | 0.275 | 0.8 | V | |
| | $V_{O(xVPP)}$ | $I_{O(xVPP)}$ at 10 mA, After reset | | 0.275 | 0.8 | | |
| I_{lkg} Leakage current | $I_{O(xVCC)}$ High-impedance state | $T_J = 25^\circ\text{C}$ | | 1 | 10 | μA | |
| | | $T_J = 125^\circ\text{C}$ | | 2 | 50 | | |
| | $I_{O(xVPP)}$ High-impedance state | $T_J = 25^\circ\text{C}$ | | 1 | 10 | | |
| | | $T_J = 125^\circ\text{C}$ | | 2 | 50 | | |
| I_{OS} Short-circuit output current limit [†] | $I_{O(xVCC)}$ | $T_J = 85^\circ\text{C}$, output powered into a short to GND | | 1 | 2.2 | A | |
| | $I_{O(xVPP)}$ | | | 250 | 500 | mA | |
| | Standby mode $I_{O(xVCC)}$ | $T_J = 85^\circ\text{C}$, Output powered into a short to GND, $\overline{\text{STBY}} = 0\text{ V}$ | | 35 | 50 | 65 | mA |
| | Standby mode $I_{O(xVPP)}$ | | | 30 | 50 | 60 | |
| Current limit response time [‡] | xVCC switch | 100-m Ω short circuit | | 100 | | μs | |
| | xVPP switch | | | 16 | | | |
| I_I Input current [§] | Normal operation and in reset mode | $I_I(3.3V)$ | $V_{O(xVCC)} = V_{O(xVPP)} = 5\text{ V}$ | 0.01 | 2 | μA | |
| | | $I_I(5V)$ | | 100 | 120 | | |
| | | $I_I(12V)$ | | 6 | 10 | | |
| | | $I_I(3.3V)$ | $V_{I(5V)} = 0$, $V_{O(xVCC)} = 3.3\text{ V}$, $V_{O(xVPP)} = 12\text{ V}$ | 100 | 120 | μA | |
| | | $I_I(5V)$ | | 0 | | | |
| | | $I_I(12V)$ | | 22 | 30 | | |
| | Shutdown mode | $I_I(3.3V)$ | $V_{O(xVCC)} = \text{Hi-Z}$, $V_{O(xVPP)} = \text{Hi-Z}$ | | 1 | μA | |
| | | $I_I(5V)$ | | | 1 | | |
| $I_I(12V)$ | | | | 1 | | | |
| Thermal shutdown [‡] | Trip point, T_J | | | 155 | | $^\circ\text{C}$ | |
| | Hysteresis | | | 10 | | | |

[†] Pulse-testing techniques maintain junction temperature close to ambient temperature (250- μs -wide pulse, less than 0.5% duty cycle); thermal effects must be taken into account separately.

[‡] Specified by design, not tested in production.

[§] Input currents do not include logic input currents (presented in electrical characteristics for logic section); clock is inactive.

NOTE: $V_{I(3.3V)}$ or $V_{I(5V)}$ must be biased for switches to function.



TPS2216
DUAL-SLOT PC CARD POWER-INTERFACE SWITCH
FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

logic section (CLOCK, DATA, LATCH, MODE, RESET, $\overline{\text{RESET}}$, $\overline{\text{STBY}}$, $\overline{\text{OC}}$)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|---------------------|-----|-----|---------------|
| Logic input current | $I_{I(\text{RESET})}$ or $I_{I(\overline{\text{RESET}})}^\dagger$ | $V_{I(\text{RESET})} = 5 \text{ V}$ or $V_{I(\overline{\text{RESET}})} = 0 \text{ V}$ | | 30 | 50 | μA |
| | | $V_{I(\text{RESET})} = 0 \text{ V}$ or $V_{I(\overline{\text{RESET}})} = 5 \text{ V}$ | | | 1 | |
| | $I_{I(\text{MODE})}^\dagger$ | $V_{I(\text{MODE})} = 5 \text{ V}$ | | 30 | 50 | |
| | | $V_{I(\text{MODE})} = 0 \text{ V}$ | | | 1 | |
| | $I_{I(\overline{\text{STBY}})}^\dagger$ | $V_{I(\overline{\text{STBY}})} = 5 \text{ V}$ | | | 1 | |
| | | $V_{I(\overline{\text{STBY}})} = 0 \text{ V}$ | | 30 | 50 | |
| $I_{I(\text{CLOCK})}$ or $I_{I(\text{DATA})}$ or $I_{I(\text{LATCH})}$ | | | | | 1 | |
| Logic input high level | $V_{I(5V)} = 5 \text{ V}$ | | 2 | | | V |
| | $V_{I(5V)} = 0 \text{ V}$ | | 2 | | | |
| Logic input low level | | | | | 0.8 | V |
| Logic output high level, $\overline{\text{OC}}$ | $V_{I(5V)} = 5 \text{ V}, I_{O} = 1 \text{ mA}$ | | $V_{I(5V)} - 0.4$ | | | V |
| | $V_{I(5V)} = 0 \text{ V}, I_{O} = 1 \text{ mA}$ | | $V_{I(3.3V)} - 0.4$ | | | |
| Logic output low level, $\overline{\text{OC}}$ | $I_{O} = 1 \text{ mA}$ | | | | 0.4 | V |

† RESET and MODE have internal 150-k Ω pulldown resistors; $\overline{\text{RESET}}$ and $\overline{\text{STBY}}$ have internal 150-k Ω pullup resistors.



TPS2216

DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

switching characteristics

| PARAMETER† | LOAD CONDITION† | TEST CONDITIONS† | MIN | TYP | MAX | UNIT |
|--|---|--|---------------|------|-----|------|
| t_r Output rise times‡ | $C_L(xVCC) = 0.1 \mu F$, $C_L(xVPP) = 0.1 \mu F$, $I_O(xVCC) = 0S$, $I_O(xVPP) = 0S$ | $V_O(xVCC)$ | | 1 | | ms |
| | | $V_O(xVPP)$ | | 0.8 | | |
| | $C_L(xVCC) = 150 \mu F$, $C_L(xVPP) = 10 \mu F$, $I_O(xVCC) = 1 A$, $I_O(xVPP) = 50 mA$ | $V_O(xVCC)$ | | 1.2 | | |
| | | $V_O(xVPP)$ | | 2.5 | | |
| t_f Output fall times‡ | $C_L(xVCC) = 0.1 \mu F$, $C_L(xVPP) = 0.1 \mu F$, $I_O(xVCC) = 0S$, $I_O(xVPP) = 0S$ | $V_O(xVCC)$ | | 0.01 | | ms |
| | | $V_O(xVPP)$ | | 0.01 | | |
| | $C_L(xVCC) = 150 \mu F$, $C_L(xVPP) = 10 \mu F$, $I_O(xVCC) = 1 A$, $I_O(xVPP) = 50 mA$ | $V_O(xVCC)$ | | 3 | | |
| | | $V_O(xVPP)$ | | 8 | | |
| t_{pd} Propagation delay‡ | $C_L(xVCC) = 0.1 \mu F$, $C_L(xVPP) = 0.1 \mu F$, $I_O(xVCC) = 0S$, $I_O(xVPP) = 0S$ | Latch↑ to xVPP (12 V) | $t_{pd}(on)$ | 3 | | ms |
| | | | $t_{pd}(off)$ | 25 | | |
| | | Latch↑ to xVPP (5 V) | $t_{pd}(on)$ | 0.6 | | |
| | | | $t_{pd}(off)$ | 8.5 | | |
| | | Latch↑ to xVPP (3.3 V), $V_I(5V) = 5 V$ | $t_{pd}(on)$ | 0.6 | | |
| | | | $t_{pd}(off)$ | 9 | | |
| | | Latch↑ to xVPP (3.3 V), $V_I(5V) = 0 V$ | $t_{pd}(on)$ | 1.4 | | |
| | | | $t_{pd}(off)$ | 9 | | |
| | Latch↑ to xVCC (5 V) | $t_{pd}(on)$ | 0.3 | | | |
| | | $t_{pd}(off)$ | 15 | | | |
| | Latch↑ to xVCC (3.3 V), $V_I(5V) = 5 V$ | $t_{pd}(on)$ | 0.2 | | | |
| | | $t_{pd}(off)$ | 15 | | | |
| | Latch↑ to xVCC (3.3 V), $V_I(5V) = 0 V$ | $t_{pd}(on)$ | 0.4 | | | |
| | | $t_{pd}(off)$ | 15 | | | |
| | $C_L(xVCC) = 150 \mu F$, $C_L(xVPP) = 10 \mu F$, $I_O(xVCC) = 1 A$, $I_O(xVPP) = 50 mA$ | Latch↑ to xVPP (12 V) | $t_{pd}(on)$ | 4.5 | | |
| | | | $t_{pd}(off)$ | 13 | | |
| Latch↑ to xVPP (5 V) | | $t_{pd}(on)$ | 3.3 | | | |
| | | $t_{pd}(off)$ | 8 | | | |
| Latch↑ to xVPP (3.3 V), $V_I(5V) = 5 V$ | | $t_{pd}(on)$ | 3 | | | |
| | | $t_{pd}(off)$ | 9 | | | |
| Latch↑ to xVPP (3.3 V), $V_I(5V) = 0 V$ | | $t_{pd}(on)$ | 3 | | | |
| | | $t_{pd}(off)$ | 9 | | | |
| Latch↑ to xVCC (5 V) | $t_{pd}(on)$ | 1 | | | | |
| | $t_{pd}(off)$ | 12 | | | | |
| Latch↑ to xVCC (3.3 V), $V_I(5V) = 5 V$ | $t_{pd}(on)$ | 0.6 | | | | |
| | $t_{pd}(off)$ | 12 | | | | |
| Latch↑ to xVCC (3.3 V), $V_I(5V) = 0 V$ | $t_{pd}(on)$ | 1 | | | | |
| | $t_{pd}(off)$ | 12 | | | | |

† Refer to *Parameter Measurement Information*

‡ Specified by design; not tested in production.

§ No card inserted, assumes 0.1- μF recommended output capacitor (see Figure 34).



TPS2216
DUAL-SLOT PC CARD POWER-INTERFACE SWITCH
FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

PARAMETER MEASUREMENT INFORMATION

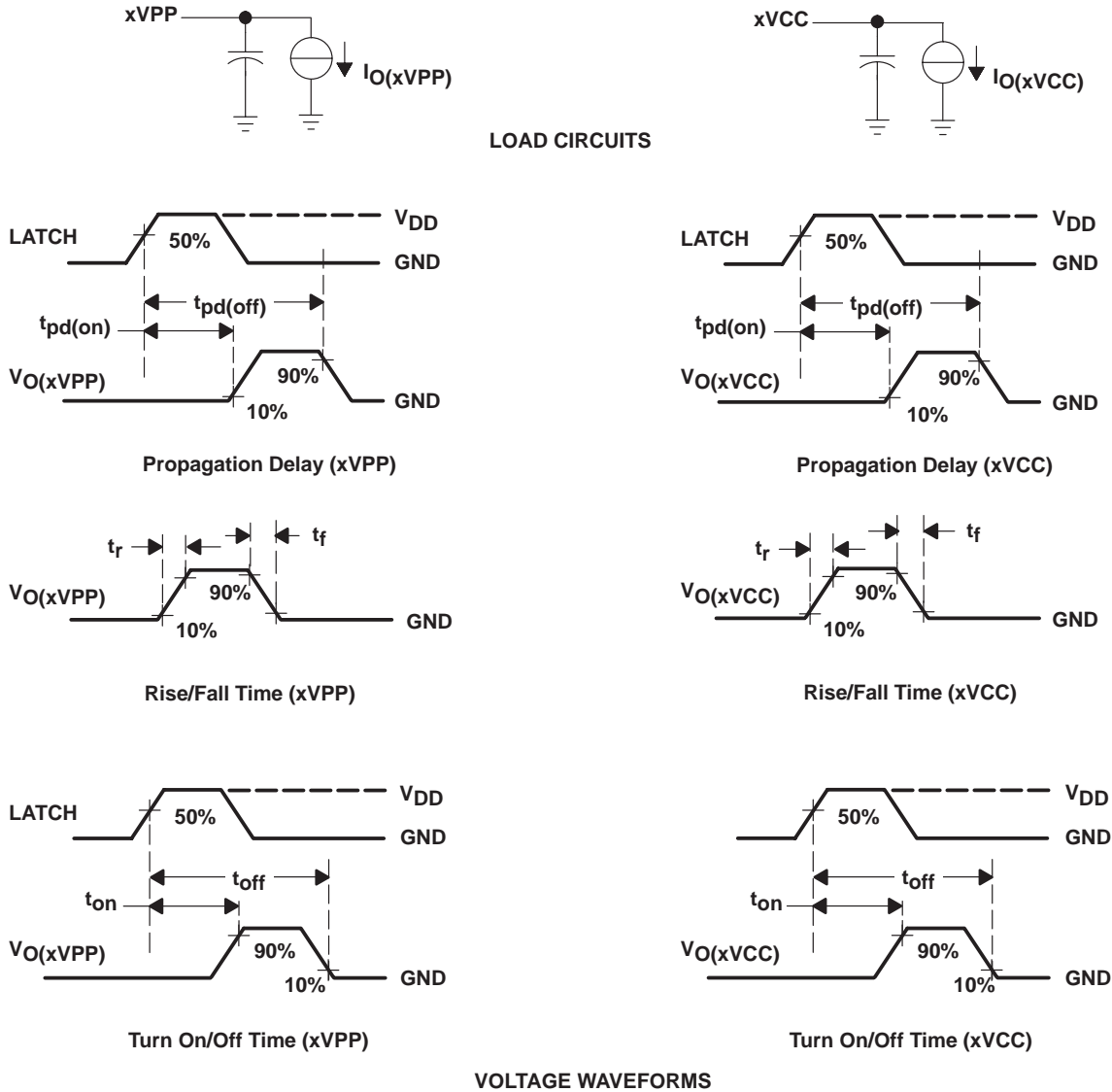
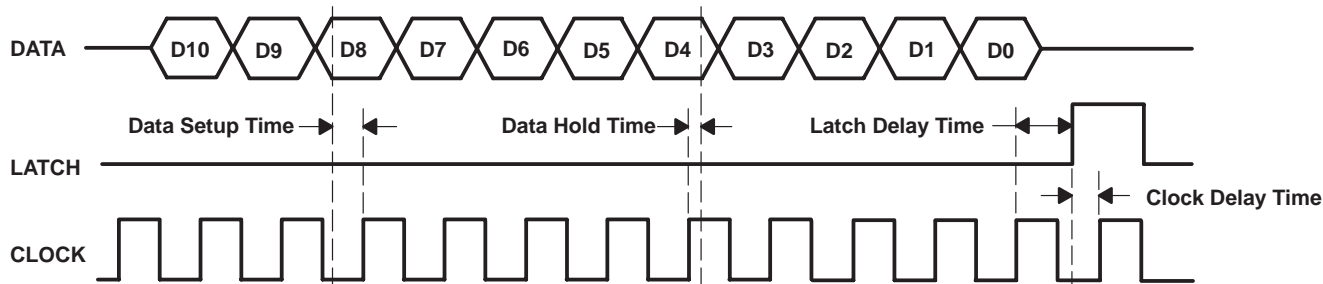


Figure 1. Test Circuits and Voltage Waveforms

TPS2216
DUAL-SLOT PC CARD POWER-INTERFACE SWITCH
FOR SERIAL PCMCIA CONTROLLERS

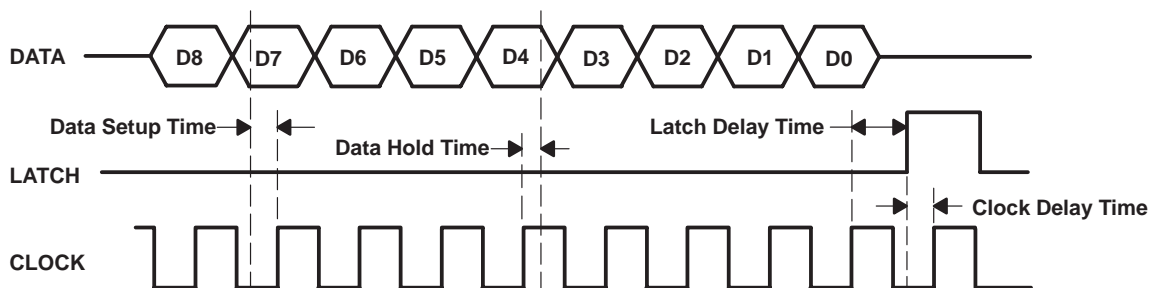
SLVS179D – MARCH 1999 – REVISED JUNE 2000

PARAMETER MEASUREMENT INFORMATION



NOTE: Data is clocked in on the positive edge of the clock. The positive edge of the latch signal should occur before the next positive edge of the clock. For definition of D0 to D10, see the control logic table.

Figure 2. Serial-Interface Timing for Independent xVPP Switching When MODE = 5 V or 3.3 V



NOTE: Data is clocked in on the positive edge of the clock. The positive edge of the latch signal should occur before the next positive edge of the clock. For definition of D0 to D8, see the control logic table.

Figure 3. Serial-Interface Timing When MODE = 0 V or Floating

Table of Timing Diagrams†

| | FIGURE |
|---|--------|
| Short-circuit current response, short applied to powered-on 5-V xVCC switch output | 4 |
| Short-circuit current response, short applied to powered-on 12-V xVPP switch output | 5 |
| OC response with ramped load on 5-V xVCC switch output | 6 |
| OC response with ramped load on 12-V xVPP switch output | 7 |

† Timing tests are conducted at free-air temperature, $V_I(5V) = 5\text{ V}$, $V_I(3.3V) = 3.3\text{ V}$, $V_I(12V) = 12\text{ V}$, $C_L = 0.1\text{ }\mu\text{F}$ on each output, $\overline{\text{STBY}}$ floating.

TPS2216
DUAL-SLOT PC CARD POWER-INTERFACE SWITCH
FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

PARAMETER MEASUREMENT INFORMATION

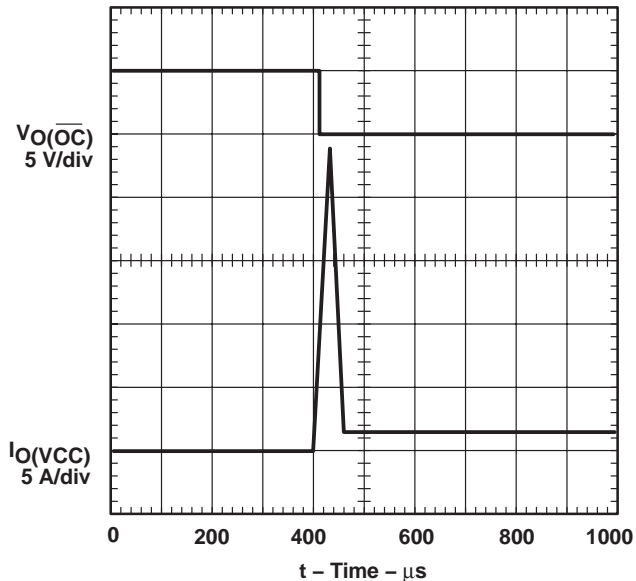


Figure 4. Short-Circuit Response, Short Applied to Powered-on 5-V xVCC-Switch Output

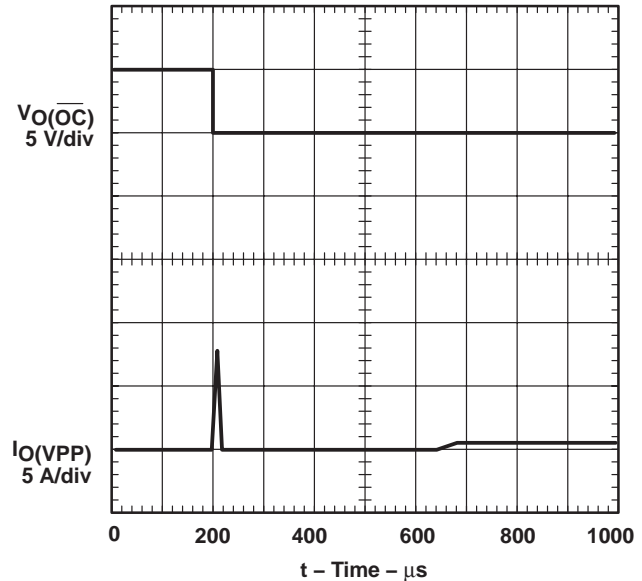


Figure 5. Short-Circuit Response, Short Applied to Powered-on 12-V xVPP-Switch Output

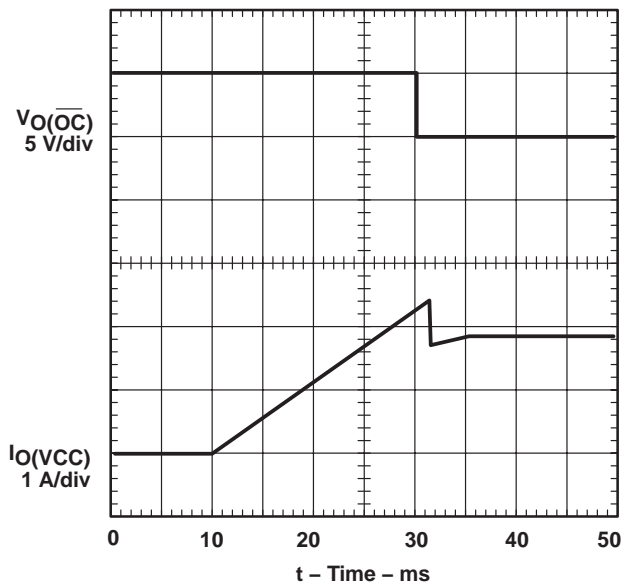


Figure 6. $\overline{V_O}$ Response With Ramped Load on 5-V xVCC-Switch Output

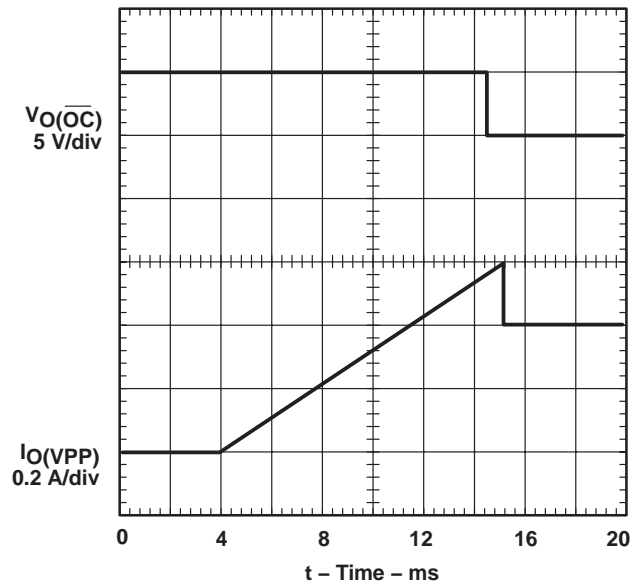


Figure 7. $\overline{V_O}$ Response With Ramped Load on 12-V xVPP-Switch Output

TPS2216

DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS

Table of Graphs

| | | | FIGURE |
|----------------|--|-------------------------|--------|
| $t_{pd(on)}$ | Turnon propagation delay time, 3.3-V xVCC switch | vs Load capacitance | 8 |
| $t_{pd(off)}$ | Turnoff propagation delay time, 3.3-V xVCC switch | vs Load capacitance | 9 |
| $t_{pd(on)}$ | Turnon propagation delay time, 5-V xVCC switch | vs Load capacitance | 10 |
| $t_{pd(off)}$ | Turnoff propagation delay time, 5-V xVCC switch | vs Load capacitance | 11 |
| $t_{pd(on)}$ | Turnon propagation delay time, 12-V xVPP switch | vs Load capacitance | 12 |
| $t_{pd(off)}$ | Turnoff propagation delay time, 12-V xVPP switch | vs Load capacitance | 13 |
| t_r | Rise time, 3.3-V xVCC switch | vs Load capacitance | 14 |
| t_f | Fall time, 3.3-V xVCC switch | vs Load capacitance | 15 |
| t_r | Rise time, 5-V xVCC switch | vs Load capacitance | 16 |
| t_f | Fall time, 5-V xVCC switch | vs Load capacitance | 17 |
| t_r | Rise time, 12-V xVPP switch | vs Load capacitance | 18 |
| t_f | Fall time, 12-V xVPP switch | vs Load capacitance | 19 |
| I_I | Input current at $V_O(xVCC) = V_O(xVPP) = 3.3\text{ V}$ | vs Junction temperature | 20 |
| | Input current at $V_O(xVCC) = V_O(xVPP) = 5\text{ V}$ | vs Junction temperature | 21 |
| | Input current at $V_O(xVCC) = 5\text{ V}$, $V_O(xVPP) = 12\text{ V}$ | vs Junction temperature | 22 |
| $r_{DS(on)}$ | Static drain-source on-state resistance, 3.3-V xVCC switch ($V_I(5V)=0$) | vs Junction temperature | 23 |
| | Static drain-source on-state resistance, 3.3-V xVCC switch | vs Junction temperature | 24 |
| | Static drain-source on-state resistance, 5-V xVCC switch | vs Junction temperature | 25 |
| | Static drain-source on-state resistance, 12-V xVPP switch | vs Junction temperature | 26 |
| $V_{IO(xVCC)}$ | DC input-to-output voltage (drop), 3.3-V xVCC switch ($V_I(5V)=0$) | vs Load current | 27 |
| | DC input-to-output voltage (drop), 3.3-V xVCC switch | vs Load current | 28 |
| | DC input-to-output voltage (drop), 5-V xVCC switch | vs Load current | 29 |
| $V_{IO(xVPP)}$ | DC input-to-output voltage (drop), 12-V xVPP switch | vs Load current | 30 |
| I_{OS} | Short-circuit current limit, 3.3-V xVCC switch | vs Junction temperature | 31 |
| | Short-circuit current limit, 5-V xVCC switch | vs Junction temperature | 32 |
| | Short-circuit current limit, 12-V xVPP switch | vs Junction temperature | 33 |

NOTE: Electrical characteristics tests are conducted at $V_I(5V) = 5\text{ V}$, $V_I(3.3V) = 3.3\text{ V}$, $V_I(12V) = 12\text{ V}$, $C_L = 0.1\text{ }\mu\text{F}$ on each output, STBY floating (unless otherwise noted on Figures).

TPS2216
DUAL-SLOT PC CARD POWER-INTERFACE SWITCH
FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS

**TURNON PROPAGATION DELAY TIME,
 3.3-V xVCC SWITCH
 vs
 LOAD CAPACITANCE**

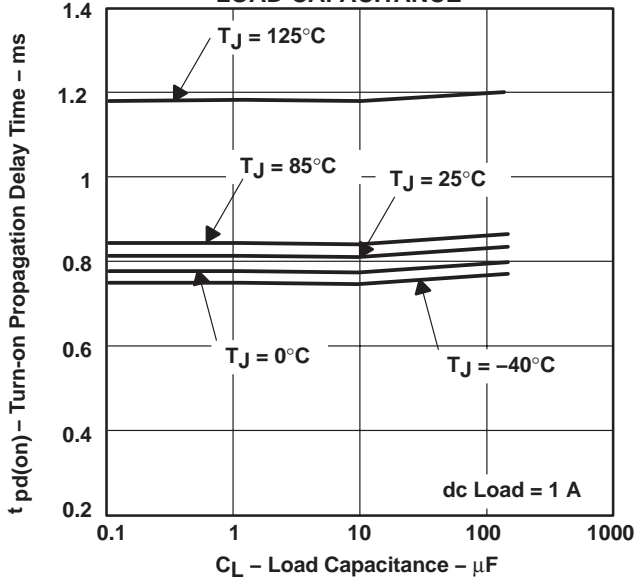


Figure 8

**TURNOFF PROPAGATION DELAY TIME,
 3.3-V xVCC SWITCH
 vs
 LOAD CAPACITANCE**

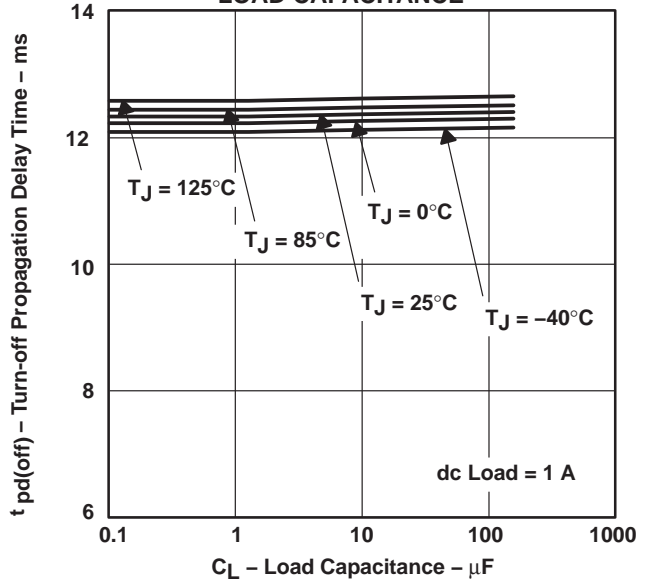


Figure 9

**TURNON PROPAGATION DELAY TIME,
 5-V xVCC SWITCH
 vs
 LOAD CAPACITANCE**

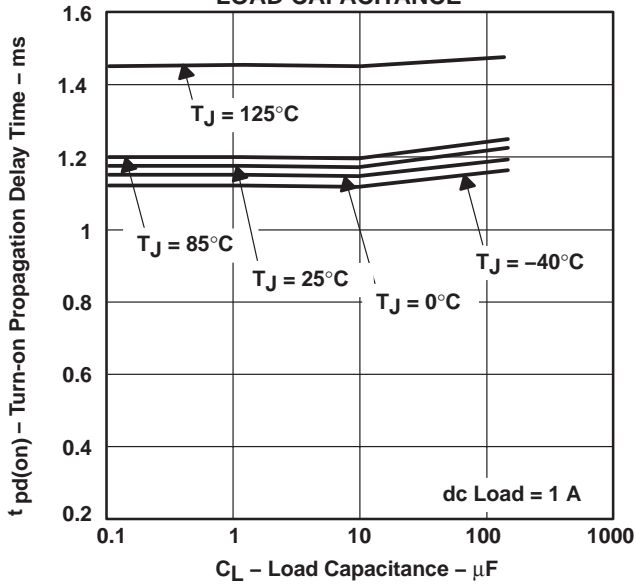


Figure 10

**TURNOFF PROPAGATION DELAY TIME,
 5-V xVCC SWITCH
 vs
 LOAD CAPACITANCE**

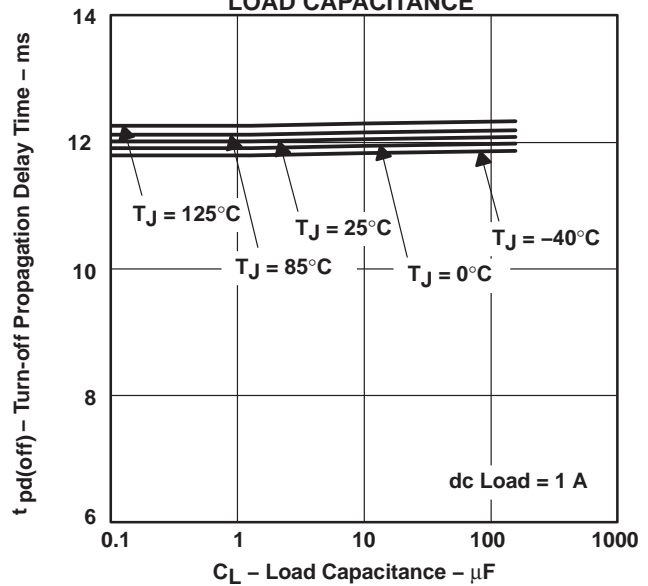
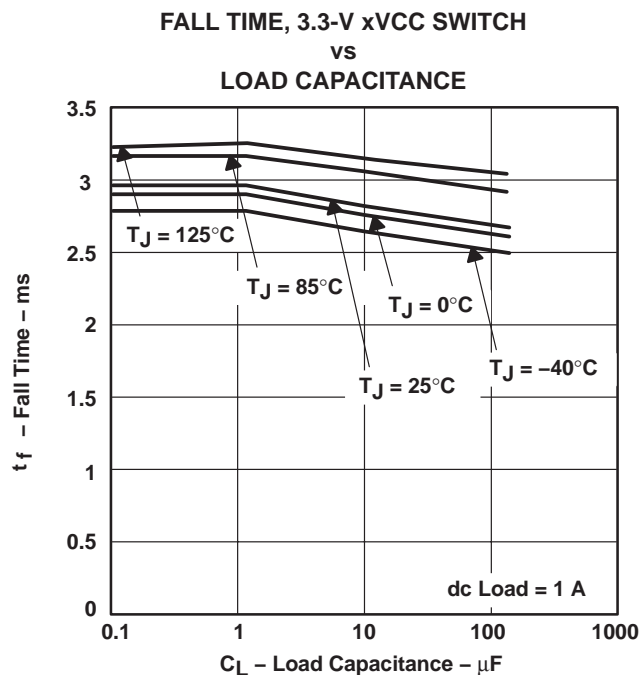
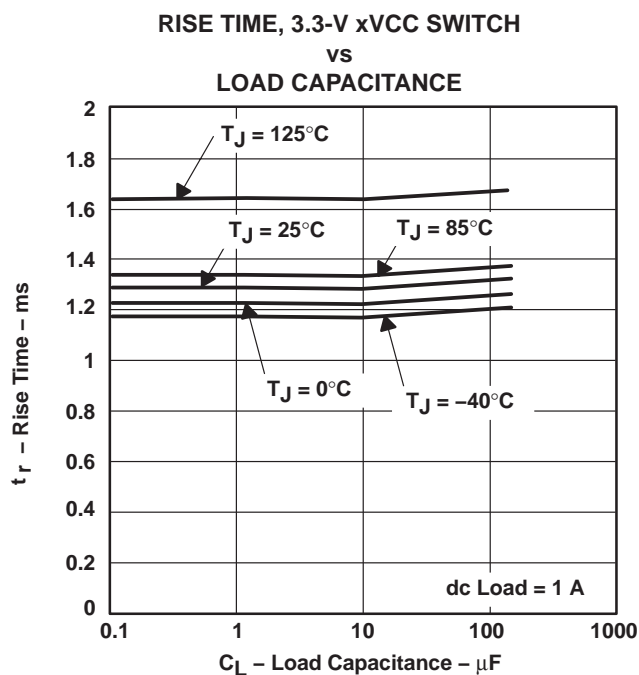
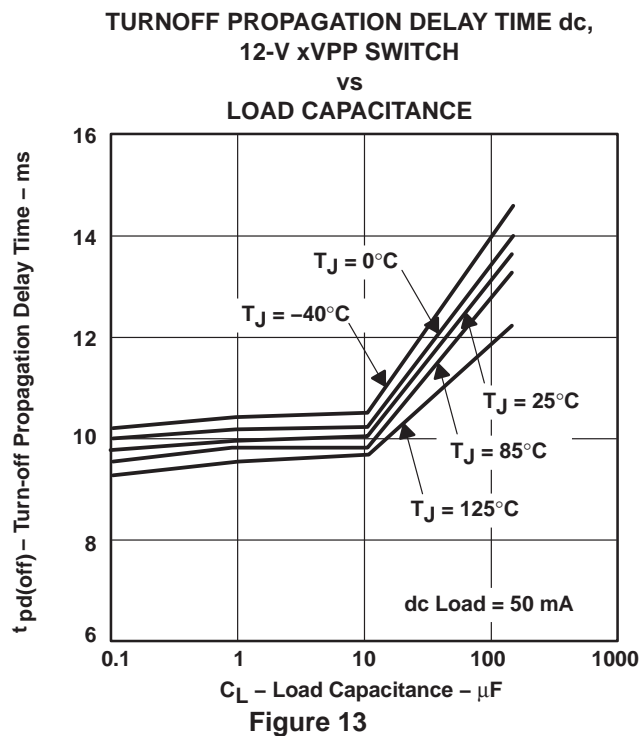
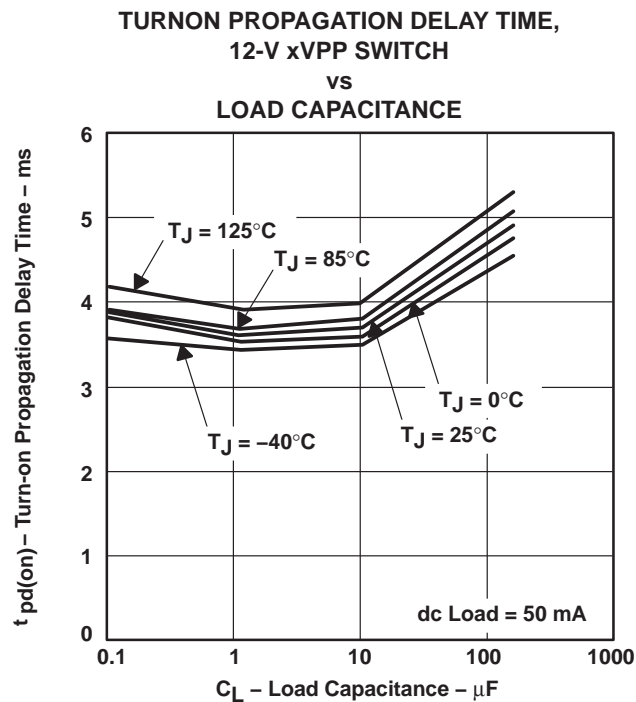


Figure 11



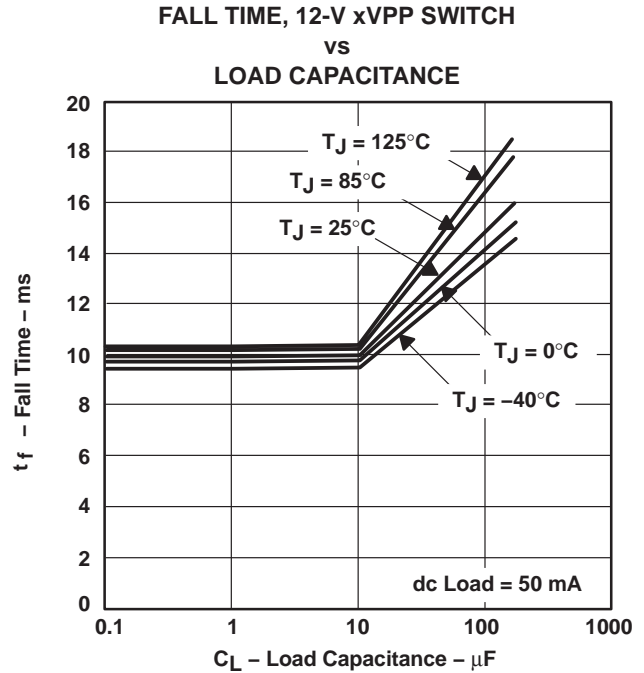
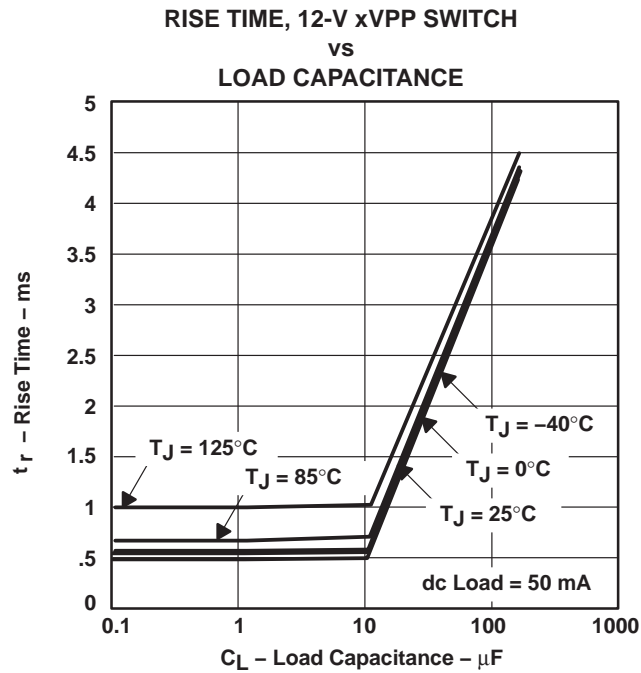
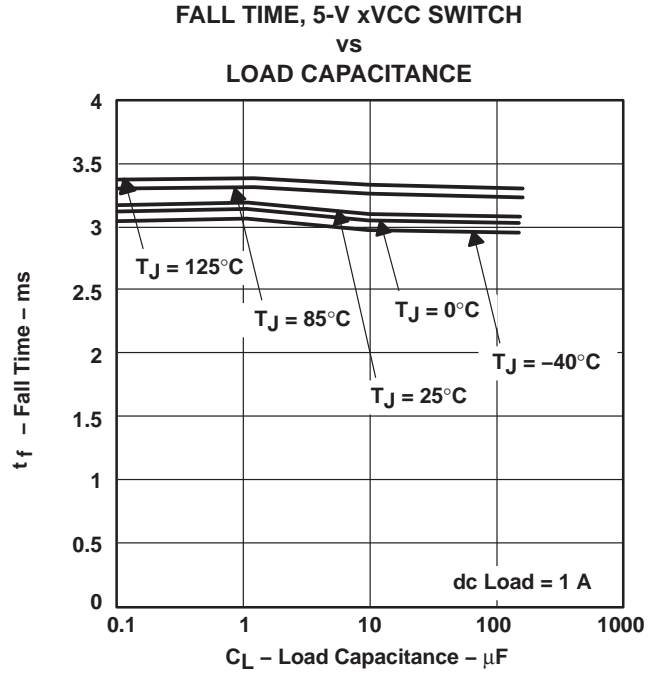
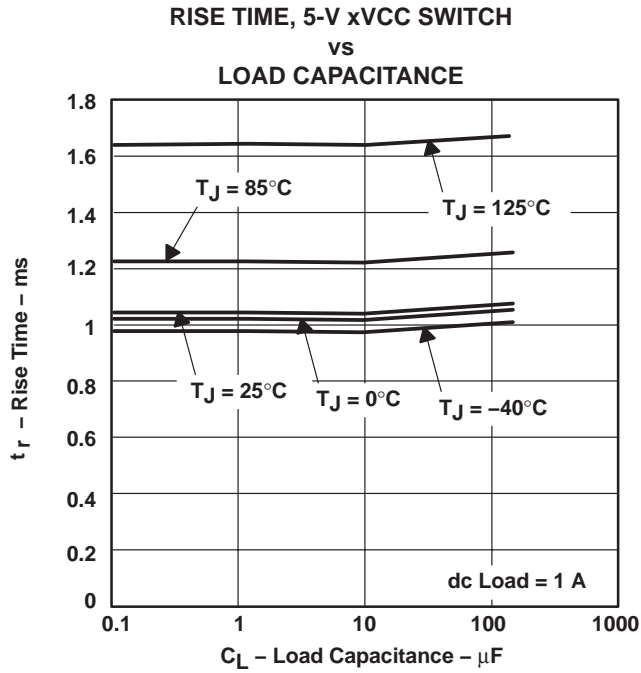
TYPICAL CHARACTERISTICS



TPS2216
DUAL-SLOT PC CARD POWER-INTERFACE SWITCH
FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

INPUT CURRENT AT $V_{I(xVCC)} = V_{I(xVPP)} = 3.3\text{ V}$
 VS

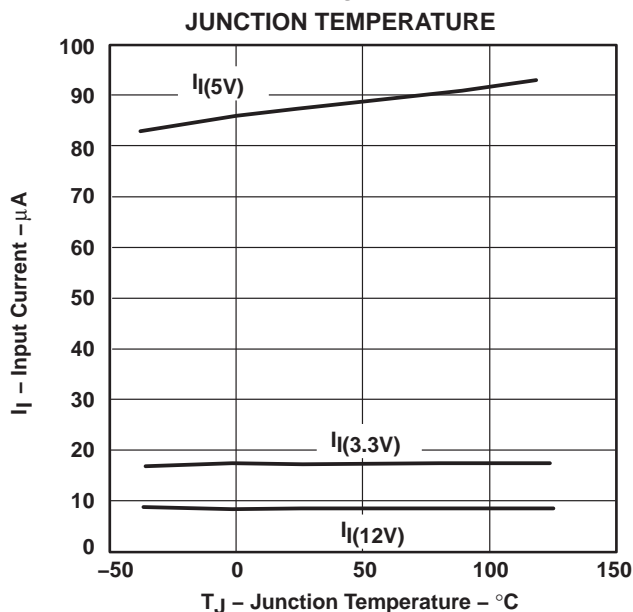


Figure 20

INPUT CURRENT AT $V_{I(xVCC)} = V_{I(xVPP)} = 5\text{ V}$
 VS

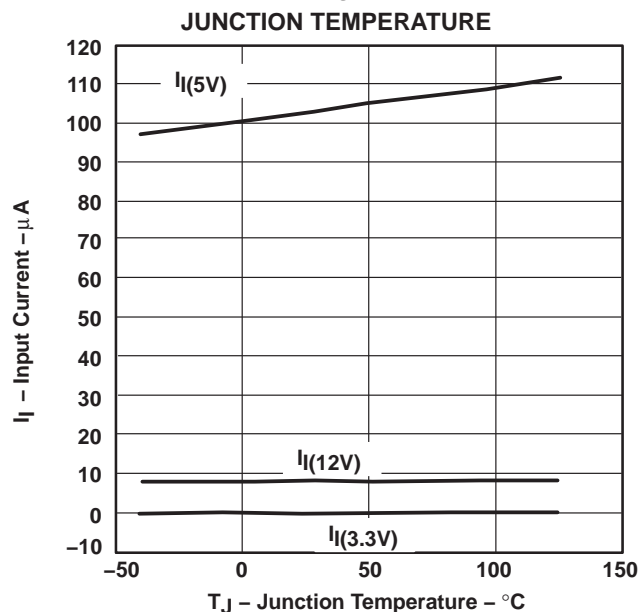


Figure 21

INPUT CURRENT AT $V_{I(xVCC)} = 5\text{ V}$, $V_{I(xVPP)} = 12\text{ V}$
 VS

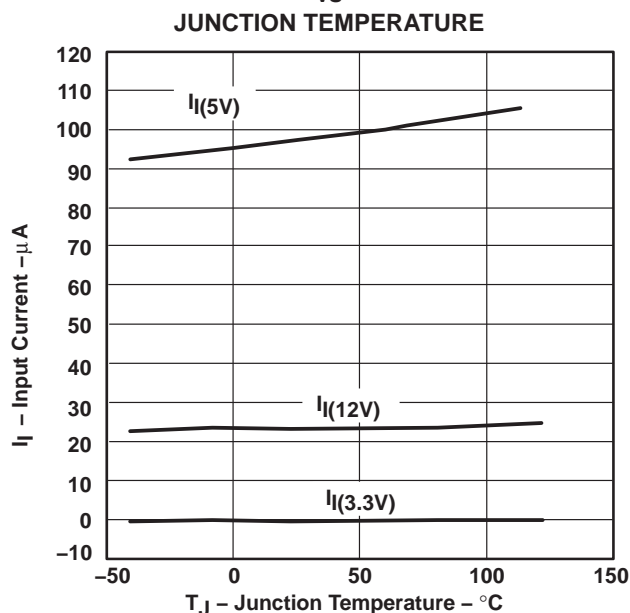


Figure 22

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
 3.3-V xVCC SWITCH

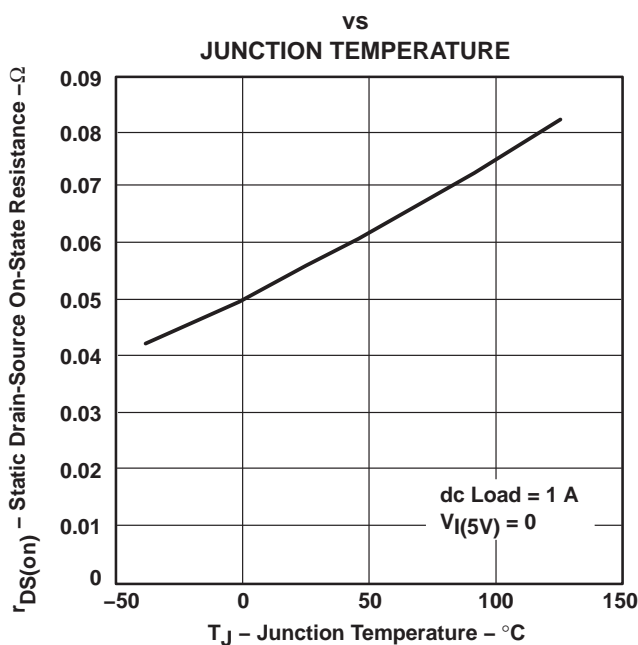


Figure 23

TPS2216
DUAL-SLOT PC CARD POWER-INTERFACE SWITCH
FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE, 3.3-V xVCC SWITCH
vs
JUNCTION TEMPERATURE

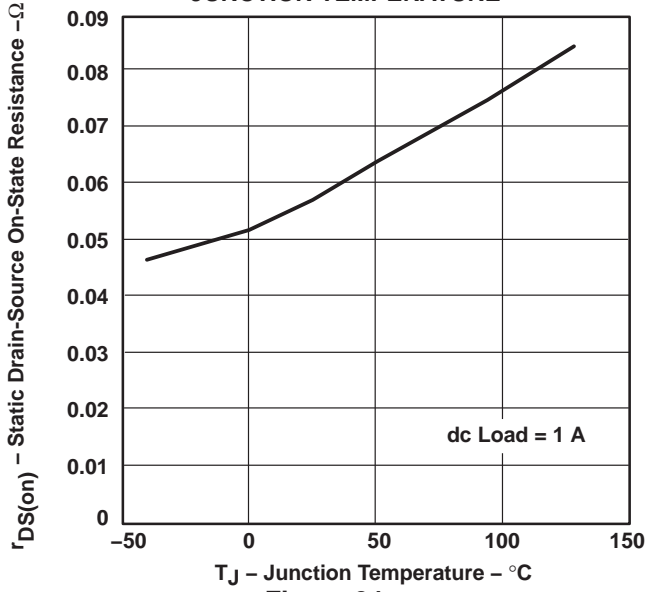


Figure 24

STATIC DRAIN-SOURCE ON-STATE RESISTANCE, 5-V xVCC SWITCH
vs
JUNCTION TEMPERATURE

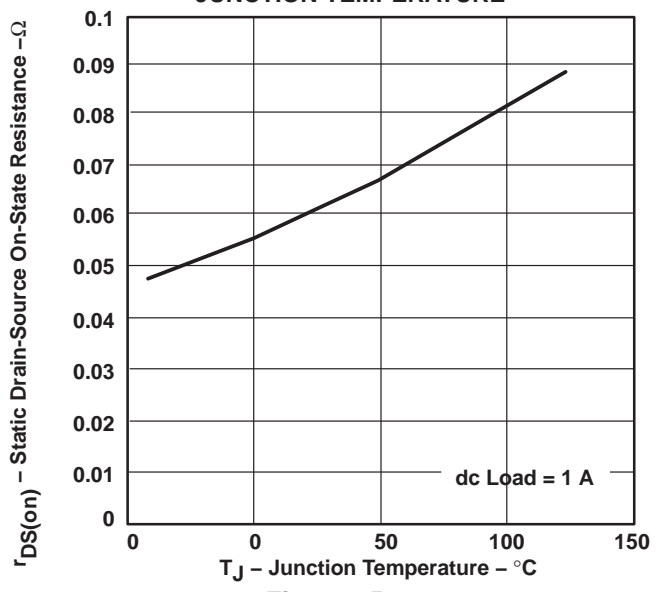


Figure 25

STATIC DRAIN-SOURCE ON-STATE RESISTANCE, 12-V xVPP SWITCH
vs
JUNCTION TEMPERATURE

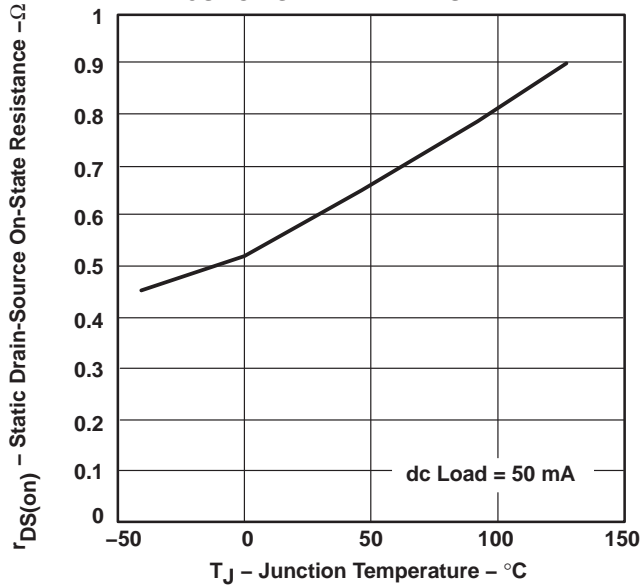


Figure 26

DC INPUT-TO-OUTPUT VOLTAGE (DROP), 3.3-V xVCC SWITCH
vs
LOAD CURRENT

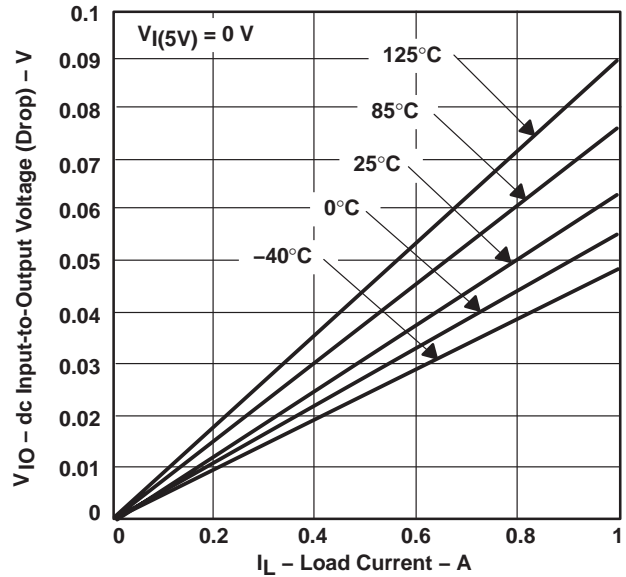


Figure 27



TPS2216 DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS

**DC INPUT-TO-OUTPUT VOLTAGE (DROP),
3.3-V xVCC SWITCH
vs
LOAD CURRENT**

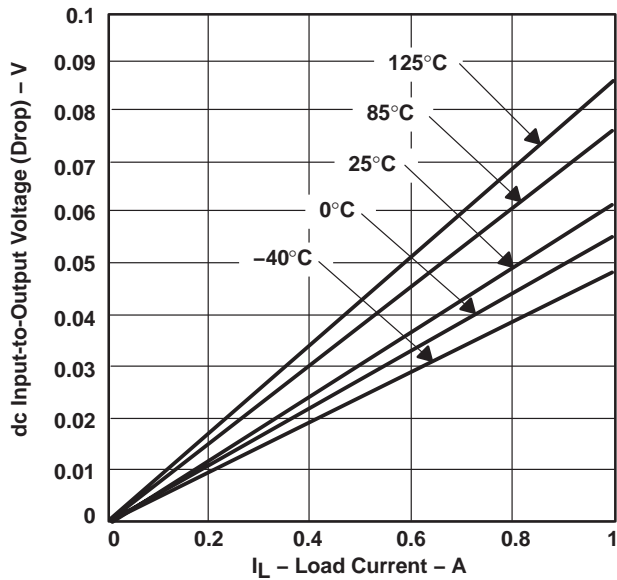


Figure 28

**DC INPUT-TO-OUTPUT VOLTAGE (DROP),
5-V xVCC SWITCH
vs
LOAD CURRENT**

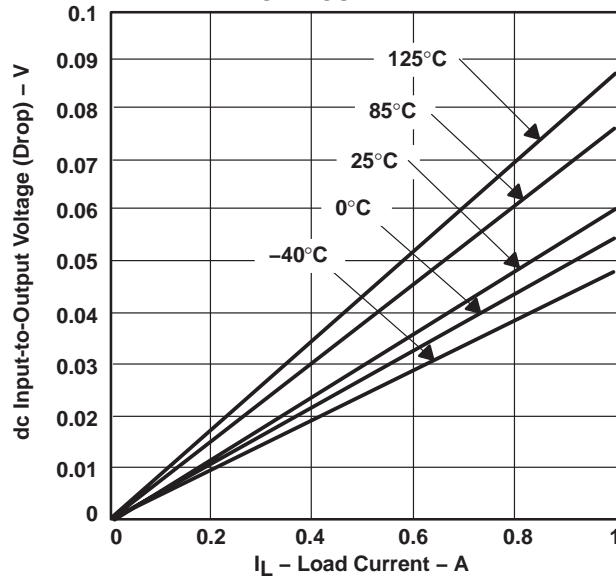


Figure 29

**DC INPUT-TO-OUTPUT VOLTAGE (DROP),
12-V xVPP SWITCH
vs
LOAD CURRENT**

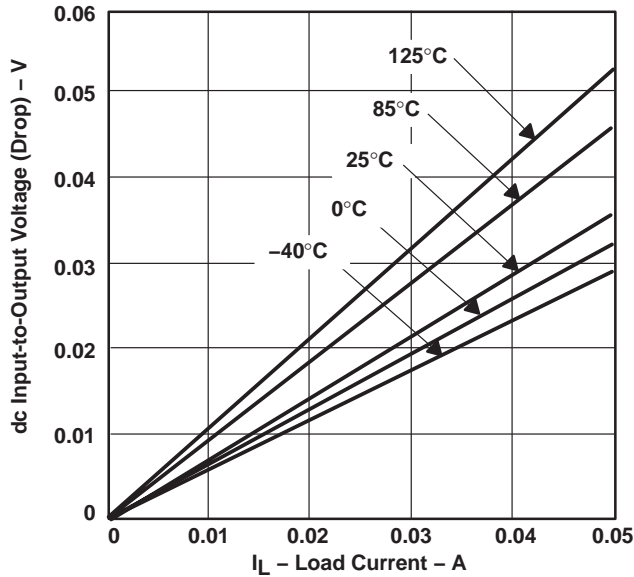


Figure 30

**SHORT-CIRCUIT CURRENT LIMIT,
3.3-V xVCC SWITCH
vs
JUNCTION TEMPERATURE**

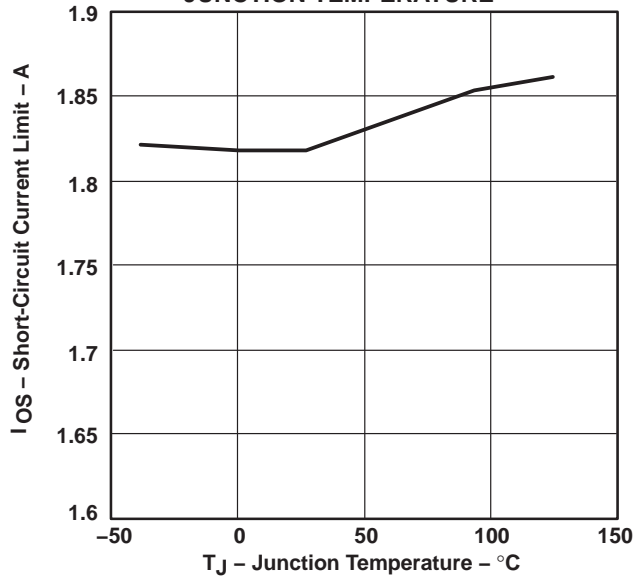


Figure 31

TPS2216 DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS

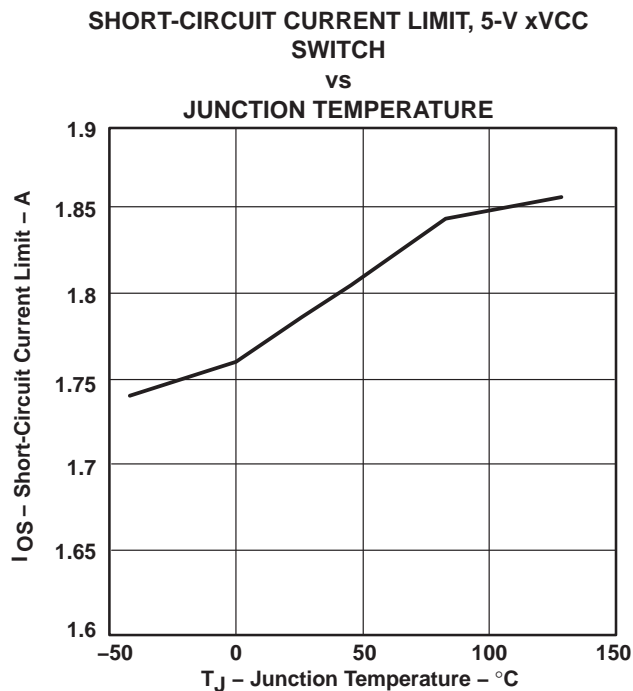


Figure 32

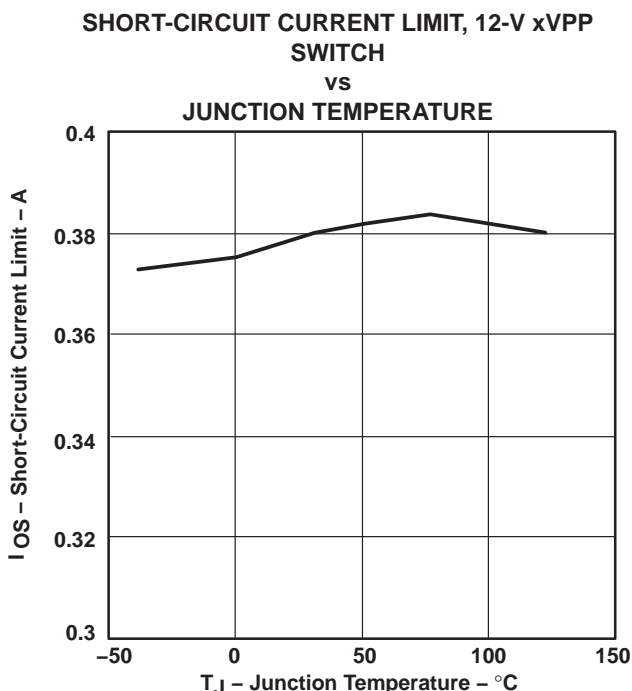


Figure 33

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited onboard memory. The idea of add-in cards quickly took hold; modems, wireless LANs, Global Positioning Satellite System (GPS), multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association), comprising members from leading computer, software, PC Card, and semiconductor manufacturers, was established. One key goal was to realize the plug-and-play concept. Cards and hosts from different vendors should be compatible or able to communicate with one another transparently.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connector. This power interface consists of two V_{CC} , two V_{pp} , and four ground terminals. Multiple V_{CC} and ground terminals minimize connector terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals, but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{pp} terminals.

APPLICATION INFORMATION

designing for voltage regulation

The current PCMCIA specification for output voltage regulation, $V_{O(\text{reg})}$, of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply has an output-voltage regulation, $V_{PS(\text{reg})}$, of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card will result from resistive losses, V_{PCB} , in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop, V_{DS} , for the TPS2216 would be the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(\text{reg})} - V_{PS(\text{reg})} - V_{PCB}$$

Typically, this would leave 100 mV for the allowable voltage drop across the 5-V switch. The specification for output voltage regulation of the 3.3-V output is 300 mV; so, using the same equation by deducting the voltage drop percentages (2%) for power-supply regulation and PCB resistive loss (1%), the allowable voltage drop for the 3.3-V switch is 200 mV. The voltage drop is the output current multiplied by the switch resistance of the TPS2216. Therefore, the maximum output current, $I_{O \text{ max}}$, that can be delivered to the PC Card in regulation is the allowable voltage drop across the IC, divided by the output-switch resistance.

$$I_{O \text{ max}} = \frac{V_{DS}}{r_{DS(\text{on})}}$$

The xVCC outputs can deliver 1 A continuously at 5 V and 3.3 V within regulation over the operating temperature range. The xVPP outputs of the IC can deliver 200 mA continuously.

overcurrent and overtemperature protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power-supply or PCB trace damage. Even systems robust enough to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. Most hosts include fuses for protection. However, the reliability of fused systems is poor, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The TPS2216 takes a two-pronged approach to overcurrent protection, which is designed to activate if an output is shorted or when an overcurrent condition is present when switches are powered up. First, instead of fuses, sense FETs monitor each of the xVCC and xVPP power outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. Excessive current generates an error signal that limits the output current of only the affected output, preventing damage to the host. Each xVCC output overcurrent limits from 1 A to 2.2 A, typically around 1.6 A; the xVPP outputs limit from 250 mA to 500 mA, typically around 375 mA.

Second, when an overcurrent condition is detected, the TPS2216 asserts an active low \overline{OC} signal that can be monitored by the microprocessor or controller to initiate diagnostics and/or send the user a warning message. In the event that an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates. This shuts down all power outputs until the device cools to within a safe operating region, which is ensured by a thermal shutdown hysteresis.

TPS2216

DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

APPLICATION INFORMATION

12-V supply not required

Many PC Card switches use the externally supplied 12 V to power gate drive and other chip functions; this requires that power be present at all times. The TPS2216 offers considerable power savings by using an internal charge pump to generate the required higher gate drive voltages from the 5-V or 3.3-V power supplies. Therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Additional power savings are realized by the IC during shutdown mode, in which quiescent current drops to a maximum of 1 μ A.

3.3-V low-voltage mode

The TPS2216 will operate in 3.3-V low-voltage mode when 3.3 V is the only available input voltage ($V_{I(5V)} = 0$, $V_{I(12V)} = 0$). This feature allows host and PC Cards to be operated in low-power 3.3-V-only modes such as sleep modes. Note that in this operation mode, the IC will derive its bias current from the 3.3-V input pin and can only provide 3.3 V to the outputs.

voltage transitioning requirement

PC Cards are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2216 meets all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This action ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. PC Card specification requires that V_{CC} be discharged within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. The TPS2216 includes discharge transistors on all xVCC and xVPP outputs to meet the specification requirement.

shutdown mode

In the shutdown mode, which can be controlled by bit D8 of the input serial DATA word, each of the xVCC and xVPP outputs is forced to a high-impedance state. In this mode, the chip quiescent current is limited to 1 μ A or less to conserve battery power.

standby mode

The TPS2216 can be put in standby mode by pulling \overline{STBY} low to conserve power during low-power operation. In this mode, all of the power outputs (xVCC and xVPP) will have a nominal current limit of 50 mA. \overline{STBY} has an internal 150-k Ω pullup resistor. The output-switch status of the device must be set, allowing the output capacitors to charge, prior to enabling the standby mode. Changing the setting of the output switches with the device in standby mode may cause an overcurrent response to be generated.

mode

The mode pin programs the switches in either TPS2216 or TPS2206 mode. An internal 150-k Ω pulldown resistor is connected to the pin. Floating or pulling the mode pin low sets the switches in TPS2206 mode; pulling the mode pin high sets the switches in TPS2216 mode. In TPS2206 mode, xVPP outputs are dependent on xVCC outputs. In TPS2216 mode, xVPP is programmed independent of xVCC. Refer to TPS2216 control-logic tables for more information.



APPLICATION INFORMATION

power supply considerations

The TPS2216 has multiple pins for each of its 3.3-V and 5-V power inputs and for the switched xVCC outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is higher than that specified, resulting in increased voltage drops and less power. It is recommended that all input and output power pins be paralleled for optimum operation. Because the two 12-V pins are not internally connected, they must be tied together externally.

To increase the noise immunity of the TPS2216, the power-supply inputs should be bypassed with a 1- μ F electrolytic or tantalum capacitor paralleled by a 0.047- μ F to 0.1- μ F ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1- μ F (or larger) ceramic capacitor; doing so improves the immunity of the IC to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the IC and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken, or allowed to fall, below -0.3 V.

RESET and $\overline{\text{RESET}}$ inputs

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying low impedance paths from xVCC and xVPP terminals to ground. A low-impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The active-high RESET or active low $\overline{\text{RESET}}$ input will close internal switches S1, S4, S7, and S11 with all other switches left open. The TPS2216 remains in the low-impedance output state until the signal is deasserted and further data is clocked in and latched. The input serial data can not be latched during reset mode. RESET and $\overline{\text{RESET}}$ are provided for direct compatibility with systems that use either an active-low or active-high reset voltage supervisor. The RESET pin has an internal 150-k Ω pulldown resistor and the $\overline{\text{RESET}}$ pin has an internal 150-k Ω pullup resistor. The device will be reset automatically when powered up.

calculating junction temperature

The switch resistance, $r_{\text{DS(on)}}$, is dependent on the junction temperature, T_J , of the die. The junction temperature is dependent on both $r_{\text{DS(on)}}$ and the current through the switch. To calculate T_J , first find $r_{\text{DS(on)}}$ from Figures 23 through 26, using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{\text{DS(on)}} \times I^2$$

Next, sum the power dissipation of all switches and calculate the junction temperature:

$$T_J = \left(\sum P_D \times R_{\theta\text{JA}} \right) + T_A$$

Where:

$R_{\theta\text{JA}}$ is the inverse of the derating factor given in the dissipation rating table.

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

logic inputs and outputs

The serial interface consists of DATA, CLOCK, and LATCH leads. The data is clocked in on the positive edge of the clock (see Figures 2 and 3). The 11-bit (D0–D10) serial data word is loaded during the positive edge of the latch signal. The positive edge of the latch signal should occur before the next positive edge of the clock occurs.

TPS2216 DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

APPLICATION INFORMATION

logic inputs and outputs (continued)

The TPS2216 serial interfaces are compatible with serial-interface PCMCIA controllers and current PCMCIA and Japan Electronic Industry Development Association (JEIDA) standards.

An overcurrent output (\overline{OC}) is provided to indicate an overcurrent or overtemperature condition in any of the xVCC and xVPP outputs as previously discussed.

TPS2216 control logic

TPS2216 mode (MODE pulled high)

xVPP

| D8 (\overline{SHDN}) | AVPP CONTROL SIGNALS | | | OUTPUT V_AVPP | BVPP CONTROL SIGNALS | | | | OUTPUT V_BVPP |
|--------------------------|----------------------|----|----|------------------|--------------------------|----|----|-----|------------------|
| | D0 | D1 | D9 | | D8 (\overline{SHDN}) | D4 | D5 | D10 | |
| 1 | 0 | 0 | X | 0 V | 1 | 0 | 0 | X | 0 V |
| 1 | 0 | 1 | 0 | 3.3 V | 1 | 0 | 1 | 0 | 3.3 V |
| 1 | 0 | 1 | 1 | 5 V | 1 | 0 | 1 | 1 | 5 V |
| 1 | 1 | 0 | X | 12 V | 1 | 1 | 0 | X | 12 V |
| 1 | 1 | 1 | X | Hi-Z | 1 | 1 | 1 | X | Hi-Z |
| 0 | X | X | X | Hi-Z | 0 | X | X | X | Hi-Z |

xVCC

| D8 (\overline{SHDN}) | AVCC CONTROL SIGNALS | | OUTPUT V_AVCC | BVCC CONTROL SIGNALS | | | OUTPUT V_BVCC |
|--------------------------|----------------------|----|------------------|--------------------------|----|----|------------------|
| | D3 | D2 | | D8 (\overline{SHDN}) | D6 | D7 | |
| 1 | 0 | 0 | 0 V | 1 | 0 | 0 | 0 V |
| 1 | 0 | 1 | 3.3 V | 1 | 0 | 1 | 3.3 V |
| 1 | 1 | 0 | 5 V | 1 | 1 | 0 | 5 V |
| 1 | 1 | 1 | 0 V | 1 | 1 | 1 | 0 V |
| 0 | X | X | Hi-Z | 0 | X | X | Hi-Z |

TPS2206 mode (MODE floating or pulled low)

xVPP

| D8 (\overline{SHDN}) | AVPP CONTROL SIGNALS | | OUTPUT V_AVPP | BVPP CONTROL SIGNALS | | | OUTPUT V_BVPP |
|--------------------------|----------------------|----|------------------|--------------------------|----|----|------------------|
| | D0 | D1 | | D8 (\overline{SHDN}) | D4 | D5 | |
| 1 | 0 | 0 | 0 V | 1 | 0 | 0 | 0 V |
| 1 | 0 | 1 | V_AVCC | 1 | 0 | 1 | V_BVCC |
| 1 | 1 | 0 | 12 V | 1 | 1 | 0 | 12 V |
| 1 | 1 | 1 | Hi-Z | 1 | 1 | 1 | Hi-Z |
| 0 | X | X | Hi-Z | 0 | X | X | Hi-Z |

xVCC

| D8 (\overline{SHDN}) | AVCC CONTROL SIGNALS | | OUTPUT V_AVCC | BVCC CONTROL SIGNALS | | | OUTPUT V_BVCC |
|--------------------------|----------------------|----|------------------|--------------------------|----|----|------------------|
| | D3 | D2 | | D8 (\overline{SHDN}) | D6 | D7 | |
| 1 | 0 | 0 | 0 V | 1 | 0 | 0 | 0 V |
| 1 | 0 | 1 | 3.3 V | 1 | 0 | 1 | 3.3 V |
| 1 | 1 | 0 | 5 V | 1 | 1 | 0 | 5 V |
| 1 | 1 | 1 | 0 V | 1 | 1 | 1 | 0 V |
| 0 | X | X | Hi-Z | 0 | X | X | Hi-Z |



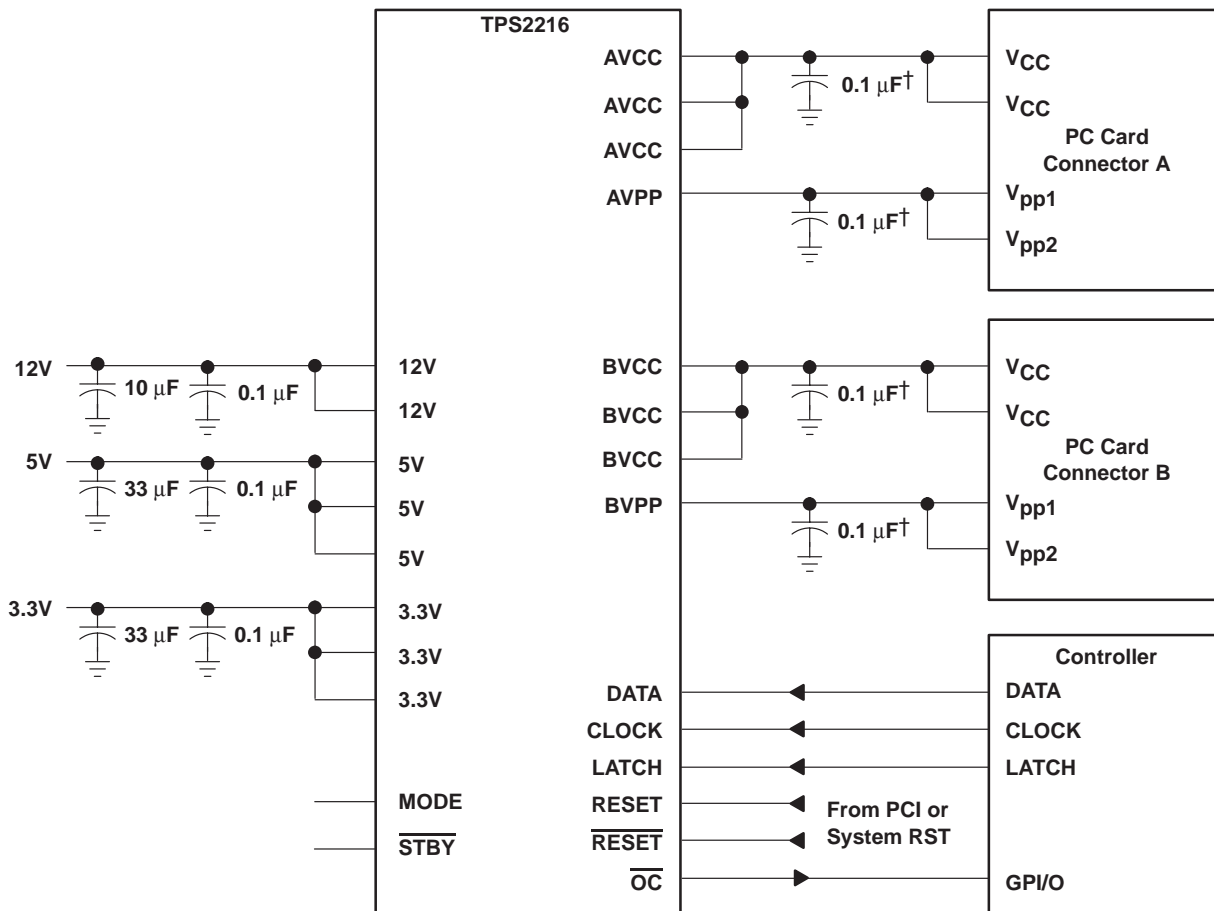
TPS2216 DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

SLVS179D – MARCH 1999 – REVISED JUNE 2000

APPLICATION INFORMATION

ESD protections (see Figure 34)

All TPS2216 inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The xVCC and xVPP outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1- μF capacitors protects the devices from discharges up to 10 kV.



† Maximum recommended output capacitance for xVCC is 220 μF and for xVPP is 10 μF without $\overline{\text{OC}}$ glitch when switches are powered on.

Figure 34. Detailed Interconnections and Capacitor Recommendations

TPS2216 DUAL-SLOT PC CARD POWER-INTERFACE SWITCH FOR SERIAL PCMCIA CONTROLLERS

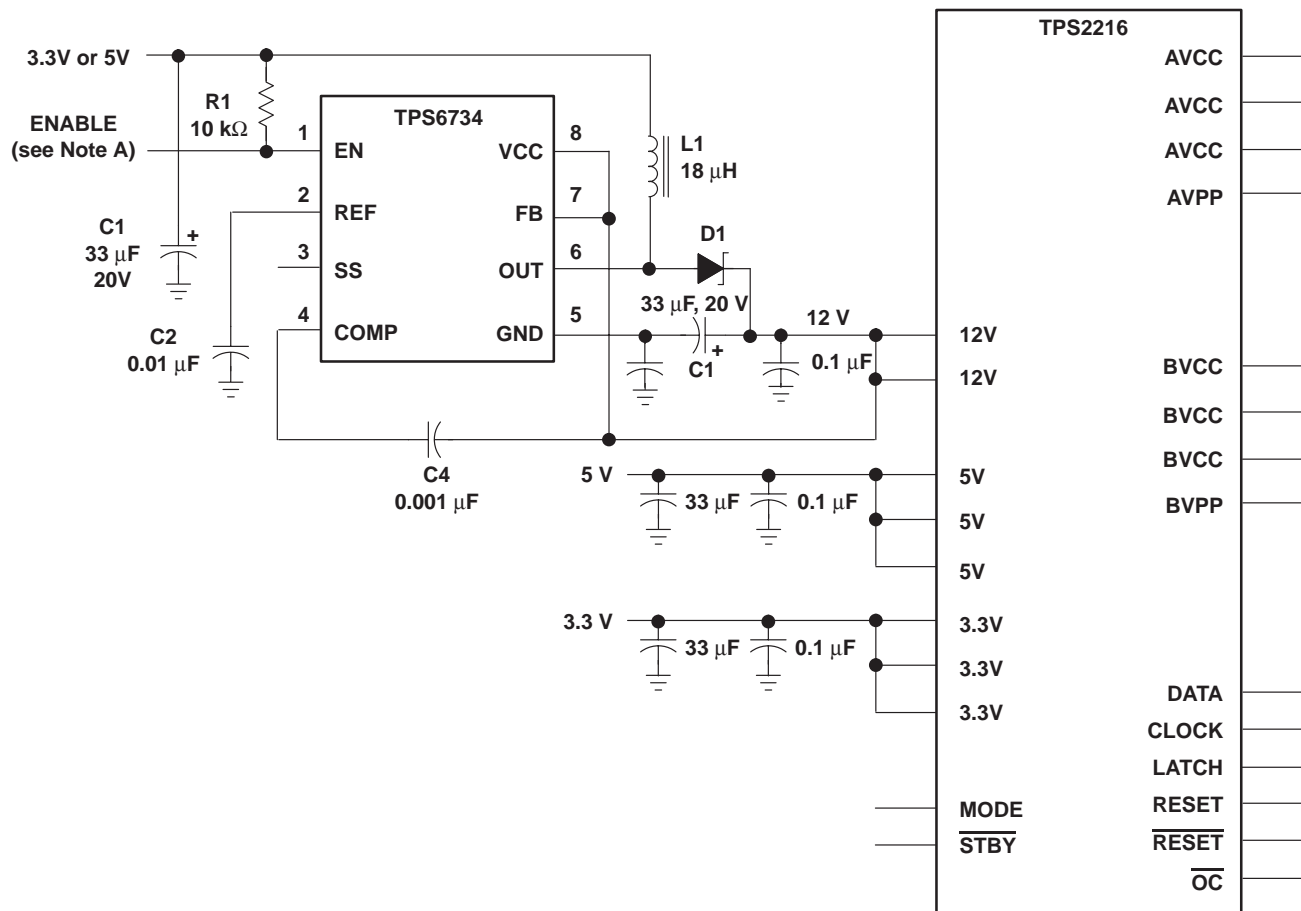
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APPLICATION INFORMATION

12-V flash memory supply

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 35, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in² of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 μ A when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7- Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).



NOTE A: The enable terminal can be tied to a general-purpose I/O terminal on the PCMCIA controller or tied high.

Figure 35. TPS2216 with TPS6734 12-V, 120-mA Supply

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS2216DAP | ACTIVE | HTSSOP | DAP | 32 | 46 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | TPS2216 | Samples |
| TPS2216DB | ACTIVE | SSOP | DB | 30 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | TPS2216 | Samples |
| TPS2216DBG4 | ACTIVE | SSOP | DB | 30 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | TPS2216 | Samples |
| TPS2216DBR | ACTIVE | SSOP | DB | 30 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | TPS2216 | Samples |
| TPS2216DBRG4 | ACTIVE | SSOP | DB | 30 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | TPS2216 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS2216DBR | SSOP | DB | 30 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

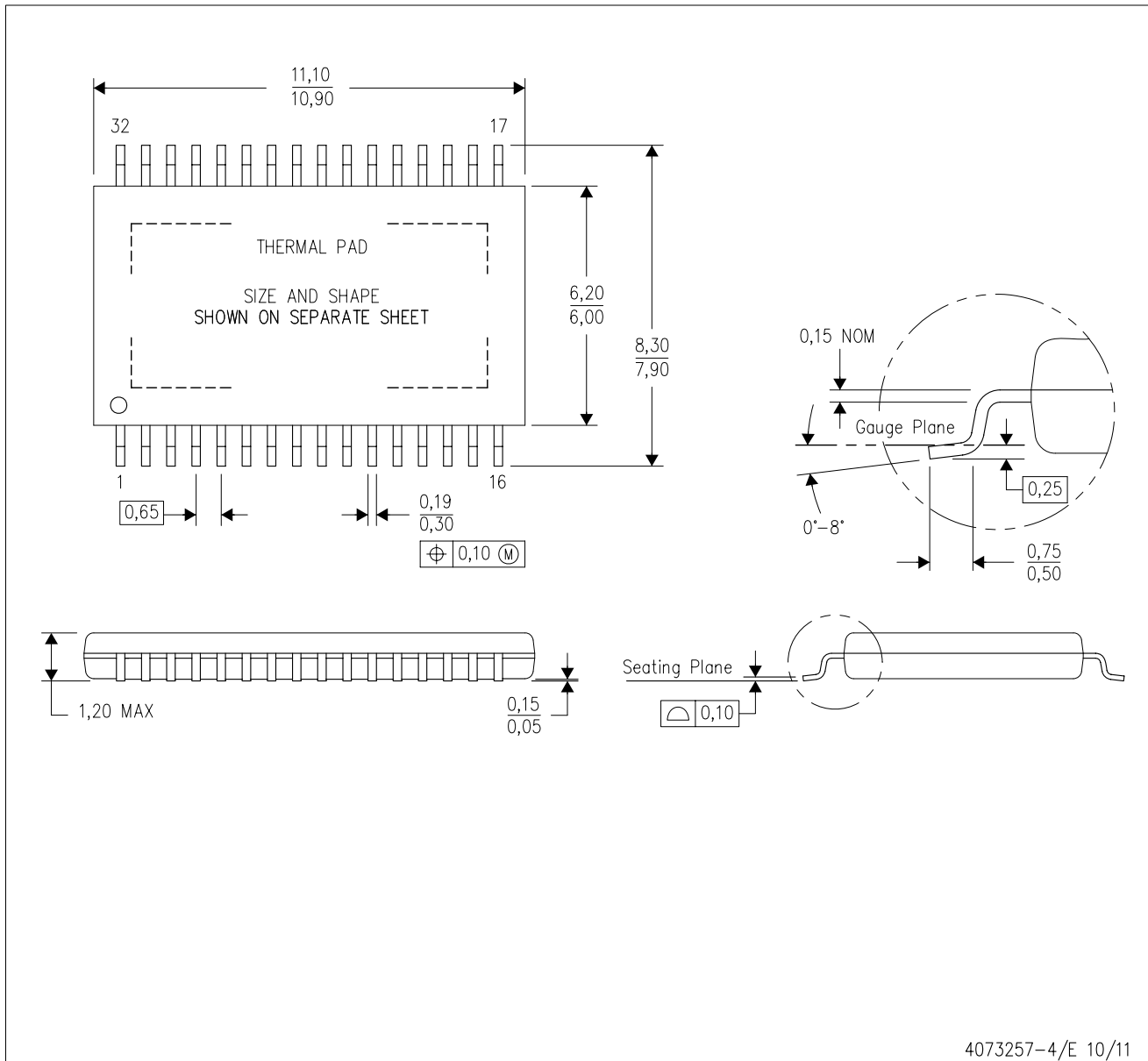


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS2216DBR | SSOP | DB | 30 | 2000 | 367.0 | 367.0 | 38.0 |

MECHANICAL DATA

DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
- \triangle Falls within JEDEC MO-153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

DAP (R-PDSO-G32)

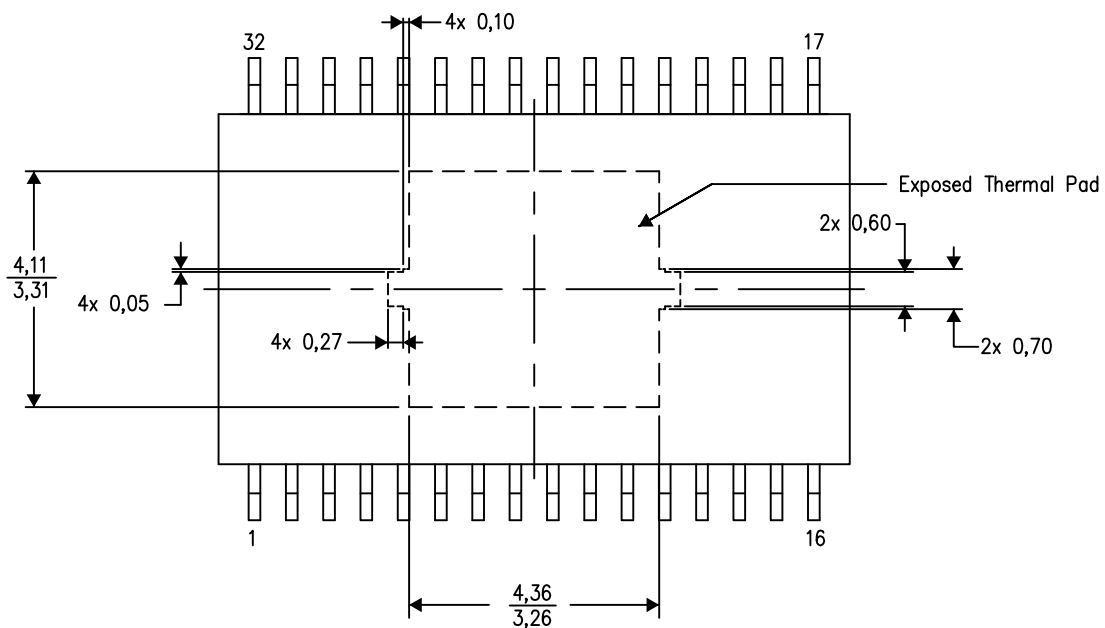
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View
Exposed Thermal Pad Dimensions

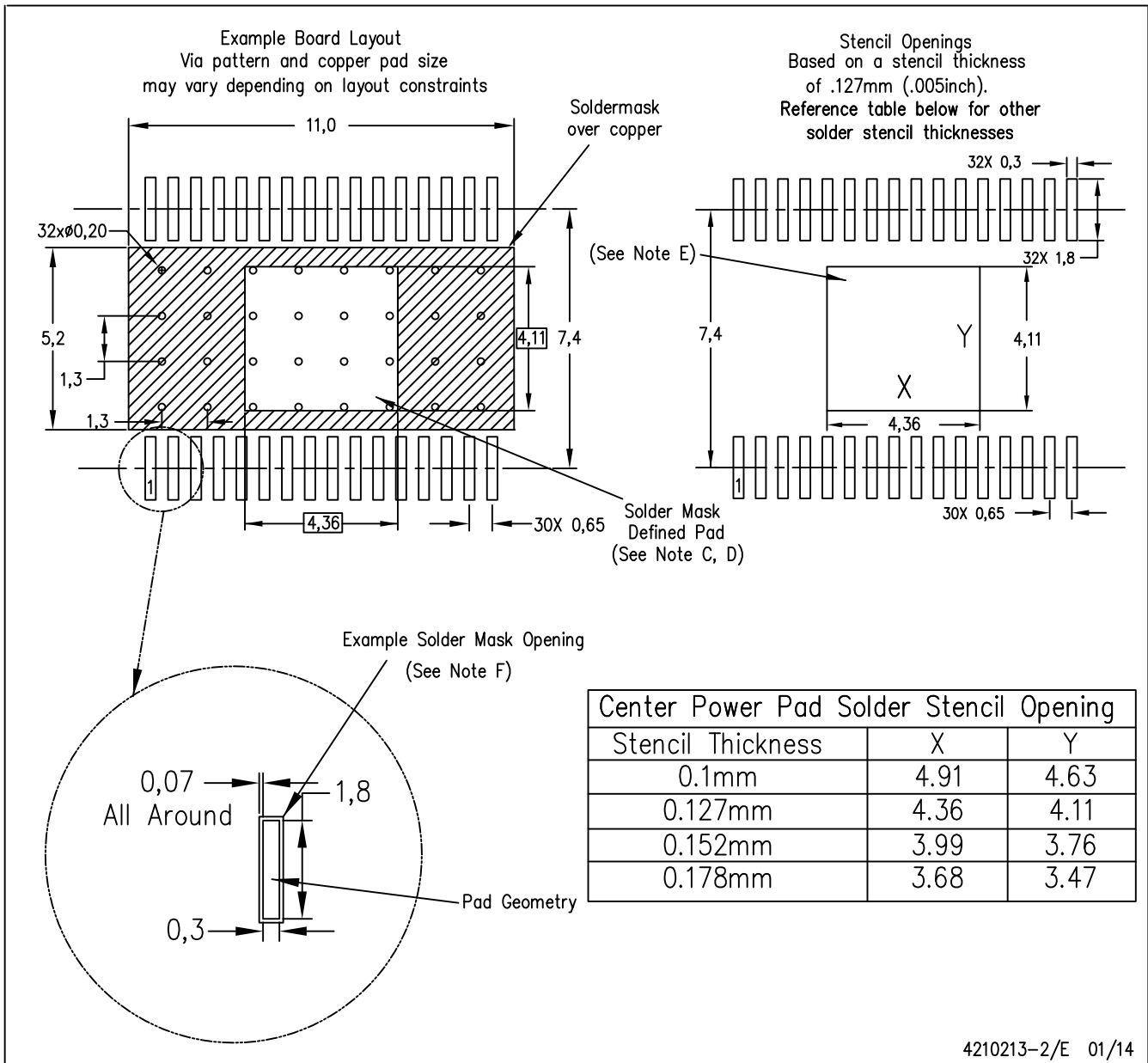
4206319-3/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

LAND PATTERN DATA

DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Contact the board fabrication site for recommended soldermask tolerances.

PowerPAD is a trademark of Texas Instruments

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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