12-Channel, 1:2 MUX/DEMUX Switch for DDR3 Applications

Check for Samples: TS3DDR3812

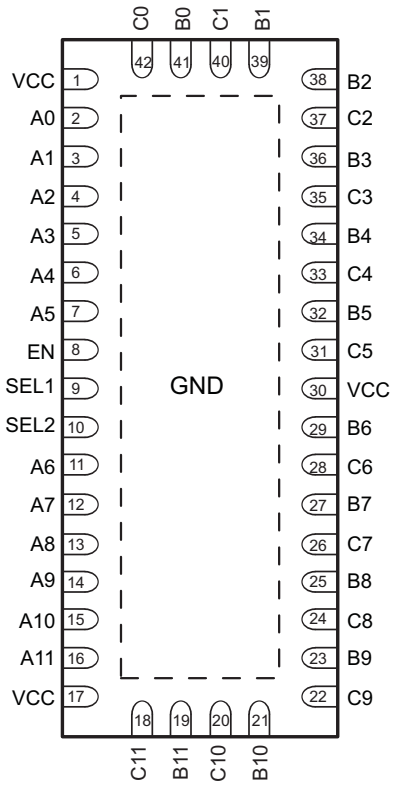
FEATURES

- **Compatible with DDR3 SDRAM Standard (JESD79-3D)**
- **Wide Bandwidth of 1.675 GHz**
- **Low Propagation Delay (t_{pd} = 40 ps Typ)**
- **Low Bit-to-Bit Skew ($t_{sk(o)}$ = 6 ps Typ)**
- **Low and Flat ON-State Resistance (r_{ON} = 8 Ω Typ)**
- **Low Input/Output Capacitance (C_{ON} = 5.6 pF Typ)**
- **Low Crosstalk (X_{TALK} = –43 dB, Typ at 250 MHz)**
- **V_{CC} Operating Range from 3 V to 3.6 V**
- **Rail-to-Rail Switching on Data I/O Ports (0 to V_{CC})**
- **Separate Switch Control Logic for Upper and Lower 6-Channels**
- **Dedicated Enable Logic Supports Hi-Z Mode**
- **I_{OFF} Protection Prevents Current Leakage in Powered Down State (V_{CC} = 0 V)**
- **ESD Performance Tested Per JESD22**
  - **2000 V Human Body Model (A114B, Class II)**
  - **1000 V Charged Device Model (C101)**
- **42-pin RUA Package (9 × 3.5 mm, 0.5 mm Pitch)**

APPLICATIONS

- **DDR3 Signal Switching**
- **DIMM Modules**
- **Notebook/Desktop PCs**
- **Servers**

Figure 1. RUA PACKAGE (TOP VIEW)



DESCRIPTION

The TS3DDR3812 is a 12-channel, 1:2 multiplexer/demultiplexer switch designed for DDR3 applications. It operates from a 3 to 3.6 V supply and offers low and flat ON-state resistance as well as low I/O capacitance which allow it to achieve a typical bandwidth of 1.675 GHz.

Channels A_0 through A_{11} are divided into two banks of six bits and are independently controlled via two digital inputs called SEL1 and SEL2. These select inputs control the switch position of each 6-bit DDR3 source and allow them to be routed to one of two end-points. Alternatively, the switch can be used to connect a single endpoint to one of two 6-bit DDR3 sources. For switching 12-bit DDR3 sources, simply connect SEL1 and SEL2 together externally and control all 12 channels with a single GPIO input. An EN input allows the entire chip to be placed into a high-impedance (Hi-Z) state while not in use.

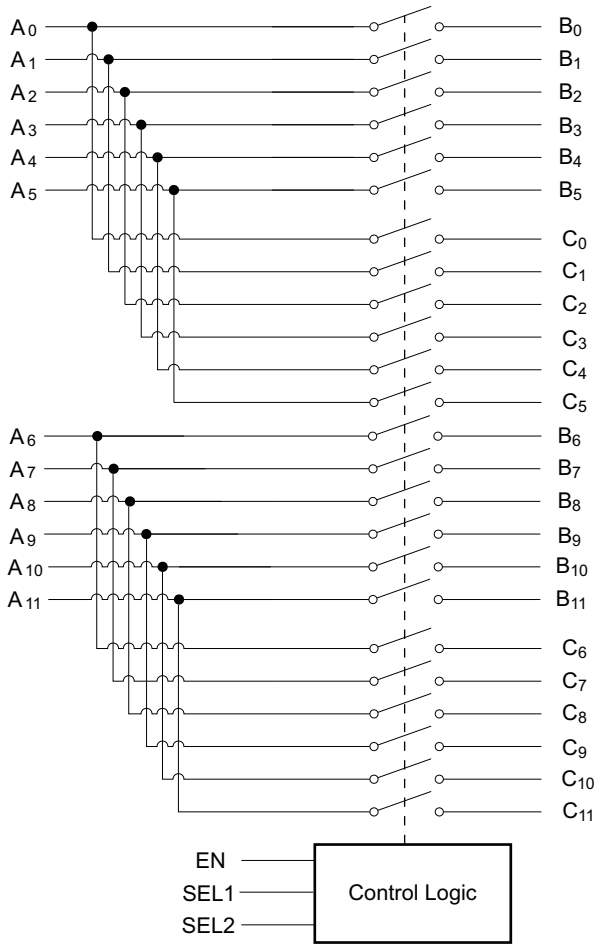
These characteristics make the TS3DDR3812 an excellent choice for use in memory, analog/digital video, LAN, and other high-speed signal switching applications.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

Figure 2. LOGIC DIAGRAM



FUNCTION TABLE

EN	SEL1	SEL2	FUNCTION
L	X	X	A_0 to A_{11}, B_0 to B_{11}, and C_0 to C_{11} are Hi-Z
H	L	L	A_0 to A_5 = B_0 to B_5 and A_6 to A_{11} = B_6 to B_{11}
H	L	H	A_0 to A_5 = B_0 to B_5 and A_6 to A_{11} = C_6 to C_{11}
H	H	L	A_0 to A_5 = C_0 to C_5 and A_6 to A_{11} = B_6 to B_{11}
H	H	H	A_0 to A_5 = C_0 to C_5 and A_6 to A_{11} = C_6 to C_{11}

TERMINAL FUNCTIONS

PIN		DESCRIPTION
NAME	NUMBER	
V_{CC}	1,17, 30	Supply Voltage
GND	ThermalPad	Ground

TERMINAL FUNCTIONS (continued)

PIN		DESCRIPTION
NAME	NUMBER	
EN	8	Enable Input
SEL1	9	Select Input
SEL2	10	Select Input
A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, A_8, A_9, A_{10}, A_{11}	2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16	Data I/Os
B_0, B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8, B_9, B_{10}, B_{11}	41, 39, 38, 36, 34, 32, 29, 27, 25, 23, 21, 19	Data I/Os
C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}	42, 40, 37, 35, 33, 31, 28, 26, 24, 22, 20, 18	Data I/Os

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
$V_{I/O}$	Analog voltage range(2)(3)(4)	A, B, C	–0.5	7	V
V_{IN}	Digital input voltage range(2)(3)	SEL1, SEL2	–0.5	7	V
$I_{I/OK}$	Analog port diode current	$V_{I/O}$ < 0		–50	mA
I_{IK}	Digital input clamp current	V_{IN} < 0		–50	mA
$I_{I/O}$	On-state switch current(5)	A, B, C	–128	128	mA
I_{DD}, I_{GND}	Continuous current through V_{DD} or GND		–100	100	mA
θ_{JA}	Package thermal impedance(6)	RUA package		31.8	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level control input voltage	SEL1, SEL2	2	5.5	V
V_{IL}	Low-level control input voltage	SEL1, SEL2	0	0.8	V
V_{IN}	Input voltage	SEL1, SEL2	0	5.5	V
$V_{I/O}$	Input/Output voltage		0	V_{CC}	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{IK}	Digital input clamp voltage	SEL1, SEL2	V_{CC} = 3.6 V, I_{IN} = –18 mA	–1.2	–0.8		V
R_{ON}	ON-state resistance	A, B, C	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -40 mA		8	12	Ω
$R_{ON(flat)}$(3)	ON-state resistance flatness	A, B, C	V_{CC} = 3 V, $V_{I/O}$ = 1.5 V and V_{CC}, $I_{I/O}$ = –40 mA		1.5		Ω
ΔR_{ON}(4)	On-state resistance match between channels	A, B, C	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = –40 mA		0.4	1	Ω
I_{IH}	Digital input high leakage current	SEL1, SEL2	V_{CC} = 3.6 V , V_{IN} = V_{DD}			±1	µA
I_{IL}	Digital input low leakage current	SEL1, SEL2	V_{CC} = 3.6 V, V_{IN} = GND			±1	µA
I_{OFF}	Leakage under power off conditions	All outputs	V_{CC} = 0 V, $V_{I/O}$ = 0 to 3.6 V, V_{IN} = 0 to 5.5 V			±1	µA
C_{IN}	Digital input capacitance	SEL1, SEL2	f = 1 MHz, V_{IN} = 0 V		2.6	3.2	pF
C_{OFF}	Switch OFF capacitance	A, B, C	f = 1 MHz, $V_{I/O}$ = 0 V, Output is open, Switch is OFF		2		pF
C_{ON}	Switch ON capacitance	A, B, C	f = 1 MHz, $V_{I/O}$ = 0 V, Output is open, Switch is ON		5.6		pF
I_{CC}	V_{CC} supply current		V_{CC} = 3.6 V, $I_{I/O}$ = 0, V_{IN} = V_{DD} or GND		300	400	µA

(1) V_I, V_O, I_I, and I_O refer to I/O pins, V_{IN} refers to the control inputs
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C
(3) $R_{ON(FLAT)}$ is the difference of R_{ON} in a given channel at specified voltages.
(4) ΔR_{ON} is the difference of R_{ON} from center port (A_5, A_6) to any other ports.

SWITCHING CHARACTERISTICS

Over recommended operation free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 4 pF (unless otherwise noted) (see Figure 7 and Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd}(2)	A or B,C	B,C or A		40		ps
t_{PZH}, t_{PZL}	SEL1	A_{0-5} or B_{0-5}, C_{0-5}	2		7	ns
	SEL2	A_{6-11} or B_{6-11}, C_{6-11}	2		7	ns
t_{PHZ}, t_{PLZ}	SEL1	A_{0-5} or B_{0-5}, C_{0-5}	2		5	ns
	SEL2	A_{6-11} or B_{6-11}, C_{6-11}	2		5	ns
$t_{sk(o)}$(3)	A or B,C	B, C or A		6	30	ps
$t_{sk(p)}$(4)	A or B, C	B, C or A		6	30	ps

(1) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port (A_5, A_6) and any other channel.
(4) Skew between opposite transitions of the same output $|t_{PHL} - t_{PLH}|$

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP(1)	UNIT
X_{TALK}	R_L = 50 Ω, f = 250 MHz (see Figure 11)	–43	dB
O_{IRR}	R_L = 50 Ω, f = 250 MHz (see Figure 12)	–42	dB
BW	R_L = 50 Ω, Switch ON (see Figure 10)	1.675	GHz

(1) All Typical Values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

OPERATING CHARACTERISTICS

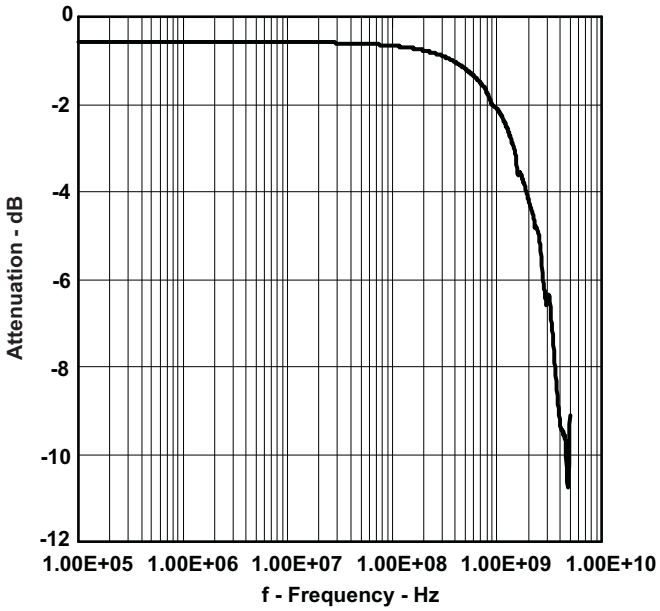


Figure 3. Gain vs Frequency

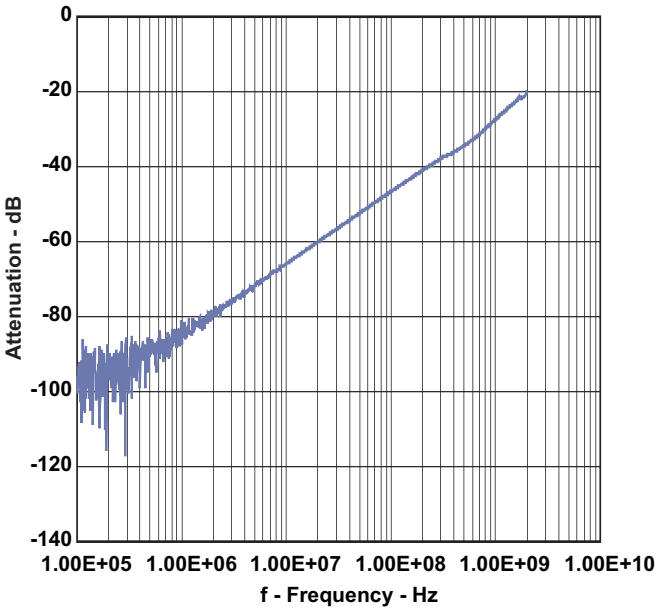


Figure 4. Off Isolation vs Frequency

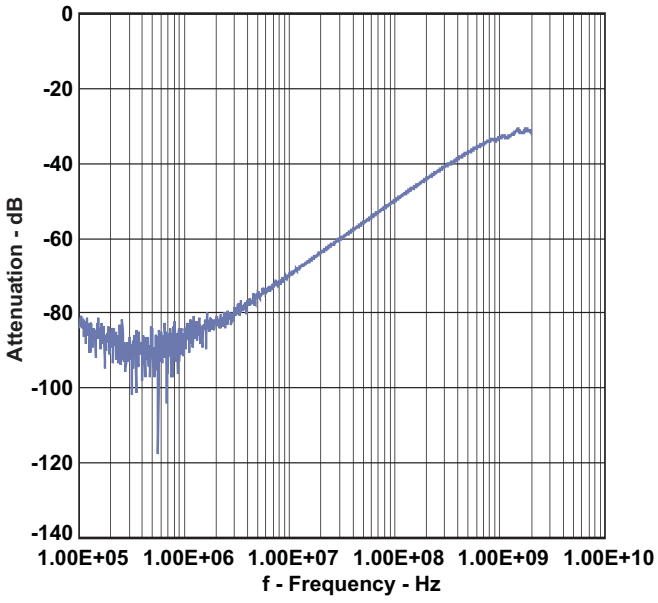


Figure 5. Crosstalk vs Frequency

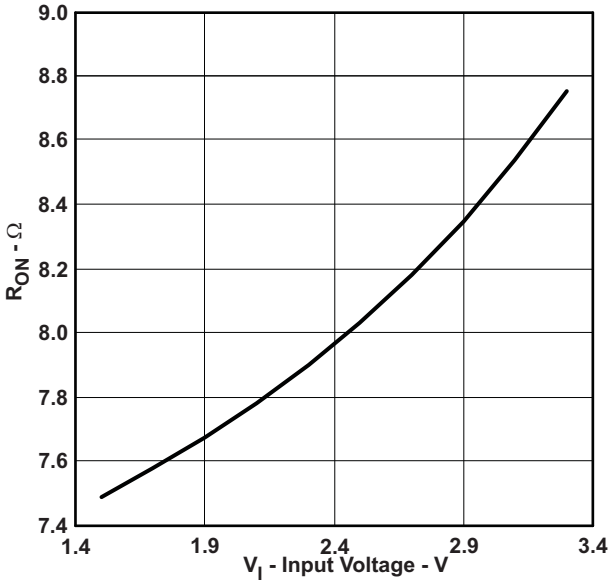
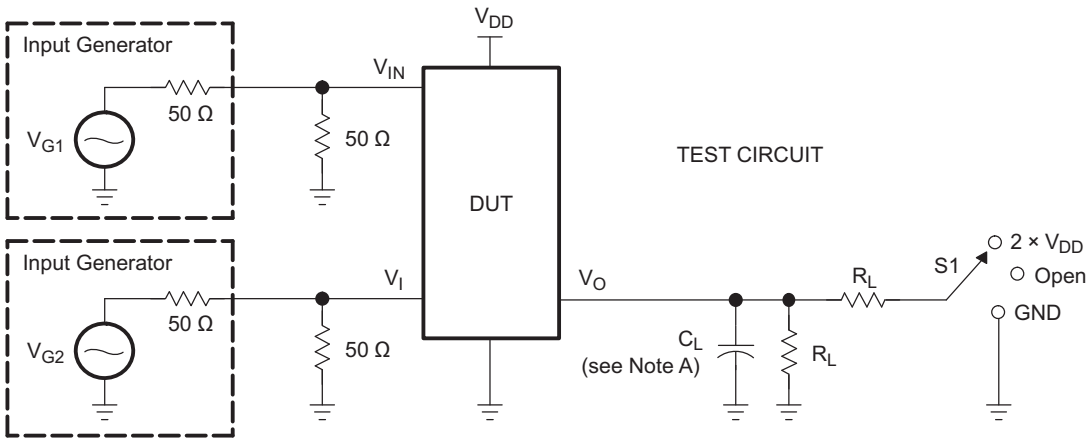


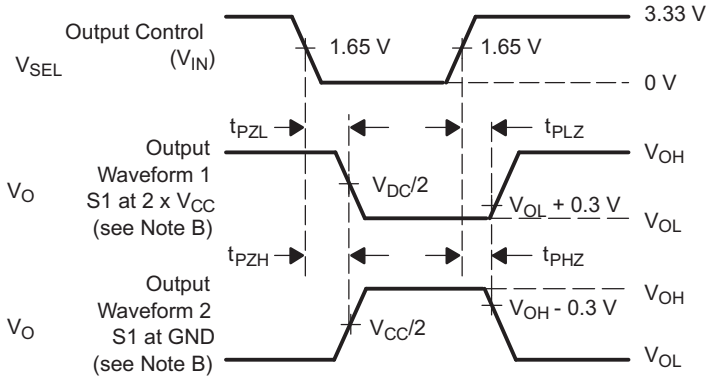
Figure 6. R_{ON} vs V_{IN}

PARAMETER MEASUREMENT INFORMATION

Enable and Disable Times



TEST	V_{DD}	S1	R_L	V_{in}	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V ± 0.3 V	2 × V_{DD}	200 Ω	GND	4 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ± 0.3 V	GND	200 Ω	V_{DD}	4 pF	0.3 V



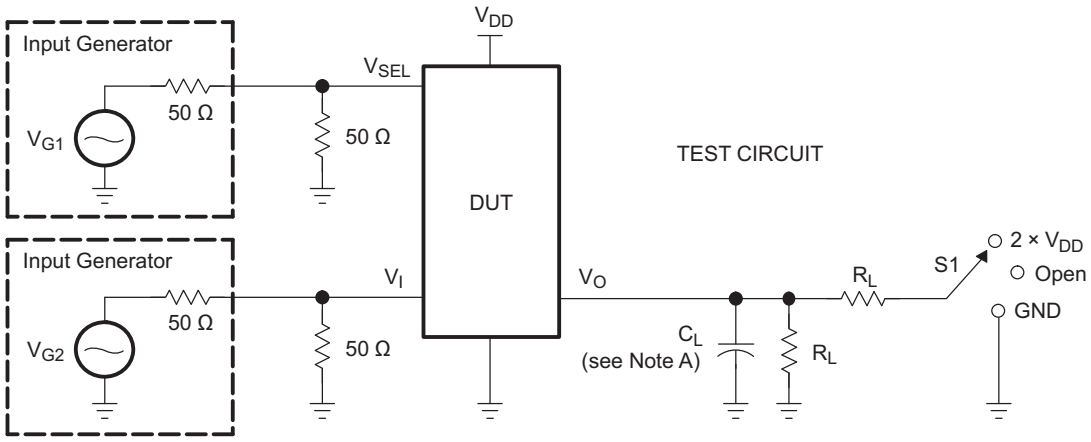
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics:PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

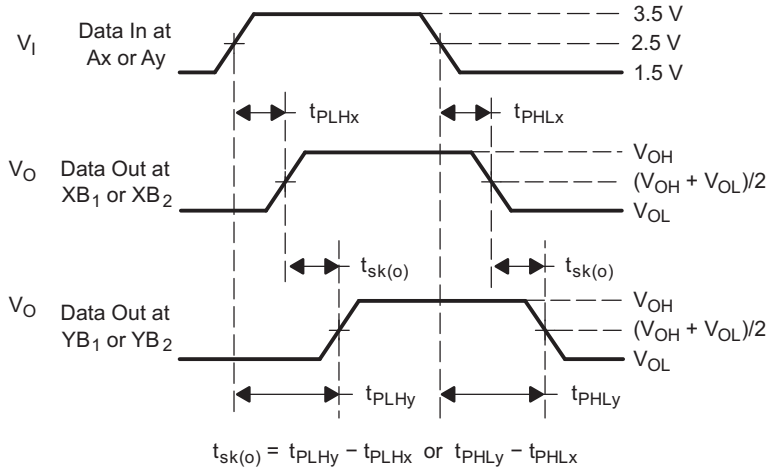
Figure 7. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

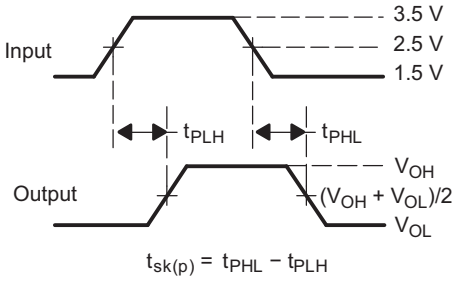
Figure 8. Skew



TEST	V_{CC}	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{CC} or GND	4 pF
$t_{sk(p)}$	3.3 V ± 0.3V	Open	200 Ω	V_{CC} or GND	4 pF



VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)



VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 9. Test Circuit andf Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

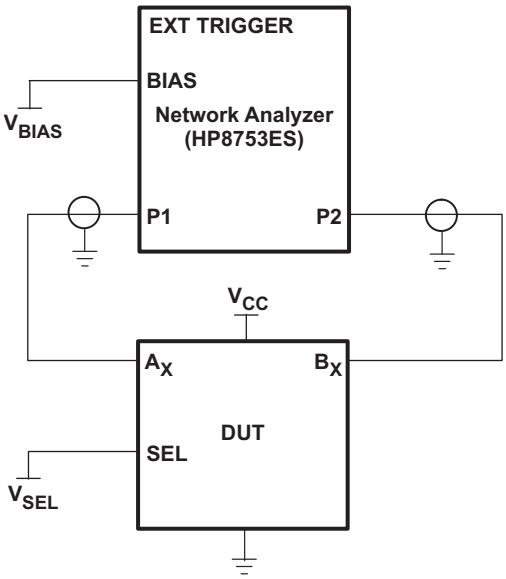


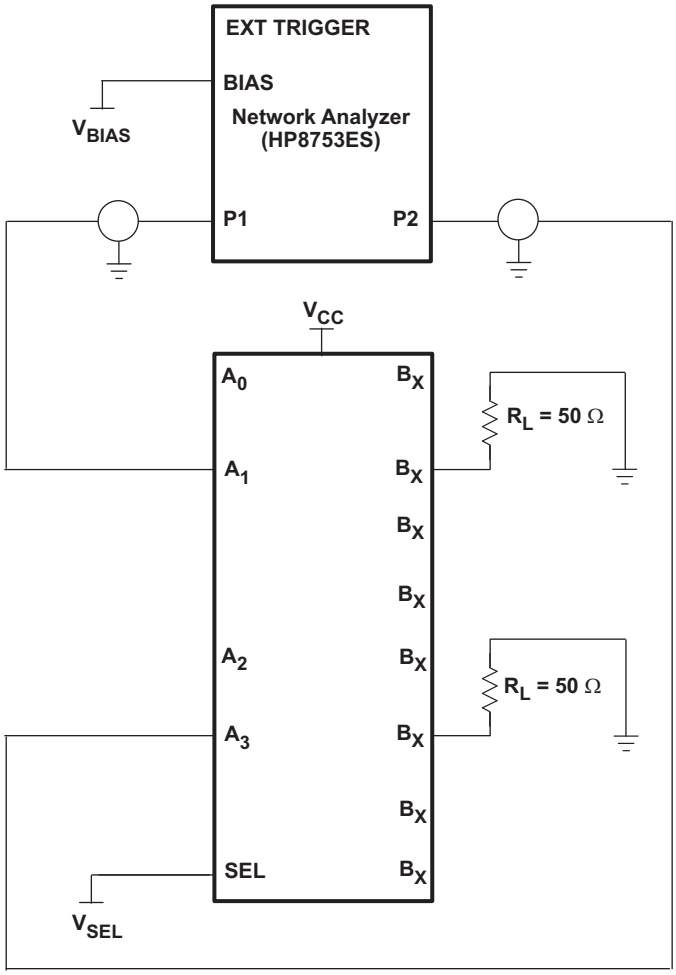
Figure 10. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at B0. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.
B. A 50 W termination resistor is needed to match the loading of the network analyzer.

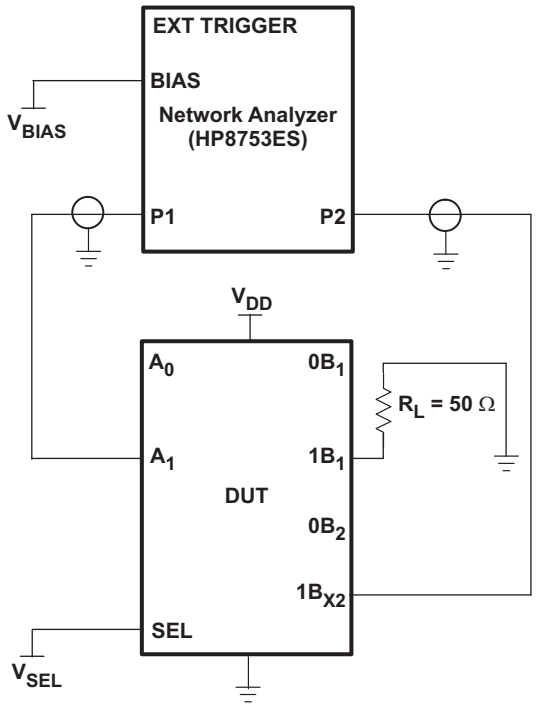
Figure 11. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{SEL} = 0 and A_1 is the input, the output is measured at A_3. All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.
B. A 50 W termination resistor is needed to match the loading of the network analyzer.

Figure 12. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} = GND and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

REVISION HISTORY

Changes from Revision A (March 2012) to Revision B **Page**

- Changed Low B Low Bit-to-Bit Skew in the FEATURES list from ($t_{sk(o)}$ = 6 ps Max) to ($t_{sk(o)}$ = 6 ps Typ) 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DDR3812RUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SL812	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

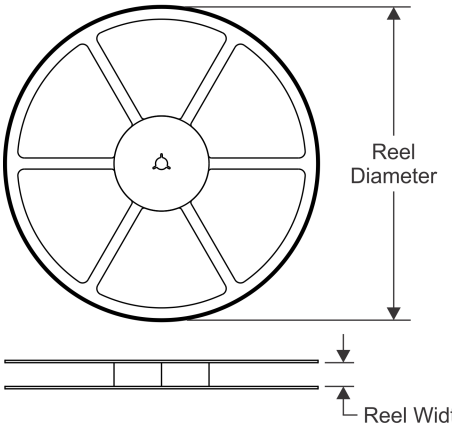
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

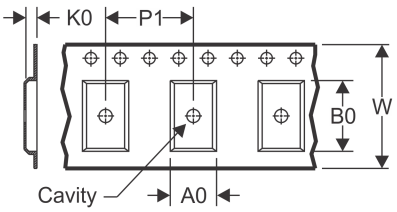
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

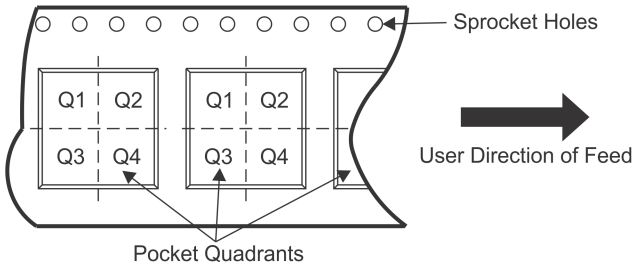


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

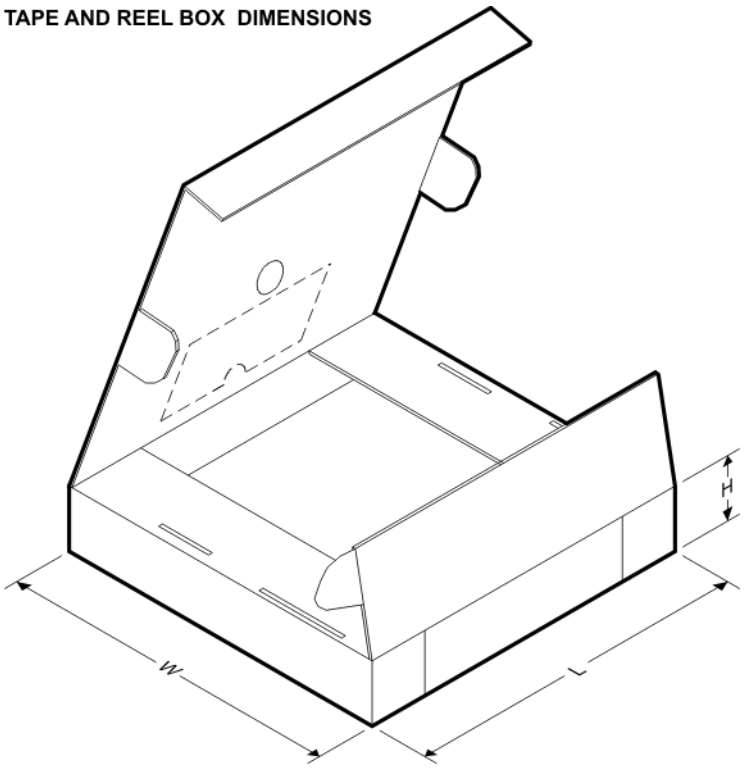
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DDR3812RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

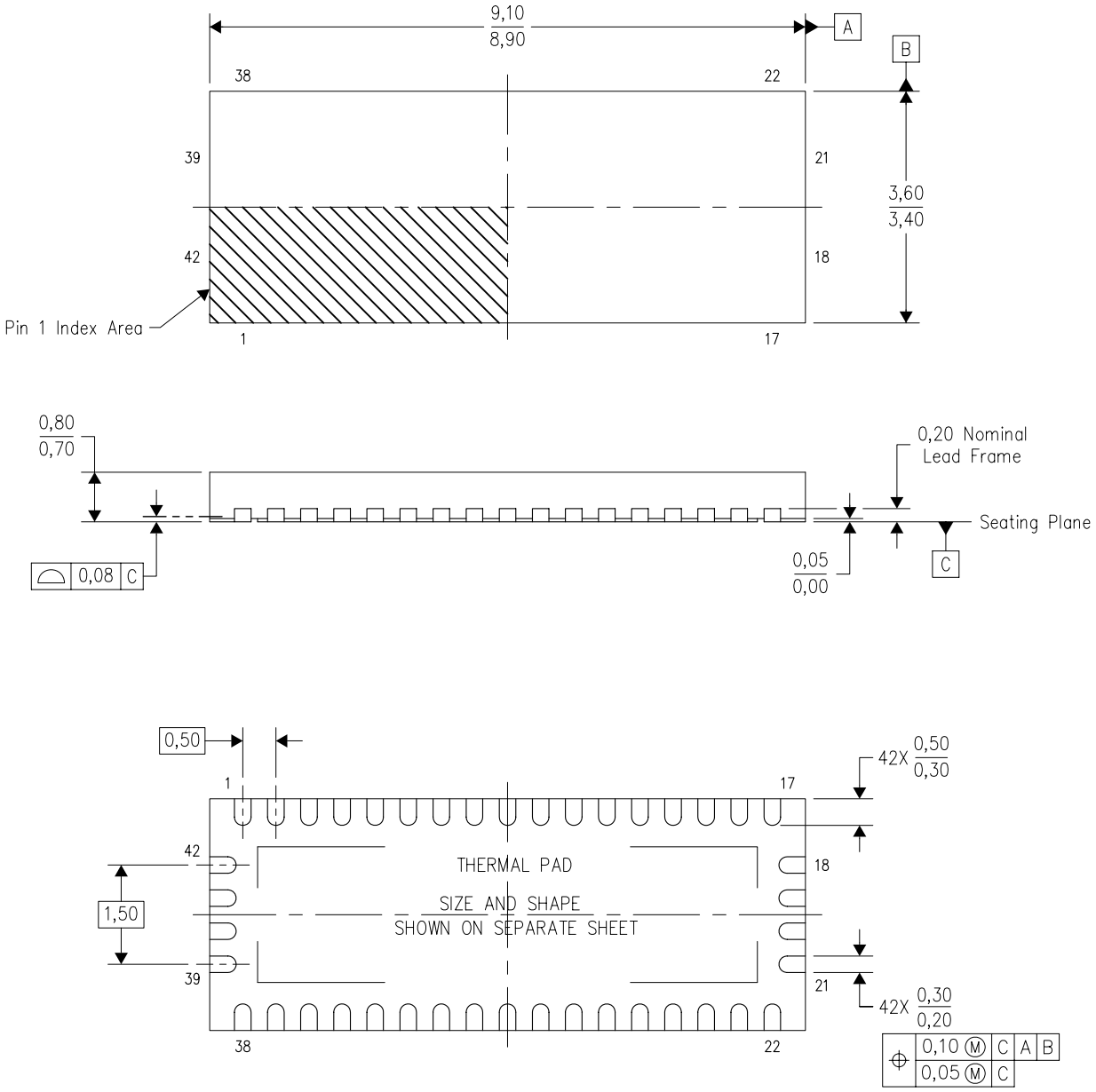
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DDR3812RUAR	WQFN	RUA	42	3000	358.0	335.0	35.0

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

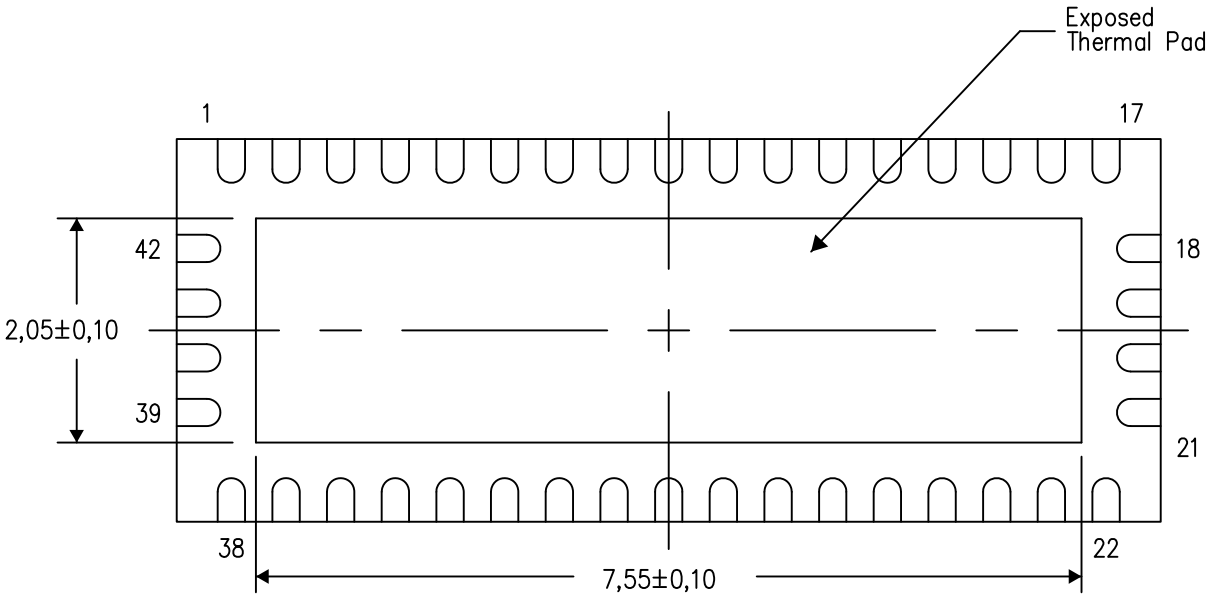
RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



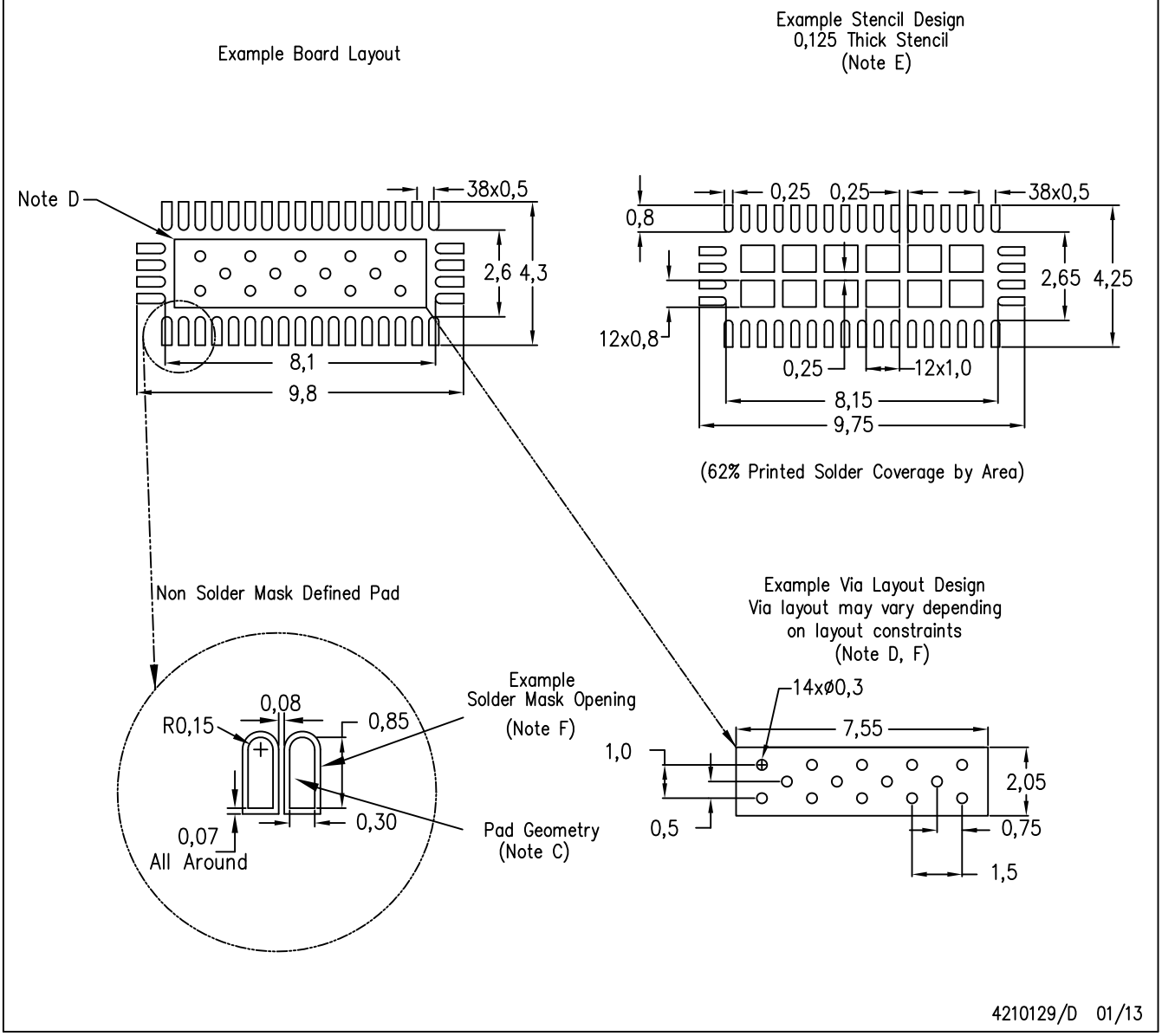
Bottom View

Exposed Thermal Pad Dimensions

4208352/E 01/13

NOTE: All linear dimensions are in millimeters

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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