BiCMOS POWER-FACTOR PREREGULATOR

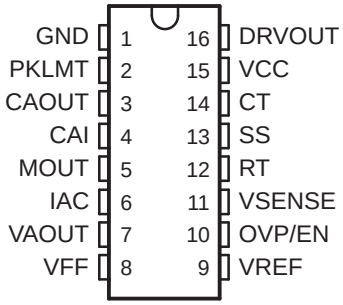
FEATURES

- Controls Boost Preregulator to Near-Unity Power Factor
- Limits Line Distortion
- World-Wide Line Operation
- Overvoltage Protection
- Accurate Power Limiting
- Average Current Mode Control
- Improved Noise Immunity
- Improved Feed-Forward Line Regulation
- Leading Edge Modulation
- 150-μA Typical Start-Up Current
- Low-Power BiCMOS Operation
- 12-V to 17-V Operation

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (–55°C/125°C) Temperature Range(1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

D, DW, N, or PW PACKAGE
(TOP VIEW)



(1) Additional temperature ranges are available - contact factory

DESCRIPTION/ORDERING INFORMATION

The UCC2817 and UCC2818 provides all the functions necessary for active power-factor-corrected preregulators. The controller achieves near-unity power factor by shaping the ac-input line current waveform to correspond to that of the ac input line voltage. Average current mode control maintains stable, low-distortion sinusoidal line current.

Designed with TI's BiCMOS process, the UCC2817 and UCC2818 offers new features, such as lower start-up current, lower power dissipation, overvoltage protection, a shunt UVLO detect circuitry, a leading-edge modulation technique to reduce ripple current in the bulk capacitor, and an improved, low-offset (±2-mV) current amplifier to reduce distortion at light load conditions.

The UCC2817 offers an on-chip shunt regulator with low start-up current suitable for applications utilizing a bootstrap supply. The UCC2818 is intended for applications with a fixed supply (V_{CC}).

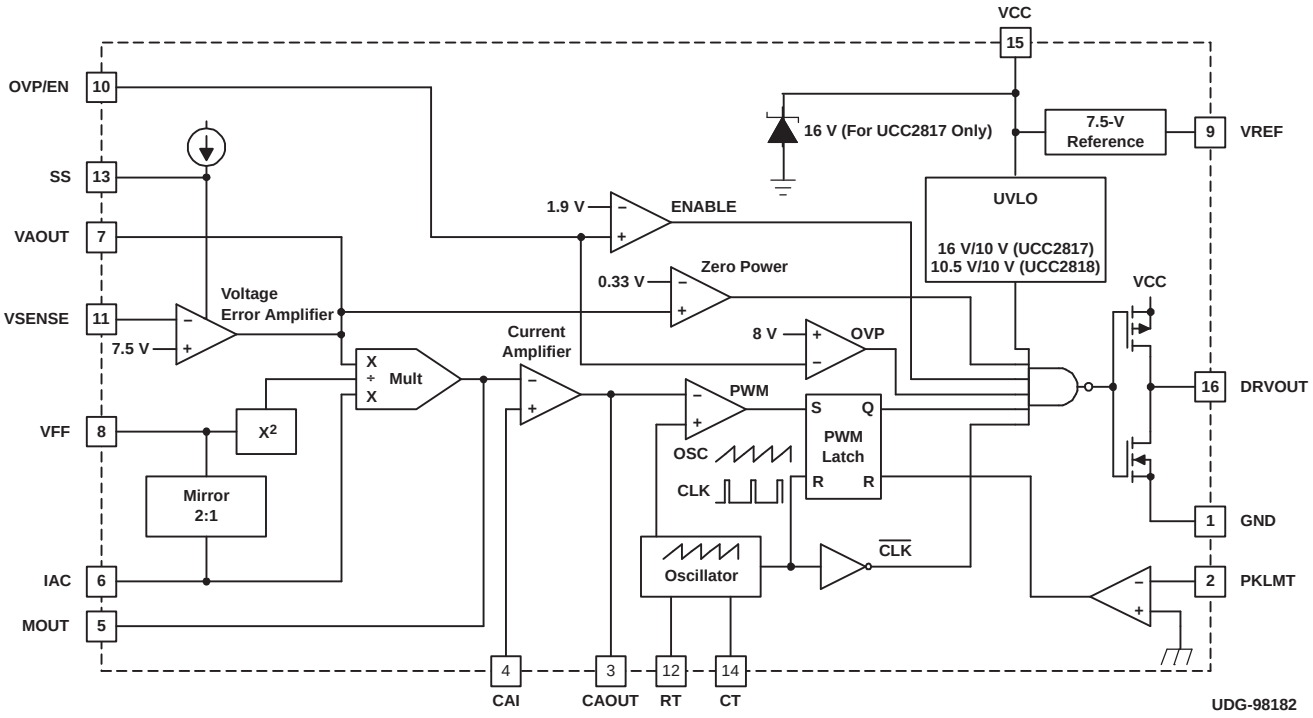
The devices are available in a 16-pin D package.

ORDERING INFORMATION

$T_A = T_J$	PACKAGE(1)		ORDERABLE PART NUMBER	TURN-ON THRESHOLD
–55°C to 125°C	SOIC – D	Reel	UCC2818MDREP	10.2 V

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

BLOCK DIAGRAM



Pin Descriptions

CAI: Current amplifier noninverting input. Place a resistor between this pin and the GND side of current sense resistor. This input and the inverting input (MOUT) remain functional down to and below GND.

CAOUT: Current amplifier output. This is the output of a wide bandwidth operational amplifier that senses line current and commands the PFC pulse-width modulator (PWM) to force the correct duty cycle. Compensation components are placed between CAOUT and MOUT.

CT: Oscillator timing capacitor. A capacitor from CT to GND sets the PWM oscillator frequency according to:

$$f \approx \left(\frac{0.6}{RT \times CT}\right)$$

The lead from the oscillator timing capacitor to GND should be as short and direct as possible.

DRVOUT: Gate drive. The output drive for the boost switch is a totem-pole MOSFET gate driver on DRVOUT. Use a series gate resistor to prevent interaction between the gate impedance and the output driver that might cause the DRVOUT to overshoot excessively. See characteristic curve (Figure 13) to determine minimum required gate resister value. Some overshoot of the DRVOUT output is always expected when driving a capacitive load.

GND: Ground. All voltages measured with respect to ground. V_{CC} and REF should be bypassed directly to GND with a 0.1-µF or larger ceramic capacitor.

IAC: Current proportional to input voltage. This input to the analog multiplier is a current proportional to instantaneous line voltage. The multiplier is tailored for very low distortion from this current input (I_{IAC}) to multiplier output. The recommended maximum I_{IAC} is 500 µA.

MOUT: Multiplier output and current amplifier inverting input. The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high-impedance input so the amplifier can be configured as a differential amplifier. This configuration improves noise immunity and allows for the leading-edge modulation operation. The multiplier output current is limited to (2 × I_{IAC}). The multiplier output current is given by the equation:

$$I_{MOUT} = \frac{I_{IAC} \times (V_{VAOUT} - 1)}{V_{VFF}^{2} \times K}$$

Where:

K = 1/V is the multiplier gain constant

OVP/EN: Over-voltage/enable. A window comparator input that disables the output driver if the boost output voltage is a programmed level above the nominal, or disables both the PFC output driver and resets SS if pulled below 1.9 V (typ).

PKLMT: PFC peak current limit. The threshold for peak limit is 0 V. Use a resistor divider from the negative side of the current sense resistor to V_{REF} to level shift this signal to a voltage level defined by the value of the sense resistor and the peak current limit. Peak current limit is reached when PKLMT voltage falls below 0 V.

RT: Oscillator charging current. A resistor from RT to GND is used to program oscillator charging current. A resistor between 10 kΩ and 100 kΩ is recommended. Nominal voltage on this pin is 3 V.

SS: Soft-start. V_{SS} is discharged for V_{VCC} low conditions. When enabled, SS charges an external capacitor with a current source. This voltage is used as the voltage error signal during start-up, enabling the PWM duty cycle to increase slowly. In the event of a V_{VCC} dropout, the OVP/EN is forced below 1.9 V (typ), SS quickly discharges to disable the PWM.

Note: In an open-loop test circuit, grounding the SS pin does not ensure 0% duty cycle. Please see the application section for details.

VAOUT: Voltage amplifier output. This is the output of the operational amplifier that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5 V to prevent overshoot.

VCC: Positive supply voltage. Connect to a stable source of at least 20 mA between 10 V and 17 V for normal operation. Bypass V_{CC} directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate gate drive signals, the output devices are inhibited unless V_{VCC} exceeds the upper under-voltage lockout voltage threshold and remains above the lower threshold.

VFF: Feed-forward voltage. The RMS voltage signal generated at this pin by mirroring 1/2 of the I_{IAC} into a single pole external filter. At low line, the VFF voltage should be 1.4 V.

VSENSE: Voltage amplifier inverting input. This is normally connected to a compensation network and to the boost converter output through a divider network.

VREF: Voltage reference output. V_{REF} is the output of an accurate 7.5-V voltage reference. This output is capable of delivering 20 mA to peripheral circuitry and is internally short-circuit current limited. VREF is disabled and remains at 0 V when V_{VCC} is below the UVLO threshold. Bypass VREF to GND with a 0.1-µF or larger ceramic capacitor for best stability. Please refer to Figure 8 and Figure 9 for VREF line and load regulation characteristics.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage			18	V
I_{CC}	Supply current			20	mA
	Gate drive current, continuous			0.2	A
	Gate drive current			1.2	A
	Input voltage	CAI, MOUT, SS		8	V
		PKLMT		5	
		VSENSE, OVP/EN		10	
	Input current	RT, IAC, PKLMT		10	mA
		V_{CC} (no switching)		20	
	Maximum negative voltage	DRVOUT, PKLMT, MOUT		–0.5	V
	Power dissipation			1	W
θ_{JA}	Package thermal impedance				°C/W
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature range		–65	150	°C
T_{sol}	Lead temperature	Soldering, 10 s		300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

PACKAGE	θ_{JC}(°C/W)	θ_{JA}(°C/W)
SOIC-16 (D)	22	40 to 70(1)

(1) Specified θ_{JA} (junction to ambient) is for devices mounted to 5-in^2 FR4 PC board with 1-oz copper, where noted. When resistance range is given, lower values are for 5-in^2 aluminum PC board. Test PWB was 0.062-in thick and typically used 0,635-mm trace widths for power packages and 1,3-mm trace widths for nonpower packages with a 100-mil × 100-mil probe land area at the end of each trace.

ELECTRICAL CHARACTERISTICS

T_A = –55°C to 125°C, T_A = T_J, V_{CC} = 12 V, R_T = 22 kΩ, C_T = 270 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current						
Supply current, off		V_{CC} = (V_{CC} turn-on threshold – 0.3 V)		150	300	µA
Supply current, on		V_{CC} = 12 V, No load on DRVOUT	2	4	6	mA
UVLO						
VCC turn-on threshold	UCC2817		15.4	16	16.6	V
VCC turn-off threshold	UCC2817		9.4	9.7		V
UVLO hysteresis	UCC2817		5.8	6.3		V
Maximum shunt voltage	UCC2817		15.4	17	17.5	V
VCC turn-on threshold	UCC2818		9.7	10.2	10.9	V
VCC turn-off threshold	UCC2818		9.4	9.7		V
UVLO hysteresis	UCC2818		0.3	0.5		V
Voltage Amplifier						
Input voltage			7.309	7.5	7.691	V
VSENSE bias current		V_{SENSE} = V_{REF}, VAOUT = 2.5 V		50	200	nA
Open-loop gain		VAOUT = 2 V to 5 V	50	90		dB
High-level output voltage		I_L = –150 µA	5.3	5.5	5.6	V
Low-level output voltage		I_L = 150 µA	0	50	150	mV
Overvoltage Protection and Enable						
Overvoltage reference			VREF + 0.48	VREF + 0.5	VREF + 0.52	V
Hysteresis			300	500	600	mV
Enable threshold			1.7	1.9	2.1	V
Enable hysteresis			0.1	0.2	0.3	V
Current Amplifier						
Input offset voltage		V_{CM} = 0 V, V_{CAOUT} = 3 V	–3.5	0	2.5	mV
Input bias current		V_{CM} = 0 V, V_{CAOUT} = 3 V		–50	–100	nA
Input offset current		V_{CM} = 0 V, V_{CAOUT} = 3 V		25	100	nA
Open-loop gain		V_{CM} = 0 V, V_{CAOUT} = 2 V to 5 V	86			dB
Common-mode rejection ratio		V_{CM} = 0 V to 1.5 V, V_{CAOUT} = 3 V	55	80		dB
High-level output voltage		I_L = –120 mA	5.6	6.5	6.9	V
Low-level output voltage		I_L = 1 mA	0.1	0.2	0.5	V
Gain bandwidth product(1)				2.5		MHz
Voltage Reference						
Input voltage			7.3	7.5	7.65	V
Load regulation		I_{REF} = 1 mA to 2 mA	0		10	mV
Line regulation		V_{CC} = 10.8 V to 15 V(2)	0		10	mV
Short-circuit current		V_{REF} = 0 V	–20	–25	–50	mA
Oscillator						
Initial accuracy		T_A = 25°C	85	100	115	kHz
Voltage stability		V_{CC} = 10.8 V to 15 V	–1.5%		1.5%	
Total variation		Line, temperature	80		120	kHz
Ramp peak voltage			4.5	5	5.5	V

(1) Ensured by design, not production tested.
(2) Reference variation for V_{CC} < 10.8 V is shown in Figure 8.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –55°C to 125°C, T_A = T_J, V_{CC} = 12 V, R_T = 22 kΩ, C_T = 270 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Ramp amplitude voltage (peak to peak)		3.5	4	4.5	V
Peak Current Limit						
	PKLMT reference voltage		–15		15	mV
	PKLMT propagation delay		150	350	500	ns
Multiplier						
I_{MOUT}	High line, low power output current	I_{AC} = 500 µA, V_{FF} = 4.7 V, VAOUT = 1.25 V	11	–6	–33	µA
	High-line, high-power output current	I_{AC} = 500 µA, V_{FF} = 4.7 V, VAOUT = 5 V	–53	–90	–112	
	Low-line, low-power output current	I_{AC} = 150 µA, V_{FF} = 1.4 V, VAOUT = 1.25 V	–8	–19	–50	
	Low-line, high-power output current	I_{AC} = 150 µA, V_{FF} = 1.4 V, VAOUT = 5 V	–268	–300	–350	
	IAC limited output current	I_{AC} = 150 µA, V_{FF} = 1.3 V, VAOUT = 5 V	–250	–300	–400	
	Gain constant (K)	I_{AC} = 200 µA, V_{FF} = 3 V, VAOUT = 2.5 V	0.5	1	1.6	1/V
I_{MOUT}	Zero current	I_{AC} = 150 µA, V_{FF} = 1.4 V, VAOUT = 0.25 V		0	–2	µA
		I_{AC} = 500 µA, V_{FF} = 4.7 V, VAOUT = 0.25 V		0	–2	
		I_{AC} = 500 µA, V_{FF} = 4.7 V, VAOUT = 0.5 V		0	–3.5	
	Power limit (I_{MOUT} × V_{FF})	I_{AC} = 150 µA, V_{FF} = 1.4 V, VAOUT = 5 V	–375	–420	–490	µW
Feed Forward						
	VFF output current	I_{AC} = 300 µA	–140	–150	–160	µA
Soft Start						
	Softstart charge current		–6	–10	–16	µA
Gate Driver						
	Pullup resistance	I_O = –100 mA to –200 mA		5	12	Ω
	Pulldown resistance	I_O = 100 mA		2	10	Ω
	Output rise time	C_L = 1 nF, R_L = 10 Ω, V_{DRVOUT} = 0.7 V to 9 V		25	50	ns
	Output fall time	C_L = 1 nF, R_L = 10 Ω, V_{DRVOUT} = 9 V to 0.7 V		10	50	ns
	Maximum duty cycle		93%	95%	99%	
	Minimum controlled duty cycle	At 100 kHz			2%	
Zero Power						
	Zero-power comparator threshold	Measured on VAOUT	0.2	0.33	0.5	V

APPLICATION INFORMATION

The UCC2817 is a BiCMOS average current mode boost controller for high-power-factor, high-efficiency, preregulator power supplies. Figure 1 shows the UCC2817 in a 250-W PFC preregulator circuit. Off-line switching power converters normally have an input current that is not sinusoidal. The input current waveform has a high harmonic content because current is drawn in pulses at the peaks of the input voltage waveform. An active power-factor correction circuit programs the input current to follow the line voltage, forcing the converter to look like a resistive load to the line. A resistive load has 0° phase displacement between the current and voltage waveforms. Power factor (PF) can be defined in terms of the phase angle between two sinusoidal waveforms of the same frequency:

$$PF = \cos \theta$$

Therefore, a purely resistive load would have a power factor of 1. In practice, power factors of 0.999 with total harmonic distortion (THD) of less than 3% are possible with a well-designed circuit. Following guidelines are provided to design PFC boost converters using the UCC2817.

NOTE: Schottky diodes, D5 and D6, are required to protect the PFC controller from electrical over stress during system power up.

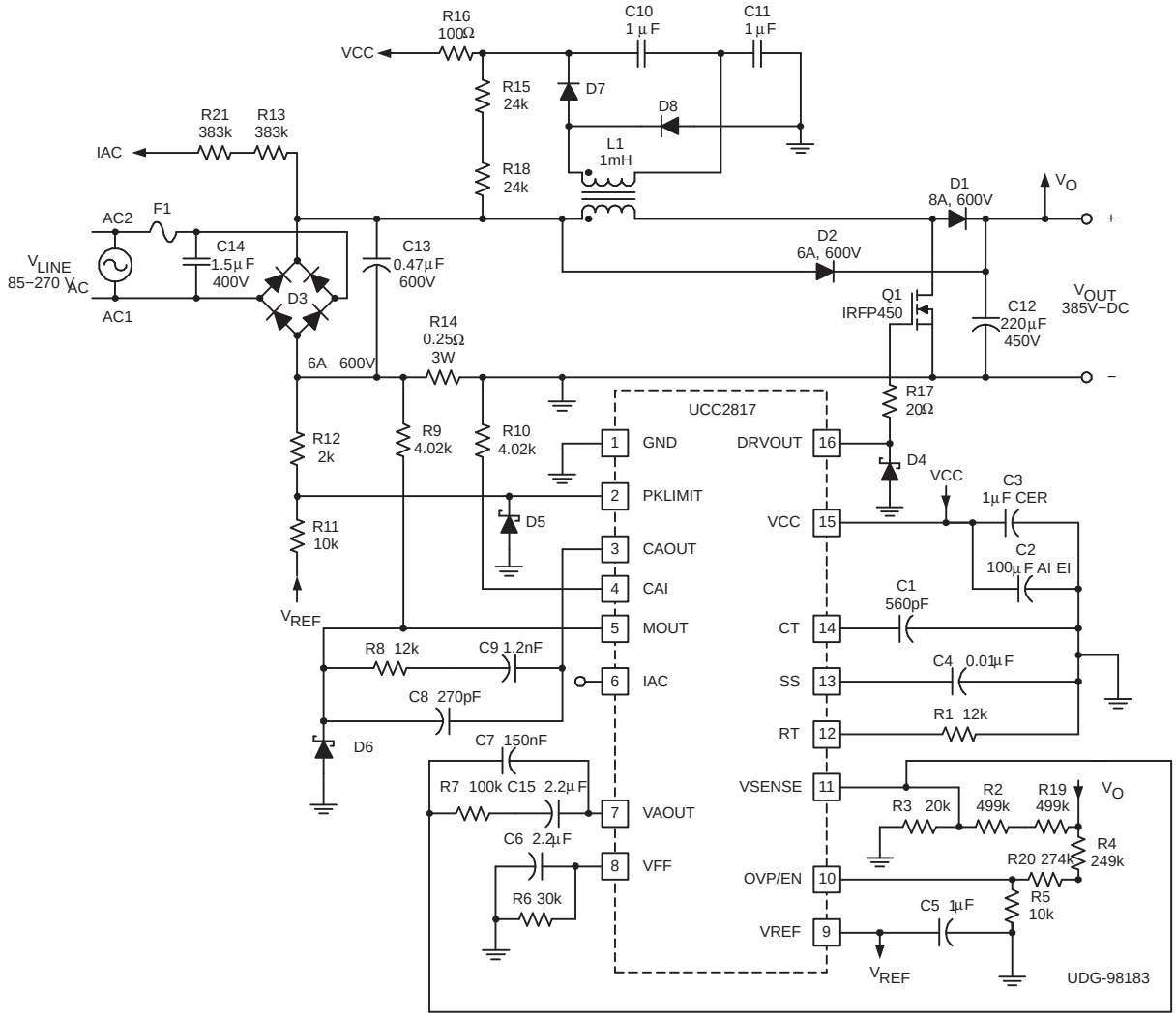


Figure 1. Typical Application Circuit

Power Stage

L_{BOOST}: The boost inductor value is determined by:

$$L_{BOOST} = \frac{\left(V_{IN(min)} \times D\right)}{(\Delta I \times fs)}$$

Where:

D = Duty cycle

ΔI = Inductor ripple current

f_S = Switching frequency

For the example circuit, a switching frequency of 100 kHz, a ripple current of 875 mA, a maximum duty cycle of 0.688, and a minimum input voltage of 85 V_{RMS} produces a boost inductor value of about 1 mH. The values used in this equation are at the peak of low line, where the inductor current and its ripple are at a maximum.

C_{OUT}: Two main criteria, the capacitance and the voltage rating, dictate the selection of the output capacitor. The value of capacitance is determined by the holdup time required for supporting the load after input ac voltage is removed. Holdup is the amount of time that the output stays in regulation after the input has been removed. For this circuit, the desired holdup time is approximately 16 ms. Expressing the capacitor value in terms of output power, output voltage, and holdup time gives the equation:

$$C_{OUT} = \frac{\left(2 \times P_{OUT} \times \Delta t\right)}{\left(V_{OUT}^{\ 2} - V_{OUT(min)}^{\ 2}\right)}$$

In practice, the calculated minimum capacitor value may be inadequate because output ripple voltage specifications limit the amount of allowable output capacitor ESR. Attaining a sufficiently low value of ESR often necessitates the use of a much larger capacitor value than calculated. The amount of output capacitor ESR allowed can be determined by dividing the maximum specified output ripple voltage by the inductor ripple current. In this design holdup time was the dominant determining factor and a 220-μF, 450-V capacitor was chosen for the output voltage level of 385 VDC at 250 W.

Power switch selection: As in any power-supply design, tradeoffs between performance, cost, and size have to be made. When selecting a power switch, it can be useful to calculate the total power dissipation in the switch for several different devices at the switching frequencies being considered for the converter. Total power dissipation in the switch is the sum of switching loss and conduction loss. Switching losses are the combination of the gate charge loss, C_{OSS} loss, and turnon and turnoff losses:

$$P_{GATE} = Q_{GATE} \times V_{GATE} \times fs$$

$$P_{COSS} = \frac{1}{2} \times C_{OSS} \times V^2_{OFF} \times fs$$

$$P_{ON} + P_{OFF} = \frac{1}{2} \times V_{OFF} \times I_L \times \left(t_{ON} + t_{OFF}\right) \times fs$$

Where:

Q_{GATE} = Total gate charge

V_{GATE} = Gate drive voltage

f_S = Clock frequency

C_{OSS} = Drain source capacitance of the MOSFET

I_L = Peak inductor current

t_{ON} and t_{OFF} = Switching times (estimated using device parameters R_{GATE}, Q_{GD} and V_{TH})

V_{OFF} = Voltage across the switch during the off time (in this case $V_{OFF} = V_{OUT}$)

Conduction loss is calculated as the product of the $R_{DS(on)}$ of the switch (at the worst-case junction temperature) and the square of RMS current:

$$P_{COND} = R_{DS(on)} \times K \times I^2_{RMS}$$

Where:

K = temperature factor found in the manufacturer's $R_{DS(on)}$ vs junction temperature curves

Calculating these losses and plotting against frequency gives a curve that enables the designer to determine which manufacturer's device has the best performance at the desired switching frequency, or which switching frequency has the least total loss for a particular power switch. For this design example, an IRFP450 HEXFET™ from International Rectifier was chosen because of its low $R_{DS(on)}$ and its V_{DSS} rating. The IRFP450 $R_{DS(on)}$ of 0.4 Ω and the maximum V_{DSS} of 500 V made it an ideal choice. A review of this procedure can be found in the Unitrode™ Power-Supply Design Seminar SEM1200, Topic 6, Design Review: 140 W (*Multiple Output High Density DC/DC Converter*).

Soft Start

The soft-start circuitry is used to prevent overshoot of the output voltage during start up. This is accomplished by slowly bringing up the voltage amplifier output (V_{VAOUT}), which allows for the PWM duty cycle to slowly increase. Use the following equation to select a capacitor for the soft-start pin.

In this example, t_{DELAY} = 7.5 ms, which yields a C_{SS} of 10 nF.

$$C_{SS} = \frac{10\ \mu A \times t_{DELAY}}{7.5\ V}$$

In an open-loop test circuit, shorting the soft-start pin to ground does not ensure 0% duty cycle. This is due to the current amplifiers input offset voltage, which could force the current amplifier output high or low depending on the polarity of the offset voltage. However, in the typical application, there is sufficient amount of inrush and bias current to overcome the current amplifier offset voltage.

Multiplier

The output of the multiplier of the UCC2817 is a signal representing the desired input line current. It is an input to the current amplifier, which programs the current loop to control the input current to give high power factor operation. As such, the proper functioning of the multiplier is key to the success of the design. The inputs to the multiplier are VAOUT, the voltage amplifier error signal, I_{IAC}, a representation of the input rectified ac line voltage, and an input voltage feed-forward signal, V_{VFF}. The output of the multiplier, I_{MOUT}, can be expressed as:

$$I_{MOUT} = I_{IAC} \times \frac{\left(V_{VAOUT} - 1\right)}{K \times V_{VFF}^{\ 2}}$$

Where:

K = Constant typically equal to 1/V

The Electrical Characteristics table covers all the required operating conditions for designing with the multiplier. Additionally, curves in Figure 10, Figure 11, and Figure 12 provide typical multiplier characteristics over its entire operating range.

The I_{IAC} signal is obtained through a high-value resistor connected between the rectified ac line and the IAC pin of the UCC2817 and UCC2818. This resistor R_{IAC} is sized to give the maximum I_{IAC} current at high line. For the UCC2817 and UCC2818, the maximum I_{IAC} current is about 500 μA. A higher current than this can drive the multiplier out of its linear range. A smaller current level is functional, but noise can become an issue, especially at low input line. Assuming a universal line operation of 85 V_{RMS} to 265 V_{RMS} gives a R_{IAC} value of 750 kΩ, because of voltage-rating constraints of a standard 1/4-W resistor, use a combination of lower-value resistors connected in series to give the required resistance and distribute the high voltage amongst the resistors. For this design example, two 383-kΩ resistors were used in series.

The current into the IAC pin is mirrored internally to the VFF pin where it is filtered to produce a voltage feed-forward signal proportional to line voltage. The VFF voltage is used to keep the power-stage gain constant, and to provide input power limiting.See the TI application report SLUA196 for detailed explanation on how the VFF pin provides power limiting. The following equation can be used to size the VFF resistor R_{VFF} to provide power limiting where $V_{IN(min)}$ is the minimum RMS input voltage, and R_{IAC} is the total resistance connected between the IAC pin and the rectified line voltage.

$$R_{VFF} = \frac{1.4\ V}{\frac{V_{IN(min)} \times 0.9}{2 \times R_{IAC}}} \approx 30\ k\Omega$$

Because the VFF voltage is generated from line voltage, it needs to be adequately filtered to reduce THD caused by the 120-Hz rectified line voltage. Refer to Unitrode Power-Supply Design Seminar, SEM-700 Topic 7 (*Optimizing the Design of a High Power Factor Preregulator*). A single pole filter was adequate for this design. Assuming that an allocation of 1.5% total harmonic distortion from this input is allowed, and that the second harmonic ripple is 66% of the input ac line voltage, the amount of attenuation required by this filter is:

$$\frac{1.5\ \%}{66\ \%} = 0.022$$

A ripple frequency (f_R) of 120 Hz and an attenuation of 0.022 requires that the pole of the filter (f_P) be placed at:

$$f_P = 120\ Hz \times 0.022 \approx 2.6\ Hz$$

The following equation can be used to select the filter capacitor C_{VFF} required to produce the desired low-pass filter.

$$C_{VFF} = \frac{1}{2 \times \pi \times R_{VFF} \times f_P} \approx 2.2\ \mu F$$

The R_{MOUT} resistor is sized to match the maximum current through the sense resistor to the maximum multiplier current. The maximum multiplier current, or $I_{MOUT(max)}$, can be determined by the equation:

$$I_{MOUT(max)} = \frac{I_{IAC@V_{IN(min)}} \times \left(V_{VAOUT(max)} - 1\ V\right)}{K \times V_{VFF\ (min)}^{2}}$$

$I_{MOUT(max)}$ for this design is approximately 315 µA. The R_{MOUT} resistor can then be determined by:

$$R_{MOUT} = \frac{V_{RSENSE}}{I_{MOUT(max)}}$$

In this example, V_{RSENSE} was selected to give a dynamic operating range of 1.25 V, which gives an R_{MOUT} of roughly 3.91 kΩ.

Voltage Loop

The second major source of harmonic distortion is the ripple on the output capacitor at the second harmonic of the line frequency. This ripple is fed back through the error amplifier and appears as a third harmonic ripple at the input to the multiplier. The voltage loop must be compensated not just for stability but also to attenuate the contribution of this ripple to the total harmonic distortion of the system (see Figure 2).

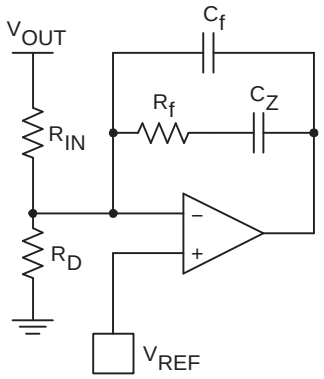


Figure 2. Voltage Amplifier Configuration

The gain of the voltage amplifier, G_{VA}, can be determined by first calculating the amount of ripple present on the output capacitor. The peak value of the second harmonic voltage is given by the equation:

$$V_{OPK} = \frac{P_{IN}}{2\pi \times f_R \times C_{OUT} \times V_{OUT}}$$

In this example, V_{OPK} = 3.91 V. Assuming an allowable contribution of 0.75% (1.5% peak to peak) from the voltage loop to the THD budget, set the gain equal to:

$$G_{VA} = \frac{\left(\Delta V_{VAOUT}\right) 0.015}{2 \times V_{OPK}}$$

Where:

ΔV_{VAOUT} = Effective output voltage range of the error amplifier (5 V for the UCC2817).

The network needed to realize this filter is comprised of an input resistor, R_{IN}, and feedback components C_f, C_Z, and R_f. The value of R_{IN} is already determined because of its function as one-half of a resistor divider from V_{OUT} feeding back to the voltage amplifier for output voltage regulation. In this case, the value was chosen to be 1 MΩ. This high value was chosen to reduce power dissipation in the resistor. In practice, the resistor value would be realized by the use of two 500-kΩ resistors in series because of the voltage rating constraints of most standard 1/4-W resistors. The value of C_f is determined by the equation:

$$C_f = \frac{1}{2\pi \times f_R \times G_{VA} \times R_{IN}}$$

In this example, C_f = 150 nF. Resistor R_f sets the dc gain of the error amplifier and, thus, determines the frequency of the pole of the error amplifier. The location of the pole can be found by setting the gain of the loop equation to one and solving for the crossover frequency. The frequency, expressed in terms of input power, can be calculated by the equation:

$$f_{VI}^{2} = \frac{P_{IN}}{(2\pi)^2 \times \Delta V_{VAOUT} \times V_{OUT} \times R_{IN} \times C_{OUT} \times C_f}$$

f_{VI} for this converter is 10 Hz. A derivation of this equation can be found in the Unitrode Power Supply Design Seminar SEM1000, Topic 1 (*A 250-kHz, 500-W Power Factor Correction Circuit Employing Zero Voltage Transitions*).

Solving for R_f becomes:

$$R_f = \frac{1}{2\pi \times f_{VI} \times C_f}$$

or R_f = 100 kΩ.

Due to the low output impedance of the voltage amplifier, capacitor C_Z was added in series with R_F to reduce loading on the voltage divider. To ensure the voltage loop crossed over at f_{VI}, C_Z was selected to add a zero at 1/10th of f_{VI}. For this design, a 2.2-µF capacitor was chosen for C_Z. The following equation can be used to calculate C_Z:

$$C_Z = \frac{1}{2 \times \pi \times \frac{f_{VI}}{10} \times R_f}$$

Current Loop

The gain of the power stage is:

$$G_{ID}(s) = \frac{V_{OUT} \times R_{SENSE}}{s \times L_{BOOST} \times V_P}$$

R_{SENSE} has been chosen to give the desired differential voltage for the current sense amplifier at the desired current limit point. In this example, a current limit of 4 A and a reasonable differential voltage to the current amplifier of 1 V gives a R_{SENSE} value of 0.25 Ω. V_P in this equation is the voltage swing of the oscillator ramp, 4 V for the UCC2817. Setting the crossover frequency of the system to 1/10th of the switching frequency, or 10 kHz, requires a power-stage gain at that frequency of 0.383. In order for the system to have a gain of 1 at the crossover frequency, the current amplifier must have a gain of $1/G_{ID}$ at that frequency. G_{EA}, the current amplifier gain is then:

$$G_{EA} = \frac{1}{G_{ID}} = \frac{1}{0.383} = 2.611$$

R_I is the R_{MOUT} resistor, previously calculated to be 3.9 kΩ (see Figure 3). The gain of the current amplifier is R_f/R_I, so multiplying R_I by G_{EA} gives the value of R_f, in this case approximately 12 kΩ. Setting a zero at the crossover frequency and a pole at one-half the switching frequency completes the current loop compensation.

$$C_Z = \frac{1}{2 \times \pi \times R_f \times f_C}$$

$$C_P = \frac{1}{2 \times \pi \times R_f \times \frac{f_s}{2}}$$

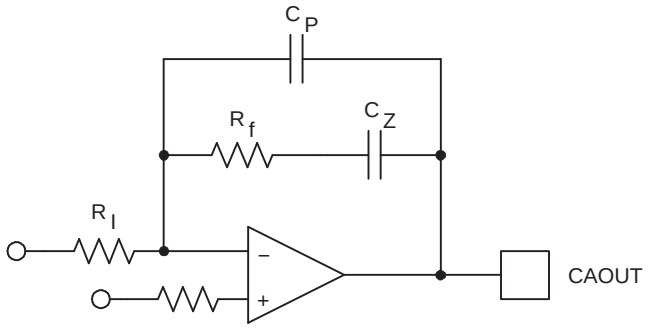


Figure 3. Current Loop Compensation

The UCC2817 current amplifier has the input from the multiplier applied to the inverting input. This change in architecture from previous TI PFC controllers improves noise immunity in the current amplifier. It also adds a phase inversion into the control loop. The UCC2817 takes advantage of this phase inversion to implement leading-edge duty cycle modulation. Synchronizing a boost PFC controller to a downstream dc-to-dc controller reduces the ripple current seen by the bulk capacitor between stages, reducing capacitor size and cost and reducing EMI. This is explained in greater detail in a following section. The UCC2817 current amplifier configuration is shown in Figure 4.

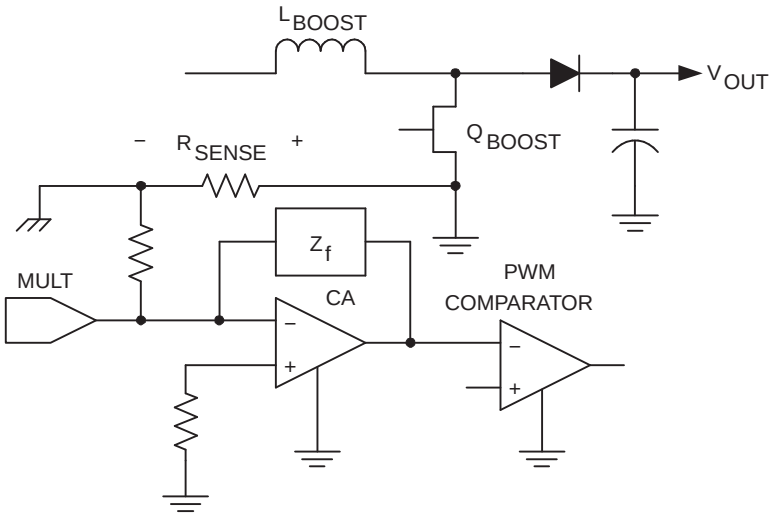


Figure 4. UCC2818 Current Amplifier Configuration

Start Up

The UCC2818 version of the device is intended to have VCC connected to a 12-V supply voltage. The UCC2817 has an internal shunt regulator enabling the device to be powered from bootstrap circuitry, as shown in the typical application circuit of Figure 1. The current drawn by the UCC2817 during undervoltage lockout, or start-up current, is typically 150 μA. Once V_{CC} is above the UVLO threshold, the device is enabled and draws 4 mA typically. A resistor connected between the rectified ac line voltage and the V_{CC} pin provides current to the shunt regulator during power up. Once the circuit is operational, the bootstrap winding of the inductor provides the V_{CC} voltage. Sizing of the start-up resistor is determined by the start-up time requirement of the system design.

$$I_C = C\frac{\Delta V}{\Delta t}$$

$$R = \frac{V_{RMS} \times 0.9}{I_C}$$

Where:

I_C = Charge current

C = Total capacitance at the V_{CC} pin

ΔV = UVLO threshold

Δt = Allowed start-up time

Assuming a 1-s allowed start-up time, a 16-V UVLO threshold, and a total V_{CC} capacitance of 100 μF, a resistor value of 51 kΩ is required at a low line input voltage of 85 V_{RMS}. The IC start-up current is sufficiently small as to be ignored in sizing the start-up resistor.

Capacitor Ripple Reduction

For a power system where the PFC boost converter is followed by a dc-to-dc converter stage, there are benefits to synchronizing the two converters. In addition to the usual advantages, such as noise reduction and stability, proper synchronization can significantly reduce the ripple currents in the boost circuit output capacitor. Figure 5 shows the impact of proper synchronization by showing a PFC boost converter together with the simplified input stage of a forward converter. The capacitor current during a single switching cycle depends on the status of the switches Q1 and Q2 and is shown in Figure 6. With a synchronization scheme that maintains conventional trailing-edge modulation on both converters, the capacitor current ripple is highest. The greatest ripple current cancellation is attained when the overlap of Q1 offtime and Q2 ontime is maximized. One method of achieving this is to synchronize the turnon of the boost diode (D1) with the turnon of Q2. This approach implies that the boost converter leading edge is pulse width modulated, while the forward converter is modulated with traditional trailing-edge PWM. The UCC2817 is designed as a leading edge modulator with easy synchronization to the downstream converter to facilitate this advantage. Table 1 compares the $I_{CB(rms)}$ for D1/Q2 synchronization as offered by UCC2817, versus the $I_{CB(rms)}$ for the other extreme of synchronizing the turnon of Q1 and Q2 for a 200-W power system with a V_{BST} of 385 V.

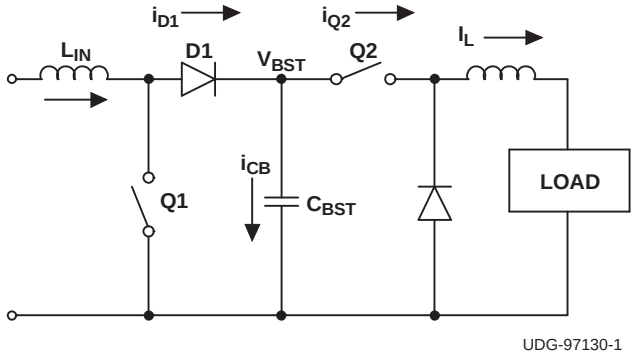


Figure 5. Simplified Representation of a Two-Stage PFC Power Supply

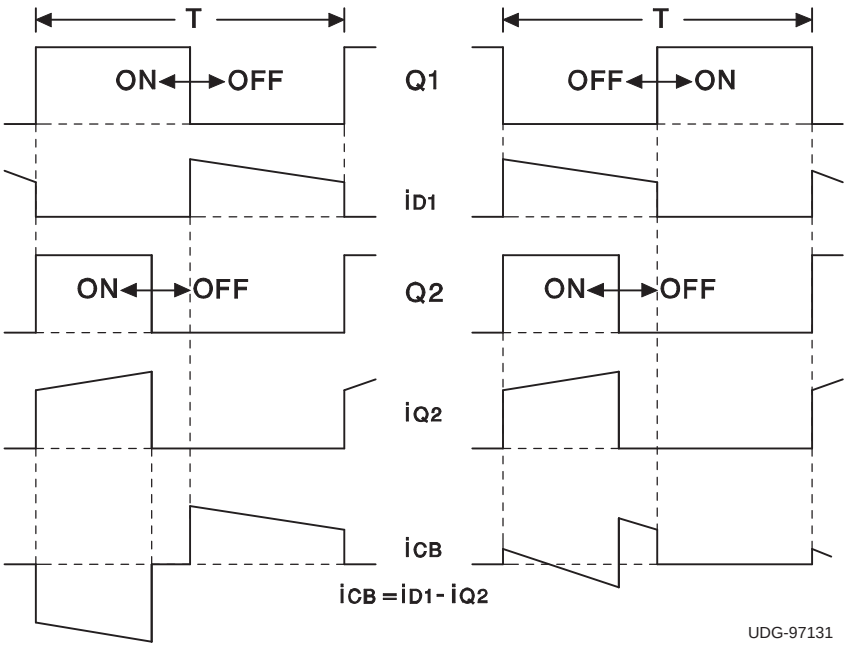


Figure 6. Timing Waveforms for Synchronization Scheme

Table 1. Effects of Synchronization on Boost Capacitor Current

	V_{IN} = 85 V		V_{IN} = 120 V		V_{IN} = 240 V	
D(Q2)	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2
0.35	1.491 A	0.835 A	1.341 A	0.663 A	1.024 A	0.731 A
0.45	1.432 A	0.93 A	1.276 A	0.664 A	0.897 A	0.614 A

Table 1 shows that the boost capacitor ripple current can be reduced by about 50% at nominal line and about 30% at high line with the synchronization scheme facilitated by the UCC2817. Figure 7 shows the suggested technique for synchronizing the UCC2817 to the downstream converter. With this technique, maximum ripple reduction as shown in Figure 6 is achievable. The output capacitance value can be significantly reduced if its choice is dictated by ripple current or the capacitor life can be increased as a result. In cost-sensitive designs where holdup time is not critical, this is a significant advantage.

An alternative method of synchronization to achieve the same ripple reduction is possible. In this method, the turnon of Q1 is synchronized to the turnoff of Q2. While this method yields almost identical ripple reduction and maintains trailing edge modulation on both converters, the synchronization is much more difficult to achieve and the circuit can become susceptible to noise as the synchronizing edge itself is being modulated.

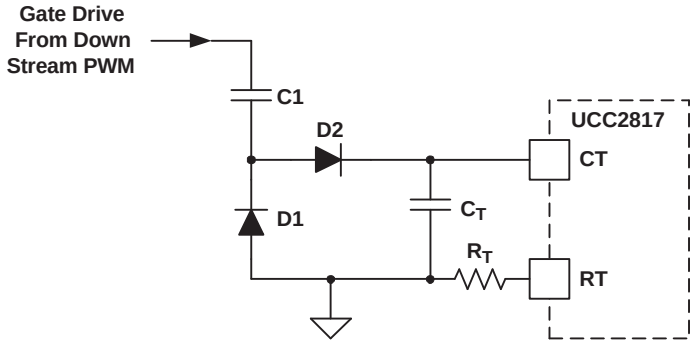


Figure 7. Synchronizing the UCC2817 to a Downstream Converter

REFERENCE VOLTAGE
vs
SUPPLY VOLTAGE

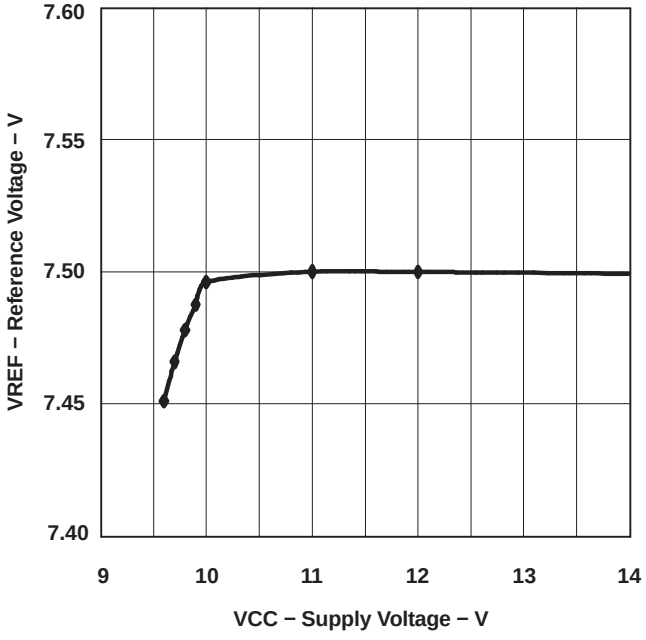


Figure 8.

REFERENCE VOLTAGE
vs
REFERENCE CURRENT

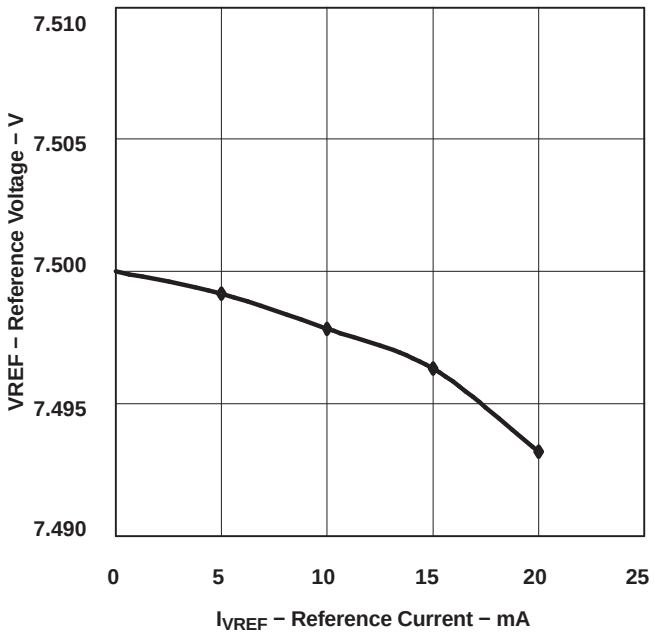


Figure 9.

MULTIPLIER OUTPUT CURRENT
vs
VOLTAGE ERROR AMPLIFIER OUTPUT

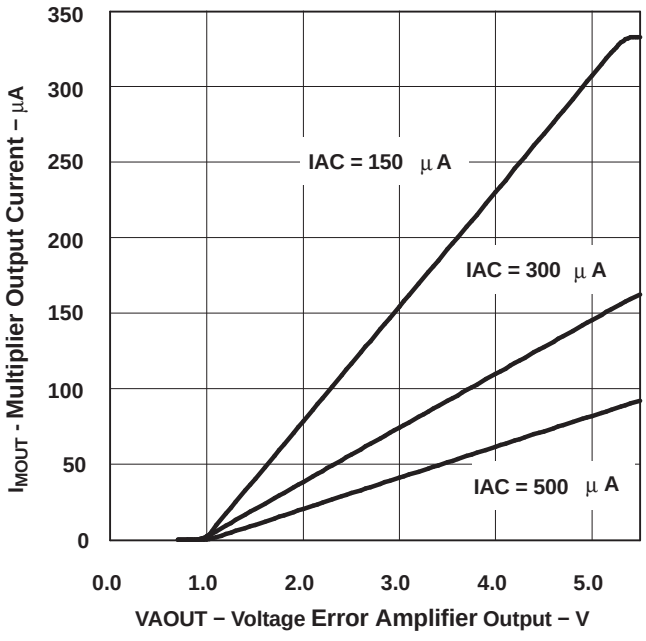


Figure 10.

MULTIPLIER GAIN
vs
VOLTAGE ERROR AMPLIFIER OUTPUT

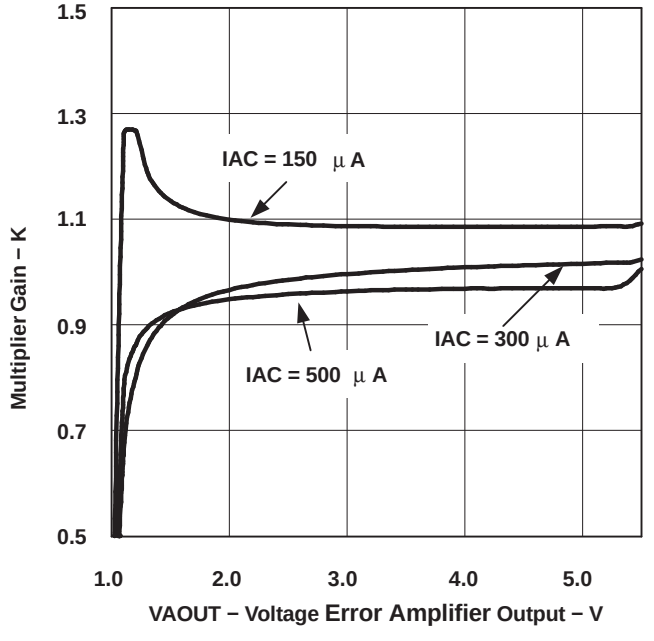


Figure 11.

MULTIPLIER CONSTANT POWER PERFORMANCE

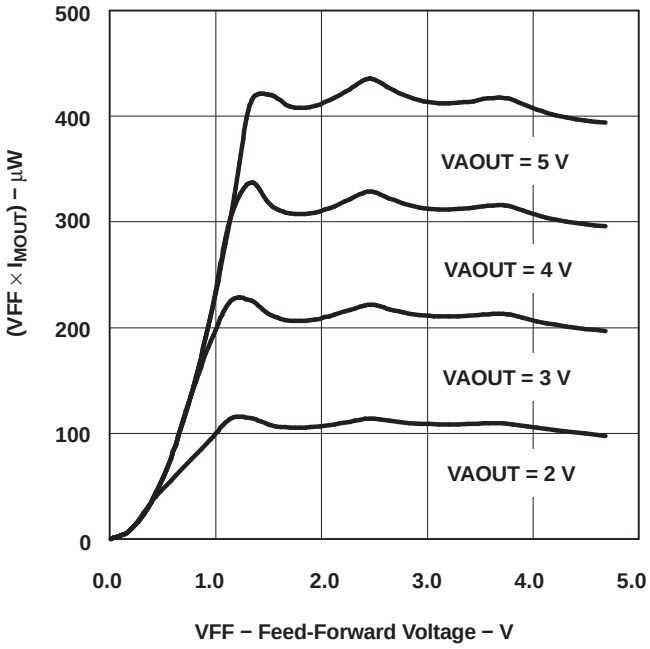


Figure 12.

RECOMMENDED MINIMUM GATE RESISTANCE
vs
SUPPLY VOLTAGE

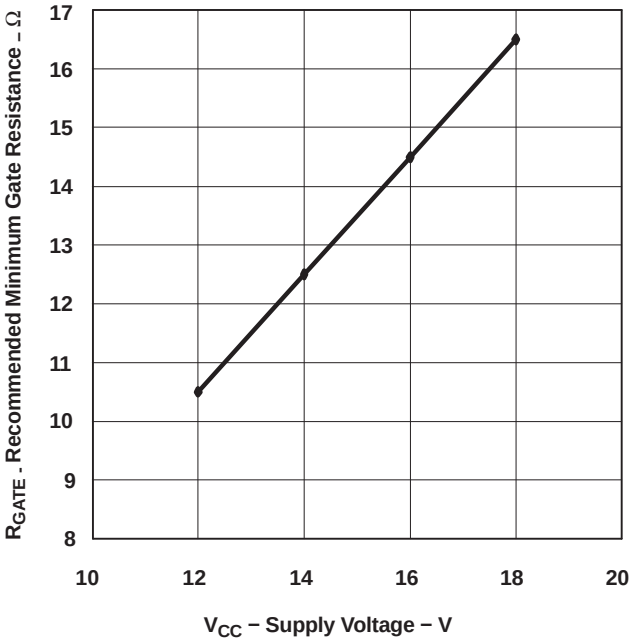


Figure 13.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2818MDREP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	UCC2818MD	Samples
V62/09617-01XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	UCC2818MD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC2818-EP :

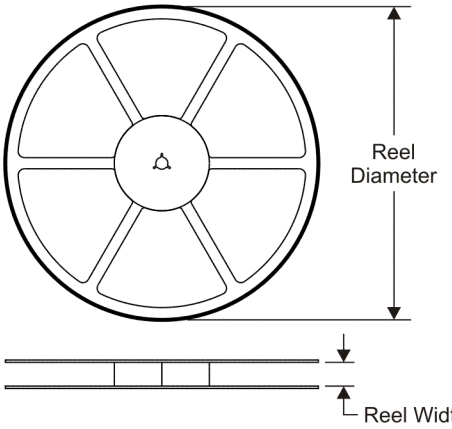
- Catalog: UCC2818

NOTE: Qualified Version Definitions:

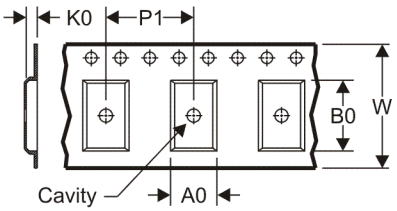
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

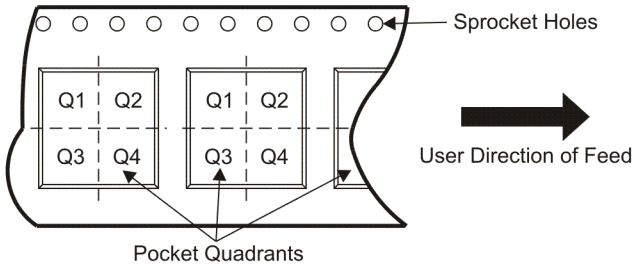


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

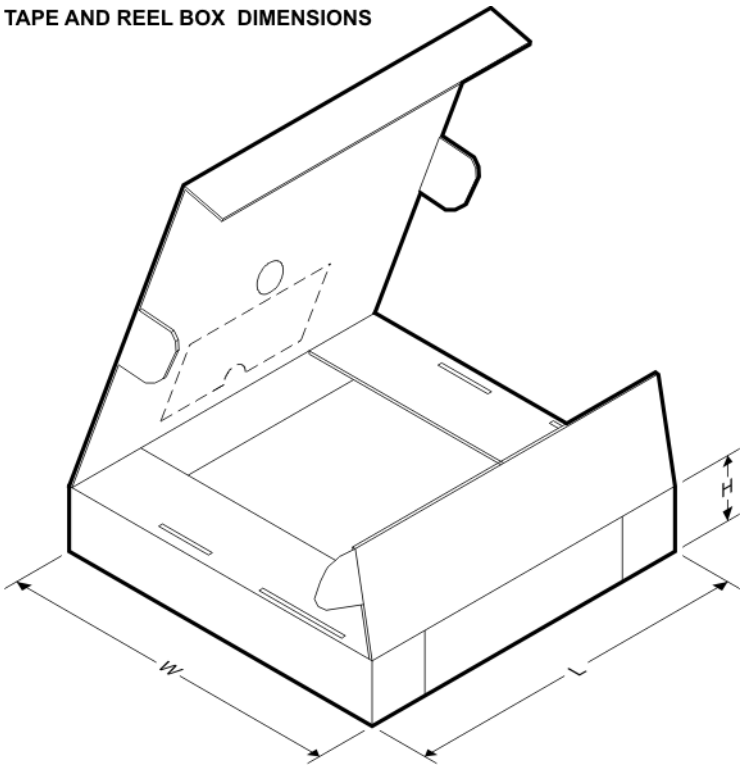
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2818MDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

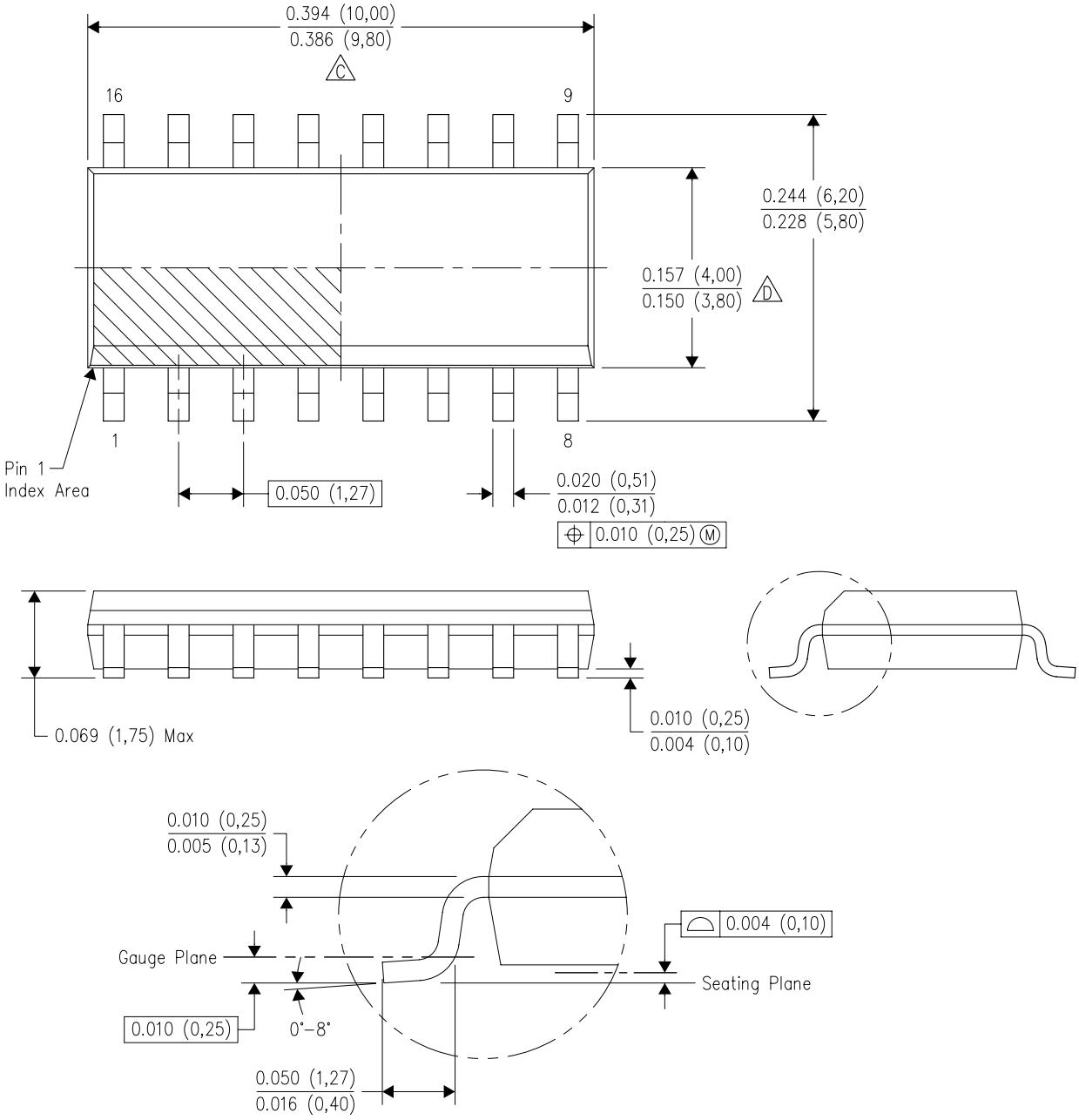
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2818MDREP	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
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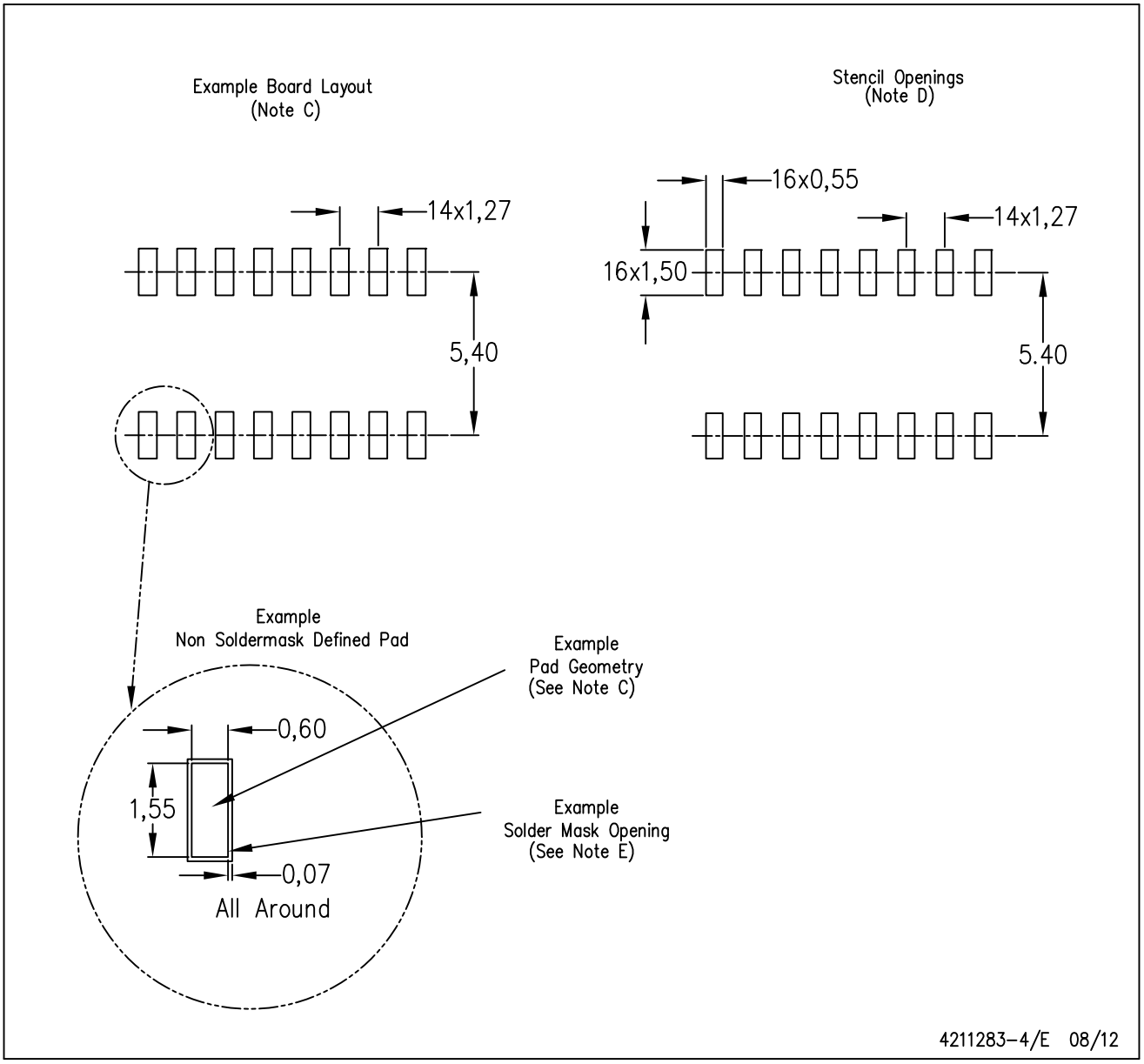
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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