SBOS117C – SEPTEMBER 2000 – REVISED APRIL 2004

Dual, VARIABLE GAIN AMPLIFIER with Low Noise Preamp

FEATURES

- **LOW NOISE PREAMP:**
  - **Low Input Noise: 1.25nV/√Hz**
  - **Active Termination Noise Reduction**
  - **Switchable Termination Value**
  - **80MHz Bandwidth**
  - **5dB to 25dB Gain Range**
  - **Differential Input/Output**
- **LOW NOISE VARIABLE GAIN AMPLIFIER:**
  - **Low Noise VCA: 3.3nV/√Hz, Differential Programming Optimizes Noise Figure**
  - **24dB to 45dB Gain**
  - **40MHz Bandwidth**
  - **Differential Input/Output**
- **LOW CROSSTALK: 52dB at Max Gain, 5MHz**
- **HIGH-SPEED VARIABLE GAIN ADJUST**
- **SWITCHABLE EXTERNAL PROCESSING**

APPLICATIONS

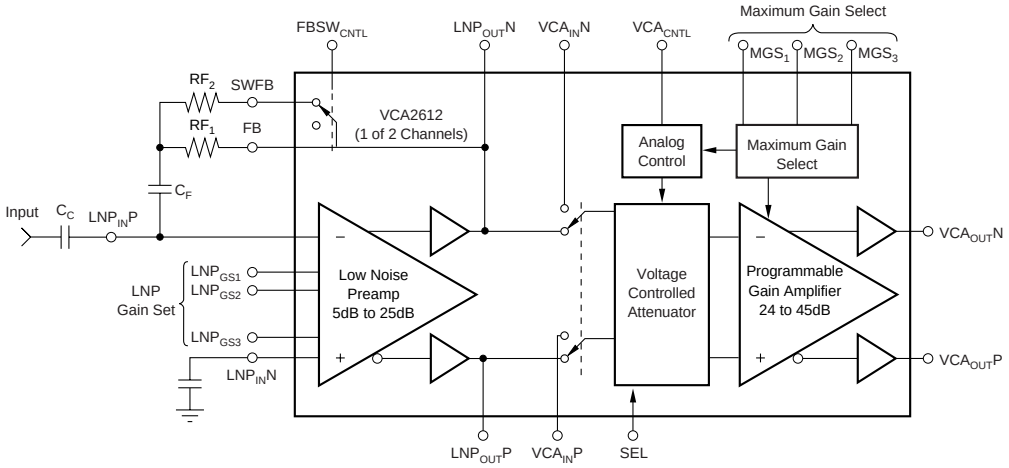
- **ULTRASOUND SYSTEMS**
- **WIRELESS RECEIVERS**
- **TEST EQUIPMENT**

DESCRIPTION

The VCA2612 is a highly integrated, dual receive channel, signal processing subsystem. Each channel of the product consists of a low noise preamplifier (LNP) and a Variable Gain Amplifier (VGA). The LNP circuit provides the necessary connections to implement Active Termination (AT), a method of cable termination which results in up to 4.6dB noise figure improvement. Different cable termination characteristics can be accommodated by utilizing the VCA2612's switchable LNA feedback pins. The LNP has the ability to accept both differential and single-ended inputs, and generates a differential output signal. The LNP provides strappable gains of 5dB, 17dB, 22dB, and 25dB.

The output of the LNP can be accessed externally for further signal processing, or fed directly into the VGA. The VCA2612's VGA section consists of two parts: the Voltage Controlled Attenuator (VCA) and the Programmable Gain Amplifier (PGA). The gain and gain range of the PGA can be digitally programmed. The combination of these two programmable elements results in a variable gain ranging from 0dB up to a maximum gain as defined by the user through external connections. The output of the VGA can be used in either a single-ended or differential mode to drive high-performance Analog-to-Digital (A/D) converters.

The VCA2612 also features low crosstalk and outstanding distortion performance. The combination of low noise and gain range programmability make the VCA2612 a versatile building block in a number of applications where noise performance is critical. The VCA2612 is available in a TQFP-48 package.



ABSOLUTE MAXIMUM RATINGS(1)

Power Supply ($+V_S$)	+6V
Analog Input	–0.3V to ($+V_S$ + 0.3V)
Logic Input	–0.3V to ($+V_S$ + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	–40°C to +150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VCA2612Y	TQFP-48	PFB	VCA2612Y	VCA2612Y/250	Tape and Reel, 250
"	"	"	"	VCA2612Y/2K	Tape and Reel, 2000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

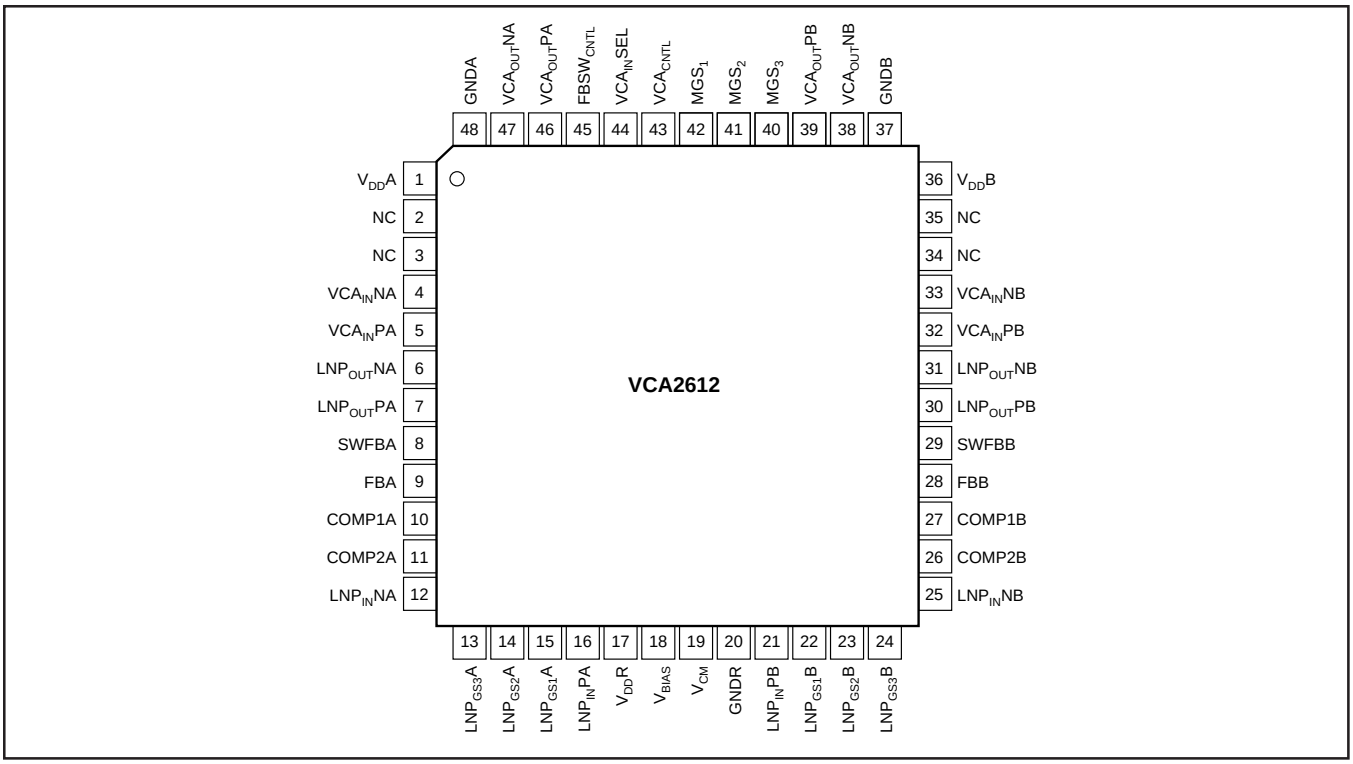
ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_{DDA} = V_{DDB} = V_{DDR} = +5V, load resistance = 500Ω on each output to ground, MGS = 011, LNP = 22dB and f_{IN} = 5MHz, unless otherwise noted. The input to the preamp (LNP) is single-ended, and the output from the VCA is single-ended unless otherwise noted.

		VCA2612Y			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PREAMPLIFIER					
Input Resistance			600		kΩ
Input Capacitance			15		pF
Input Bias Current			1		nA
CMRR	f = 1MHz, VCA_{CNTL} = 0.2V		50		dB
Maximum Input Voltage	Preamp Gain = +5dB		1		V_{PP}
	Preamp Gain = +25dB		112		mV_{PP}
Input Voltage Noise(1)	Preamp Gain = +5dB		3.5		$nV/\sqrt{Hz}$
	Preamp Gain = +25dB		1.25		$nV/\sqrt{Hz}$
Input Current Noise	Independent of Gain		0.35		$pA/\sqrt{Hz}$
Noise Figure, R_S = 75Ω, R_{IN} = 75Ω(1)	R_F = 550Ω, Preamp Gain = 22dB, PGA Gain = 39dB		6.2		dB
Bandwidth	Gain = 22dB		80		MHz
PROGRAMMABLE VARIABLE GAIN AMPLIFIER					
Peak Input Voltage	Differential		2		V_{PP}
–3dB Bandwidth			40		MHz
Slew Rate			300		V/µs
Output Signal Range	R_L ≥ 500Ω Each Side to Ground		2		V_{PP}
Output Impedance	f = 5MHz		1		Ω
Output Short-Circuit Current			±40		mA
Third Harmonic Distortion	f = 5MHz, V_{OUT} = 1V_{PP}, VCA_{CNTL} = 3.0V	–45	–71		dBc
Second Harmonic Distortion	f = 5MHz, V_{OUT} = 1V_{PP}, VCA_{CNTL} = 3.0V	–45	–63		dBc
IMD, Two-Tone	V_{OUT} = 2V_{PP}, f = 1MHz		–80		dBc
	V_{OUT} = 2V_{PP}, f = 10MHz		–80		dBc
1dB Compression Point	f = 5MHz, Output Referred, Differential		6		V_{PP}
Crosstalk	V_{OUT} = 1V_{PP}, f = 1MHz, Max Gain Both Channels		68		dB
Group Delay Variation	1MHz < f < 10MHz, Full Gain Range		±2		ns
DC Output Level, V_{IN} = 0			2.5		V
ACCURACY					
Gain Slope			10.9		dB/V
Gain Error				±1(2)	dB
Output Offset Voltage			±50		mV
Total Gain	VCA_{CNTL} = 0.2V	18	21	24	dB
	VCA_{CNTL} = 3.0V	47	50	53	dB
GAIN CONTROL INTERFACE					
Input Voltage (VCA_{CNTL}) Range			0.2 to 3.0		V
Input Resistance			1		MΩ
Response Time	45dB Gain Change, MGS = 111		0.2		µs
POWER SUPPLY					
Operating Temperature Range		–40		+85	°C
Specified Operating Range		4.75	5.0	5.25	V
Power Dissipation	Operating, Both Channels		410	495	mW
Thermal Resistance, θ_{JA}	TQFP-48		56.5		°C/W

NOTE: (1) For preamp driving VGA. (2) Referenced to best fit dB-linear curve.

PIN CONFIGURATION



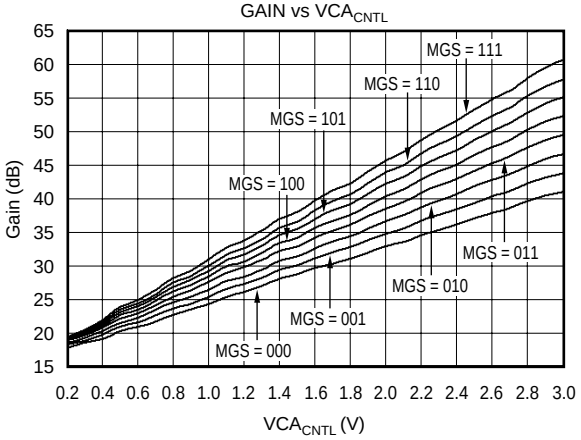
PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION	PIN	DESIGNATOR	DESCRIPTION
1	V_{DD}A	Channel A +Supply (+5V)	25	LNP_{IN}NB	Channel B LNP Inverting Input
2	NC	Do Not Connect	26	COMP2B	Channel B Frequency Compensation 2
3	NC	Do Not Connect	27	COMP1B	Channel B Frequency Compensation 1
4	VCA_{IN}NA	Channel A VCA Negative Input	28	FBB	Channel B Feedback Output
5	VCA_{IN}PA	Channel A VCA Positive Input	29	SWFBB	Channel B Switched Feedback Output
6	LNP_{OUT}NA	Channel A LNP Negative Output	30	LNP_{OUT}PB	Channel B LNP Positive Output
7	LNP_{OUT}PA	Channel A LNP Positive Output	31	LNP_{OUT}NB	Channel B LNP Negative Output
8	SWFBA	Channel A Switched Feedback Output	32	VCA_{IN}PB	Channel B VCA Positive Input
9	FBA	Channel A Feedback Output	33	VCA_{IN}NB	Channel B VCA Negative Input
10	COMP1A	Channel A Frequency Compensation 1	34	NC	Do Not Connect
11	COMP2A	Channel A Frequency Compensation 2	35	NC	Do Not Connect
12	LNP_{IN}NA	Channel A LNP Inverting Input	36	V_{DD}B	Channel B +Analog Supply (+5V)
13	LNP_{GS3}A	Channel A LNP Gain Strap 3	37	GNDB	Channel B Analog Ground
14	LNP_{GS2}A	Channel A LNP Gain Strap 2	38	VCA_{OUT}NB	Channel B VCA Negative Output
15	LNP_{GS1}A	Channel A LNP Gain Strap 1	39	VCA_{OUT}PB	Channel B VCA Positive Output
16	LNP_{IN}PA	Channel A LNP Noninverting Input	40	MGS_3	Maximum Gain Select 3 (LSB)
17	V_{DD}R	+Supply for Internal Reference (+5V)	41	MGS_2	Maximum Gain Select 2
18	V_{BIAS}	0.01µF Bypass to Ground	42	MGS_1	Maximum Gain Select 1 (MSB)
19	V_{CM}	0.01µF Bypass to Ground	43	VCA_{CNTL}	VCA Control Voltage
20	GNDR	Ground for Internal Reference	44	VCA_{IN}SEL	VCA Input Select, HI = External
21	LNP_{IN}PB	Channel B LNP Noninverting Input	45	$FBSW_{CNTL}$	Feedback Switch Control: HI = ON
22	LNP_{GS1}B	Channel B LNP Gain Strap 1	46	VCA_{OUT}PA	Channel A VCA Positive Output
23	LNP_{GS2}B	Channel B LNP Gain Strap 2	47	VCA_{OUT}NA	Channel A VCA Negative Output
24	LNP_{GS3}B	Channel B LNP Gain Strap 3	48	GNDA	Channel A Analog Ground

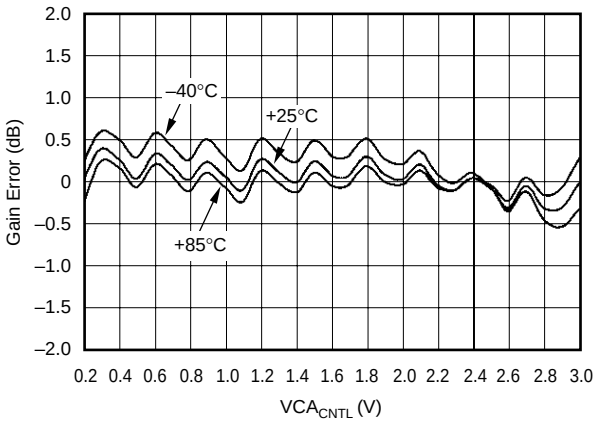
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{DDA} = V_{DDB} = V_{DDR} = +5V, load resistance = 500Ω on each output to ground, MGS = 011, LNP = 22dB and f_{IN} = 5MHz, unless otherwise noted. The input to the preamp (LNP) is single-ended, and the output from the VCA is single-ended unless otherwise noted. This results in a 6dB reduction in signal amplitude compared to differential operation.

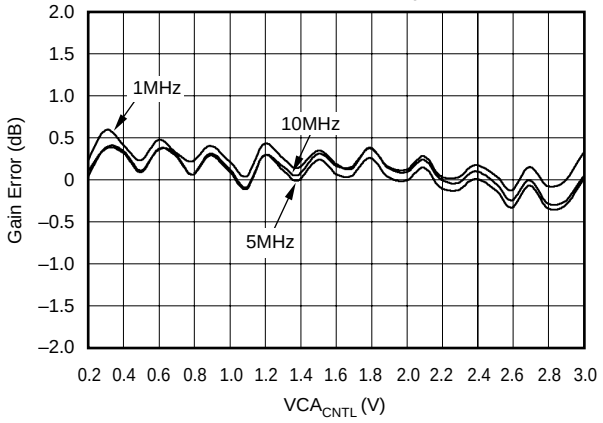
GAIN vs VCA_{CNTL}



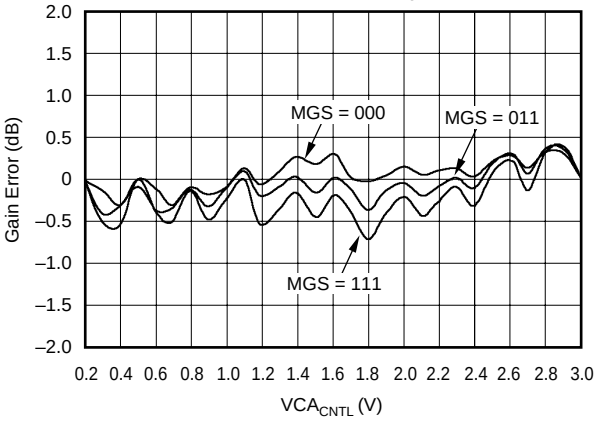
GAIN ERROR vs TEMPERATURE



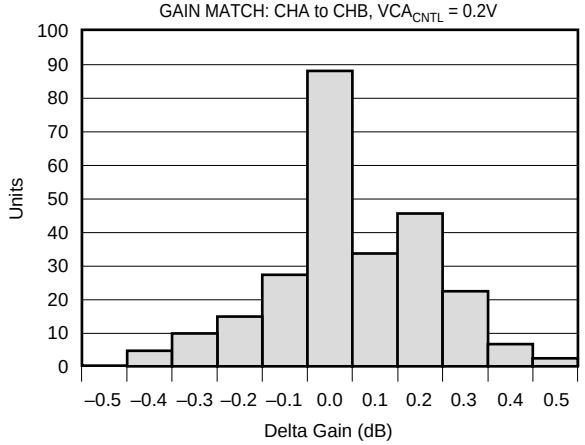
GAIN ERROR vs VCA_{CNTL}



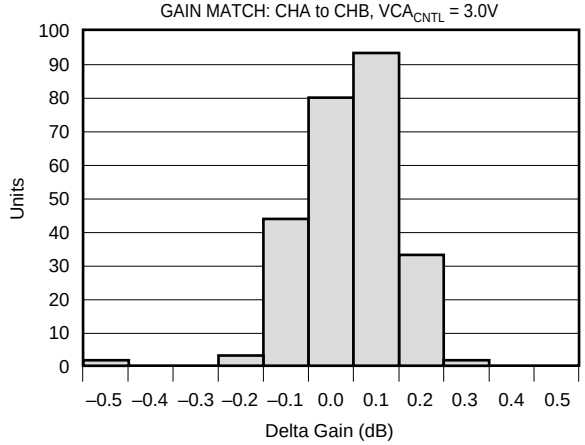
GAIN ERROR vs VCA_{CNTL}



GAIN MATCH: CHA to CHB, VCA_{CNTL} = 0.2V



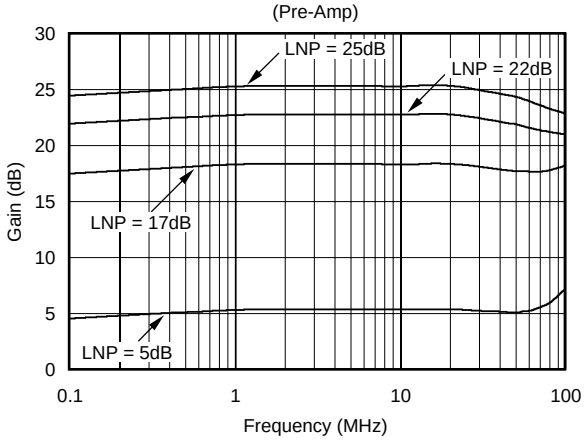
GAIN MATCH: CHA to CHB, VCA_{CNTL} = 3.0V



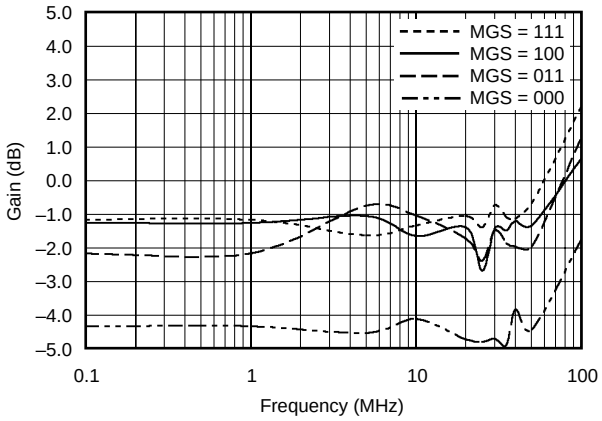
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DDA} = V_{DDB} = V_{DDR} = +5V, load resistance = 500Ω on each output to ground, MGS = 011, LNP = 22dB and f_{IN} = 5MHz, unless otherwise noted. The input to the preamp (LNP) is single-ended, and the output from the VCA is single-ended unless otherwise noted. This results in a 6dB reduction in signal amplitude compared to differential operation.

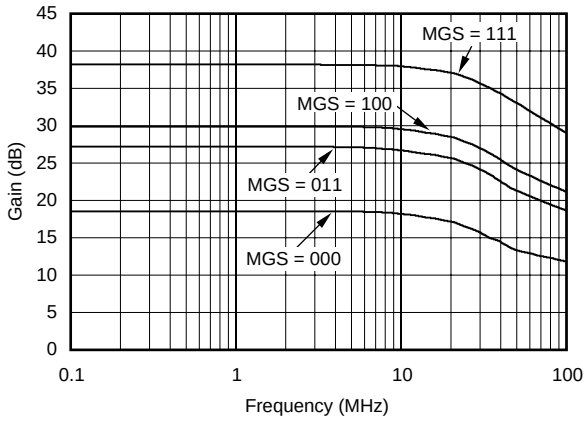
GAIN vs FREQUENCY
(Pre-Amp)



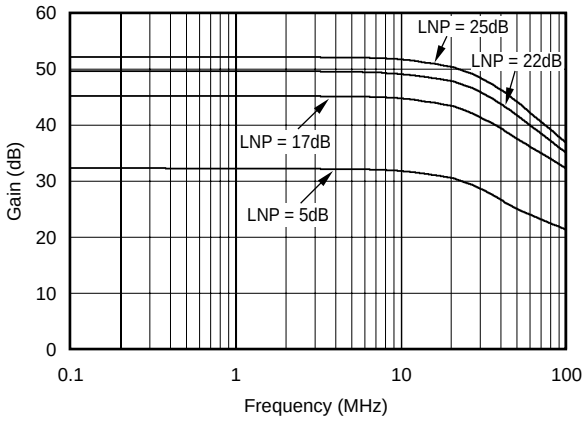
GAIN vs FREQUENCY
(VCA and PGA, VCA_{CNTL} = 0.2V)



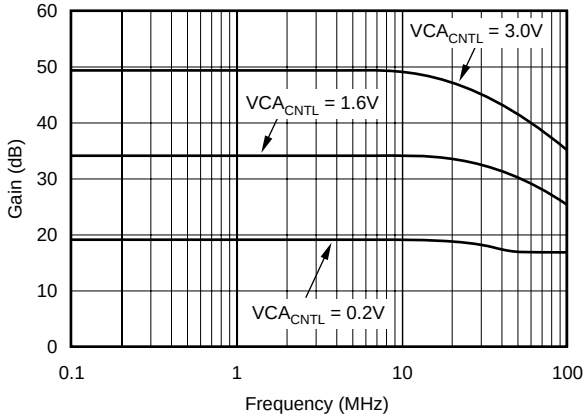
GAIN vs FREQUENCY
(VCA and PGA, VCA_{CNTL} = 3.0V)



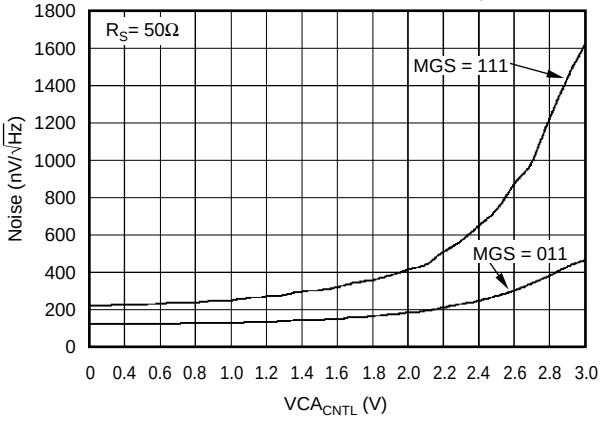
GAIN vs FREQUENCY
(VCA_{CNTL} = 3.0V)



GAIN vs FREQUENCY
(LNP = 22dB)



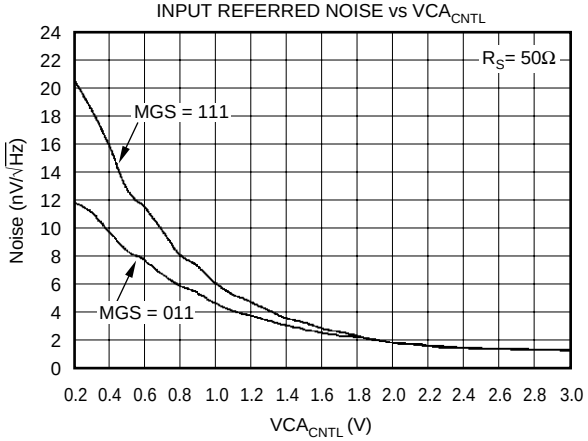
OUTPUT REFERRED NOISE vs VCA_{CNTL}



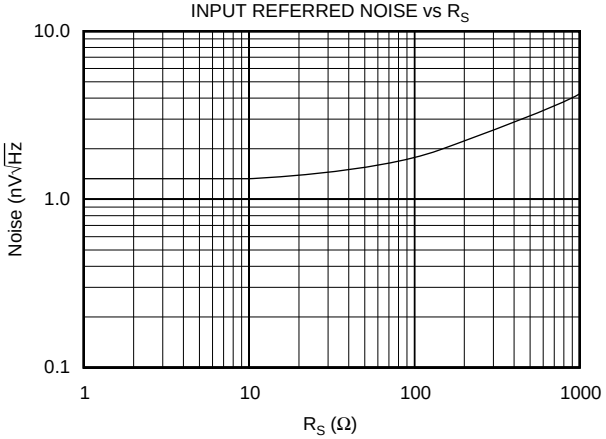
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DDA} = V_{DDB} = V_{DDR} = +5V, load resistance = 500Ω on each output to ground, MGS = 011, LNP = 22dB and f_{IN} = 5MHz, unless otherwise noted. The input to the preamp (LNP) is single-ended, and the output from the VCA is single-ended unless otherwise noted. This results in a 6dB reduction in signal amplitude compared to differential operation.

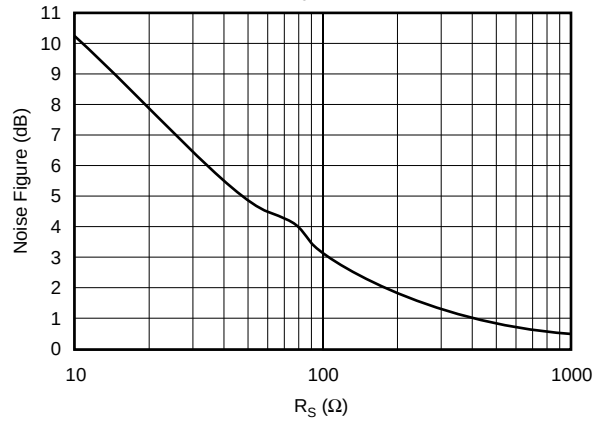
INPUT REFERRED NOISE vs VCA_{CNTL}



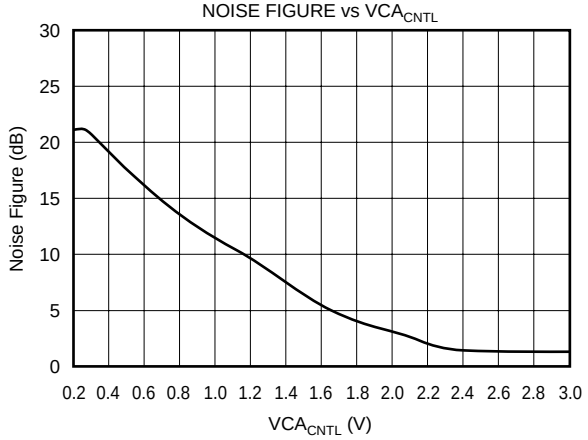
INPUT REFERRED NOISE vs R_S



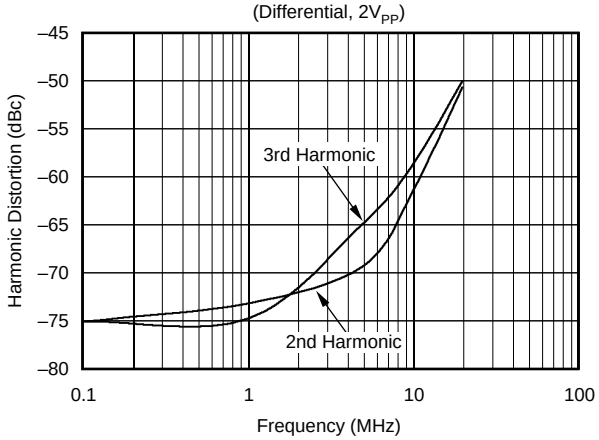
NOISE FIGURE vs R_S
(VCA_{CNTL} = 3.0V)



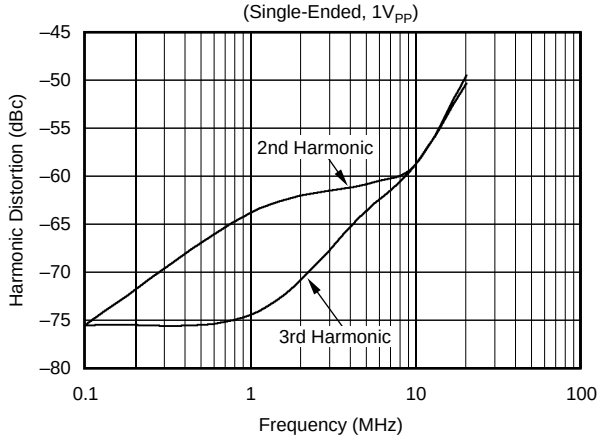
NOISE FIGURE vs VCA_{CNTL}



LNP vs FREQUENCY
(Differential, $2V_{PP}$)



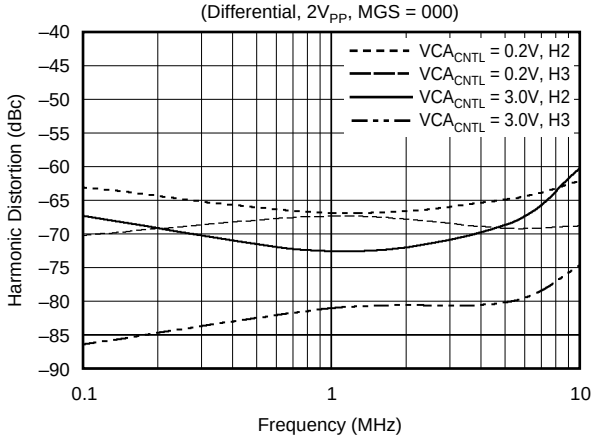
LNP vs FREQUENCY
(Single-Ended, $1V_{PP}$)



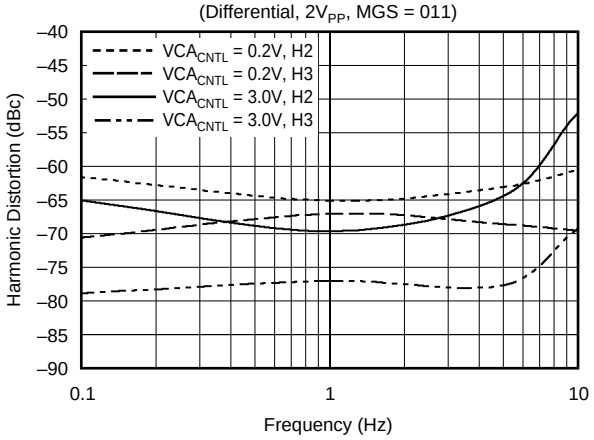
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DDA} = V_{DDB} = V_{DDR} = +5V, load resistance = 500Ω on each output to ground, MGS = 011, LNP = 22dB and f_{IN} = 5MHz, unless otherwise noted. The input to the preamp (LNP) is single-ended, and the output from the VCA is single-ended unless otherwise noted. This results in a 6dB reduction in signal amplitude compared to differential operation.

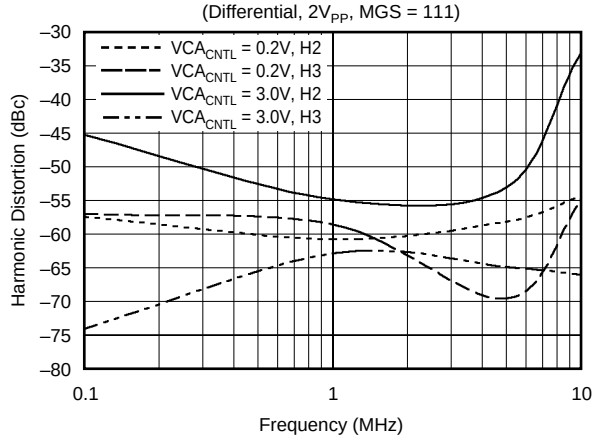
HARMONIC DISTORTION vs FREQUENCY
(Differential, $2V_{PP}$, MGS = 000)



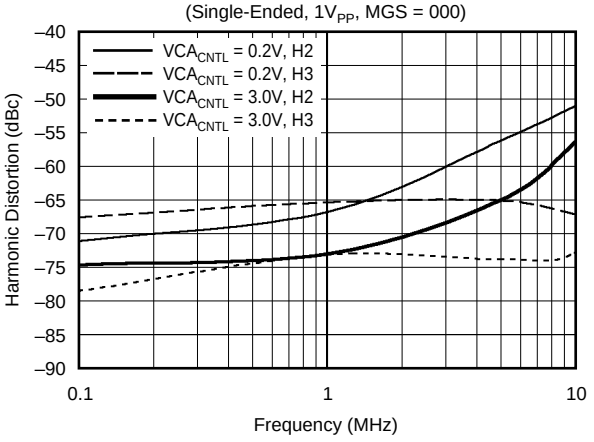
HARMONIC DISTORTION vs FREQUENCY
(Differential, $2V_{PP}$, MGS = 011)



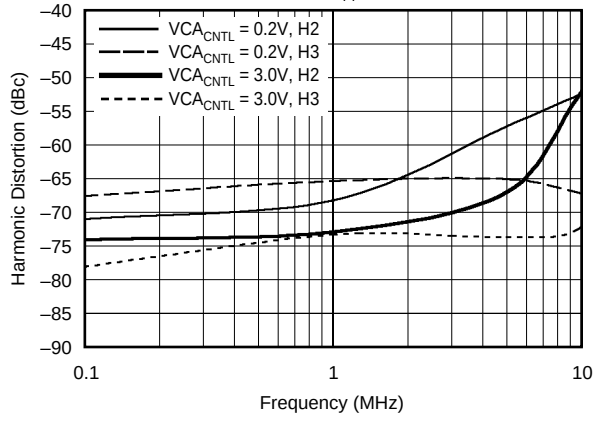
HARMONIC DISTORTION vs FREQUENCY
(Differential, $2V_{PP}$, MGS = 111)



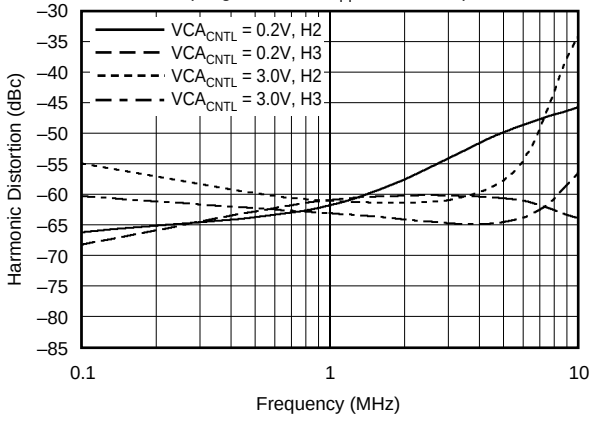
HARMONIC DISTORTION vs FREQUENCY
(Single-Ended, $1V_{PP}$, MGS = 000)



HARMONIC DISTORTION vs FREQUENCY
(Single-Ended, $1V_{PP}$, MGS = 011)



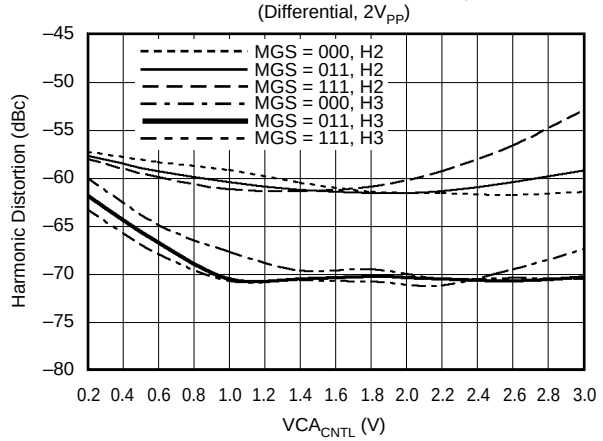
HARMONIC DISTORTION vs FREQUENCY
(Single-Ended, $1V_{PP}$, MGS = 111)



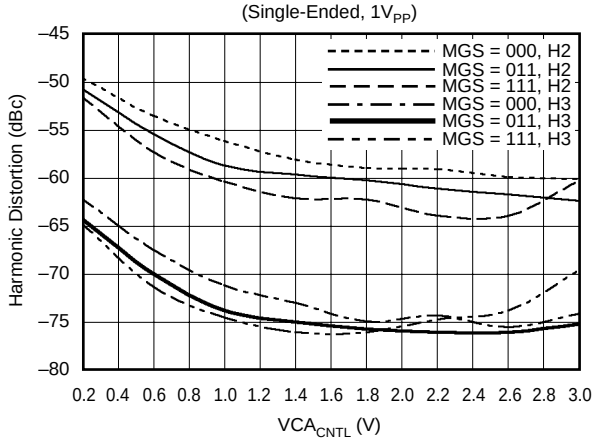
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DDA} = V_{DDB} = V_{DDR} = +5V, load resistance = 500Ω on each output to ground, MGS = 011, LNP = 22dB and f_{IN} = 5MHz, unless otherwise noted. The input to the preamp (LNP) is single-ended, and the output from the VCA is single-ended unless otherwise noted. This results in a 6dB reduction in signal amplitude compared to differential operation.

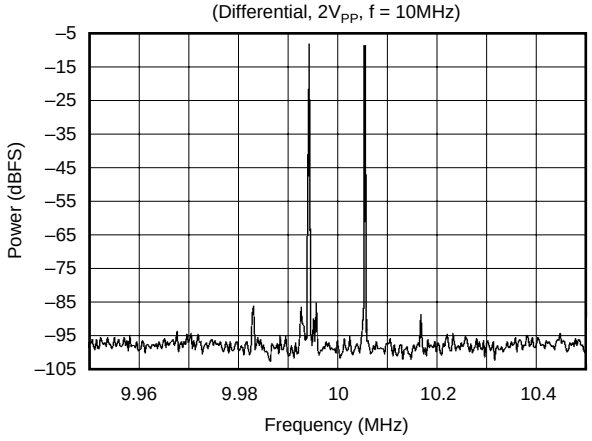
HARMONIC DISTORTION vs VCA_{CNTL}
(Differential, $2V_{PP}$)



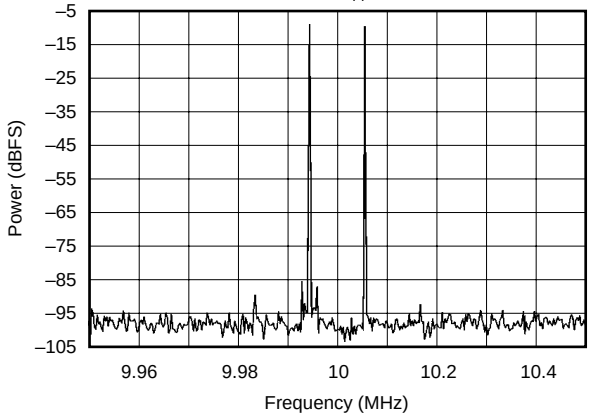
HARMONIC DISTORTION vs VCA_{CNTL}
(Single-Ended, $1V_{PP}$)



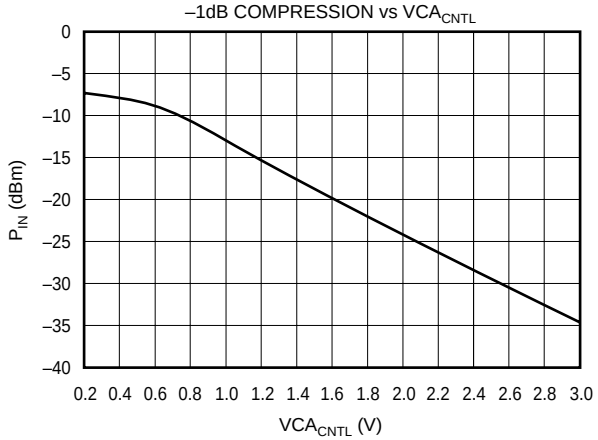
INTERMODULATION DISTORTION
(Differential, $2V_{PP}$, f = 10MHz)



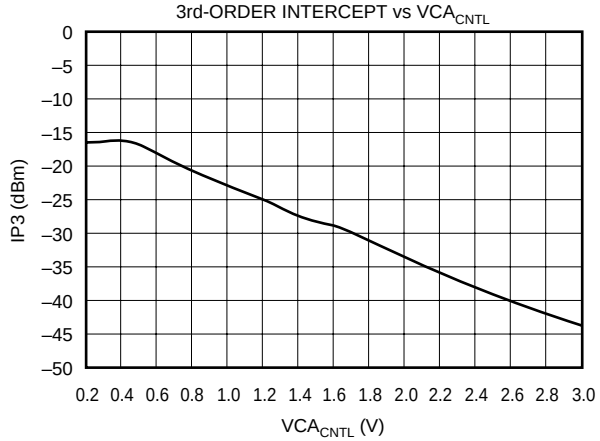
INTERMODULATION DISTORTION
(Single-Ended, $1V_{PP}$, f = 10MHz)



–1dB COMPRESSION vs VCA_{CNTL}



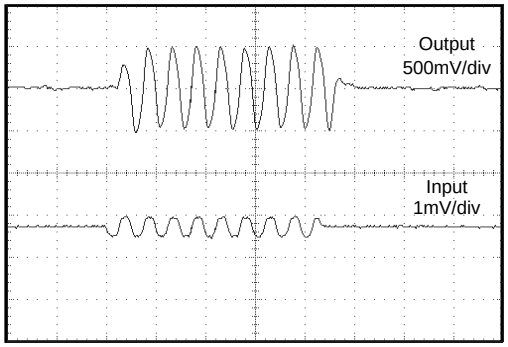
3rd-ORDER INTERCEPT vs VCA_{CNTL}



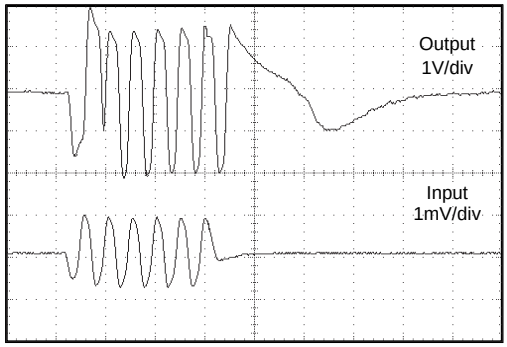
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DDA} = V_{DDB} = V_{DDR} = +5V, load resistance = 500Ω on each output to ground, MGS = 011, LNP = 22dB and f_{IN} = 5MHz, unless otherwise noted. The input to the preamp (LNP) is single-ended, and the output from the VCA is single-ended unless otherwise noted. This results in a 6dB reduction in signal amplitude compared to differential operation.

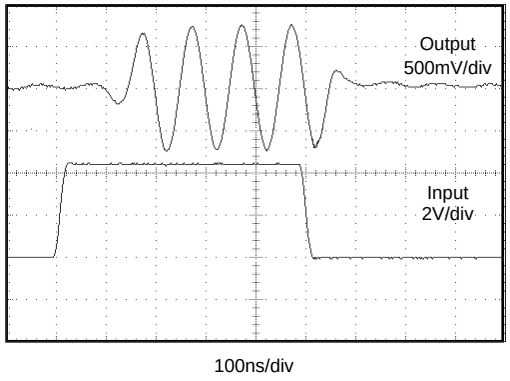
PULSE RESPONSE (BURSTS)
(Differential, VCA_{CNTL} = 3.0V, MGS = 111)



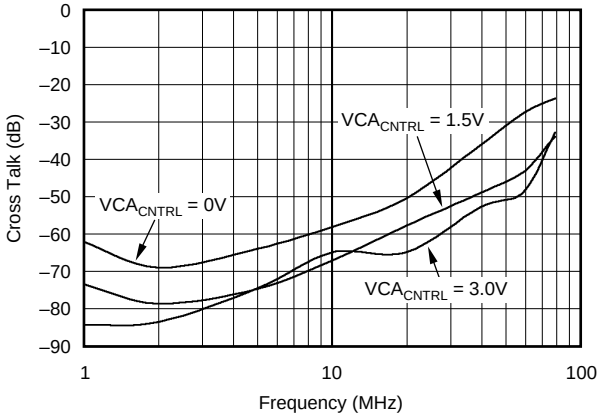
OVERLOAD RECOVERY
(Differential, VCA_{CNTL} = 3.0V, MGS = 111)



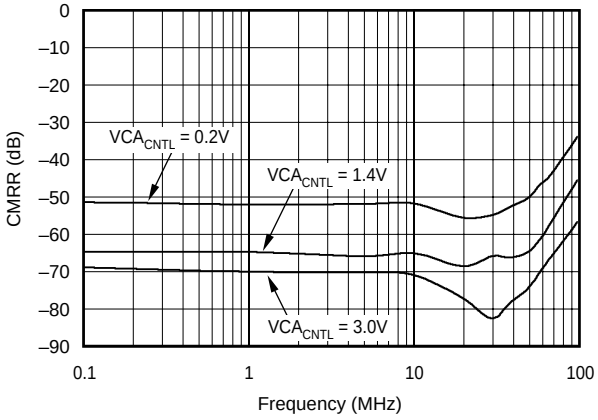
GAIN RESPONSE
(Differential, VCA_{CNTL} Pulsed, MGS = 111)



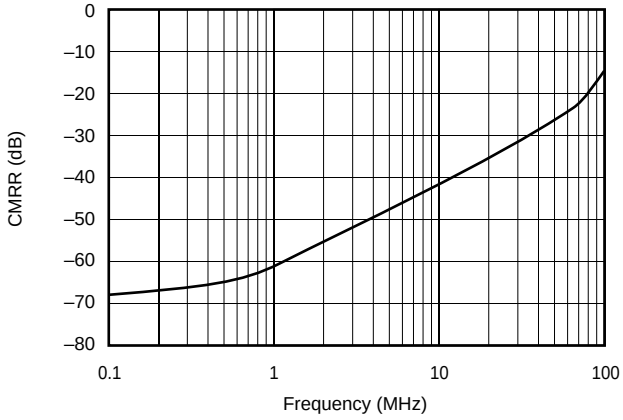
CROSS TALK vs FREQUENCY
(Single-Ended, 1Vp-p, MGS = 011)



CMRR vs FREQUENCY
(VCA only)



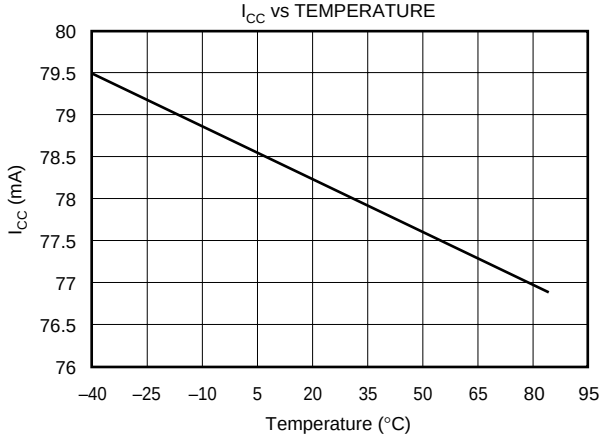
CMRR vs FREQUENCY
(LNP only)



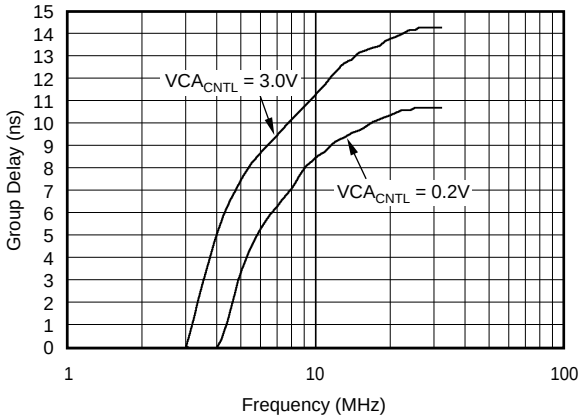
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DDA} = V_{DDB} = V_{DDR} = +5V, load resistance = 500Ω on each output to ground, MGS = 011, LNP = 22dB and f_{IN} = 5MHz, unless otherwise noted. The input to the preamp (LNP) is single-ended, and the output from the VCA is single-ended unless otherwise noted. This results in a 6dB reduction in signal amplitude compared to differential operation.

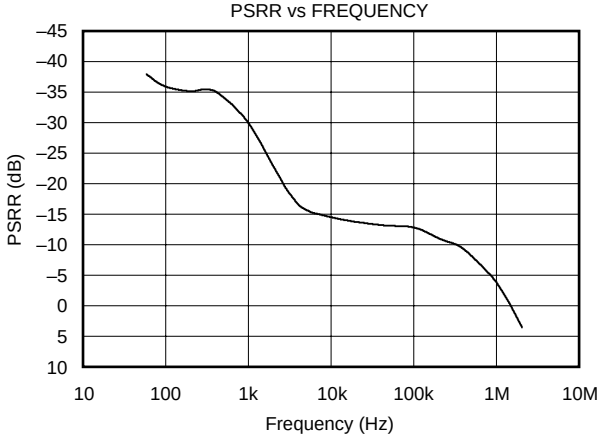
I_{CC} vs TEMPERATURE



GROUP DELAY vs FREQUENCY



PSRR vs FREQUENCY



THEORY OF OPERATION

The VCA2612 is a dual-channel system consisting of three primary blocks: a Low Noise Preamplifier (LNP), a Voltage Controlled Attenuator (VCA), and a Programmable Gain Amplifier (PGA). For greater system flexibility, an onboard multiplexer is provided for the VCA inputs, selecting either the LNP outputs or external signal inputs. Figure 1 shows a simplified block diagram of the dual-channel system.

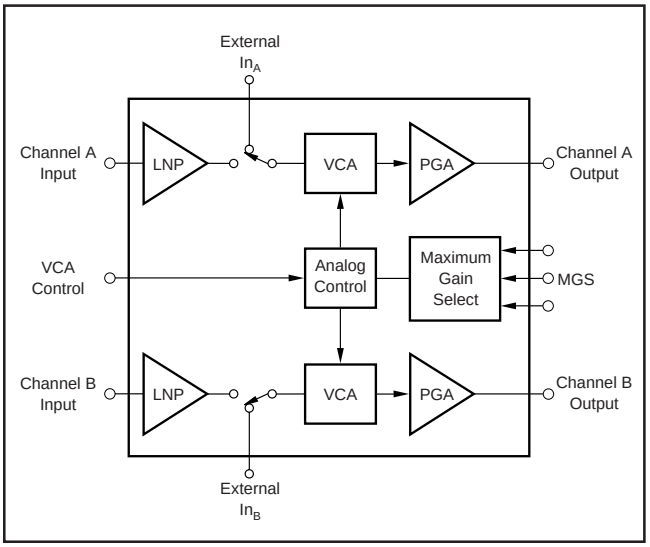


FIGURE 1. Simplified Block Diagram of the VCA2612.

LNP—OVERVIEW

The LNP input may be connected to provide active-feedback signal termination, achieving lower system noise performance than conventional passive shunt termination. Even lower noise performance is obtained if signal termination is not required. The unterminated LNP input impedance is 600kΩ. The LNP can process fully differential or single-ended signals in each channel. Differential signal processing results in significantly reduced 2nd-harmonic distortion and improved rejection of common-mode and power supply noise. The first gain stage of the LNP is AC-coupled into its output buffer with a 44µs time constant (3.6kHz high-pass characteristic). The buffered LNP outputs are designed to drive the succeeding VCA directly or, if desired, external loads as low as 135Ω with minimal impact on signal distortion. The LNP employs very low impedance local feedback to achieve stable gain with the lowest possible noise and distortion. Four pin-programmable gain settings are available: 5dB, 17dB, 22dB, and 25dB. Additional intermediate gains can be programmed by adding trim resistors between the Gain Strap programming pins.

The common-mode DC level at the LNP output is nominally 2.5V, matching the input common-mode requirement of the VCA for simple direct coupling. When external signals are fed to the VCA, they should also be set up with a 2.5VDC common-mode level. Figure 2 shows a circuit that demonstrates the recommended coupling method using an external op amp. The V_{CM} node shown in the drawing is the V_{CM} output (pin 19). Typical R and C values are shown, yielding a high-pass time constant similar to that of the LNP. If a different common-mode referencing method is used, it is important that the common-mode level be within 10mV of the V_{CM} output for proper operation.

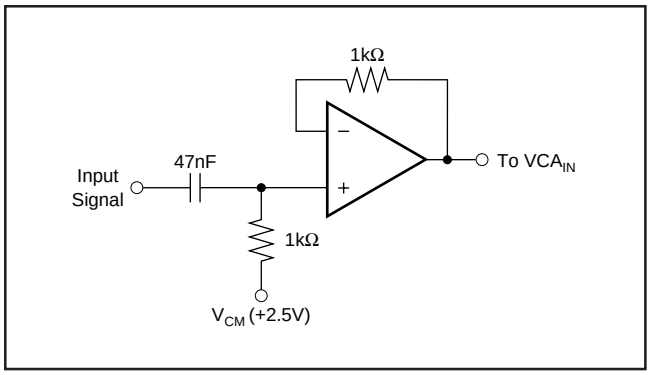


FIGURE 2. Recommended Circuit for Coupling an External Signal into the VCA Inputs.

VCA—OVERVIEW

The magnitude of the differential VCA input signal (from the LNP or an external source) is reduced by a programmable attenuation factor, set by the analog VCA Control Voltage (VCA_{CNTL}) at pin 43. The maximum attenuation factor is further programmable by using the three MGS bits (pins 40-42). Figure 3 illustrates this dual-adjustable characteristic. Internally, the signal is attenuated by having the analog VCA_{CNTL} vary the channel resistance of a set of shunt-connected FET transistors. The MGS bits effectively adjust the overall size of the shunt FET by switching parallel components in or out under logic control. At any given maximum gain setting, the analog variable gain characteristic is linear in dB as a function of the control voltage, and is created as a piecewise approximation of an ideal dB-linear transfer function. The VCA gain control circuitry is common to both channels of the VCA2612.

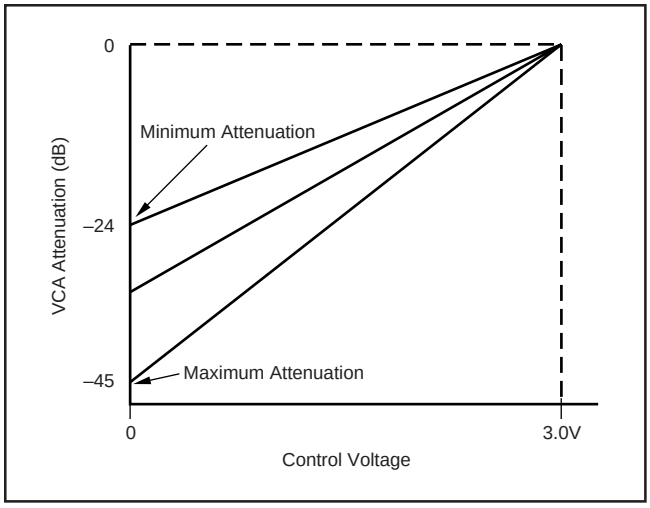


FIGURE 3. Swept Attenuator Characteristic.

PGA OVERVIEW AND OVERALL DEVICE CHARACTERISTICS

The differential output of the VCA attenuator is then amplified by the PGA circuit block. This post-amplifier is programmed by the same MGS bits that control the VCA attenuator, yielding an overall swept-gain amplifier characteristic in which the VCA • PGA gain varies from 0dB (unity) to a programmable peak gain of 24dB, 27dB, 30dB, 33dB, 36dB, 39dB, 42dB, or 45dB.

The *GAIN vs VCA$_{CNTL}$* curve on page 4 shows the composite gain control characteristic of the entire VCA2612. Setting VCA$_{CNTL}$ to 3.0V causes the digital MGS gain control to step in 3dB increments. Setting VCA$_{CNTL}$ to 0V causes all the MGS-controlled gain curves to converge at one point. The gain at the convergence point is the LNP gain less 6dB, because the measurement setup looks at only one side of the differential PGA output, resulting in 6dB lower signal amplitude.

ADDITIONAL FEATURES—OVERVIEW

Overload protection stages are placed between the attenuator and the PGA, providing a symmetrically clipped output whenever the input becomes large enough to overload the PGA. A comparator senses the overload signal amplitude and substitutes a fixed DC level to prevent undesirable overload recovery effects. As with the previous stages, the VCA is AC-coupled into the PGA. In this case, the coupling time constant varies from 5µs at the highest gain (45dB) to 59µs at the lowest gain (25dB).

The VCA2612 includes a built-in reference, common to both channels, to supply a regulated voltage for critical areas of the circuit. This reduces the susceptibility to power supply variation, ripple, and noise. In addition, separate power supply and ground connections are provided for each channel and for the reference circuitry, further reducing interchannel cross-talk.

Further details regarding the design, operation and use of each circuit block are provided in the following sections.

LOW NOISE PREAMPLIFIER (LNP)—DETAIL

The LNP is designed to achieve a low noise figure, especially when employing active termination. Figure 4 is a simplified schematic of the LNP, illustrating the differential input and output capability. The input stage employs low resistance local feedback to achieve stable low noise, low distortion performance with very high input impedance. Normally, low noise circuits exhibit high power consumption due to the large bias currents required in both input and output stages. The LNP uses a patented technique that combines the input and output stages such that they share the same bias current. Transistors Q_4 and Q_5 amplify the signal at the gate-source input of Q_4, the +IN side of the LNP. The signal is further amplified by the Q_1 and Q_2 stage, and then by the final Q_3 and R_L gain stage, which uses the same bias current as the input devices Q_4 and Q_5. Devices Q_6 through Q_{10} play the same role for signals on the –IN side.

The differential gain of the LNP is given in Equation (1):

$$\text{Gain} = 2 \bullet \left[\frac{R_L}{R_S} \right] \quad (1)$$

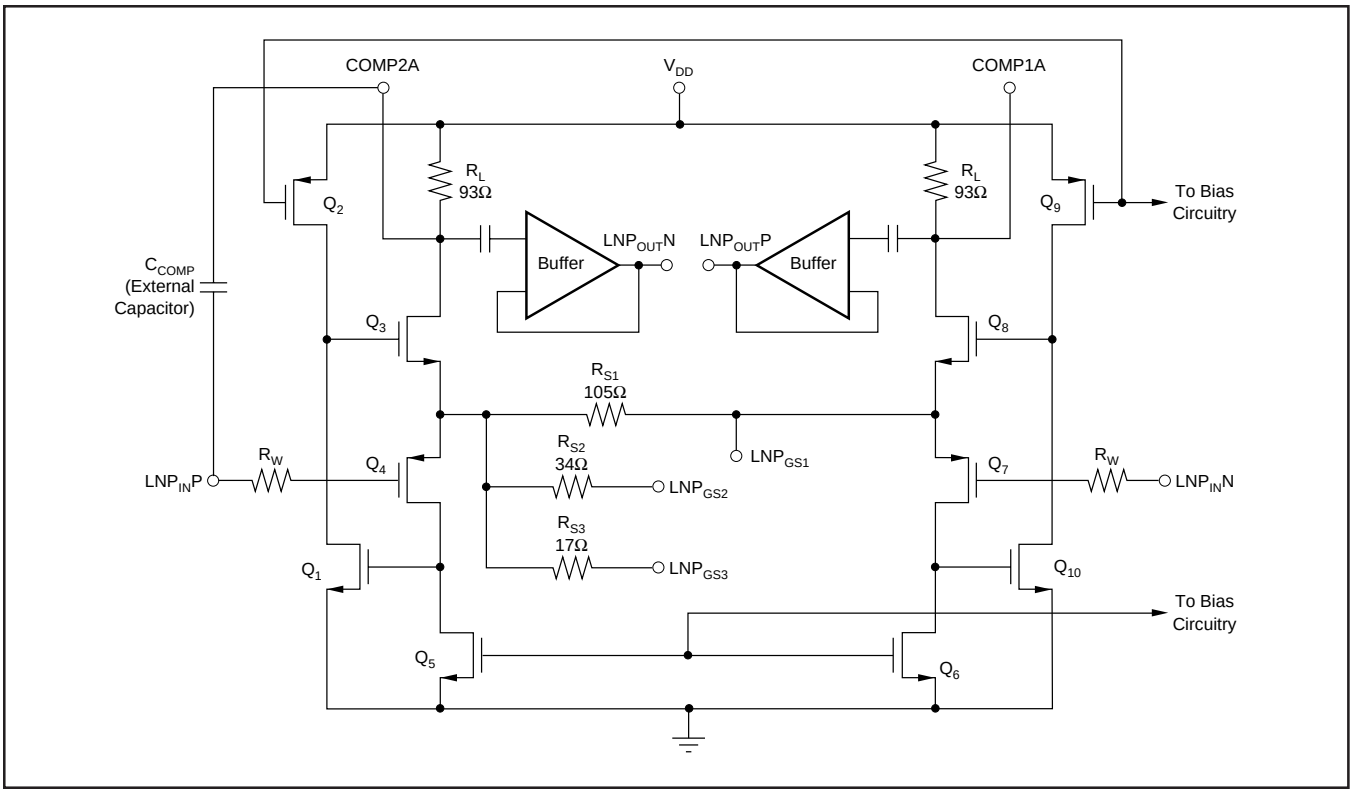


FIGURE 4. Schematic of the Low Noise Preamplifier (LNP).

where R_L is the load resistor in the drains of Q_3 and Q_8, and R_S is the resistor connected between the sources of the input transistors Q_4 and Q_7. The connections for various R_S combinations are brought out to device pins $LNPG_{S1}$, $LNPG_{S2}$, and $LNPG_{S3}$ (pins 13-15 for channel A, 22-24 for channel B). These Gain Strap pins allow the user to establish one of four fixed LNP gain options as shown in Table I.

LNP PIN STRAPPING	LNP GAIN (dB)
$LNPG_{S1}$, $LNPG_{S2}$, $LNPG_{S3}$ Connected Together	25
$LNPG_{S1}$ Connected to $LNPG_{S3}$	22
$LNPG_{S1}$ Connected to $LNPG_{S2}$	17
All Pins Open	5

TABLE I. Pin Strappings of the LNP for Various Gains.

It is also possible to create other gain settings by connecting an external resistor between $LNPG_{S1}$ on one side, and $LNPG_{S2}$ and/or $LNPG_{S3}$ on the other. In that case, the internal resistor values shown in Figure 4 should be combined with the external resistor to calculate the effective value of R_S for use in Equation (1). The resulting expression for external resistor value is given in Equation (2).

$$R_{EXT} = \frac{2R_{S1}R_L + 2R_{FIX}R_L - Gain \bullet R_{S1}R_{FIX}}{Gain \bullet R_{S1} - 2R_L} \qquad (2)$$

where R_{EXT} is the externally selected resistor value needed to achieve the desired gain setting, R_{S1} is the fixed parallel resistor in Figure 4, and R_{FIX} is the effective fixed value of the remaining internal resistors: R_{S2}, R_{S3}, or (R_{S2} || R_{S3}) depending on the pin connections.

Note that the best process and temperature stability will be achieved by using the pre-programmed fixed gain options of Table I, since the gain is then set entirely by internal resistor ratios, which are typically accurate to ±0.5%, and track quite well over process and temperature. When combining external resistors with the internal values to create an effective R_S value, note that the internal resistors have a typical temperature coefficient of +700ppm/°C and an absolute value tolerance of approximately ±5%, yielding somewhat less predictable and stable gain settings. With or without external resistors, the board layout should use short Gain Strap connections to minimize parasitic resistance and inductance effects.

The overall noise performance of the VCA2612 will vary as a function of gain. Table II shows the typical input- and output-referred noise densities of the entire VCA2612 for maximum VCA and PGA gain; i.e., VCA_{CNTL} set to 3.0V and all MGS bits set to *1*. Note that the input-referred noise values include the contribution of a 50Ω fixed source impedance, and are therefore somewhat larger than the intrinsic input noise. As the LNP gain is reduced, the noise contribution from the VCA/PGA portion becomes more significant, resulting in higher input-referred noise. However, the output-referred noise, which is indicative of the overall SNR at that gain setting, is reduced.

To preserve the low noise performance of the LNP, the user should take care to minimize resistance in the input lead. A parasitic resistance of only 10Ω will contribute 0.4nV/$\sqrt{Hz}$.

	NOISE (nV/$\sqrt{Hz}$)	
LNP GAIN (dB)	Input-Referred	Output-Referred
25	1.54	2260
22	1.59	1650
17	1.82	1060
5	4.07	597

TABLE II. Noise Performance for MGS = 111 and VCA_{CNTL} = 3.0V.

The LNP is capable of generating a $2V_{PP}$ differential signal. The maximum signal at the LNP input is therefore $2V_{PP}$ divided by the LNP gain. An input signal greater than this would exceed the linear range of the LNP, an especially important consideration at low LNP gain settings.

ACTIVE FEEDBACK WITH THE LNP

One of the key features of the LNP architecture is the ability to employ active-feedback termination to achieve superior noise performance. Active feedback termination achieves a lower noise figure than conventional shunt termination, essentially because no signal current is wasted in the termination resistor itself. Another way to understand this is as follows: Consider first that the input source, at the far end of the signal cable has a cable-matching source resistance of R_S. Using conventional shunt termination at the LNP input, a second terminating resistor of value R_S is connected to ground. Therefore, the signal loss is 6dB due to the voltage divider action of the series and shunt R_S resistors. The effective source resistance has been reduced by the same factor of 2, but the noise contribution has been reduced by only the $\sqrt{2}$, only a 3dB reduction. Therefore, the net theoretical SNR degradation is 3dB, assuming a noise-free amplifier input. (In practice, the amplifier noise contribution will degrade both the unterminated and the terminated noise figures, somewhat reducing the distinction between them.)

See Figure 5 for an amplifier using active feedback. This diagram appears very similar to a traditional inverting amplifier. However, the analysis is somewhat different because the gain *A* in this case is not a very large open-loop op amp gain; rather, it is the relatively low and controlled gain of the LNP itself. Thus, the impedance at the inverting amplifier terminal will be reduced by a finite amount, as given in the familiar relationship of Equation (3):

$$R_{IN} = \frac{R_F}{(1+A)} \qquad (3)$$

where R_F is the feedback resistor (supplied externally between the $LNP_{IN}P$ and FB terminals for each channel), A is the user-selected gain of the LNP, and R_{IN} is the resulting amplifier input impedance with active feedback. In this case, unlike the conventional termination above, both the signal voltage and the R_S noise are attenuated by the same factor

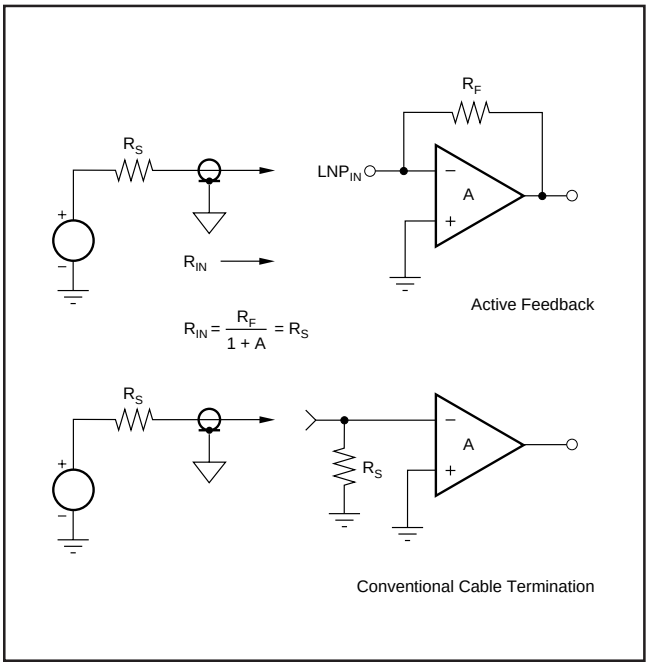


FIGURE 5. Configurations for Active Feedback and Conventional Cable Termination.

of two (6dB) before being re-amplified by the *A* gain setting. This avoids the extra 3dB degradation due to the square-root effect described above, the key advantage of the active termination technique.

As mentioned above, the previous explanation ignored the input noise contribution of the LNP itself. Also, the noise contribution of the feedback resistor must be included for a completely correct analysis. The curves given in Figures 6 and 7 allow the VCA2612 user to compare the achievable noise figure for active and conventional termination methods. The left-most set of data points in each graph give the results for typical 50Ω cable termination, showing the worst noise figure but also the greatest advantage of the active feedback method.

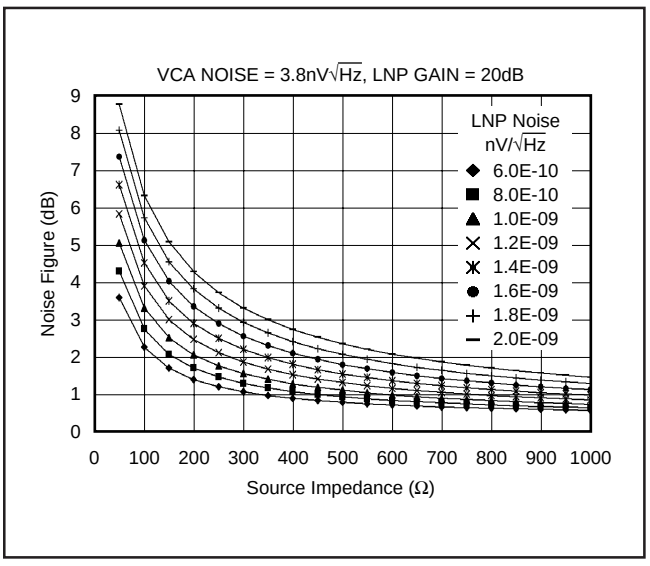


FIGURE 6. Noise Figure for Active Termination.

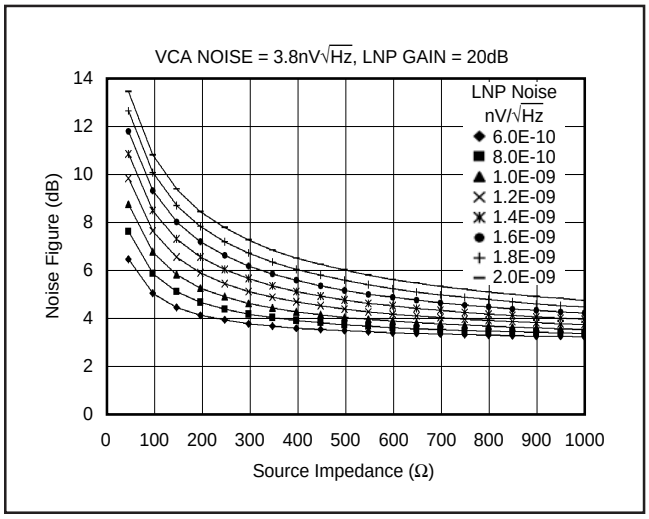


FIGURE 7. Noise Figure for Conventional Termination.

A switch, controlled by the $FBSW_{CNTL}$ signal on pin 45, enables the user to reduce the feedback resistance by adding an additional parallel component, connected between the $LNP_{IN}P$ and SWFB terminals. The two different values of feedback resistance will result in two different values of active-feedback input resistance. Thus, the active-feedback impedance can be optimized at two different LNP gain settings. The switch is connected at the buffered output of the LNP and has an *ON* resistance of approximately 1Ω.

When employing active feedback, the user should be careful to avoid low-frequency instability or overload problems. Figure 8 illustrates the various low-frequency time constants. Referring again to the input resistance calculation of Equation (3), and considering that the gain term *A* falls off below 3.6kHz, it is evident that the effective LNP input impedance will rise below 3.6kHz, with a DC limit of approximately R_F. To avoid interaction with the feedback pole/zero at low frequencies, and to avoid the higher signal levels resulting from the rising impedance characteristic, it is recommended that the external R_FC_C time constant be set to about 5µs.

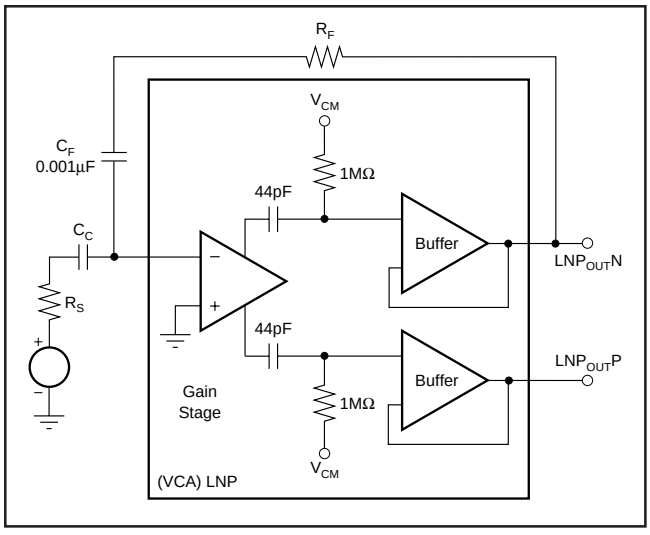


FIGURE 8. Low Frequency LNP Time Constants.

Achieving the best active feedback architecture is difficult with conventional op amp circuit structures. The overall gain *A* must be negative in order to close the feedback loop, the input impedance must be high to maintain low current noise and good gain accuracy, but the gain ratio must be set with very low value resistors to maintain good voltage noise. Using a two-amplifier configuration (noninverting for high impedance plus inverting for negative feedback reasons) results in excessive phase lag and stability problems when the loop is closed. The VCA2612 uses a patented architecture that achieves these requirements, with the additional benefits of low power dissipation and differential signal handling at both input and output.

For greatest flexibility and lowest noise, the user may wish to shape the frequency response of the LNP. The COMP1 and COMP2 pins for each channel (pins 10 and 11 for channel A, pins 26 and 27 for channel B) correspond to the drains of Q_3 and Q_8 in Figure 4. A capacitor placed between these pins will create a single-pole low-pass response, in which the effective *R* of the *RC* time constant is approximately 186Ω.

COMPENSATION WHEN USING ACTIVE FEEDBACK

The typical open-loop gain versus frequency characteristic for the LNP is shown in Figure 9. The –3dB bandwidth is approximately 180MHz and the phase response is such that when feedback is applied the LNP will exhibit a peaked response or might even oscillate. One method for compensating for this undesirable behavior is to place a compensation capacitor at the input to the LNP, as shown in Figure 10. This method is effective when the desired –3dB bandwidth is much less than the open-loop bandwidth of the LNP. This compensation technique also allows the total compensation capacitor to include any stray or cable capacitance that is associated with the input connection. Equation 4 relates the bandwidth to the various impedances that are connected to the LNP.

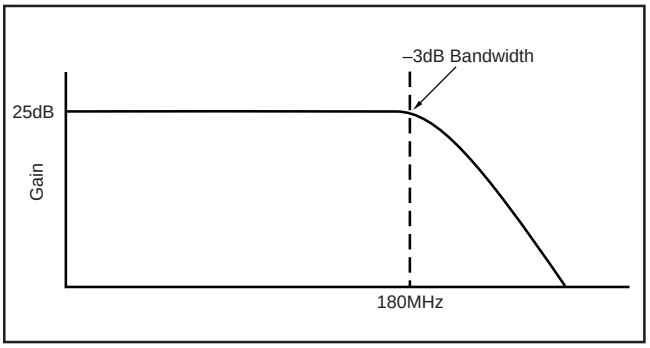


FIGURE 9. Open-Loop Gain Characteristic of LNP.

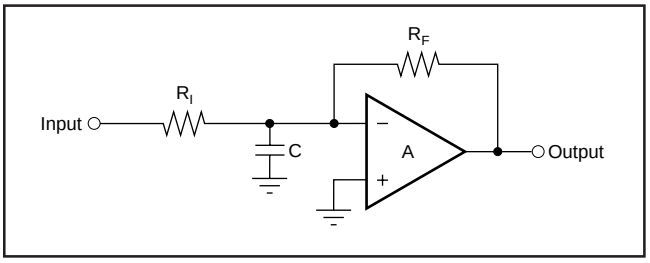


FIGURE 10. LNP with Compensation Capacitor.

$$BW = \frac{(A+1)R_I + R_F}{2pC(R_I)(R_F)} \quad (4)$$

LNP OUTPUT BUFFER

The differential LNP output is buffered by wideband class AB voltage followers which are designed to drive low impedance loads. This is necessary to maintain LNP gain accuracy, since the VCA input exhibits gain-dependent input impedance. The buffers are also useful when the LNP output is brought out to drive external filters or other signal processing circuitry. Good distortion performance is maintained with buffer loads as low as 135Ω. As mentioned previously, the buffer inputs are AC-coupled to the LNP outputs with a 3.6kHz high-pass characteristic, and the DC common-mode level is maintained at the correct V_{CM} for compatibility with the VCA input.

VOLTAGE-CONTROLLED ATTENUATOR (VCA)—DETAIL

The VCA is designed to have a *dB-linear* attenuation characteristic, i.e. the gain loss in dB is constant for each equal increment of the VCA_{CNTL} control voltage. See Figure 11 for a diagram of the VCA. The attenuator is essentially a variable voltage divider consisting of one series input resistor, R_S, and ten identical shunt FETs, placed in parallel and controlled by sequentially activated clipping amplifiers. Each clipping amplifier can be thought of as a specialized voltage comparator with a *soft* transfer characteristic and well-controlled output limit voltages. The reference voltages V1 through V10 are equally spaced over the 0V to 3.0V control voltage range. As the control voltage rises through the input range of each clipping amplifier, the amplifier output will rise from 0V (FET completely *ON*) to $V_{CM} – V_T$ (FET nearly *OFF*), where V_{CM} is the common source voltage and V_T is the threshold voltage of the FET. As each FET approaches its *OFF* state and the control voltage continues to rise, the next clipping amplifier/FET combination takes over for the next portion of the piecewise-linear attenuation characteristic. Thus, low control voltages have most of the FETs turned *ON*, while high control voltages have most turned *OFF*. Each FET acts to decrease the shunt resistance of the voltage divider formed by R_S and the parallel FET network.

The attenuator is comprised of two sections, with five parallel clipping amplifier/FET combinations in each. Special reference circuitry is provided so that the ($V_{CM} – V_T$) limit voltage will track temperature and IC process variations, minimizing the effects on the attenuator control characteristic.

In addition to the analog VCA_{CNTL} gain setting input, the attenuator architecture provides digitally programmable adjustment in eight steps, via the three Maximum Gain Setting (MGS) bits. These adjust the maximum achievable gain

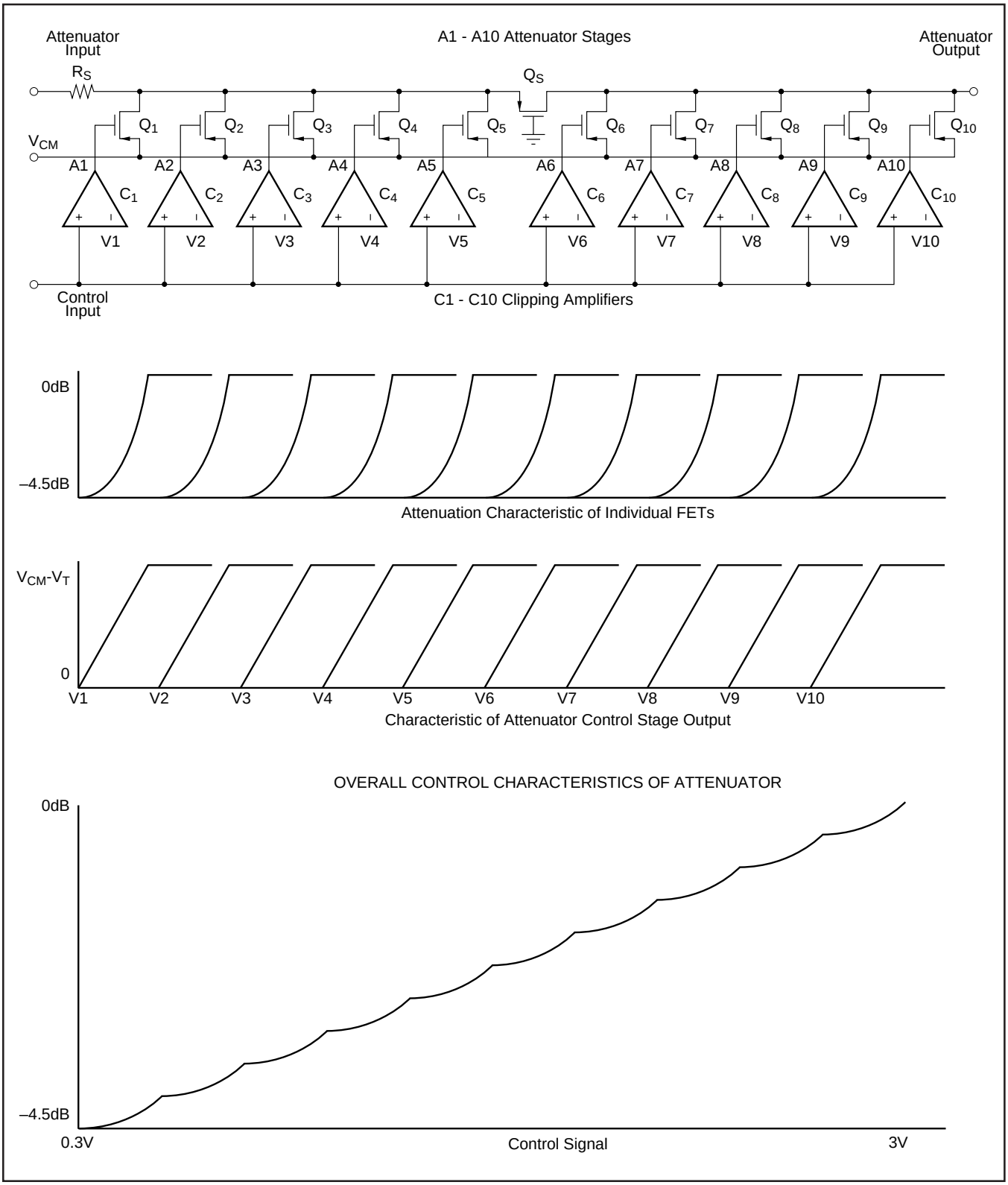


FIGURE 11. Piecewise Approximation to Logarithmic Control Characteristics.

(corresponding to minimum attenuation in the VCA, with VCA_{CNTL} = 3.0V) in 3dB increments. This function is accomplished by providing multiple FET sub-elements for each of the Q_1 to Q_{10} FET shunt elements shown in Figure 11. In the simplified diagram of Figure 12, each shunt FET is shown as two sub-elements, Q_{NA} and Q_{NB}. Selector switches, driven by the MGS bits, activate either or both of the sub-element FETs to adjust the maximum R_{ON} and thus achieve the stepped attenuation options.

The VCA can be used to process either differential or single-ended signals. Fully differential operation will reduce 2nd-harmonic distortion by about 10dB for full-scale signals.

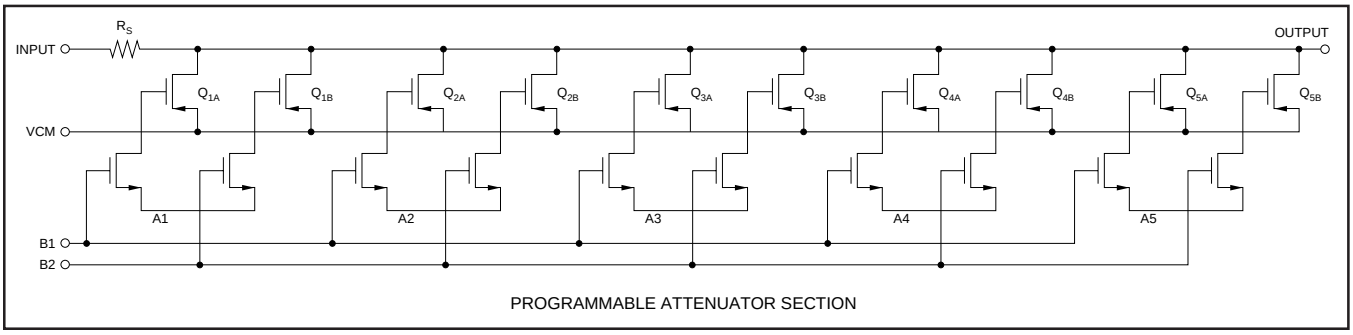


FIGURE 12. Programmable Attenuator Section.

Input impedance of the VCA will vary with gain setting, due to the changing resistances of the programmable voltage divider structure. At large attenuation factors (i.e., low gain settings), the impedance will approach the series resistor value of approximately 135Ω.

As with the LNP stage, the VCA output is AC-coupled into the PGA. This means that the attenuation-dependent DC common-mode voltage will not propagate into the PGA, and so the PGA's DC output level will remain constant.

Finally, note that the VCA_{CNTL} input consists of FET gate inputs. This provides very high impedance and ensures that multiple VCA2612 devices may be connected in parallel in with no significant loading effects. The nominal voltage range for the VCA_{CNTL} input spans from 0V to 3V. Over driving this input (≤ 5V) does not affect the performance.

OVERLOAD RECOVERY CIRCUITRY—DETAIL

With a maximum overall gain of 70dB, the VCA2612 is prone to signal overloading. Such a condition may occur in either the LNP or the PGA depending on the various gain and attenuation settings available. The LNP is designed to produce low-distortion outputs as large as $1V_{PP}$ single-ended ($2V_{PP}$ differential). Therefore the maximum input signal for linear operation is $2V_{PP}$ divided by the LNP differential gain setting. Clamping circuits in the LNP ensure that larger input amplitudes will exhibit symmetrical clipping and short recovery times. The VCA itself, being basically a voltage divider, is intrinsically free of overload conditions. However, the PGA post-amplifier is vulnerable to sudden overload, particularly at high gain settings. Rapid overload recovery is essential in many signal processing applications such as ultrasound imaging. A special comparator circuit is provided at the PGA input which detects overrange signals (detection level dependent on PGA gain setting). When the signal exceeds the comparator input threshold, the VCA output is blocked and an appropriate fixed DC level is substituted, providing fast and clean overload recovery. The basic architecture is shown in Figure 13. Both high and low overrange conditions are sensed and corrected by this circuit.

Figures 14 and 15 show typical overload recovery waveforms with MGS = 100, for VCA + PGA minimum gain (0dB) and maximum gain (36dB), respectively. LNP gain is set to 25dB in both cases.

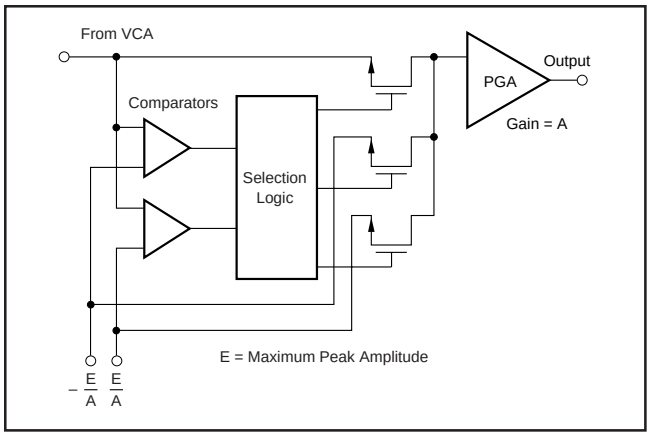


FIGURE 13. Overload Protection Circuitry.

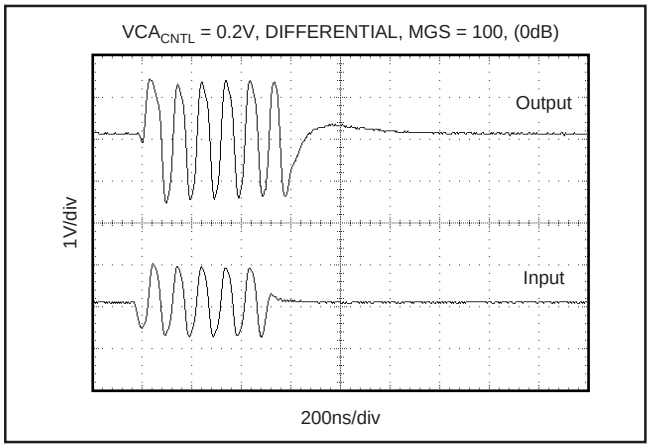


FIGURE 14. Overload Recovery Response For Minimum Gain.

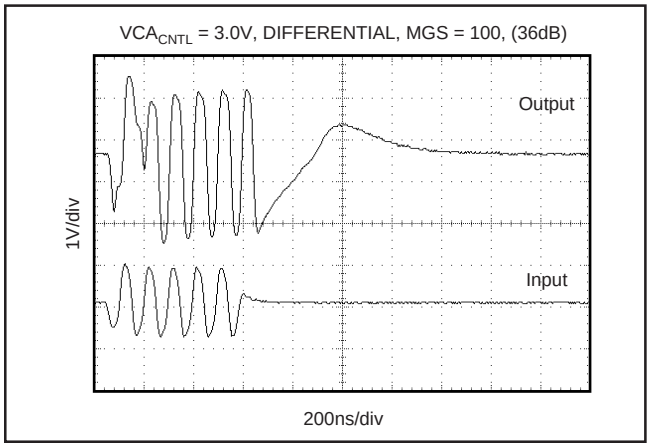


FIGURE 15. Overload Recovery Response For Maximum Gain.

INPUT OVERLOAD RECOVERY

One of the most important applications for the VCA2612 is processing signals in an ultrasound system. The ultrasound signal flow begins when a large signal is applied to a transducer, which converts electrical energy to acoustic energy. It is not uncommon for the amplitude of the electrical signal that is applied to the transducer to be ±50V or greater. To prevent damage, it is necessary to place a protection circuit between the transducer and the VCA2612, as shown in Figure 16. Care must be taken to prevent any signal from turning the ESD diodes on. Turning on the ESD diodes inside the VCA2612 could cause the input coupling capacitor (C_C) to charge to the wrong value.

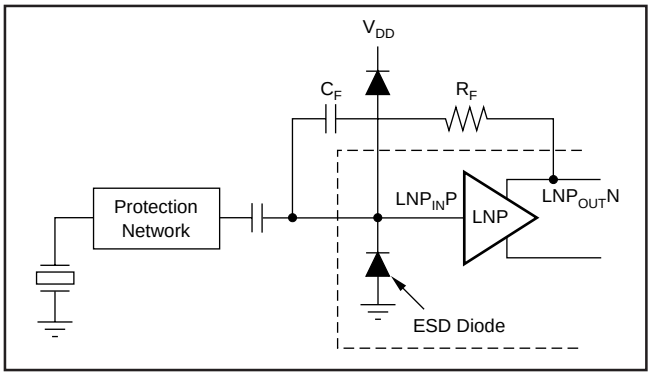


FIGURE 16. VCA2612 Diode Bridge Protection Circuit.

PGA POST-AMPLIFIER—DETAIL

Figure 17 shows a simplified circuit diagram of the PGA block. As described previously, the PGA gain is programmed with the same MGS bits which control the VCA maximum attenuation factor. Specifically, the PGA gain at each MGS setting is the inverse (reciprocal) of the maximum VCA attenuation at that setting. Therefore, the VCA + PGA overall gain will always be 0dB (unity) when the analog VCA_{CNTL} input is set to 0V (= maximum attenuation). For VCA_{CNTL} = 3V (no attenuation), the VCA + PGA gain will be controlled by the programmed PGA gain (24dB to 45dB in 3dB steps).

For clarity, the gain and attenuation factors are detailed in Table III.

MGS SETTING	ATTENUATOR GAIN VCA_{CNTL} = 0V to 3V	DIFFERENTIAL PGA GAIN	ATTENUATOR + DIFF. PGA GAIN
000	–24dB to 0dB	24dB	0dB to 24dB
001	–27dB to 0dB	27dB	0dB to 27dB
010	–30dB to 0dB	30dB	0dB to 30dB
011	–33dB to 0dB	33dB	0dB to 33dB
100	–36dB to 0dB	36dB	0dB to 36dB
101	–39dB to 0dB	39dB	0dB to 39dB
110	–42dB to 0dB	42dB	0dB to 42dB
111	–45dB to 0dB	45dB	0dB to 45dB

TABLE III. MGS Settings.

The PGA architecture consists of a differential, programmable-gain voltage to current converter stage followed by transimpedance amplifiers to create and buffer each side of the differential output. The circuitry associated with the voltage to current converter is similar to that previously described for the LNP, with the addition of eight selectable PGA gain-setting resistor combinations (controlled by the MGS bits) in place of the fixed resistor network used in the LNP. Low input noise is also a requirement of the PGA design due to the large amount of signal attenuation which can be inserted between the LNP and the PGA. At minimum VCA attenuation (used for small input signals) the LNP noise dominates; at maximum VCA attenuation (large input signals) the PGA noise dominates. Note that if the PGA output is used single-ended, the apparent gain will be 6dB lower.

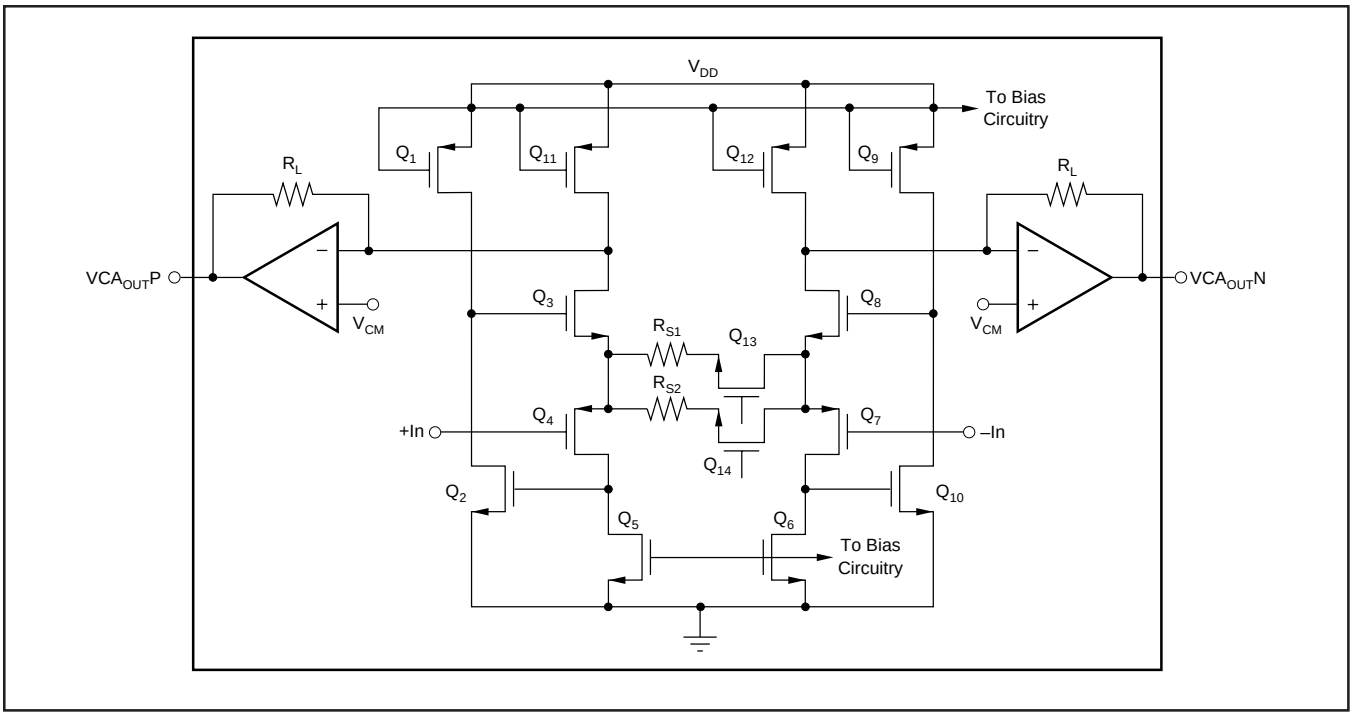


FIGURE 17. Simplified Block Diagram of the PGA Section Within the VCA2612.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VCA2612Y/250	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		VCA2612Y	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

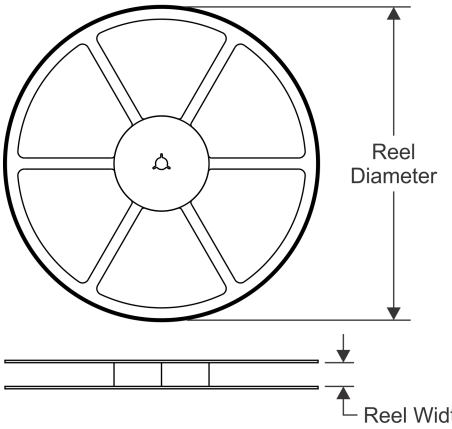
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

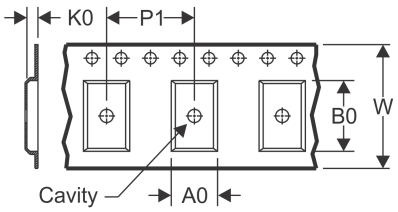
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

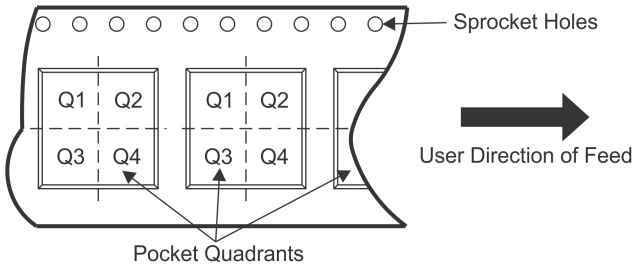


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

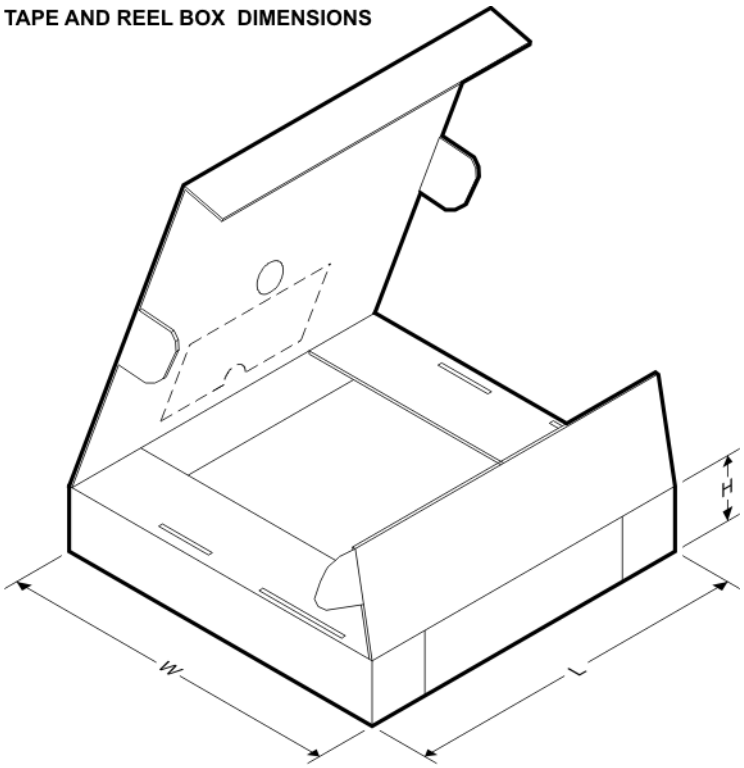
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VCA2612Y/250	TQFP	PFB	48	250	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

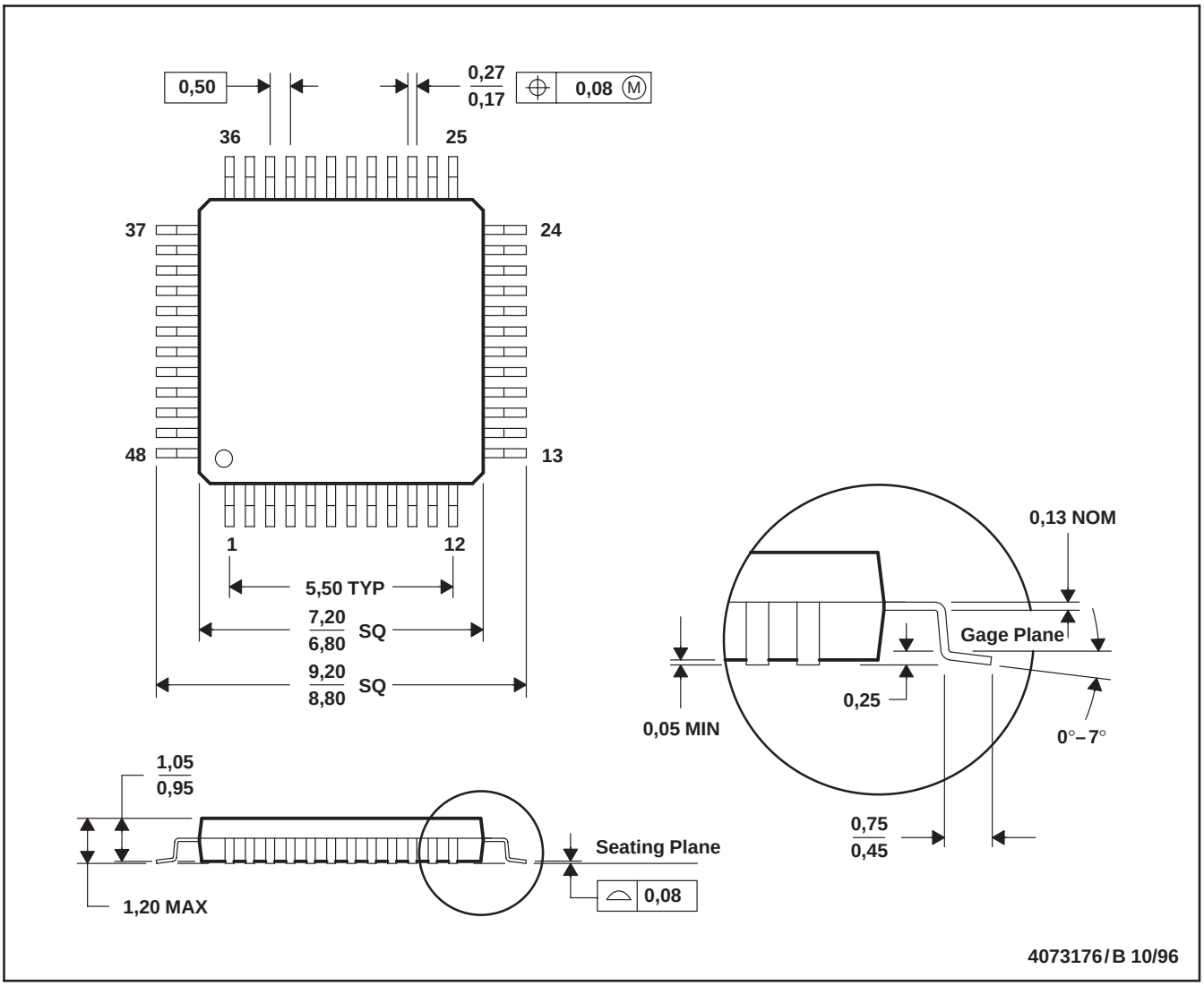


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VCA2612Y/250	TQFP	PFB	48	250	336.6	336.6	31.8

MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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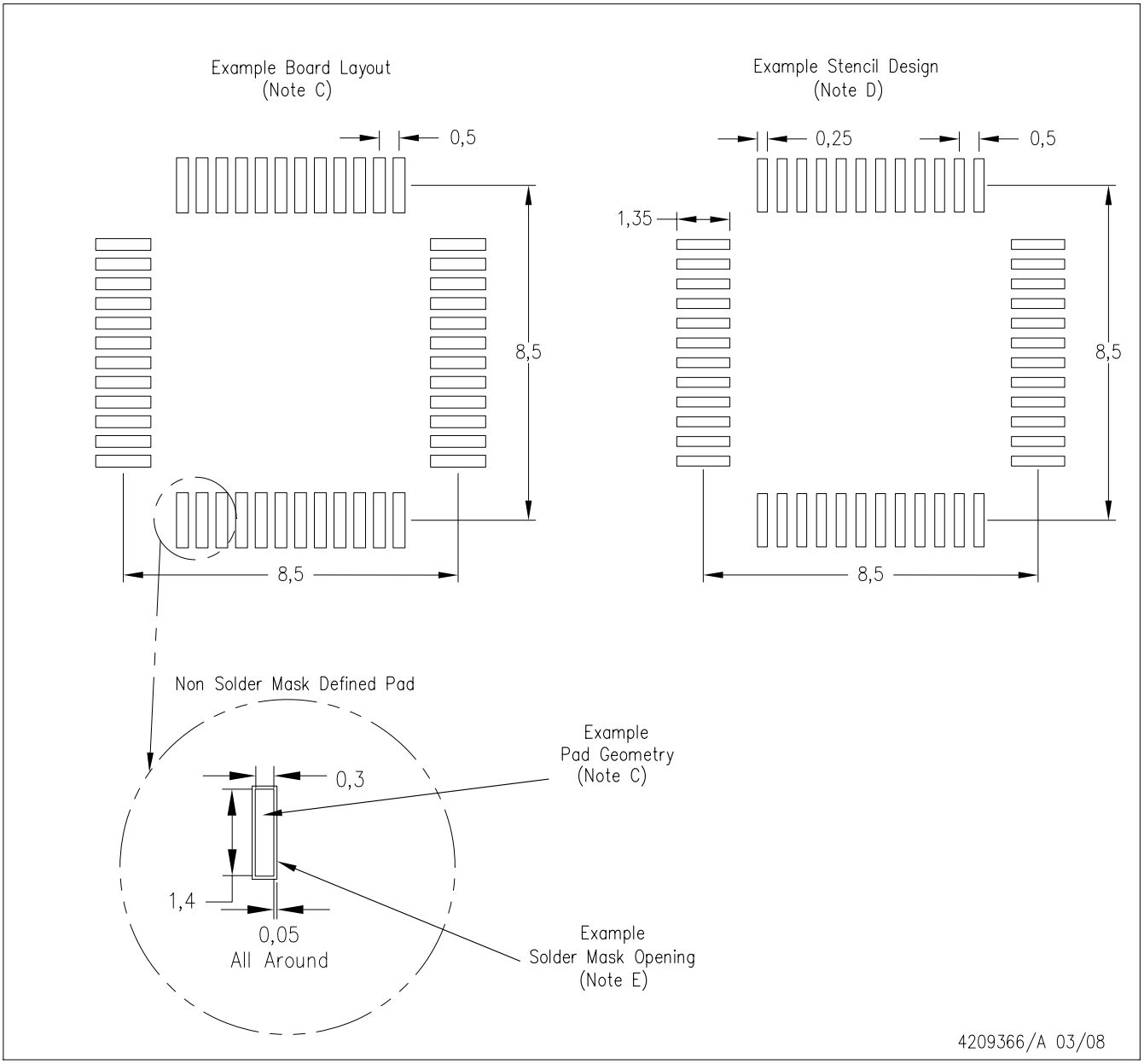

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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