TEXAS INSTRUMENTS

TPS650531, TPS650532
TPS65053, TPS65058

SLVS754D – MARCH 2007 – REVISED JANUARY 2015

TPS6505xx 5-Channel Power Management IC With Two Step-Down Converters and Three Low-Input Voltage LDOs

1 Features

- Up To 95% Efficiency
- Output Current for DC-DC Converters:
  - TPS65053: DCDC1 = 1 A; DCDC2 = 0.6 A
  - TPS650531, TPS650532: DCDC1 = 1 A; DCDC2 = 1 A
  - TPS65058: DCDC1 = 0.6 A; DCDC2 = 1 A
- TPS65053, TPS650531, TPS650532: DC-DC Converters Externally Adjustable
- TPS65058: DCDC1 Fixed at 3.3V, DCDC2 selectable between 1.8V and 1.2V with Dynamic Voltage Scaling for Core Processor Supply
- V_{IN} Range for DC-DC Converters From 2.5 V to 6 V
- 2.25-MHz Fixed Frequency Operation
- Power Save Mode at Light Load Current
- 180° Out-of-Phase Operation
- Output Voltage Accuracy in PWM Mode ±1%
- Total Typical 32-µA Quiescent Current for Both DC-DC Converters
- 100% Duty Cycle for Lowest Dropout
- One General-Purpose 400-mA LDO
- Two General-Purpose 200-mA LDOs
- V_{IN} Range for LDOs from 1.5 V to 6.5 V
- Output Voltage for LDOs:
  - TPS65053 / TPS650531 / TPS650532: VLDO1 and VLDO2 Externally Adjustable, VLDO3 = 1.3 V / 1.2 V / 1.5 V
  - TPS65058: VLDO1 = 3.3 V, VLDO2 selectable between 1.8V and 1.2V, VLDO2 selectable between 1.8V and 1.3V

2 Applications

- Cell Phones, Smart Phones
- WLAN
- PDAs, Pocket PCs, GPS
- OMAP™ and Low-Power DSP Supply
- Portable Media Players
- Digital Cameras
- Satellite Radio Modules

3 Description

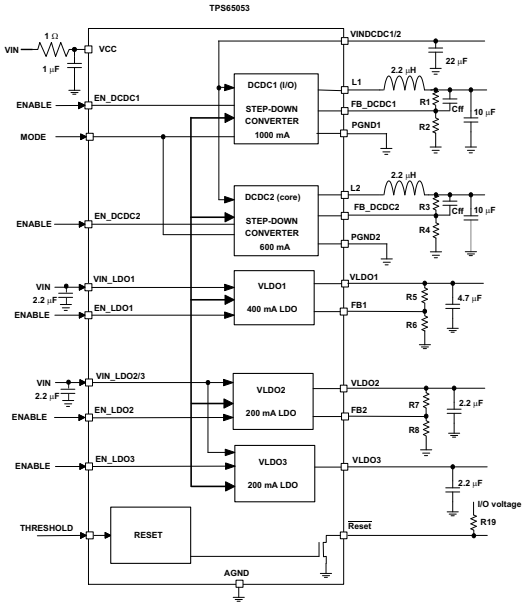
The TPS6505xx family of devices are integrated power management ICs for applications powered by one Li-Ion or Li-Polymer cell, which require multiple power rails. The TPS6505xx devices provide two highly efficient, 2.25-MHz step-down converters targeted at providing the core voltage and I/O voltage in a processor-based system. Both step-down converters enter a low power mode at light load for maximum efficiency across the widest possible range of load currents. For low noise applications the devices can be forced into fixed frequency PWM mode by pulling the MODE pin high. The TPS6505xx devices also integrate one 400-mA LDO and two 200-mA LDO voltage regulators. Each LDO operates with an input voltage range between 1.5 V and 6.5 V allowing them to be supplied from one of the step-down converters or directly from the main battery.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65053	VQFN (24)	4.00 mm x 4.00 mm
TPS650531		
TPS650532		
TPS65058		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



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4 Revision History

Changes from Revision C (June 2009) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (February 2008) to Revision C — **Page**

- Changed devices TPS650531 and TPS650532 to the Features and Ordering Information table. ... 1

Changes from Revision A (September 2007) to Revision B — **Page**

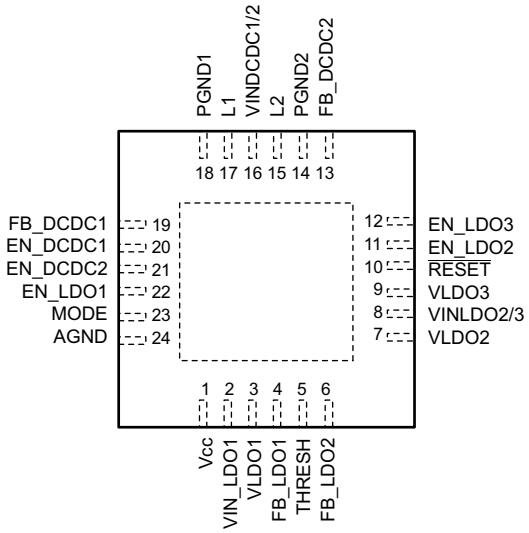
- Changed the Functional Block Diagram - DCDC1 (I/O) Step-Down Converter From: 600 mA To: 1000 mA. ... 14

Changes from Original (March 2007) to Revision A — **Page**

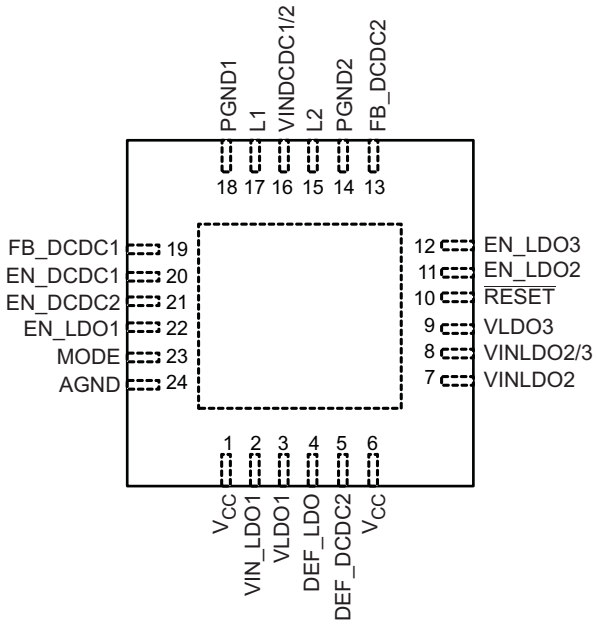
- Added Output voltage range for LDO1, LDO2 and LDO3 to the Abs Max table ... 5
- Changed Output voltage range for LDO1 and LDO2 In the ROC table From: Max = V_{INLDO1}, V_{INLDO2} To: 3.6V ... 5

5 Pin Configuration and Functions

RGE Package - TPS65053x
24 Pins
Top View



RGE Package - TPS65058
24 Pins
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS65053, TPS650531, TPS650532	TPS65058		
AGND	24	24	I	Analog GND, connect to PGND and PowerPAD™
DEF_DCDC2	—	5	I	Switches output votlage at DCDC2, logic HIGH = 1.8V, logic LOW = 1.2V
DEF_LDO	—	4	I	Switches output votlage at LDO2, logic HIGH = 1.8V, logic LOW = 1.2V
				Switches output votlage at LDO3, logic HIGH = 1.8V, logic LOW = 1.3V
EN_DCDC1	20	20	I	Enable Input for converter 1, active high
EN_DCDC2	21	21	I	Enable Input for converter 2, active high
EN_LDO1	22	22	I	Enable input for LDO1. Logic high enables the LDO, logic low disables the LDO.
EN_LDO2	11	11	I	Enable input for LDO2. Logic high enables the LDO, logic low disables the LDO.
EN_LDO3	12	12	I	Enable input for LDO3. Logic high enables the LDO, logic low disables the LDO.
FB_DCDC1	19	19	I	Input to adjust output voltage of converter 1 between 0.6 V and V_I. Connect external resistor divider between VOUT1, this pin and GND.
FB_DCDC2	13	13	I	Input to adjust output voltage of converter 2 between 0.6V and VIN. Connect external resistor divider between VOUT2, this pin and GND.
FB_LDO1	4	—	1	Feedback input for the external voltage divider.
FB_LDO2	6	—	I	Feedback input for the external voltage divider.
L1	17	17	O	Switch pin of converter 1. Connected to Inductor
L2	15	15	O	Switch Pin of converter 2. Connected to Inductor.
MODE	23	23	I	Select between Power Save Mode and forced PWM Mode for DCDC1 and DCDC2. In Power Save Mode, PFM is used at light loads, PWM for higher loads. If PIN is set to high level, forced PWM Mode is selected. If Pin has low level, then the device operates in Power Save Mode.
PGND1	18	18	I	GND for converter 1
PGND2	14	14	I	GND for converter 2
PowerPAD™	—	—	—	Connect to GND
V_{CC}	1	1, 6	I	Power supply for digital and analog circuitry of DCDC1, DCDC2 and LDOs. This pin must be connected to the same voltage supply as VINDCDC1/2.
VINDCDC1/2	16	16	I	Input voltage for VDCDC1 and VDCDC2 step-down converter. This must be connected to the same voltage supply as V_{CC}.
VINLDO1	2	2	I	Input voltage for LDO1
VINLDO2/3	8	8	I	Input voltage for LDO2 and LDO3
VLDO1	3	3	O	Output voltage of LDO1
VLDO2	7	7	O	Output voltage of LDO2
VLDO3	9	9	O	Output voltage of LDO3
THRESHOLD	5	—	I	Reset input
$\overline{\text{RESET}}$	10	10	O	Open drain active low reset output, 100 ms reset delay time.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage on all pins except AGND, PGND, and EN_LDO1 pins with respect to AGND	–0.3	7	V
	Input voltage on EN_LDO1 pin with respect to AGND	–0.3	Vcc + 0.5	V
I_I	Current at VINDCDC1/2, L1, PGND1, L2, PGND2	1800	1800	mA
	Current at all other pins	1000	1000	mA
V_O	Output voltage for LDO1, LDO2 and LDO3	–0.3	4.0	V
T_A	Operating free-air temperature	–40	85	°C
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{INDCDC1/2}$	Input voltage range for step-down converters	2.5		6	V
V_{DCDC1}	Output voltage range for VDCDC1 step-down converter for externally adjustable versions	0.6		$V_{INDCDC1}$	V
V_{DCDC2}	Output voltage range for VDCDC2 step-down converter for externally adjustable versions	0.6		$V_{INDCDC2}$	V
V_{INLDO1}, $V_{INLDO2/3}$	Input voltage range for LDOs	1.5		6.5	V
V_{LDO1-2}	Output voltage range for LDO1 and LDO2 for externally adjustable versions	1		3.6	V
	Output voltage for LDO1 on TPS65058		3.3		V
	Output voltage for LDO2 on TPS65058 (DEF_LDO = 1 / 0)		1.8 / 1.2		V
V_{LDO3}	Output voltage for LDO3 on TPS65053		1.3		V
	Output voltage for LDO3 on TPS650531		1.2		
	Output voltage for LDO3 on TPS650532		1.5		
	Output voltage for LDO3 on TPS65058 (DEF_LDO = 1 / 0)		1.8 / 1.3		V
$I_{OUTDCDC1}$	Output current at L1 for TPS65053, TPS650531, TPS650532			1000	mA
	Output current at L1 for TPS65058			600	mA
L1	Inductor at L1(1)	1.5	2.2		µH
$C_{INDCDC1/2}$	Input capacitor at $V_{INDCDC1/2}$ (1)	22			µF
$C_{OUTDCDC1}$	Output capacitor at V_{DCDC1} (1)	10	22		µF
$I_{OUTDCDC2}$	Output current at L2 for TPS65053			600	mA
	Output current at L2 for TPS650531, TPS650532, TPS65058			1000	

(1) See the *Application Information* section of this data sheet for more details.

Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
L2	Inductor at L2 (1)	1.5	2.2		µH
$C_{OUTDCDC2}$	Output capacitor at V_{DCDC2} (1)	10	22		µF
C_{VCC}	Input capacitor at VCC (1)	1			µF
C_{in1-2}	Input capacitor at VINLDO1, VINLDO2/3 (1)	2.2			µF
C_{OUT1}	Output capacitor at VLDO1 (1)	4.7			µF
C_{OUT2-3}	Output capacitor at VLDO2-3 (1)	2.2			µF
I_{LDO1}	Output current at VLDO1			400	mA
$I_{LDO2,3}$	Output current at VLDO2,3			200	mA
T_A	Operating ambient temperature range	–40		85	°C
T_J	Operating junction temperature range	–40		125	°C
R_{CC}	Resistor from battery voltage to V_{CC} used for filtering (2)		1	10	Ω

(2) Up to 2 mA can flow into V_{CC} when both converters are running in PWM, this resistor causes the UVLO threshold to be shifted accordingly.

6.4 Thermal Information

THERMAL METRIC (1)		TPS65053 VQFN 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.2	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	8.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Dissipation Ratings

PACKAGE	$R_{\theta JA}$ (1)	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RGE	35 K/W	2.8 W	28 mW/K	1.57 W	1.14 W

(1) The thermal resistance junction to case of the RGE package is 2 K/W measured on a high K board.

6.6 Electrical Characteristics

V_{cc} = VINDCDC1/2 = 3.6V, EN = V_{cc}, MODE = GND, L = 2.2µH, C_{OUT} = 22µF, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_{cc}	Input voltage range			2.5		6	V
I_Q	Operating quiescent current Total current into V_{CC}, VINDCDC1/2, VINLDO1, VINLDO2/3		One converter, I_{OUT} = 0 mA.PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = Vin OR EN_DCDC2 = Vin; EN_LDO1= EN_LDO2 = EN_LDO3 = GND		20	30	µA
			Two converters, I_{OUT} = 0 mA, PFM mode enabled (Mode = 0) device not switching, EN_DCDC1 = Vin AND EN_DCDC2 = Vin; EN_LDO1 = EN_LDO2 = EN_LDO3 = GND		32	40	µA
			One converter, I_{OUT} = 0 mA, PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = Vin OR EN_DCDC2 = Vin; EN_LDO1 = EN_LDO2 = EN_LDO3 = Vin		145	210	µA
I_Q	Operating quiescent current into V_{CC}		One converter, I_{OUT} = 0 mA, Switching with no load (Mode = Vin), PWM operation EN_DCDC1 = Vin OR EN_DCDC2 = Vin; EN_LDO1 = EN_LDO2 = EN_LDO3 = GND		0.85		mA
			Two converters, I_{OUT} = 0 mA, Switching with no load (Mode = Vin), PWM operation EN_DCDC1 = Vin AND EN_DCDC2 = Vin; EN_LDO1 = EN_LDO2 = EN_LDO3 = GND		1.25		mA
$I_{(SD)}$	Shutdown current		EN_DCDC1 = EN_DCDC2 = GND EN_LDO1 = EN_LDO2 = EN_LDO3 = GND		9	12	µA
UVLO	Undervoltage lockout threshold for DCDC converters and LDOs		Voltage at V_{CC}		1.8	2	V
EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, MODE							
V_{IH}	High-level input voltage		MODE, EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3	1.2		V_{CC}	V
V_{IL}	Low-level input voltage		MODE, EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3	0		0.4	V
I_{IN}	Input bias current		MODE, EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, MODE = GND or VIN		0.01	1	µA
POWER SWITCH							
$r_{DS(on)}$ High Side	P-channel MOSFET on resistance for TPS65053, TPS650531, TPS650532	DCDC1, DCDC2	VINDCDC1/2 = 3.6 V		280	630	mΩ
			VINDCDC1/2 = 2.5 V		400		
	P-channel MOSFET on resistance for TPS65058	DCDC1, DCDC2	VINDCDC1/2 = 3.6 V		250	350	mΩ
			VINDCDC1/2 = 2.5 V		380	500	
I_{LD_PMOS}	P-channel leakage current		$V_{(DS)}$ = 6 V			1	µA
$r_{DS(on)}$ Low-Side	N-channel MOSFET on resistance for TPS65053, TPS650531, TPS650532	DCDC1, DCDC2	VINDCDC1/2 = 3.6 V		220	450	mΩ
			VINDCDC1/2 = 2.5 V		320		
	N-channel MOSFET on resistance for TPS65058	DCDC1, DCDC2	VINDCDC1/2 = 3.6 V		180	250	mΩ
			VINDCDC1/2 = 2.5 V		250		
I_{LK_NMOS}	N-channel leakage current		$V_{(DS)}$ = 6 V		7	10	µA
$I_{(LIMF)}$	Forward Current Limit PMOS (High-Side) and NMOS (Low side)	DCDC1 (TPS65053, TPS650531, TPS650532)	2.5 V ≤ V_{IN} ≤ 6 V	1.19	1.4	1.65	A
		DCDC1 (TPS65058)		0.85	1	1.15	
		DCDC2 (TPS65053)		0.85	1	1.15	
		DCDC2 (TPS650531, TPS650532, TPS65058)		1.19	1.4	1.65	
T_{SD}	Thermal shutdown		Increasing junction temperature		150		°C
	Thermal shutdown hysteresis		Decreasing junction temperature		20		°C

Electrical Characteristics (continued)

V_{cc} = VINDCDC1/2 = 3.6V, EN = V_{cc}, MODE = GND, L = 2.2µH, C_{OUT} = 22µF, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR							
f_{SW}	Oscillator frequency			2.025	2.25	2.475	MHz
OUTPUT							
V_{OUT}	Output voltage range for externally adjustable versions			0.6		V_{IN}	V
V_{ref}	Reference voltage				600		mV
V_{OUT}	DC output voltage accuracy	DCDC1, DCDC2(1)	V_{IN} = 2.5 V to 6 V, Mode = GND, PFM operation, 0 mA < I_{OUT} < I_{OUTMAX}	-2%	0	2%	
			V_{IN} = 2.5 V to 6 V, Mode = V_{IN}, PWM operation, 0 mA < I_{OUT} < I_{OUTMAX}	–1%	0	1%	
ΔV_{OUT}	Power save mode ripple voltage(2)		I_{OUT} = 1 mA, Mode = GND, V_O = 1.3 V, Bandwidth = 20 MHz		25		mV_{PP}
t_{Start}	Start-up time		Time from active EN to Start switching		170		µs
t_{Ramp}	V_{OUT} Ramp up Time		Time to ramp from 5% to 95% of V_{OUT}		750		µs
	$\overline{RESET}$ delay time		Input voltage at threshold pin rising	80	100	120	ms
V_{OL}	$\overline{RESET}$ output low voltage		I_{OL} = 1 mA, Vthreshold < 1 V			0.2	V
	$\overline{RESET}$ sink current				1		mA
	$\overline{RESET}$ output leakage current		(Vthreshold > 1 V for TPS65053, TPS650531, TPS650532)		10		nA
V_{th}	Threshold voltage TPS65053, TPS650531, TPS650532		falling voltage	0.98	1	1.02	V
VLDO1, VLDO2, VLDO3 LOW DROPOUT REGULATORS							
V_{INLDO}	Input voltage range for LDO1, LDO2, LDO3			1.5		6.5	V
V_{LDO1}	LDO1 output voltage range for TPS65053, TPS650531, TPS650532			1		3.6	V
	LDO1 output voltage for TPS65058				3.3		V
V_{LDO2}	LDO2 output voltage range for TPS65053, TPS650531, TPS650532			1		3.6	V
	LDO2 output voltage for TPS65058		DEF_LDO = 1 / 0		1.8 / 1.2		V
V_{LDO3}	LDO3 output voltage for TPS65053				1.3		V
	LDO3 output voltage for TPS650531				1.2		
	LDO3 output voltage for TPS650532				1.5		
	LDO3 output voltage for TPS65058		DEF_LDO = 1 / 0		1.8 / 1.3		
$V_{(FB)}$	Feedback voltage for FB_LDO1, FB_LDO2		for externally adjustable versions		1		V
I_O	Maximum output current for LDO1			400			mA
	Maximum output current for LDO2, LDO3			200			mA
$I_{(SC)}$	LDO1 short-circuit current limit		V_{LDO1} = GND			850	mA
	LDO2 & LDO3 short-circuit current limit		V_{LDO2} = GND, V_{LDO3} = GND			420	mA
	Dropout voltage at LDO1		I_O = 400 mA, V_{INLDO1} = 1.8 V			280	mV
	Dropout voltage at LDO2, LDO3		I_O = 200 mA, VINLDO2/3 = 1.8 V			280	mV
	Output voltage accuracy for LDO1, LDO2, LDO3(1)		I_O = 10 mA	–2%		1%	
	Line regulation for LDO1, LDO2, LDO3		$V_{INLDO1,2}$ = $V_{LDO1,2}$ + 0.5 V (min. 2.5 V) to 6.5V, I_O = 10 mA	–1%		1%	
	Load regulation for LDO1, LDO2, LDO3		I_O = 0 mA to 400 mA for LDO1 I_O = 0 mA to 200 mA for LDO2, LDO3	–1%		1%	
	Regulation time for LDO1, LDO2, LDO3		Load change from 10% to 90%		25		µs
	Regulation time for LDO1, LDO2, LDO3 for TPS65058		Load change from 10% to 90%		10		µs
PSRR	Power Supply Rejection Ratio		f = 10 kHz; I_O = 50 mA; V_I = V_O + 1 V				

(1) Output voltage specification does not include tolerance of external voltage programming resistors.
(2) In Power Save Mode, operation is typically entered at I_{PSM} = V_{IN} / 32 Ω.

Electrical Characteristics (continued)

V_{cc} = VINDCDC1/2 = 3.6V, EN = V_{cc}, MODE = GND, L = 2.2µH, C_{OUT} = 22µF, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(DIS)}$	Internal discharge resistor at VLDO1, VLDO2, VLDO3	Active when LDO is disabled		350		Ω
	Internal discharge resistor at VLDO1, VLDO2, VLDO3 for TPS65058	Active when LDO is disabled		300		Ω
	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C

6.7 Typical Characteristics

Table 1. Table Of Graphs for TPS6505xx

			FIGURE
η	Efficiency converter 1	vs Load current PWM/PFM mode	Figure 1
η	Efficiency converter 1	vs Load current PWM mode	Figure 2
η	Efficiency converter 2	vs Load current PWM/PFM mode	Figure 3
η	Efficiency converter 2	vs Load current PWM mode	Figure 4
	Output voltage ripple in PFM mode	Scope plot	Figure 5
	Output voltage ripple in PWM mode	Scope plot	Figure 6
	DCDC1, DCDC2, LDO1 startup timing	Scope plot	Figure 7
	LDO1 to LDO3 startup timing	Scope plot	Figure 8
	DCDC1 Load transient response in PWM mode	Scope plot	Figure 9
	DCDC1 Load transient response in PFM mode	Scope plot	Figure 10
	DCDC2 Load transient response in PWM mode	Scope plot	Figure 11
	DCDC2 Load transient response in PFM mode	Scope plot	Figure 12
	DCDC1 Line transient response in PWM mode	Scope plot	Figure 13
	DCDC2 Line transient response in PWM mode	Scope plot	Figure 14
	LDO1 Load transient response	Scope plot	Figure 15
	LDO3 Load transient response	Scope plot	Figure 16
	LDO1 Line transient response	Scope plot	Figure 17
	LDO1 Power supply rejection ratio	vs frequency	Figure 18

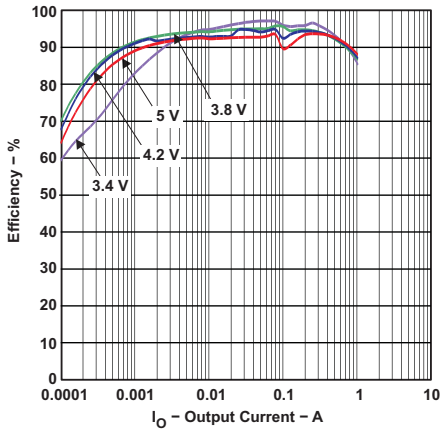


Figure 1. Efficiency vs Output Current

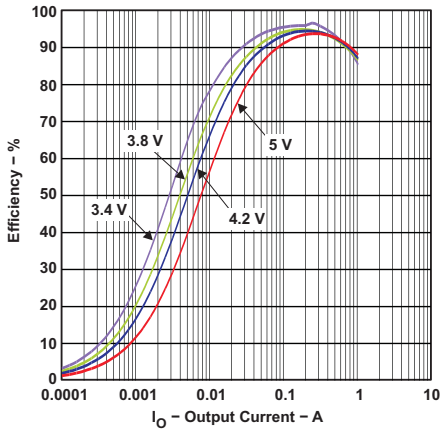


Figure 2. Efficiency vs Output Current

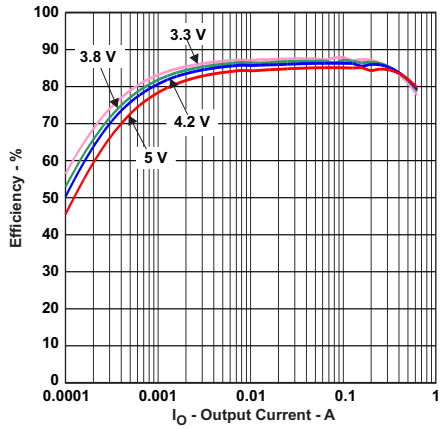


Figure 3. Efficiency vs Output Current

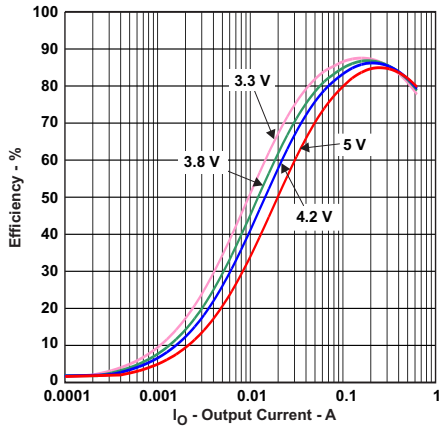


Figure 4. Efficiency vs Output Current

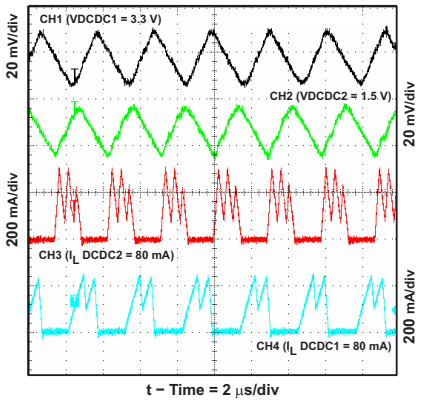


Figure 5. Output Voltage Ripple PWM/PFM Mode = Low

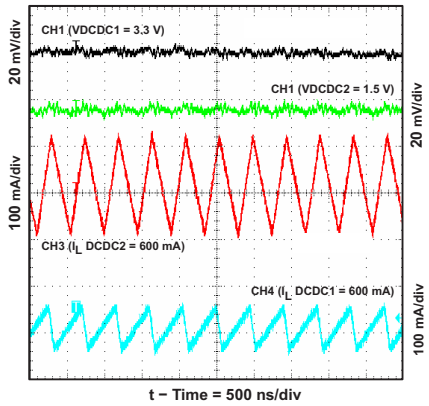


Figure 6. Output Voltage Ripple PWM Mode = High

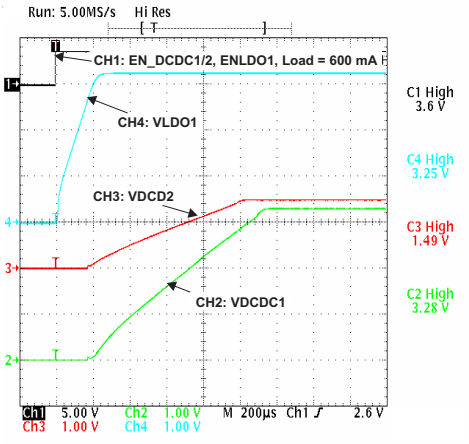


Figure 7. DCDC1 Startup Timing

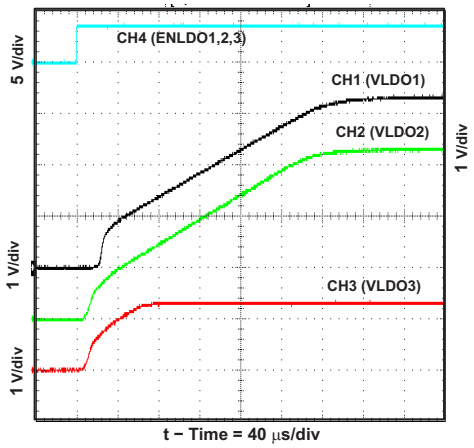


Figure 8. LDO1 to LDO3 Startup Timing

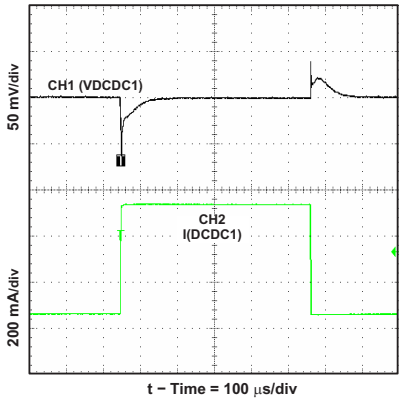


Figure 9. DCDC1 Load Transient Response

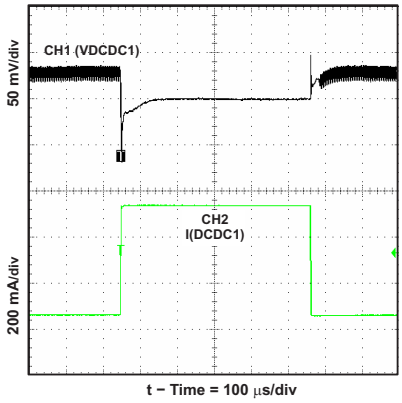


Figure 10. DCDC1 Load Transient Response

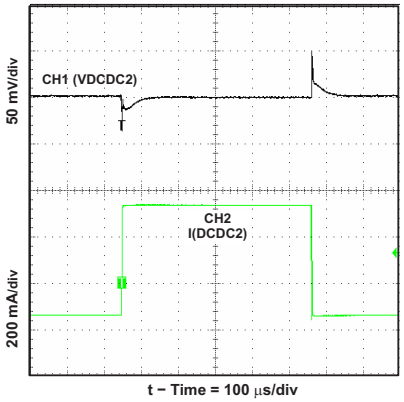


Figure 11. DCDC2 Load Transient Response

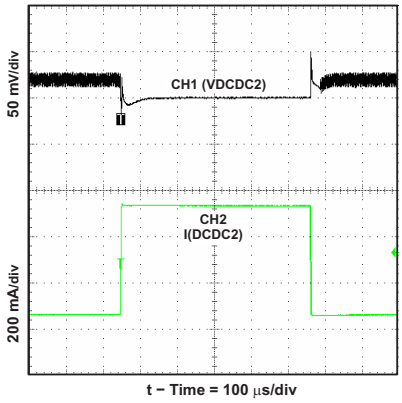


Figure 12. DCDC2 Load Transient Response

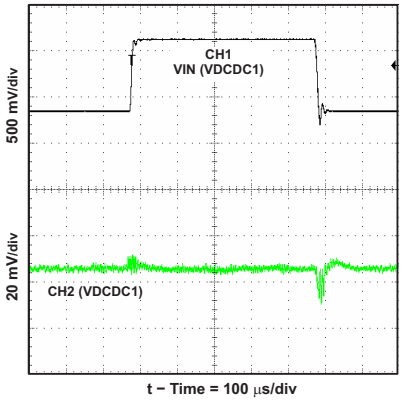


Figure 13. DCDC1 Line Transient Response

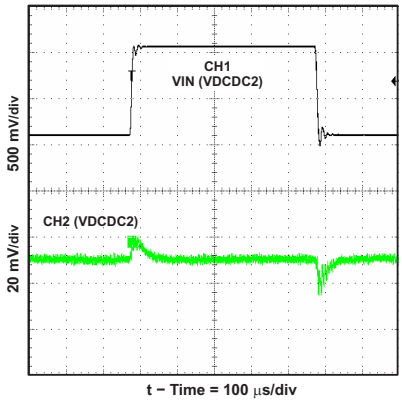


Figure 14. DCDC2 Line Transient Response

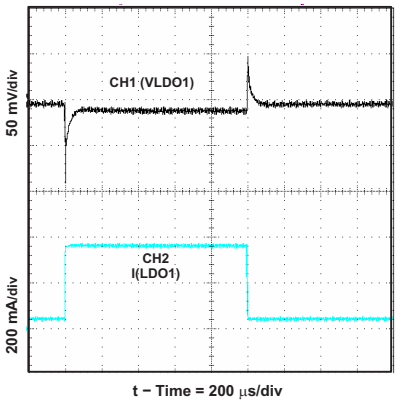


Figure 15. LDO1 Load Transient Response

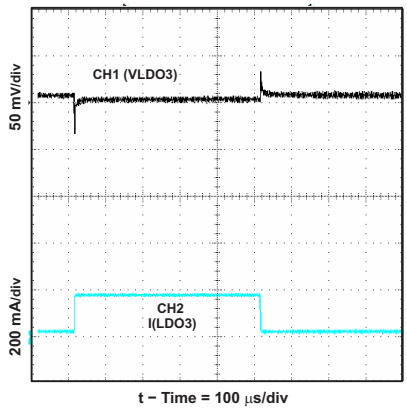


Figure 16. LDO3 Load Transient Response

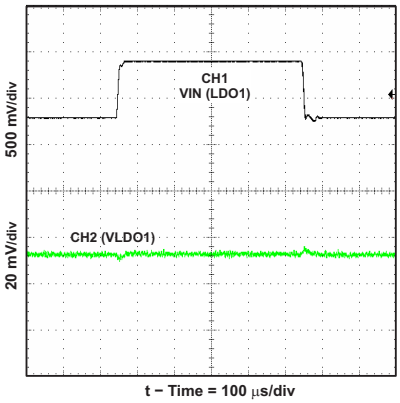


Figure 17. LDO1 Line Transient Response

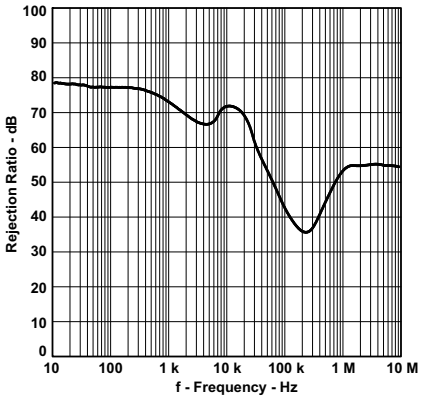


Figure 18. LDO1 Power Supply Rejection Ratio vs Frequency

7 Detailed Description

7.1 Overview

The TPS6505xx include two synchronous step-down converters. The converters operate with 2.25 MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converters automatically enter Power Save Mode and operate with PFM (Pulse Frequency Modulation).

During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator will also turn off the switch in case the current limit of the P-channel switch is exceeded. After the adaptive dead time prevents shoot through current, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

The two DC-DC converters operate synchronized to each other, with converter 1 as the master. A 180 ° phase shift between Converter 1 and Converter 2 decreases the input RMS current. Therefore smaller input capacitors can be used.

The converters output voltage is set by an external resistor divider connected to FB_DCDC1 or FB_DCDC2, respectively. See *Application and Implementation* for more details.

7.2 Functional Block Diagrams

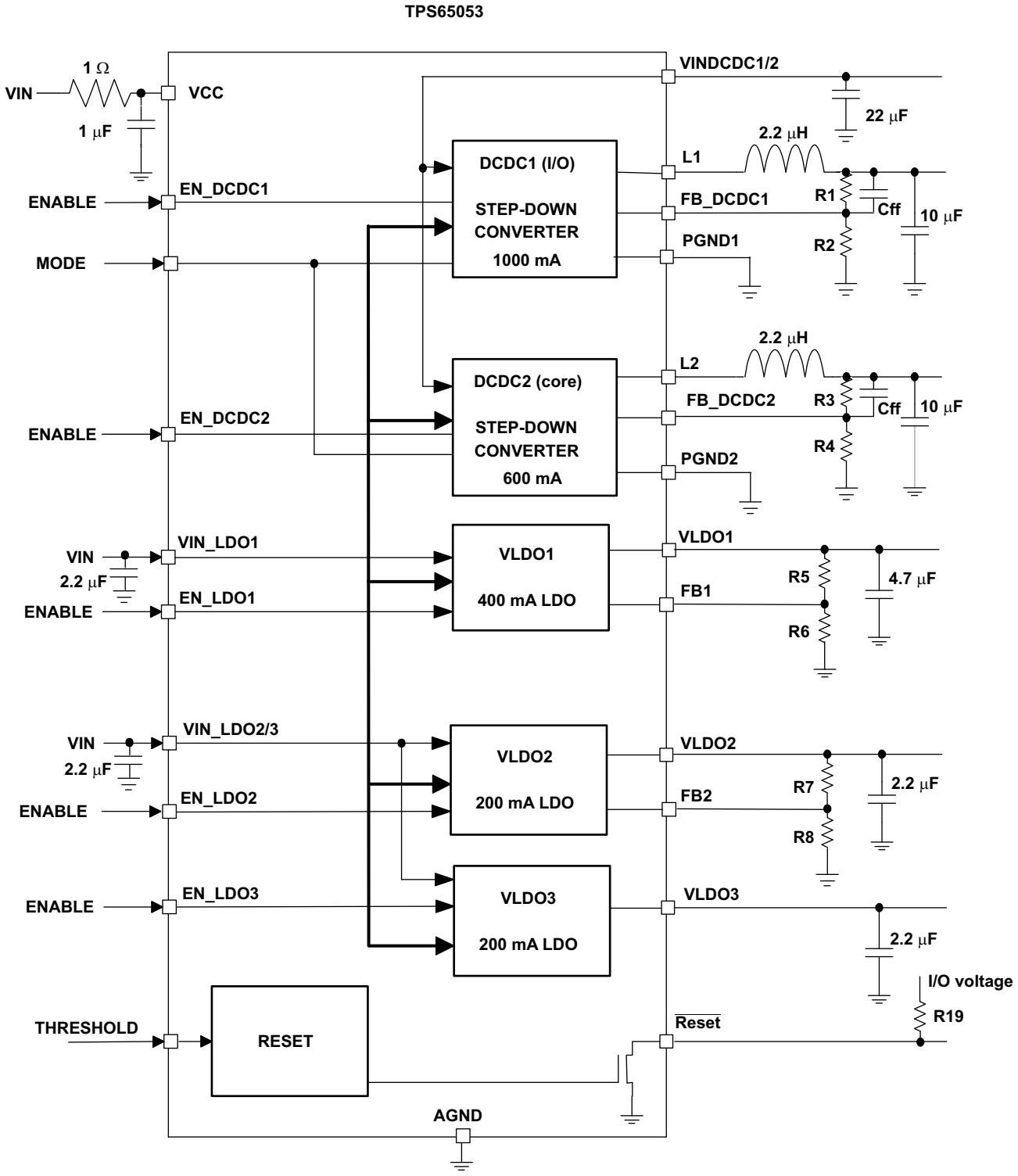


Figure 19. TPS65053 Functional Block Diagram

Functional Block Diagrams (continued)

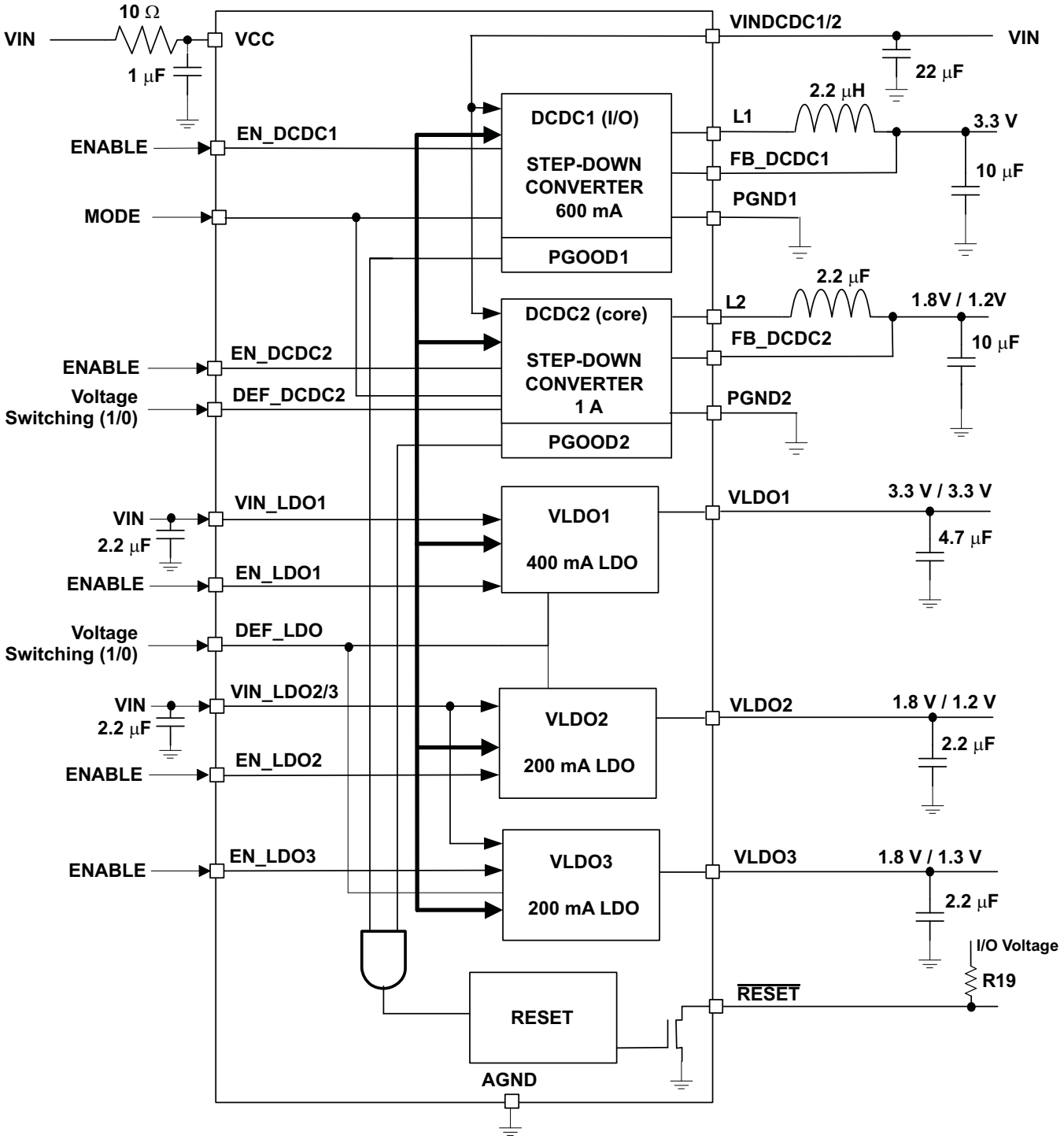


Figure 20. TPS65058 Functional Block Diagram

7.3 Feature Description

7.3.1 Power Save Mode

The Power Save Mode is enabled with Mode Pin set to low. If the load current decreases, the converters will enter Power Save Mode operation automatically. During Power Save Mode the converters operate with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage typically 1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

In order to optimize the converter efficiency at light load the average current is monitored and if in PWM mode the inductor current remains below a certain threshold, then Power Save Mode is entered. The typical threshold can be calculated according to:

Average output current threshold to enter PFM mode:

$$I_{PFM\_enter} = \frac{VIN_{DCDC}}{32\Omega} \quad (1)$$

Average output current threshold to leave PFM mode:

$$I_{PFM\_leave} = \frac{VIN_{DCDC}}{24\Omega} \quad (2)$$

During the Power Save Mode the output voltage is monitored with a comparator. As the output voltage falls below the skip comparator threshold (skip comp) of $V_{OUTnominal}$ +1%, the P-channel switch will turn on and the converter effectively delivers a constant current as defined above. If the load is below the delivered current then the output voltage will rise until the same threshold is crossed again, whereupon all switching activity ceases, hence reducing the quiescent current to a minimum until the output voltage has dropped below the threshold again. If the load current is greater than the delivered current then the output voltage will fall until it crosses the skip comparator low (Skip Comp Low) threshold set to 1% below nominal Vout, whereupon Power Save Mode is exited and the converter returns to PWM mode.

These control methods reduce the quiescent current typically to 12µA per converter and the switching frequency to a minimum thereby achieving the highest converter efficiency. The PFM mode operates with very low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor; increasing capacitor values will make the output ripple tend to zero.

The Power Save Mode can be disabled by driving the MODE pin high. Both converters will operate in fixed PWM mode. Power Save Mode Enable/Disable applies to both converters.

7.3.1.1 Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is activated in Power Save Mode operation when the converter runs in PFM Mode. It provides more headroom for both the voltage drop at a load step increase and the voltage increase at a load throw-off. This improves load transient behavior.

At light loads, in which the converters operate in PFM Mode, the output voltage is regulated typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage will drop until it reaches the skip comparator low threshold set to –1% below the nominal value and enters PWM mode. During a load throw off from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel switch.

Feature Description (continued)

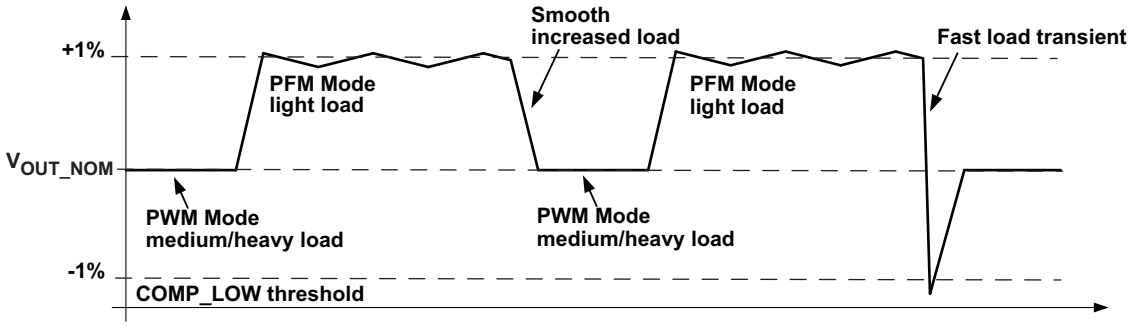


Figure 21. Dynamic Voltage Positioning

7.3.1.2 Soft Start

The two converters have an internal soft start circuit that limits the inrush current during start-up. During soft start, the output voltage ramp up is controlled as shown in Figure 22.

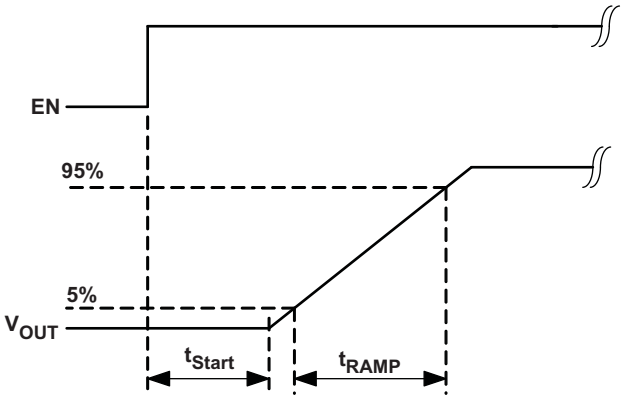


Figure 22. Soft Start

7.3.1.3 100% Duty Cycle Low Dropout Operation

The converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range, i.e. The minimum input voltage to maintain regulation depends on the load current and output voltage and can be calculated as:

$$Vin_{min} = Vout_{max} + Iout_{max} \times \left(RDSon_{max} + R_L\right) \quad (3)$$

where

- $Iout_{max}$ = maximum output current plus inductor ripple current
- $RDSon_{max}$ = maximum P-channel switch $r_{DS(on)}$
- R_L = DC resistance of the inductor
- $Vout_{max}$ = nominal output voltage plus maximum output voltage tolerance

With decreasing load current, the device automatically switches into pulse skipping operation in which the power stage operates intermittently based on load demand. By running cycles periodically the switching losses are minimized and the device runs with a minimum quiescent current maintaining high efficiency.

In power save mode the converter only operates when the output voltage trips below its nominal output voltage. It ramps up the output voltage with several pulses and goes again into power save mode once the output voltage exceeds the nominal output voltage.

Feature Description (continued)

7.3.1.4 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning by disabling the converter at low input voltages and from excessive discharge of the battery. The undervoltage lockout threshold is typically 1.8 V, max 2 V.

7.3.2 Mode Selection

The MODE pin allows mode selection between forced PWM Mode and power Save Mode for both converters. Connecting this pin to GND enables the automatic PWM and power save mode operation. The converters operate in fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, maintaining high efficiency over a wide load current range.

Pulling the MODE pin high forces both converters to operate constantly in the PWM mode even at light load currents. The advantage is the converters operate with a fixed frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads. For additional flexibility it is possible to switch from power save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

7.3.3 Enable

The devices have a separate enable pin for each of the DCDC converters and for each of the LDO to start up independently. If EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3 are set to high, the corresponding converter starts up with soft start as previously described.

Pulling the enable pin low forces the device into shutdown, with a shutdown quiescent current as defined in the electrical characteristics. In this mode, the P and N-Channel MOSFETs are turned-off, the and the entire internal control circuitry is switched-off. If disabled, the outputs of the LDOs are pulled low by internal 350-Ω resistors, actively discharging the output capacitor. For proper operation the enable pins must be terminated and must not be left unconnected.

7.3.4 Dynamic Ouput Voltage Scaling

The TPS65058 has the feature: dynamic voltage scaling intended for core processor supply. The voltage scaling can be used for any application or to simply select the output voltage. The following description applies only to TPS65058.

The output voltage of the DCDC Converter 2 can be selected by a logic level on pin DEF_DCDC2. The output voltage can be changed dynamically during operation. The slew rate of the change of output voltage is controlled on DCDC2 to be 9.6mV/µs.

The output voltages on the LDOs can also be changed dynamically between two voltages by changing the logic level on pin DEF_LDO.

The output voltage options are:

Table 2. Output Voltage Selection

DEF_LDO	**1**	**0**
LDO1	3.3 V	3.3 V
LDO2	1.8 V	1.2 V
LDO3	1.8 V	1.3 V
DEF_DCDC2	**1**	**0**
DCDC2	1.8 V	1.2 V

7.3.5 $\overline{\text{RESET}}$ on the TPS65053x

The TPS65053x contain circuitry that can generate a reset pulse for a processor with a 100 ms delay time. The input voltage at a comparator is sensed at an input called THRESHOLD. When the voltage exceeds the 1V threshold, the output goes high after a 100 ms delay time. This circuitry is functional as soon as the supply voltage at Vcc exceeds the undervoltage lockout threshold. The RESET circuitry is active even if all DCDC converters and LDOs are disabled.

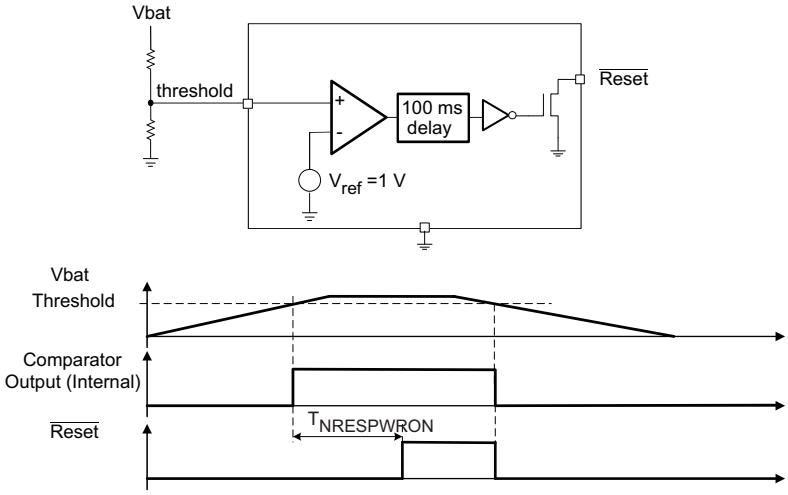


Figure 23. $\overline{\text{RESET}}$ Pulse Circuit for TPS65053x

7.3.6 $\overline{\text{RESET}}$ Generation and Output Monitoring on the TPS65058

The TPS65058 contains a monitor circuitry that monitors the outputs of the DCDC converters and applies a reset pulse to the $\overline{\text{RESET}}$ pin. As soon as the supply voltage on the VCC pin is above the undervoltage lockout threshold, the $\overline{\text{RESET}}$ pin is pulled low. After the enabling of both DCDC converters, the output voltages are monitored. When both outputs are within 95% of the desired output voltage, the reset timer is started and after a delay of 100ms the $\overline{\text{Reset}}$ output is switched to high impedance. If one of the output voltages is outside of the regulation band (90% of the desired value) the $\overline{\text{RESET}}$ pin remains to be pulled to ground. After both outputs are back in regulation, the 100ms timer is started, and after 100ms the $\overline{\text{RESET}}$ output is again switched to high impedance.

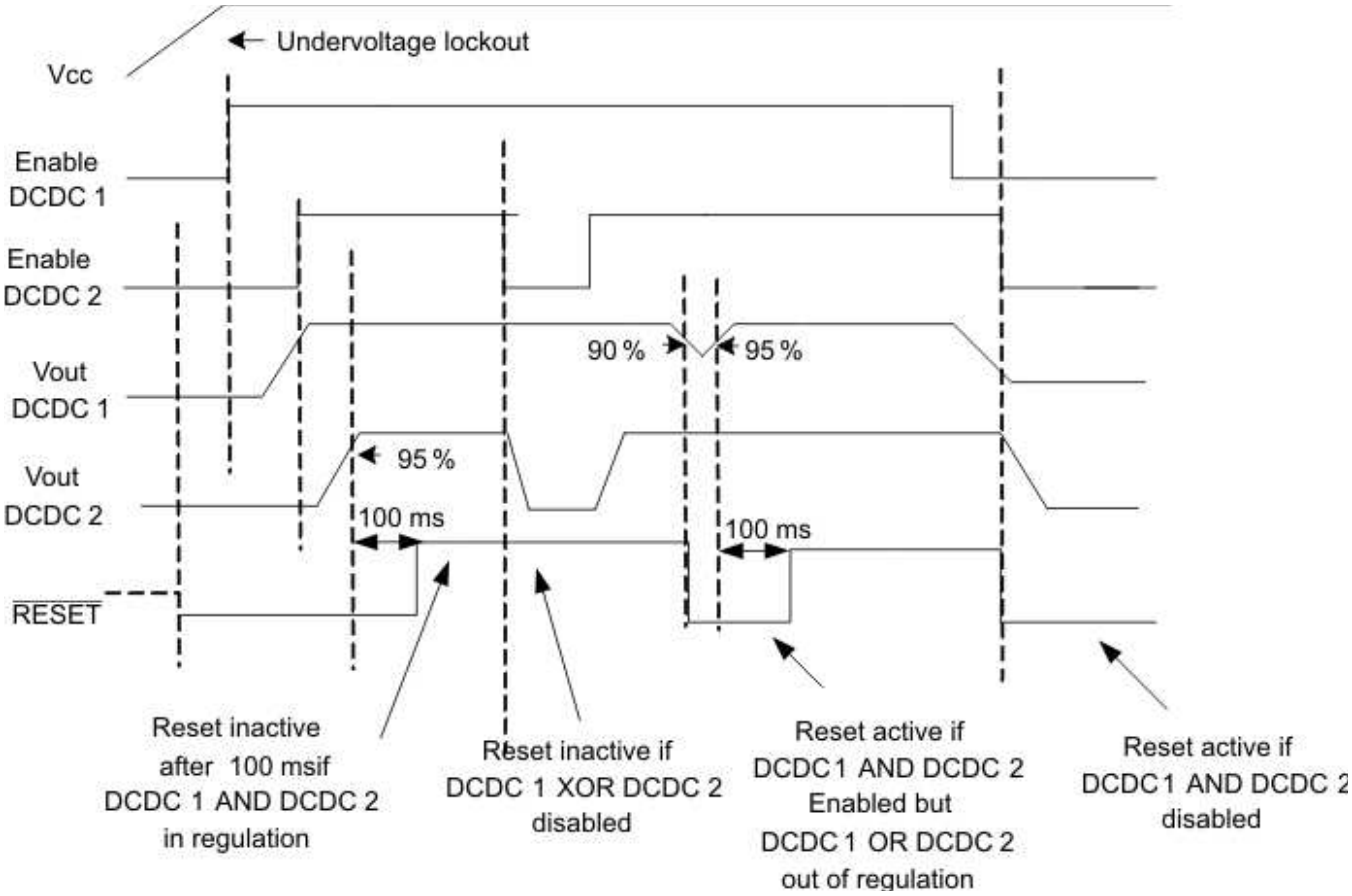


Figure 24. $\overline{\text{RESET}}$ Pulse Circuit for TPS65058

7.3.7 Short-Circuit Protection

All outputs are short circuit protected with a maximum output current as defined in the *Electrical Characteristics*.

7.3.8 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds typically 150°C for the DCDC converters, the device goes into thermal shutdown. In this mode, the P and N-Channel MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again. A thermal shutdown for one of the DCDC converters will disable both converters simultaneously.

The thermal shutdown temperature for the LDOs are set to typically 140°C. Therefore a LDO which may be used to power an external voltage will never heat up the chip high enough to turn off the DCDC converters. If one LDO exceeds the thermal shutdown temperature, all LDOs will turn off simultaneously.

7.4 Device Functional Modes

This device has only one functional mode which is ON. The device enters this state if the device is within the operational VIN range on the VCC pin. The converters and LDOs can be enabled and/or disabled in this state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This device integrates two step-down converters and three LDOs which can be used to power the voltage rails needed by a processor or any other application. The PMIC can be controlled via the ENABLE and MODE pins or sequenced from the VIN using RC delay circuits. There is a logic output, $\overline{\text{RESET}}$, provide the application processor or load a logic signal indicating power good or reset.

8.2 Typical Application

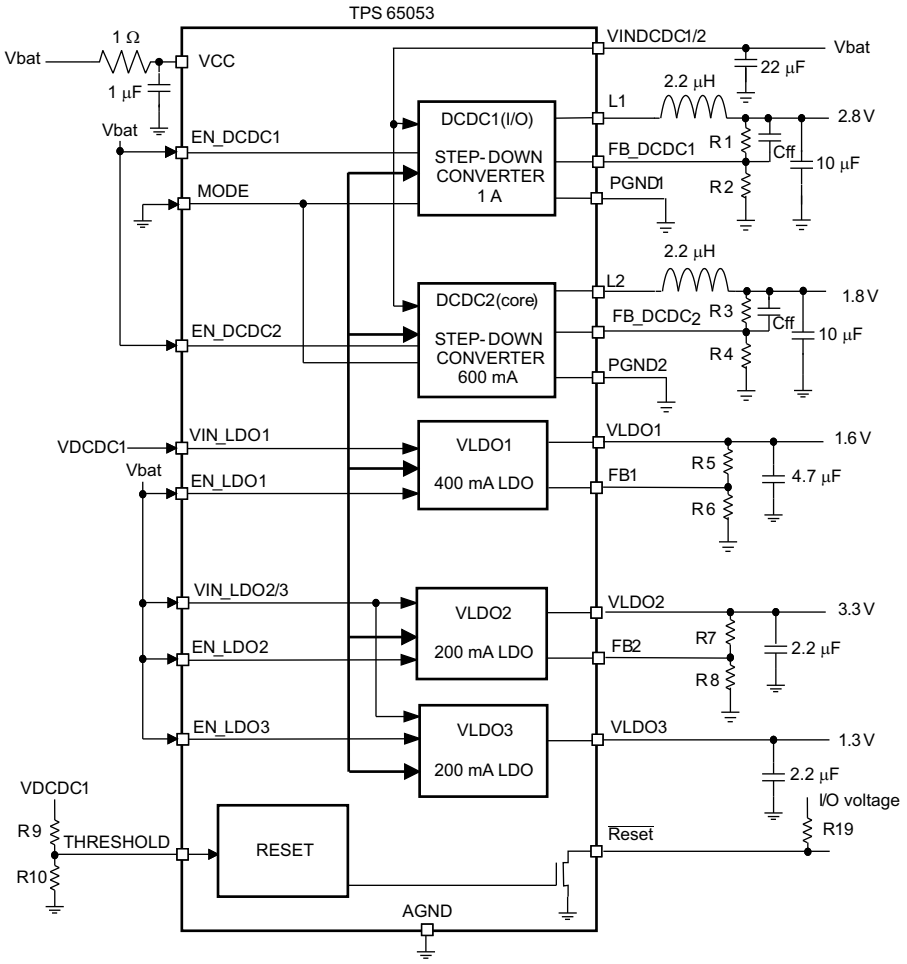


Figure 25. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

The TPS6505x has only a few design requirements. The check list below lists the design requirements across all application uses of the device.

- 1-µF Bypass cap on VCC, located as close as possible to the VCC pin to ground.
- VCC and VINDCDC1/2 must be connected to the same voltage supply with minimal voltage difference.
- Input capacitors must be present on the VINDCDC1/2, VIN_LDO1, and VIN_LDO2/3 supplies if used.
- Output filters must be used on the outputs of the DCDC converters if used.
- Output capacitors must be used on the outputs of the LDOs if used.

8.2.2 Detailed Design Procedure

The TPS6505x requires design for each regulator whether DCDC or LDO. First, the output votlage must be selected or set. Then, each DCDC converter requires an output filter, input capacitor, and feedback circuit and each LDO requires an output capacitor and input capacitor. The following sections discuss the procedure for designing for output voltages, DCDCs, and LDOs.

8.2.2.1 DCDC Output Voltage Setting

The output voltage of the DCDC converters can be set by an external resistor network and can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \tag{4}$$

with an internal reference voltage V_{ref}, 0.6 V (typical).

It is recommended to set the total resistance of R1 + R2 to less than 1 MΩ. The resistor network connects to the input of the feedback amplifier; therefore, need some small feedforward capacitor in parallel to R1. A typical value of 47 pF is sufficient.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB\_DCDC1}}\right) - R2 \tag{5}$$

Table 3. Typical Resistor Values

OUTPUT VOLTAGE	R1	R2	NOMINAL VOLTAGE	TYPICAL CFF
3.3 V	680 kΩ	150 kΩ	3.32 V	47 pF
3.0 V	510 kΩ	130 kΩ	2.95 V	47 pF
2.85 V	560 kΩ	150 kΩ	2.84 V	47 pF
2.5 V	510 kΩ	160 kΩ	2.51 V	47 pF
1.8 V	300 kΩ	150 kΩ	1.80 V	47 pF
1.6 V	200 kΩ	120 kΩ	1.60 V	47 pF
1.5 V	300 kΩ	200 kΩ	1.50 V	47 pF
1.2 V	330 kΩ	330 kΩ	1.20 V	47 pF

8.2.2.2 LDO Output Voltage Setting

The output voltage of LDO1 and LDO2 can be set by an external resistor network and can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R5}{R6}\right) \tag{6}$$

with an internal reference voltage, V_{REF}, typical 1 V.

It is recommended to set the total resistance of R5 + R6 to less than 1 MΩ. Typically, there is no feedforward capacitor needed at the voltage dividers for the LDOs.

$$V_{OUT} = V_{FB\_LDOx} \times \frac{R5 + R6}{R6} \qquad R5 = R6 \times \left(\frac{V_{OUT}}{V_{FB\_LDOx}}\right) - R6 \tag{7}$$

Typical Application (continued)

Table 4. Typical Resistor Values

OUTPUT VOLTAGE	R5	R6	NOMINAL VOLTAGE
3.3 V	300 kΩ	130 kΩ	3.31 V
3 V	300 kΩ	150 kΩ	3.00 V
2.85 V	240 kΩ	130 kΩ	2.85 V
2.80 V	360 kΩ	200 kΩ	2.80 V
2.5 V	300 kΩ	200 kΩ	2.50 V
1.8 V	240 kΩ	300 kΩ	1.80 V
1.5 V	150 kΩ	300 kΩ	1.50 V
1.3 V	36 kΩ	120 kΩ	1.30 V
1.2 V	100 kΩ	510 kΩ	1.19 V
1.1 V	33 kΩ	330 kΩ	1.1 V

8.2.2.3 Low Dropout Voltage Regulators

The low dropout voltage regulators are designed to be stable with low value ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 280mV at rated output current. Each LDO supports a current limit feature. The LDOs are enabled by the EN_LDO1, EN_LDO2, and EN_LDO3 pin. The output voltage of LDO1 and LDO2 is set using an external resistor divider whereas LDO3 has a fixed output voltage of 1.30 V for TPS65053, 1.20 V for TPS650531 and 1.50 V for TPS650532.

The minimum input capacitor on VIN_LDO1 and on VIN_LDO2/3 is 2.2 µF minimum. LDO1 is designed to be stable with an output capacitor of 4.7 µF minimum; whereas, LDO2 and LDO3 are stable with a minimum capacitor value of 2.2 µF.

8.2.2.4 DCDC Output Filter Design (Inductor and Output Capacitor)

8.2.2.4.1 Inductor Selection

The two converters operate typically with 2.2-µH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For output voltages higher than 2.8 V, an inductor value of 3.3 µH minimum should be selected, otherwise the inductor current will ramp down too fast causing imprecise internal current measurement and therefore increased output voltage ripple under some operating conditions in PFM mode.

The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance will influence directly the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency.

Equation 8 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 8. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \qquad I_{Lmax} = I_{out}max + \frac{\Delta I_L}{2} \tag{8}$$

where

- f = Switching Frequency (2.25-MHz typical)
- L = Inductor Value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum Inductor current

The highest inductor current occurs at maximum Vin. Open core inductors have a soft saturation characteristic, and they can normally handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies. Refer to Table 5 and the typical applications for possible inductors.

Table 5. Tested Inductors

INDUCTOR TYPE	INDUCTOR VALUE	SUPPLIER
LPS3010	2.2 µH	Coilcraft
LPS3015	3.3 µH	Coilcraft
LPS4012	2.2 µH	Coilcraft
VLF4012	2.2 µH	TDK

8.2.2.4.2 Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the two converters allow the use of small ceramic capacitors with a typical value of 10 µF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended. See the recommended components in Table 4.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. Just for completeness, the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (9)$$

At nominal load current, the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (10)$$

Where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the converters operate in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

8.2.2.5 DCDC Input Capacitor Selection

Because of the nature of the buck converter, having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10 µF. The input capacitor can be increased without any limit for better input voltage filtering.

Table 6. Possible Capacitors For DCDC Converters and LDOS

CAPACITOR VALUE	SIZE	SUPPLIER	TYPE
2.2 µF	0805	TDK C2012X5R0J226MT	Ceramic
2.2 µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	0805	TDK C2012X5R0J106M	Ceramic

8.2.2.6 Sequencing and Output Logic Signal RESET

To sequence the TPS6505x, the regulators can be sequenced by using the enable pins on each DCDC and LDO. A sequencer could be used but, simply looping back the output voltages of the preceeding rail to the enable input of the following rail can sequence the PMIC with minimal cost and solution area. Simple and small RC delay circuits could be added to create timing delays for enabling if needed.

Use the THRESHOLD and $\overline{\text{RESET}}$ feature to provide a logic signal to the application or processor. THRESHOLD requires a voltage divider if the signal being monitored is desired to trigger $\overline{\text{RESET}}$ at a point higher than 1V.

8.2.3 Application Curves

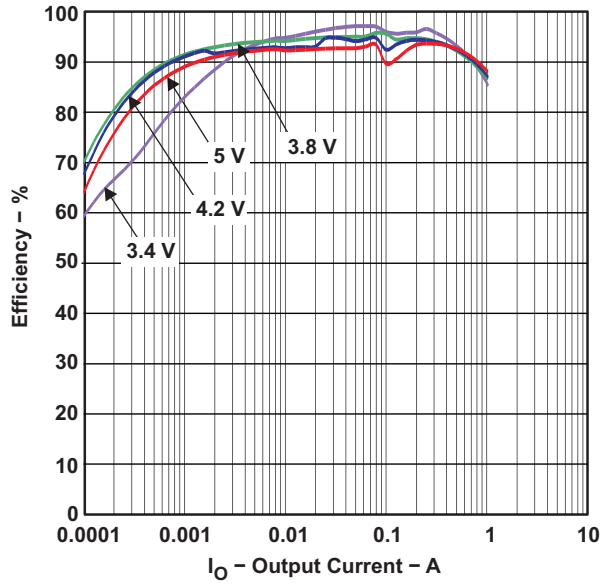


Figure 26. Efficiency Converter 1 on TPS65053

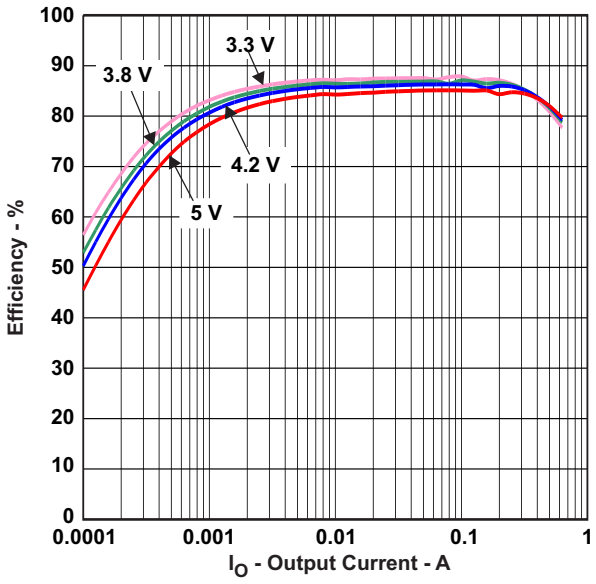


Figure 27. Efficiency Converter 2 on TPS65053

9 Power Supply Recommendations

Any supply between 2.5 V and 6 V will work as long as the power supply can supply enough current at the VIN voltage that the application demands.

10 Layout

10.1 Layout Guidelines

- The input capacitors for the DCDC converters should be placed as close as possible to the VINDCDC1/2 pin and the PGND1 and PGND2 pins.
- The inductor of the output filter should be placed as close as possible to the device to provide the shortest switch node possible, reducing the noise emitted into the system and increasing the efficiency.
- Sense the feedback voltage from the output at the output capacitors to ensure the best DC accuracy. Feedback should be routed away from noisey sources such as the inductor. If possible route on the opposing side as the swiitch node and inductor and place a GND plane between the feedback and the noisey sources or keepout underneath them entirely.
- Place the output capacitors as close as possible to the inductor to reduce the feedback loop as much as possible. This will ensure best regulation at the feedback point.
- Place the device as close as possible to the the most demanding or sensitive load. The output capacitors should be placed close to the input of the load. This will ensure the best AC performance possible.
- The input and output capacitors for the LDOs should be placed close to the device for best regulation performance.
- The use a one common ground plane is recommended for the device layout. The AGND can be separated from the PGND but, a large low parasitic PGND is required to connect the PGNDx pins to the CIN and external PGND connections.

10.2 Layout Example

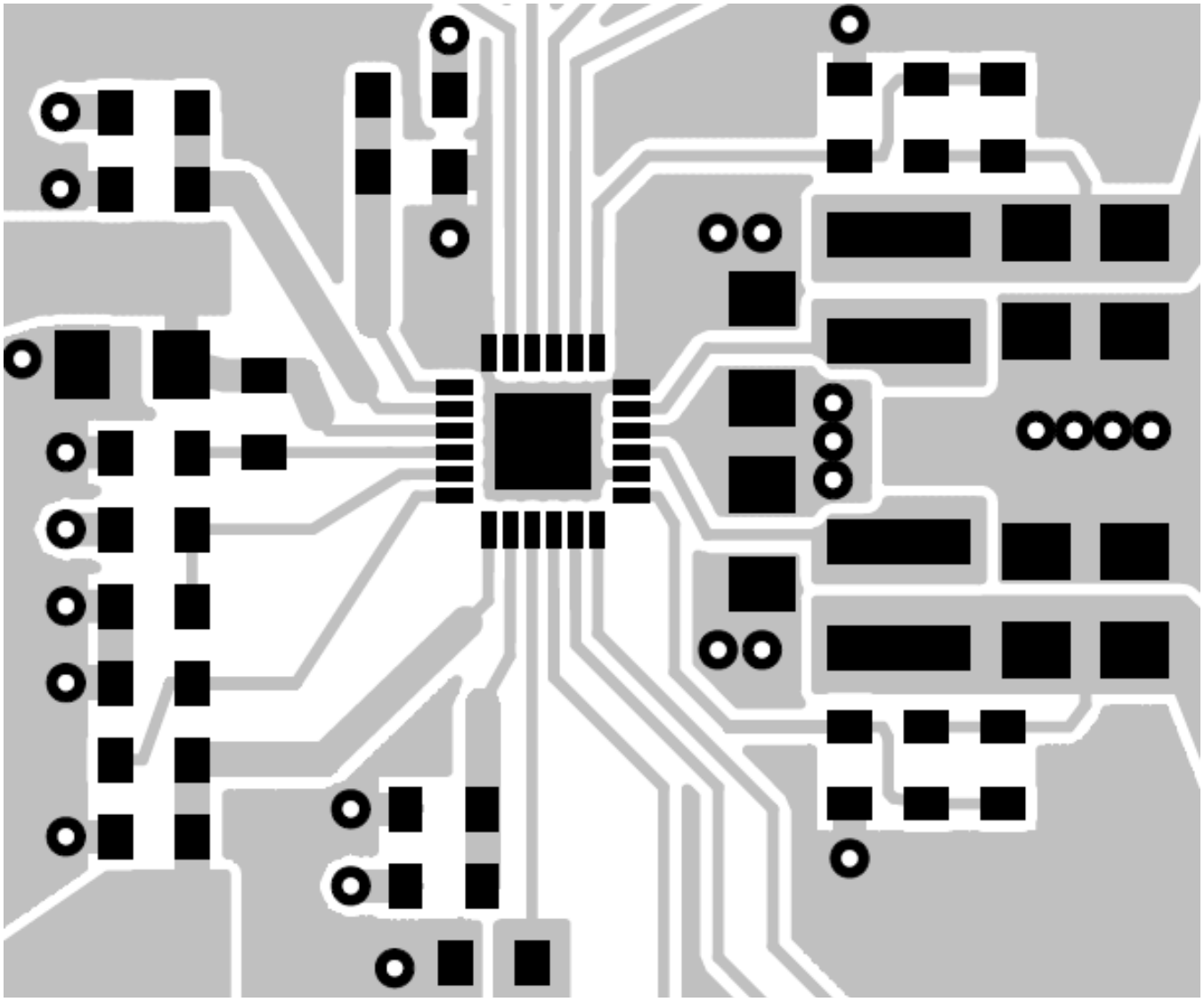


Figure 28. Layout Example Schematic for TPS65053

11 Device and Documentation Support

11.1 Device Support

For device support, submit questions to the E2E forum at:

http://e2e.ti.com/support/power_management/pmu/f/200

For frequently asked questions (FAQs) on the TPS6505x, refer to the FAQ at:

http://e2e.ti.com/support/power_management/pmu/w/design_notes/2910.tps6505x-faqs

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11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS65053	Click here	Click here	Click here	Click here	Click here
TPS650531	Click here	Click here	Click here	Click here	Click here
TPS650532	Click here	Click here	Click here	Click here	Click here
TPS65058	Click here	Click here	Click here	Click here	Click here

11.3 Trademarks

OMAP, PowerPAD are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS650531RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 650531	Samples
TPS650531RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 650531	Samples
TPS650532RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 650532	Samples
TPS650532RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 650532	Samples
TPS65053RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65053	Samples
TPS65053RGERG4	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65053	Samples
TPS65053RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65053	Samples
TPS65053RGETG4	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65053	Samples
TPS65058RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65058	Samples
TPS65058RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65058	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS65053 :

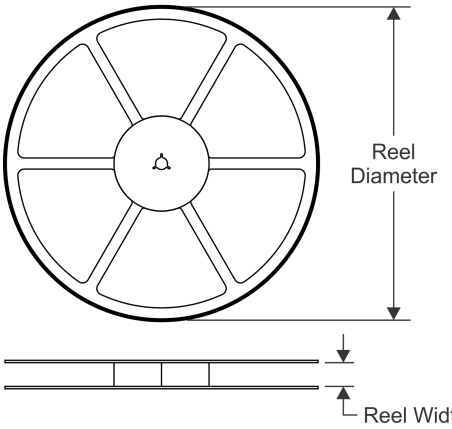
- Automotive: TPS65053-Q1

NOTE: Qualified Version Definitions:

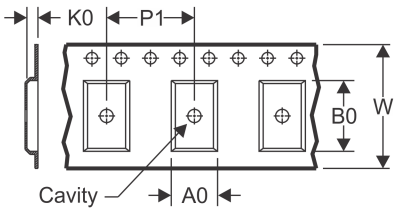
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

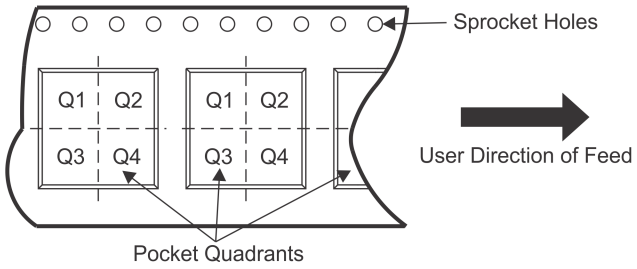


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

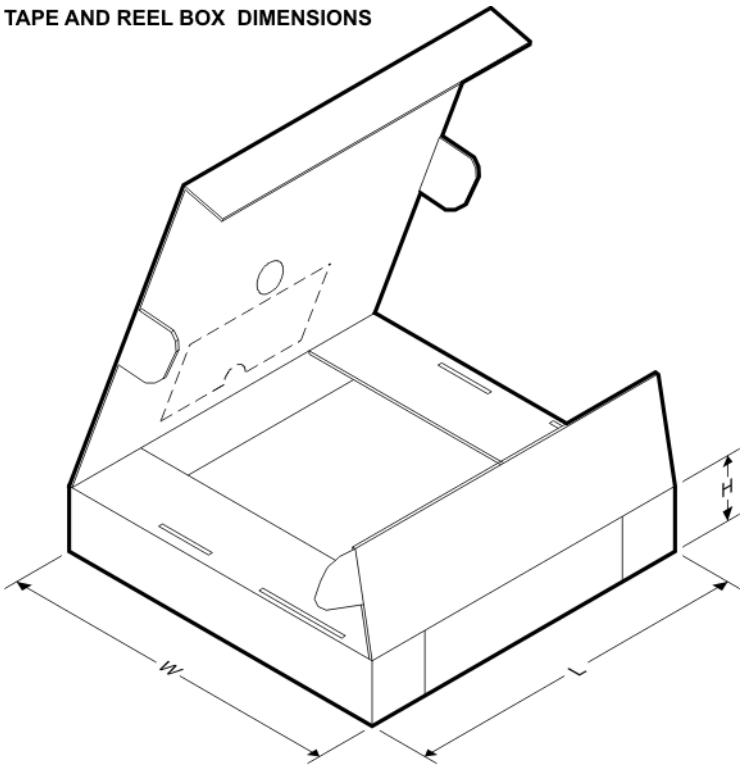
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS650531RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS650531RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS650532RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS650532RGER	VQFN	RGE	24	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2
TPS650532RGET	VQFN	RGE	24	250	180.0	12.5	4.35	4.35	1.1	8.0	12.0	Q2
TPS650532RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65053RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65053RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65058RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65058RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

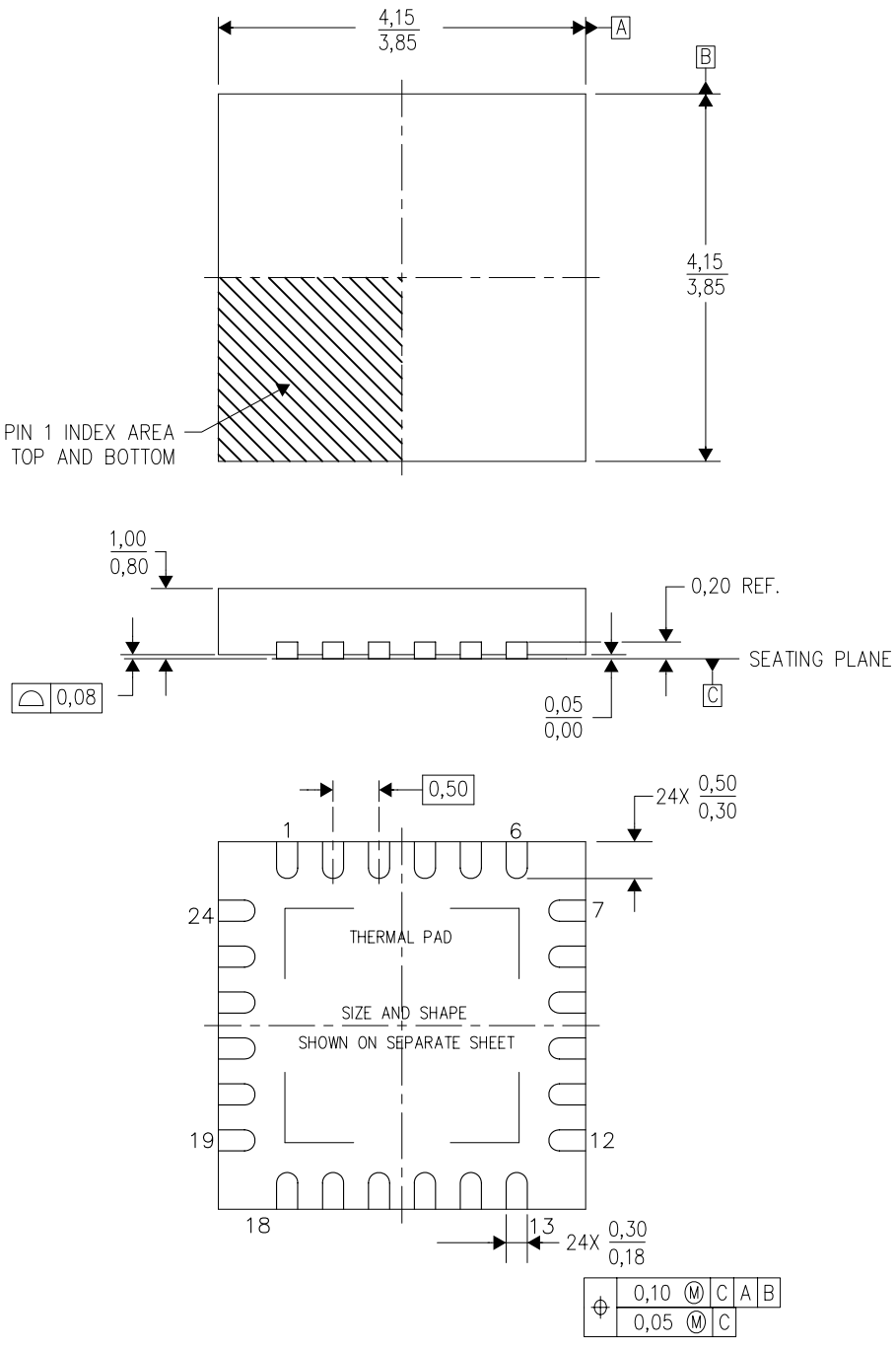
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS650531RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS650531RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS650532RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS650532RGER	VQFN	RGE	24	3000	338.0	355.0	50.0
TPS650532RGET	VQFN	RGE	24	250	338.0	355.0	50.0
TPS650532RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS65053RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS65053RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS65058RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS65058RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

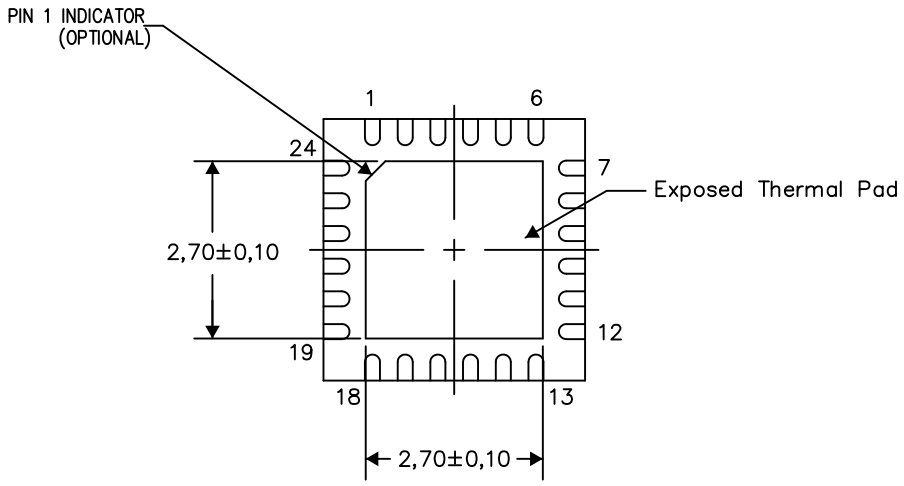
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



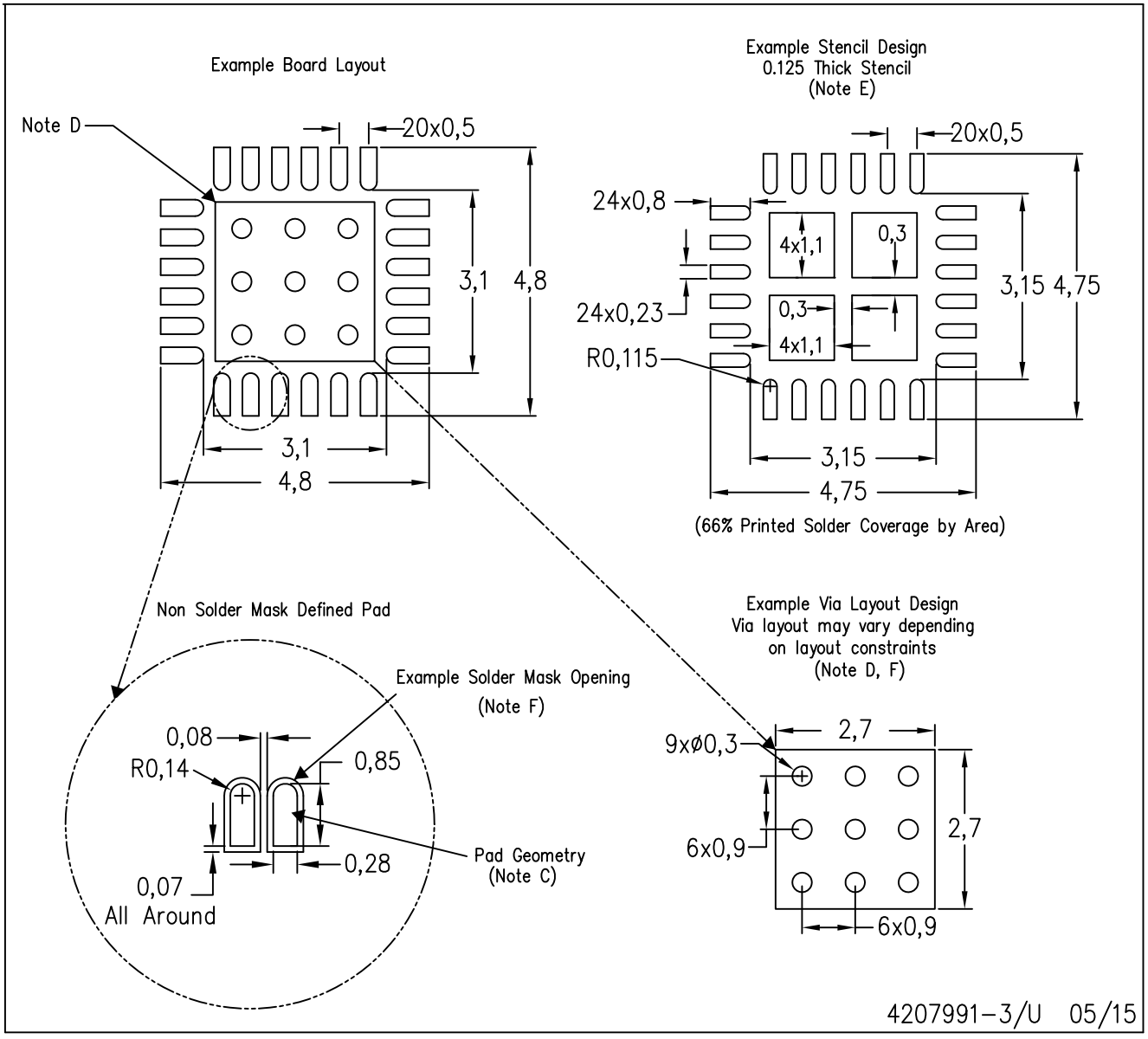
Bottom View

Exposed Thermal Pad Dimensions

4206344–5/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
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Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
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