TSU8111 Dual SP2T USB 2.0 High Speed Switch with Single Cell Charger

1 Features

- Dual Single-Pole Double-Throw (SP2T) USB 2.0 High Speed Switch
  - UART Path Supports either UART or USB 2.0 High Speed Signals
- Integrated Single-Cell Charger
  - Integrated Low Dropout Linear Regulator (LDO)
  - 1% Charge Voltage Regulation Accuracy
  - 8% Charge Current Accuracy
  - Programmable Charging Current Limit up to 950 mA for Wall Adapters
- USB Battery Charging Specification v1.1 (BCv1.1) Compliant Charger Detection
  - VBUS Detection
  - Data Contact Detection
  - Primary and Secondary Detection
  - USB Chargers (DCP, CDP, SDP) Supported
- 5-bit Accessory Detection on ID pin
  - Automatic Switching by Accessory Type
- I^2C Interface
  - Manual Switching Capability
  - Interrupts Generated for Attach and Detach
  - Supports Control Signals Used in Manufacturing (JIG, BOOT)
- 28-V Tolerance on VBUS Pin With Overvoltage Protection
- Thermal Regulation and Thermal Shutdown for Output Current Control
- JESD 22 ESD Performance
  - 12-kV Human Body Model (VBUS/DP_CON/DM_CON/ID_CON)
  - 2-kV Human Body Model (All Other Pins)
- IEC ESD Performance
  - ±4-kV Contact Discharge (IEC 61000-4-2) (VBUS/DP_CON/DM_CON/ID_CON to GND)
- Surge Protection on VBUS/DP_CON/DM_CON/ID_CON to GND
  - Protects USB Connector Pins Without External Components

2 Applications

- Mobile Phones
- Netbooks/Notebooks
- Tables
- Portable Handheld Devices

3 Description

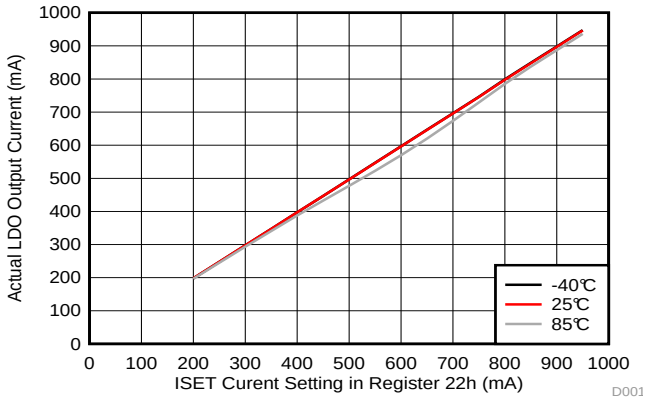
The TSU8111 is a dual single-pole double-throw (SP2T) micro-USB switch with an integrated linear charger. The integrated charger eliminates the need for an external charger IC, reducing cost and board space. The device operates from either a USB port or dedicated charger and supports charging currents of up to 950 mA. Power for the device is supplied through VBAT or through VBUS when attached. The TSU8111 detects BCv1.1-compatible chargers as well as accessories that use an ID resistor. The USB switch matrix can be controlled either by automatic detection or manually through I^2C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TSU8111	DSBGA (20)	2.14 mm × 1.76 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Actual Fast-charging Current vs Register Setting Across Device Temperature Range



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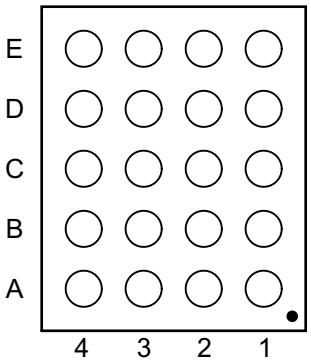
4 Revision History

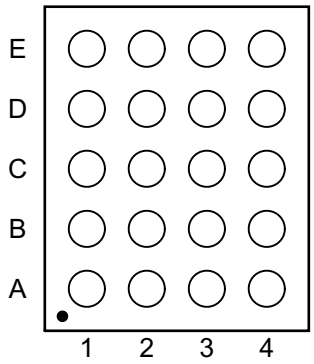
Changes from Original (September 2012) to Revision A	Page
• Changed this data sheet to new SDS format plus replaced all text, tables and graphics.	1

5 Pin Configuration and Functions

YFP Package
(TOP VIEW)



YFP Package
(BOTTOM VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	B2	O	BOOT mode used for factory test modes. Push-pull output (active high)
DM_CON	C4	I/O	USB DM connected to USB receptacle
DM_HT	D1	I/O	USB DM on device side
DP_CON	D4	I/O	USB DP connected to USB receptacle
DP_HT	E1	I/O	USB DP on device side
GND	A2, D3	—	Ground
ID_CON	E4	I/O	USB ID connected to USB receptacle
INTB	C3	O	Interrupt to host. Push-pull output (active high)
JIG	C2	O	JIG detection used for factory test modes. Open-drain output (active low)
RxD	C1	I/O	UART Rx – capable of passing USB 2.0 HS signals
SCL	E3	I	I^2C clock
SDA	E2	I/O	I^2C data
TxD	B1	I/O	UART Tx – capable of passing USB 2.0 HS signals
VBAT	A3, B3	I	Supply voltage from battery
VBUS	A4, B4	I	Supply voltage from micro-USB connector. Charger is enabled when this supply is present.
VDDIO	D2	I	I^2C and interrupt interface logic supply voltage
VLDO	A1	O	Low dropout regulator (LDO) charger output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage	V_{BAT}		–0.5	6	V
	V_{BUS}		–0.5	28	
	V_{DDIO}		–0.5	4.6	
Input-output terminal voltage, V_{IO}	V_{DM_CON}, V_{DP_CON}, V_{ID_CON}, V_{DP_HT}, V_{DM_HT}		–0.5	V_{BAT} + 0.5 (2)	V
	V_{RxD}, V_{TxD}		–0.5	V_{BAT} + 0.5 (2)	
	V_{SDA}		–0.5	4.6	
Output voltage	V_{LDO}		–0.5	6	V
	V_{JIG}		–0.5	V_{BAT} + 0.5 (2)	
	V_{INTB}, V_{BOOT}		–0.5	4.6	
Input current	I_{BAT}			1	A
	I_{BUS}			1	
	I_K	Analog port diode current	–50	50	mA
	I_{IK}	Digital logic input clamp current	–50		
	I_{SCL}		–50	50	
Input-output terminal current, I_{IO}	I_{SDA}		–50	50	mA
	$I_{IO(on)}$	On-state continuous switch current	–60	60	
	$I_{IO(peak)}$	On-state peak switch current	–150	150	
Output current	I_{LDO}			100	mA
	I_{GND}				
	I_{INTB}, I_{BOOT}		–50	50	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If V_{BUS} is present without V_{BAT}, then the absolute maximum voltage is V_{BUS} + 0.5 V, and shall not exceed 6 V in total.

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), stress voltage (1)	VBUS, DP_CON, DM_CON, ID_CON	–12	12	kV
		Charged device model (CDM), stress voltage (2)	All other pins	–2	2	
		IEC-61000-4-2 contact discharge		–4	4	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	V_{BAT}	3	4.4	V
	V_{BUS}	4	6.5	
	V_{DDIO}	1.65	3.6	
Input-output terminal voltage, V_{IO}	V_{DM_CON}, V_{DP_CON}, V_{ID_CON}, V_{DP_HT}, V_{DM_HT}, V_{RxD}, V_{TxD}	0	3.6	V
ID pin capacitance	C_{ID}		1	nF
LDO output capacitance	C_{LDO}	1		
Operating free-air temperature	T_A	–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		TSU8111 YFP 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	10.4	
ψ_{JT}	Junction-to-top characterization parameter	1.8	
ψ_{JB}	Junction-to-board characterization parameter	10.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{BAT} = 3 V to 4.4 V, V_{DDIO} = 2.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
USB and UART PATHS[1]							
R_{ON}	On-state resistance	V_I = 0 V to 3.6 V, I_O = –2 mA, V_{BAT} = 3.6 V			8		Ω
ΔR_{ON}	On-state resistance match between channels	V_I = 0.4 V, I_O = –2 mA, V_{BAT} = 3.6 V			0.5		Ω
$R_{ON(flat)}$	On-state resistance flatness	V_I = 0 V to 3.6 V, I_O = –2 mA, V_{BAT} = 3.6 V			0.7		Ω
$I_{IO(OFF)}$	Off-state leakage current	V_I = 0.3 V, V_O = 2.7 V or V_I = 2.7 V, V_O = 0.3 V, V_{BAT} = 4.4 V, Switch off			45		nA
$I_{IO(ON)}$	On-state leakage current	V_I = OPEN, V_O = 0.3 V or 2.7 V, $V_{BA}T$ = 4.4 V, Switch on			50		nA
$C_{I(OFF)}$	Off-state capacitance at input	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch off			4		pF
$C_{O(OFF)}$	Off-state capacitance at output	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch off			7.5		pF
$C_{I(ON)}$	On-state capacitance at input	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch off			8.6		pF
$C_{O(ON)}$	On-state capacitance at output	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch off			8.6		pF
BW	Bandwidth	R_L = 50 Ω, Switch on			820		MHz
O_{ISO}	Off isolation	f = 240 MHz, R_L = 50 Ω, Switch off			-36		dB
X_{TALK}	Crosstalk	f = 240 MHZ, R_L = 50 Ω			-35		dB
LINEAR CHARGER[2]							
$V_{CHG(OK)}$	Charger input voltage OK threshold	$V_{BUS} – V_{BAT}$	Rising		250		mV
			Falling		45		
$V_{BUS(OVP)}$	VBUS over-voltage protection (default 7.5 V)	I^2C register 22h [7:6] = 00			6		V
		I^2C register 22h [7:6] = 01			6.5		
		I^2C register 22h [7:6] = 10			7		
		I^2C register 22h [7:6] = 11			7.5		

(1) V_O is equal to the asserted voltage on DP_CON and DM_CON. V_I is equal to the asserted voltage on DP_HT and DM_HT pins. I_O is equal to the current out of the DP_CON and DM_CON pins. I_I is equal to the current into the DP_HT and DM_HT pins.
(2) Fast charging current will fall below listed values when junction temperature rises above 85°C due to thermal regulation circuitry.

Electrical Characteristics (continued)

V_{BAT} = 3 V to 4.4 V, V_{DDIO} = 2.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BUS(OVP,fail)}$	VBUS over-voltage falling threshold for restart charging			320		mV
V_{PRECHG}	Pre-charge threshold voltage			2.5		V
$V_{CHG(RST)}$	Charge restart threshold (default 100 mV)	I^2C register 20h [6:5] = 00		130		mV
		I^2C register 20h [6:5] = 01		130		
		I^2C register 20h [6:5] = 10		190		
		I^2C register 20h [6:5] = 11		240		
$V_{DO(LDO)}$	LDO dropout voltage	V_{BUS} = 4.5 V, I_{LDO} = 50 mA		150		mV
V_{LDO}	LDO output voltage	$V_{LDO} + V_{DO(LDO)} \le V_{BUS} \le V_{BUS(OVP)}$		4.9		V
I_{LDO}	LDO output current	V_{LDO} = 0 V			50	mA
I_{PRECHG}	Default pre-charge current	V_{BAT} = 2 V		90		mA
C_{LDO}	LDO output capacitance			1		µF
T_{PRECHG}	Pre-charge timeout			30		min
V_{SET}	Charging voltage	I^2C register 21h [3:0] = 0000		4		V
		I^2C register 21h [3:0] = 0001		4.02		
		I^2C register 21h [3:0] = 0010		4.04		
		I^2C register 21h [3:0] = 0011		4.06		
		I^2C register 21h [3:0] = 0100		4.08		
		I^2C register 21h [3:0] = 0101		4.1		
		I^2C register 21h [3:0] = 0110		4.12		
		I^2C register 21h [3:0] = 0111		4.14		
		I^2C register 21h [3:0] = 1000		4.16		
		I^2C register 21h [3:0] = 1001		4.18		
		I^2C register 21h [3:0] = 1010 (default)		4.2		
		I^2C register 21h [3:0] = 1011		4.22		
		I^2C register 21h [3:0] = 1100		4.24		
		I^2C register 21h [3:0] = 1101		4.26		
		I^2C register 21h [3:0] = 1110		4.28		
		I^2C register 21h [3:0] = 1111		4.35		
I_{SET}	Fast charging current	I^2C register 22h [3:0] = 0000		200		mA
		I^2C register 22h [3:0] = 0001		250		
		I^2C register 22h [3:0] = 0010		300		
		I^2C register 22h [3:0] = 0011		350		
		I^2C register 22h [3:0] = 0100		400		
		I^2C register 22h [3:0] = 0101 (default)		450		
		I^2C register 22h [3:0] = 0110		500		
		I^2C register 22h [3:0] = 0111		550		
		I^2C register 22h [3:0] = 1000		600		
		I^2C register 22h [3:0] = 1001		650		
		I^2C register 22h [3:0] = 1010		700		
		I^2C register 22h [3:0] = 1011		750		
		I^2C register 22h [3:0] = 1100		800		
		I^2C register 22h [3:0] = 1101		850		
		I^2C register 22h [3:0] = 1110		900		
		I^2C register 22h [3:0] = 1111		950		
		Charging current accuracy	-8%		8%	

Electrical Characteristics (continued)

V_{BAT} = 3 V to 4.4 V, V_{DDIO} = 2.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{FULL}	Full charge current	I^2C register 22h [7:4] = 0000		50		mA
		I^2C register 22h [7:4] = 0001		60		
		I^2C register 22h [7:4] = 0010		70		
		I^2C register 22h [7:4] = 0011		80		
		I^2C register 22h [7:4] = 0100		90		
		I^2C register 22h [7:4] = 0101 (default)		100		
		I^2C register 22h [7:4] = 0110		110		
		I^2C register 22h [7:4] = 0111		120		
		I^2C register 22h [7:4] = 1000		130		
		I^2C register 22h [7:4] = 1001		140		
		I^2C register 22h [7:4] = 1010		150		
		I^2C register 22h [7:4] = 1011		160		
		I^2C register 22h [7:4] = 1100		170		
		I^2C register 22h [7:4] = 1101		180		
		I^2C register 22h [7:4] = 1110		190		
		I^2C register 22h [7:4] = 1111		200		
I^2C INTERFACE (SCL and SDA)						
V_{IH}	High-level input voltage		V_{DDIO} × 0.7		V_{DDIO}	V
V_{IL}	Low-level input voltage		0		V_{DDIO} × 0.3	V
V_{OH}	High-level output voltage	I_{OH} = –3 mA	V_{DDIO} × 0.7		V_{DDIO}	V
V_{OL}	Low-level output voltage	I_{OL} = 3 mA	0		0.4	V
DIGITAL SIGNAL OUTPUTS – JIG, INTB, and BOOT						
$V_{OL(JIG)}$	Low-level output voltage	I_{OL} = 10 mA, V_{BAT} = 3.0 V			0.5	V
$V_{OH(INTB,BOOT)}$	High-level output voltage	I_{OH} = -4 mA, V_{DDIO} = 1.65 V	1.16		V_{DDIO}	V
$V_{OL(INTB,BOOT)}$	Low-level output voltage	I_{OL} = 4 mA, V_{DDIO} = 1.65 V	0		0.33	V
CURRENT CONSUMPTION						
$I_{BAT(standby)}$	VBAT standby current consumption	V_{BUS} = 0 V, idle state		27	36	µA
$I_{BAT(operating)}$	VBAT operating current consumption	V_{BUS} = 0 V, USB switch closed		100	150	µA
I_{BUS}	VBUS operating current consumption	V_{BUS} = 5 V, VBAT floating	0.6		0.75	mA
VOLTAGE PROTECTION						
$V_{BUS(UVLO)}$	V_{BUS} under voltage – upper threshold	V_{BUS} rising		2.85		V
	V_{BUS} under voltage – lower threshold	V_{BUS} falling		2.55		
$V_{BUS(valid)}$	V_{BUS} interrupt threshold	V_{BUS} rising		3.6		V
$V_{BAT(UVLO)}$	V_{BAT} under voltage – upper threshold	V_{BAT} rising		2.65		V
	V_{BAT} under voltage – lower threshold	V_{BAT} falling		2.45		

6.6 Timing Requirements

		MIN	TYP	MAX	UNIT
f_{SCL}	I^2C clock frequency	64		400	kHz

6.7 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Switch turn-on time	From receipt of I^2C ACK bit		57		µs
t_{off}	Switch turn-off time	From receipt of I^2C ACK bit		5.2		µs

6.8 Typical Characteristics

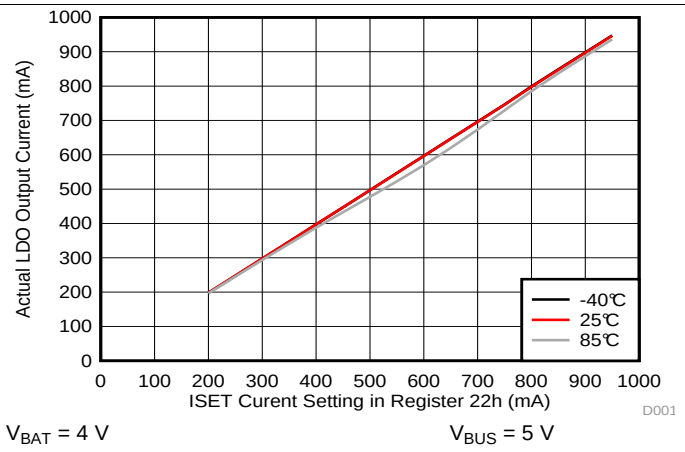


Figure 1. Actual Fast-charging Current vs Register Setting Across Device Temperature Range

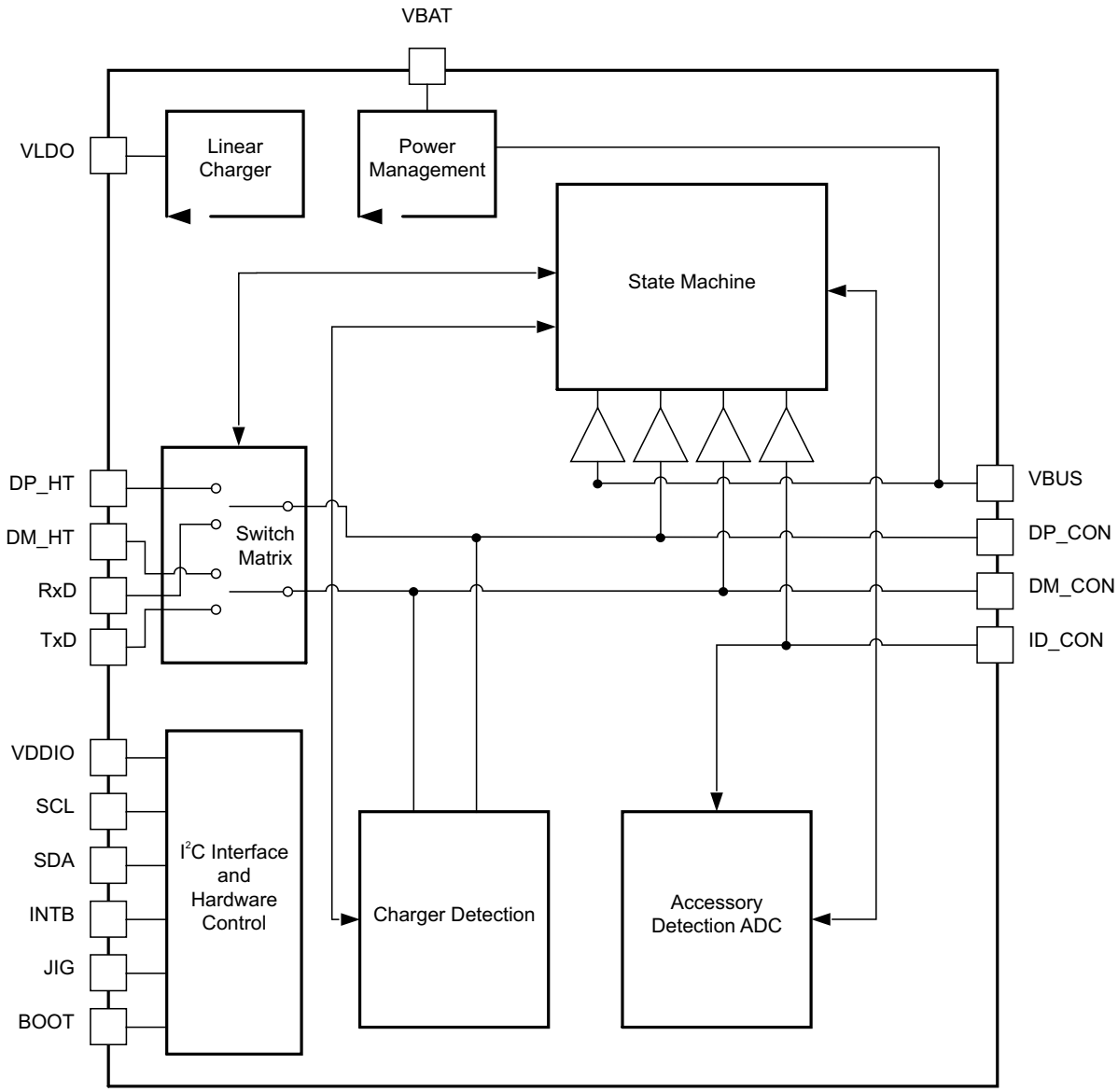
7 Detailed Description

7.1 Overview

The TSU8111 is designed to interface a portable device (PD) to external peripherals through a micro-USB connector.

The device will automatically detect accessories via the mini-USB or micro-USB 5-pin connectors. The type of accessory detected will be stored in the TSU8111's I^2C registers, and can be read by the host processor. The TSU8111 has a network of USB 2.0 High Speed switches that can be automatically opened and closed based on the accessory detected. See *Automatic Switching Mode* for details of which switches are closed during each mode of operation. The TSU8111 also offers a manual switching mode through I^2C, allowing the host processor to decide which switches will be opened and closed.The TSU8111 also provides a linear charger with a maximum programmable charging current of 950 mA.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Linear Charger

The TSU8111 has a linear battery charger with charging currents adjustable from 200 mA to 950 mA. If 3.7 V < V_{BUS} < 7.5 V and V_{BUS} > V_{BAT} + 250 mV, then the charger starts charging automatically. If V_{BAT} < V_{PRECHG}, the device starts with a pre-charge mode with a charging current of 90 mA. Once V_{BAT} reaches V_{PRECHG}, the device switches to fast charge mode with soft start. When V_{BAT} approaches V_{SET}, constant-voltage (CV) charging mode starts with programmed regulation voltage. At CV mode, if the charging current reaches the programmed full charge current, the TSU8111 will generate an interrupt to the host indicating a full charge and will start the charger shutoff timer. If the shutoff timer is disabled, the charger stays at CV mode until stopped by the host processor.

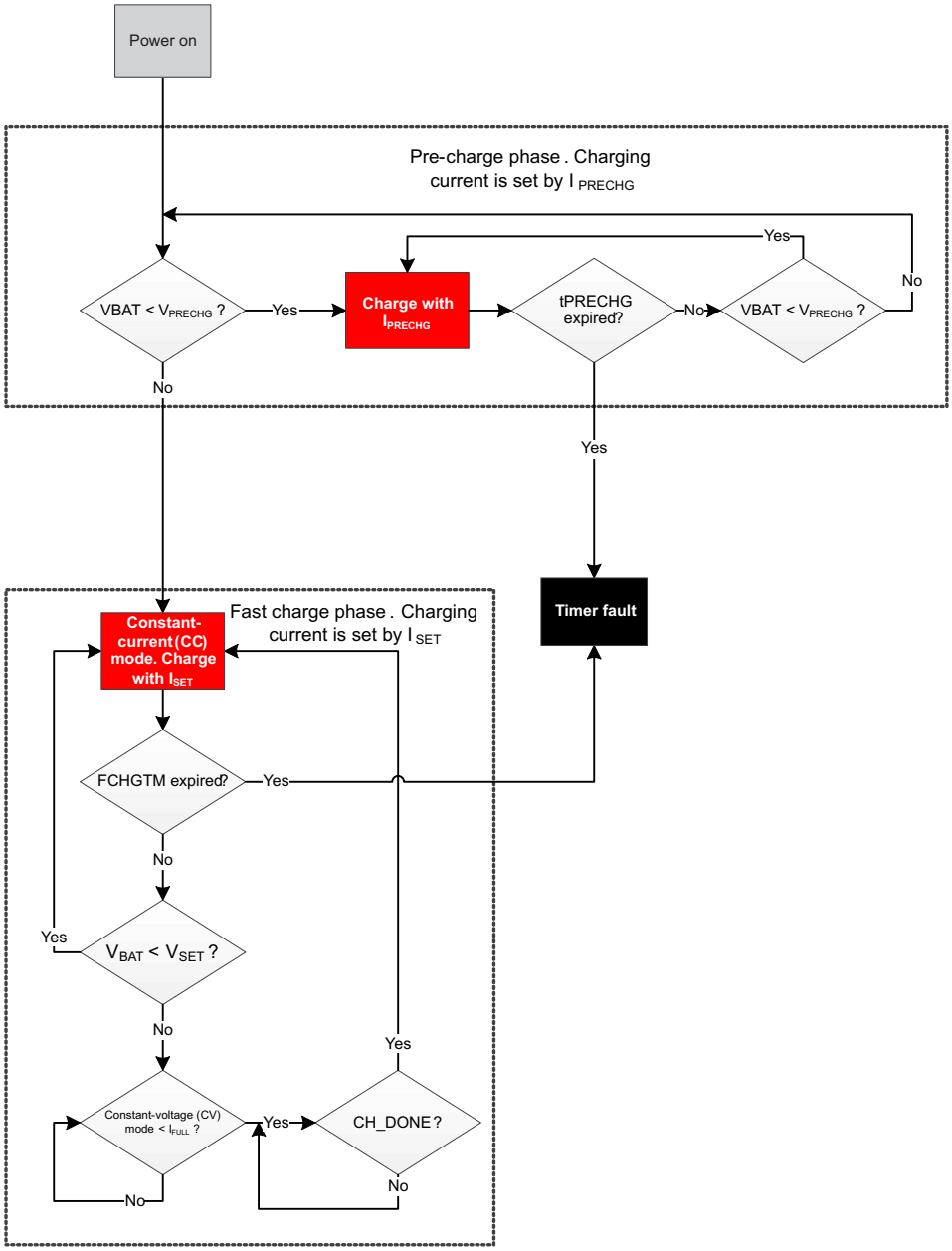


Figure 2. TSU8111 Charger Flow Chart

Feature Description (continued)

7.3.2 Voltage Protection

7.3.2.1 Overvoltage Protection

When V_{BUS} rises above $V_{BUS(OVP)}$, the linear charger is turned off, removing power from the circuit. The OVP EN interrupt bit is set high when an overvoltage condition is detected. When the input voltage returns below $V_{BUS(OVP)} – V_{BUS(OVP(hys))}$ and remains above $V_{BUS(UVLO)}$, the charger is turned on again.

7.3.2.2 Undervoltage Protection

The TSU8111 is powered off when V_{BUS} and V_{BAT} are below the lower thresholds of $V_{BUS(UVLO)}$ and $V_{BAT(UVLO)}$. When V_{BAT} rises above 2.5 V, the device will be turned on but the linear charger will remain powered off. Both the TSU8111 and the linear charger will only be turned on when V_{BUS} > 3.7 V and $V_{BUS} – V_{BAT}$ > 250 mV.

7.3.3 Power-on Reset

When power is applied to VBAT, an internal power-on reset holds the TSU8111 in a reset condition. When V_{BAT} reaches V_{POR}, the TSU8111 I^2C registers and state machine initialize to their default states.

After the initial power-up phase, V_{BAT} must be lowered below 0.2 V and then back up to V_{DDIO} to initiate a power reset cycle.

7.3.4 Software Reset

To initiate a software reset on the TSU8111, perform the steps below:

1. Hold SDA and SCL low for at least 30 ms to reset the digital logic of the TSU8111.
2. Write a 1 to bit 0 of register 1Bh. This will reset the TSU8111, and the bit will be cleared after the reset. After the reset, INTB will keep low until the INT Mask bit of register 02h is cleared.

7.3.5 Power Supervisor

The TSU8111 uses V_{BAT} as the primary supply voltage. V_{BUS} is the secondary supply. V_{DDIO} is used for I^2C communication.

7.4 Device Functional Modes

7.4.1 Standby Mode

Standby mode is the default mode upon power up and occurs when no accessory is attached. During this time, the VBUS and ID lines are continually monitored through comparators to determine when an accessory is attached. If an accessory is attached, then the TSU8111 will enter either automatic or manual switching mode, depending on bit 2 in register 02h.

7.4.2 Automatic Switching Mode

The TSU8111 uses a current source and an internal comparator to detect a resistance on the ID pin. The current source creates V_{ID} on the ID pin, which is compared to a changing V_{REF} input to the comparator. An incrementing 5-bit counter increases VREF until the comparator output changes. At this point, the TSU8111 latches the 5-bit counter value and determines the accessory type from Table 1.

When the TSU8111 detects VBUS but no ID resistor, the TSU8111 runs charger detection on the DP and DM lines. The TSU8111 can detect chargers compatible with the USB Battery Charging Specification version 1.1 (BCv1.1). The switch status for the BCv1.1 charger types can be found at the end of Table 1.

Device Functional Modes (continued)

Table 1. Accessory and Charger Detection Lookup Table

ACCESSORY	DETECTED IMPEDANCE ON ID (kΩ)	RESISTOR TOLERANCE (%)	5-BIT COUNTER ADC VALUE	SWITCH STATE		FACTORY CABLE	
				DP / DM			
				DP_HT / DM_HT	RxD / TxD	JIG	BOOT
OTG	0	N/A	00000	**ON**	OFF	OFF	OFF
MHL	1	5	00000	OFF	OFF	OFF	OFF
Audio Device Type 3	28.7	5	01110	OFF	OFF	OFF	OFF
Reserved Accessory #1	34	5	01111	OFF	OFF	OFF	OFF
Reserved Accessory #2	40.2	5	10000	OFF	OFF	OFF	OFF
Reserved Accessory #3	49.9	5	10001	OFF	OFF	OFF	OFF
Reserved Accessory #4	64.9	5	10010	OFF	OFF	OFF	OFF
Audio Device Type 2	80.27	5	10011	OFF	OFF	OFF	OFF
Phone Powered Device	102	5	10100	OFF	**ON**	OFF	OFF
TTY Converter	121	5	10101	OFF	OFF	OFF	OFF
UART Cable	150	5	10110	OFF	**ON**	OFF	OFF
Type 1 Charger	200	5	10111	**ON**	OFF	OFF	OFF
Factory Mode Cable – Boot Off USB	255	5	11000	**ON**	OFF	**ON**	OFF
Factory Mode Cable – Boot On USB	301	5	11001	**ON**	OFF	**ON**	**ON**
Audio / Video Cable	365	5	11010	OFF	OFF	OFF	OFF
Type 2 Charger	442	5	11011	**ON**	OFF	OFF	OFF
Factory Mode Cable – Boot Off UART	523	5	11100	OFF	**ON**	**ON**	OFF
Factory Mode Cable – Boot On UART	619	5	11101	OFF	**ON**	**ON**	**ON**
Stereo Headset with Remote (Audio Device Type 1)	1000.07	10	11110	OFF	OFF	OFF	OFF
Monio/Stereo Headset (Audio Device Type 1)	1002	10	11110	OFF	OFF	OFF	OFF
No ID	N/A	N/A	11111	OFF	OFF	OFF	OFF
USB Standard Downstream Port (SDP)	N/A	N/A	11111	**ON**	OFF	OFF	OFF
USB Charging Downstream Port (CDP)	N/A	N/A	11111	**ON**	OFF	OFF	OFF
Dedicated Charging Port (DCP)	N/A	N/A	11111	OFF	OFF	OFF	OFF

7.4.3 Manual Switching Mode

Write a 0 to bit 2 of register 02h to enable manual switching mode. The switch status of DP and DM can then be controlled by writing to register 13h [7:2]. See *Register Map* for details about switch status using register 13h.

7.5 Programming

The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^2C communication with this device is initiated by the master sending a START condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 3). After the start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

Programming (continued)

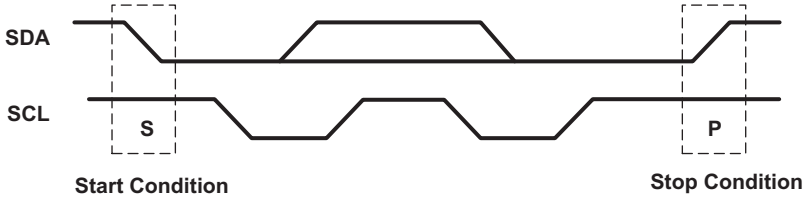


Figure 3. Definition of START and Stop Conditions

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data are the output only if complete bytes are received and acknowledged. The output data is valid at time tpv after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I^2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (START or STOP). See Figure 4.

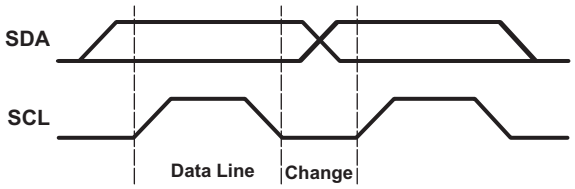


Figure 4. Bit Transfer

A STOP condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 3).

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitted must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 5). Setup and hold times must be taken into account.

Programming (continued)

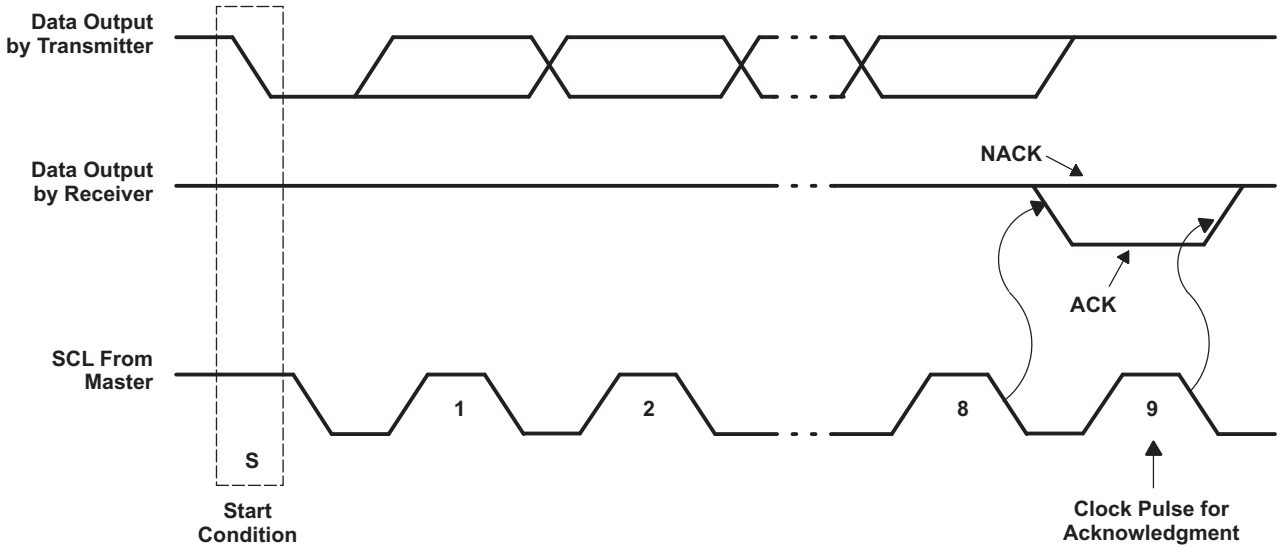


Figure 5. Acknowledgement on I2C Bus

7.5.1 Writes

Data is transmitted to the TSU8111 by sending the device slave address and setting the LSB to a logic 0 (see Figure 6 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. The next byte is written to the specified register on the rising edge of the ACK clock pulse.

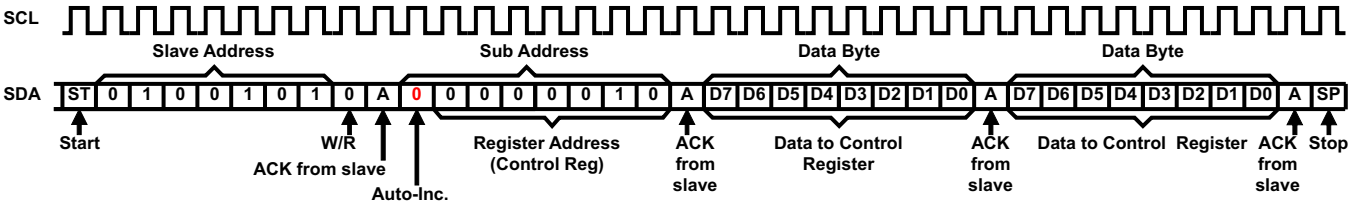


Figure 6. Repeated Data Write to a Single Register

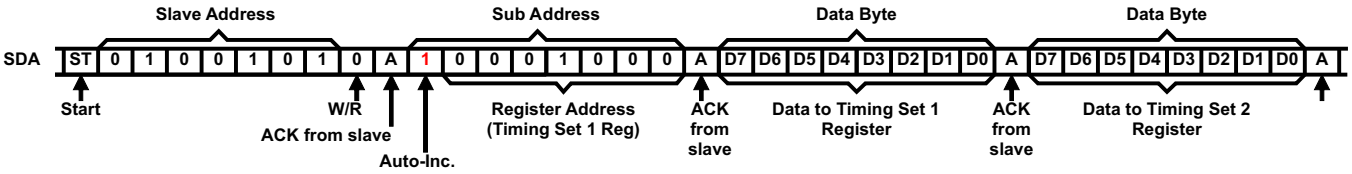


Figure 7. Burst Data Write to Multiple Registers

7.5.2 Reads

The bus master must first send the TSU8111 slave address with the LSB set to logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device slave address is sent again but, this time, the LSB is set to logic 1. Data from the register defined by the command byte then is sent by the TSU8111. Data is clocked into the SDA output shift register on the rising edge of the ACK clock pulse, see Figure 8.

Programming (continued)

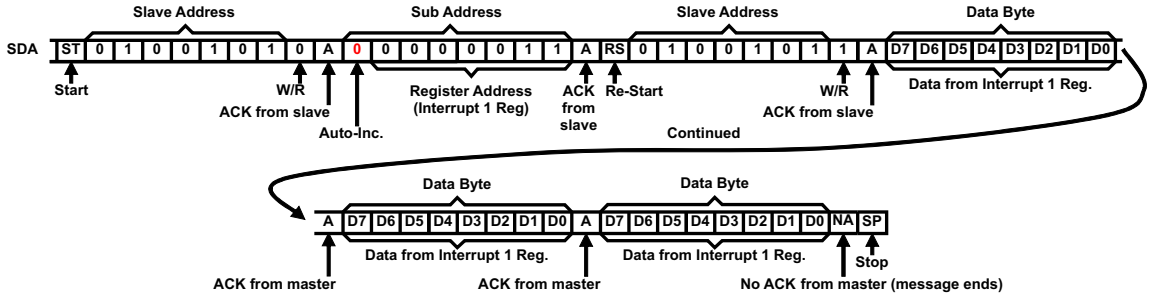


Figure 8. Repeated Data Read from a Single Register – Combined Mode

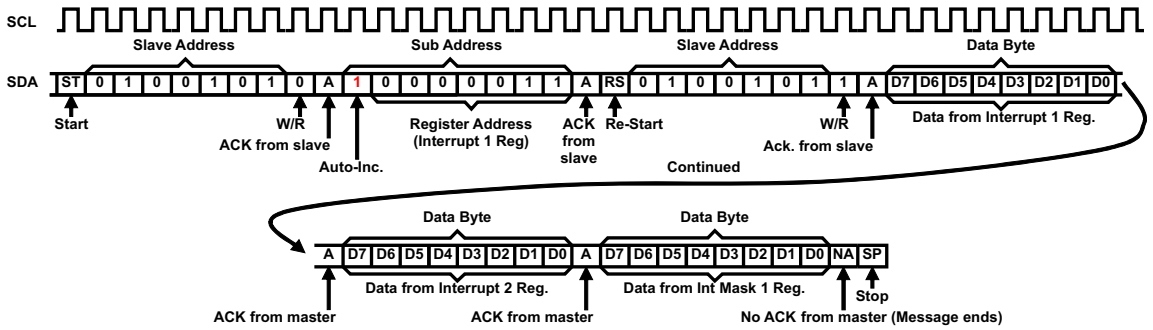


Figure 9. Burst Data Read from Multiple Registers – Combined Mode

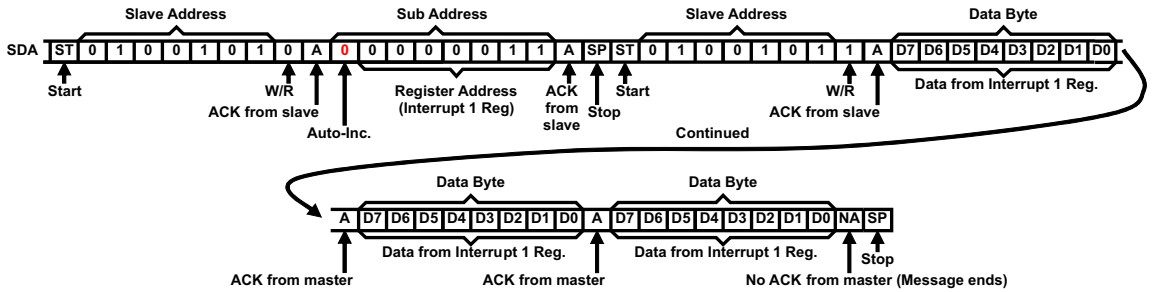


Figure 10. Repeated Data Read from a Single Register – Split Mode

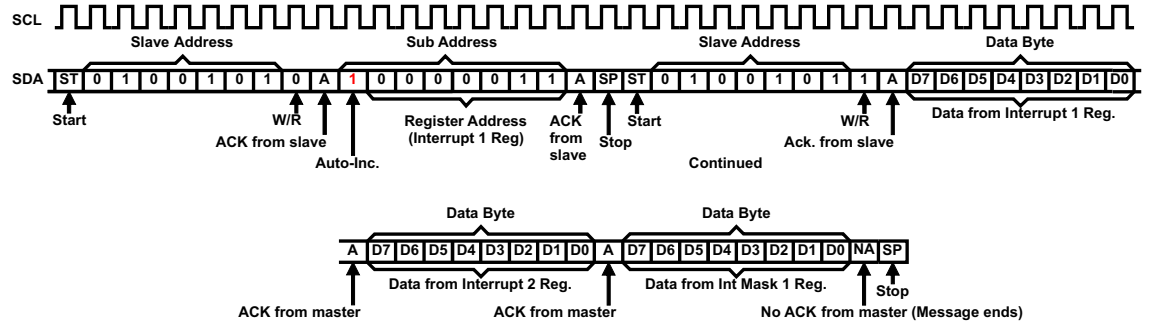


Figure 11. Burst Data Read from Multiple Registers – Split Mode

Programming (continued)

Additional notes on I^2C interface:

1. SDA is pulled low on ACK from either the slave or the master.
2. Register writes always require sub-address writes before the first data byte.
3. Repeated data writes to a single register continue indefinitely until stop or restart.
4. Repeated data reads from a single register continue indefinitely until no ACK from master.
5. Burst data writes start at the specified register address, then advance to the next register address, even to the read-only registers. For these registers, data write appears to occur, though no data are changed by the writes. After register 14h is written, writing resumes to register 01h and continues until stop or restart.
6. Burst data reads start at the specified register address, then advance to the next register address. Once register 14h is read, reading resumes from register 01h and continues until no ACK from master.

7.6 Register Map(1)(2)

(1) Write “0” to the blank register bits.
(2) Values read from the blank register bits are invalid and undefined.

ADDR	REGISTER	TYPE	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
01h	Device ID	R	1011010	Version ID					Vendor ID		
02h	Control	R/W	xxx11111				Switch Open	Raw Data	Manual Sw.	Wait	INT Mask
03h	Interrupt 1	R	x0000000		VBUS	OVP EN	LKR	LKP	KP	Detach	Attach
04h	Interrupt 2	R	x0000000		OTP EN	CONNECT	Stuck Key RCV	Stuck Key	ADC Change	Reserved Attach	A/V Charging
05h	Interrupt Mask 1	R/W	x0000000		VBUS	OVP EN	LKR	LKP	KP	Detach	Attach
06h	Interrupt Mask 2	R/W	x0000000		OTP EN	CONNECT	Stuck Key RCV	Stuck Key	ADC Change	Reserved Attach	Charging A/V
07h	ADC	R	xxx11111				ADC Value				
08h	Timing Set 1	R/W	0	Key Press				Device Wake Up			
09h	Timing Set 2	R/W	0	Switching Wait				Long Key Press			
0Ah	Device Type 1	R	0	USB OTG	DCP	CDP	Type 1 / Type 2 charger	UART	USB	VBUS	MHL
0Bh	Device Type 2	R	0	Audio Type 3	Audio / Video	TTY	PPD	JIG UART OFF	JIG UART ON	JIG USB OFF	JIG USB ON
0Ch	Button 1	R	0	7	6	5	4	3	2	1	Send End
0Dh	Button 2	R	x0000000		Unknown	Error	12	11	10	9	8
13h	Manual SW 1	R/W	000000xx	DM Switching			DP Switching				
14h	Manual SW 2	R/W	xxxx00xx					BOOT SW	JIG ON		
1Bh	Reset	W	11111111								Reset
20h	Charger Control 1	R/W	11000	CH DIS	CHRSTTH		CHENOV	FCMEN		FCHGTM	
21h	Charger Control 2	R/W	11010	IFULL				CV SET			
22h	Charger Control 3	R//W	11010101	OVPV		AUTOSTOP	ISET L	ISET			
24h	Charger Interrupt	R	xx0xxxxx			CH FAULT	CH DONE	CH CV	CH FC	CH PC	CH IDLE
25h	Charger Interrupt Mask	R/W	xx0xxxxx			CH FAULT	CH DONE	CH CV	CH FC	CH PC	CH IDLE
26h	Charger Status	R	xx0xxxxx	FTE	PTE	CH FAULT	CH DONE	CH CV	CH FC	CH PC	CH IDLE

7.6.1 Device ID (01h) Register Field Descriptions

Table 2. Device ID (01h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Version ID	R	01011	Unique identifier for chip version (01011)
2-0	Vendor ID	R	010	Unique identifier 010 for Texas Instruments

7.6.2 Control (02h) Register Field Descriptions

Table 3. Control (02h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Blank	N/A	N/A	N/A
4	Switch Open	R/W	1	0: Open all switches 1: Automatic switching by accessory detection
3	Raw Data	R/W	1	0: Continue reading ID pin resistance after impedance has been detected 1: When ID resistance is connected, do not run ID detection again until the next attach/detach
2	Manual Sw.	R/W	1	0: Manual switching mode enabled and controlled by register 13h 1: Automatic switching by accessory detection
1	Wait	R/W	1	0: Wait until host resets this bit high 1: Wait until switching timer has expired
0	INT Mask	R/W	1	0: Unmask interrupt 1: Mask interrupt

7.6.3 Interrupt 1 (03h) Register Field Descriptions

Table 4. Interrupt 1 (03h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Unused	N/A	N/A	N/A
6	VBUS	R/Clr	0	1: VBUS detected
5	OVP EN	R/Clr	0	1: Overvoltage detected
4	LKR	R/Clr	0	1: Long key release
3	LKP	R/Clr	0	1: Long key press
2	KP	R/Clr	0	1: Key press
1	Detach	R/Clr	0	1: Accessory detach detected
0	Attach	R/Clr	0	1: Accessory attach detected

7.6.4 Interrupt 2 (04h) Register Field Descriptions

Table 5. Interrupt 2 (04h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Unused	N/A	N/A	N/A
6	OTP EN	R	0	1: Over-temperature protection enabled
5	Connect	R	0	1: Switch is connected (closed)
4	Stuck Key RCV	R	0	1: Stuck key is recovered
3	Stuck Key	R	0	1: Stuck key is detected
2	ADC_Change	R	0	1: ADC value is changed when Raw Data is enabled
1	Reserved_Attach	R	0	1: Reserved device is attached
0	A/V_Charging	R	0	1: Charger detected when A/V cable is attached

7.6.5 Interrupt Mask 1 (05h) Register Field Descriptions

Table 6. Interrupt Mask 1 (05h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Unused	N/A	N/A	N/A
6	VBUS	R/W	0	0: Unmask VBUS interrupt 1: Mask VBUS interrupt
5	OVP EN	R/W	0	0: Unmask OVP EN interrupt 1: Mask OVP EN interrupt
4	LKR	R/W	0	0: Unmask long key release interrupt 1: Mask long key release interrupt
3	LKP	R/W	0	0: Unmask long key press interrupt 1: Mask long key press interrupt
2	KP	R/W	0	0: Unmask key press interrupt 1: Mask key press interrupt
1	Detach	R/W	0	0: Unmask detach interrupt 1: Mask detach interrupt
0	Attach	R/W	0	0: Unmask attach interrupt 1: Mask attach interrupt

7.6.6 Interrupt Mask 2 (06h) Register Field Descriptions

Table 7. Interrupt Mask 2 (06h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Unused	R/W	N/A	N/A
6	OTP EN	R/W	0	0: Unmask OTP EN interrupt 1: Mask OTP EN interrupt
5	Connect	R/W	0	0: Unmask connect interrupt 1: Mask connect interrupt
4	Stuck Key	R/W	0	0: Unmask Stuck Key RCV interrupt 1: Mask Stuck Key RCV interrupt
3	Stuck Key	R/W	0	0: Unmask Stuck Key interrupt 1: Mask Stuck Key interrupt
2	ADC Change	R/W	0	0: Unmask ADC Change interrupt 1: Mask ADC Change interrupt
1	Reserved	R/W	0	0: Unmask Reserved Attach interrupt 1: Mask Reserved Attach interrupt
0	A/V Charging	R/W	0	0: Unmask A/V Charging interrupt 1: Mask A/V Charging interrupt

7.6.7 ADC (07h) Register Field Descriptions

Table 8. ADC (07h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	N/A	N/A
4-0	ADC value	R	11111	5-bit ADC counter value latched after accessory detection on ID pin

7.6.8 Timing Set 1 (08h) Register Field Descriptions

Table 9. Timing Set 1 (08h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Key press	R/W	0000	Normal key press duration 0000: 100 ms 0001: 200 ms 0010: 300 ms 0011: 400 ms 0100: 500 ms 0101: 600 ms 0110: 700 ms 0111: 800 ms 1000: 900 ms 1001: 1000 ms Any other value: invalid
3-0	Device wake up	R/W	0000	Device wake up duration 0000: 50 ms 0001: 100 ms 0010: 150 ms 0011: 200 ms 0100: 300 ms 0101: 400 ms 0110: 500 ms 0111: 600 ms 1000: 700 ms 1001: 800 ms 1010: 900 ms 1011: 1000 ms Any other value: invalid

7.6.9 Timing Set 2 (09h) Register Field Descriptions

Table 10. Timing Set 2 (09h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Switching wait	R/W	0000	Wait time between detection complete and switching 0000: 10 ms 0001: 30 ms 0010: 50 ms 0011: 70 ms 0100: 90 ms 0101: 110 ms 0110: 130 ms 0111: 150 ms 1000: 170 ms 1001: 190 ms 1010: 210 ms Any other value: invalid

Table 10. Timing Set 2 (09h) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	Long key press	R/W	0000	Long key press duration 0000: 300 ms 0001: 400 ms 0010: 500 ms 0011: 600 ms 0100: 700 ms 0101: 800 ms 0110: 900 ms 0111: 1000 ms 1000: 1100 ms 1001: 1200 ms 1010: 1300 ms 1011: 1400 ms 1100: 1500 ms Any other value: invalid

7.6.10 Device Type 1 (0Ah) Register Field Descriptions

Table 11. Device Type 1 (0Ah) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	USB OTG	R	0	USB on-the-go (OTG) device
6	DCP	R	0	Dedicated charging port
5	CDP	R	0	Charging downstream port
4	Type1/Type2 charger	R	0	Type 1 / Type 2 charger
3	UART	R	0	UART
2	USB	R	0	USB host
1	VBUS	R	0	VBUS valid
0	MHL	R	0	MHL device

7.6.11 Device Type 2 (0Bh) Register Field Descriptions

Table 12. Device Type 2 (0Bh) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Audio Type 3	R	0	Audio type 3 cable
6	Audio / Video	R	0	Audio / video cable
5	TTY	R	0	TTY converter
4	PPD	R	0	Phone-powered device
3	JIG UART OFF	R	0	Factory mode cable
2	JIG UART ON	R	0	Factory mode cable
1	JIG USB OFF	R	0	Factory mode cable
0	JIG USB ON	R	0	Factory mode cable

7.6.12 Button 1 (0Ch) Register Field Descriptions

Table 13. Button 1 (0Ch) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	7	R	0	Number 7 key is pressed
6	6	R	0	Number 6 key is pressed
5	5	R	0	Number 5 key is pressed
4	4	R	0	Number 4 key is pressed
3	3	R	0	Number 3 key is pressed
2	2	R	0	Number 2 key is pressed
1	1	R	0	Number 1 key is pressed
0	Send End	R	0	Send End key is pressed

7.6.13 Button 2 (0Dh) Register Field Descriptions

Table 14. Button 2 (0Dh) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Unused	N/A	N/A	N/A
6	Unknown	R	0	Unknown key is pressed
5	Error	R	0	Error key is pressed
4	12	R	0	Number 12 key is pressed
3	11	R	0	Number 11 key is pressed
2	10	R	0	Number 10 key is pressed
1	9	R	0	Number 9 key is pressed
0	8	R	0	Number 8 key is pressed

7.6.14 Manual SW 1 (13h) Register Field Descriptions

Table 15. Manual SW 1 (13h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	DM switching	R/W	000	000: Open all switches 001: DM is connected to DM_HT 010: Open all switches 011: DM is connected to TxD Any other value: invalid
4-2	DP switching	R/W	000	000: Open all switches 001: DP is connected to DP_HT 010: Open all switches 011: DP is connected to RxD Any other value: invalid
1-0	Unused	N/A	N/A	N/A

7.6.15 Manual SW 2 (14h) Register Field Descriptions

Table 16. Manual SW 2 (14h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Unused	N/A	N/A	N/A
3	BOOT SW	R/W	0	0: Low 1: High
2	JIG ON	R/W	0	0: High impedance 1: GND
1-0	Unused	N/A	N/A	N/A

7.6.16 Reset (1Bh) Register Field Descriptions

Table 17. Reset (1Bh) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Unused	N/A	N/A	N/A
0	Reset	W	0	1: Write this value (1) to reset the device. 0: Set to this value (0) after reset completed.

7.6.17 Charger control 1 (20h) Register Field Descriptions

Table 18. Charger control 1 (20h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH DIS	R/W	0	Force charger disable 0: Normal charger operation mode 1: Disable charger. Override charger detection and CHENOV
6-5	CHRSTTH	R/W	0	Charging restart threshold voltage 00: 130 mV 01: 130 mV 10: 190 mV 11: 240mV
4	CHENOV	R/W	1	Charger enabled override 0: Charger enabled is controlled by charger detection. Charger is enabled is DCP, CDP, or Carkit charger is detected. 1: Charge is always enabled.
3	FCMEN	R/W	1	Fast charge mode enable. Device should be in pre-charge before setting FCMEN = 0 to disable Fast Charge mode. 0: Fast charge mode is disabled. Charger remains in pre-charge mode. 1: Enable fast charge mode.
2	Unused	N/A	N/A	N/A
1-0	FCHGTM	R/W	0	Fast charge timer – These bits control the maximum amount of time that the charger will spend in fast charge mode. If the timer is over this time, FTE is changed to 1. 00: 5 hours 01: 6 hours 10: 7 hours 11: Disable fast charge timer

7.6.18 Charger control 2 (21h) Register Field Descriptions

Table 19. Charger control 2 (21h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IFULL		0001	Charge done current threshold level 0000: 50 mA 0001: 60 mA 0010: 70 mA 0011: 80 mA 0100: 90 mA 0101: 100 mA 0110: 110 mA 0111: 120 mA 1000: 130 mA 1001: 140 mA 1010: 150 mA 1011: 160 mA 1100: 170 mA 1101: 180 mA 1110: 190 mA 1111: 200 mA

Table 19. Charger control 2 (21h) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CV SET		1010	Constant voltage mode voltage - in fast charge mode, when the battery voltage reaches this value, the charger transitions from fast charge mode to constant voltage charge mode. 0000: 4.00 V 0001: 4.02 V 0010: 4.04 V 0011: 4.06 V 0100: 4.08 V 0101: 4.10 V 0110: 4.12 V 0111: 4.14 V 1000: 4.16 V 1001: 4.18 V 1010: 4.20 V 1011: 4.22 V 1100: 4.24 V 1101: 4.26 V 1110: 4.28 V 1111: 4.35 V

7.6.19 Battery Charger Control 3 (22h) Register Field Descriptions

Table 20. Battery Charger Control 3 (22h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OVP	R/W	0011	These bits set the overvoltage protection threshold. 00: 6.0 V 01: 6.5 V 10: 7.0 V 11: 7.5 V
5	AUTOSTOP	R/W	0000	Auto charging stop 0: Disable charging shutoff and keep CV mode 1: Enable charging shutoff after 30-minute timer
4	ISET L	R/W	0001	This bit is used in conjunction with ISET[3:0], and it determines the fast charge mode current limit. 0: 90 mA 1: 200 mA to 950 mA
3-0	ISET	R/W	0101	This sets the fast charge mode current. 0000: 200 mA 0001: 250 mA 0010: 300 mA 0011: 350 mA 0100: 400 mA 0101: 450 mA 0110: 500 mA 0111: 550 mA 1000: 600 mA 1001: 650 mA 1010: 700 mA 1011: 750 mA 1100: 800 mA 1101: 850 mA 1110: 900 mA 1111: 950 mA

7.6.20 Charger Interrupt (24h) Register Field Descriptions

Table 21. Charger Interrupt (24h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Unused	N/A	0	Always reads 0
5	CH Fault	R/Clr	0	1: Charger in fault state
4	CH DONE	R/Clr	0	1: Charge complete / top-off mode
3	CH CV	R/Clr	0	1: Charger state in constant voltage (CV) mode
2	CH FC	R/Clr	0	1: Charger state in fast charge mode (constant current)
1	CH PC	R/Clr	0	1: Charger state in pre-charge mode
0	CH IDLE	R/Clr	0	1: Charge state idle

7.6.21 Charger Interrupt Mask (25h) Register Field Descriptions

Table 22. Charger Interrupt Mask (25h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Unused	N/A	0	Always reads 0
5	CH_Fault	R/W	0	0: Unmask CH Fault interrupt 1: Mask CH Fault interrupt
4	CH_DONE	R/W	0	0: Unmask CH Done interrupt 1: Mask CH Done interrupt
3	CH_CV	R/W	0	0: Unmask CH CV interrupt 1: Mask CH CV interrupt
2	CH_FC	R/W	0	0: Unmask CH FC interrupt 1: Mask CH FC interrupt
1	CH_PC	R/W	0	0: Unmask CH PC interrupt 1: Mask CH PC interrupt
0	CH_IDLE	R/W	0	0: Unmask CH IDLE interrupt 1: Mask CH IDLE interrupt

7.6.22 Charger Status (26h) Register Field Descriptions

Table 23. Charger Status (26h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FTE	R/W	0	Fast charge timer expired interrupt 0: Timer not expired 1: 30-minute fast charge timer expired. Charge disabled. Restart when re-attaching charger or toggling CHENOV.
6	PTE	R/W	0	Pre-charge timer expired interrupt 0: Timer not expired 1: 30-minute pre-charge timer has expired. Charger disabled. Restart when re-attaching charger or toggling CHENOV.
5	CH Fault	R/W	0	1: Charger fault other than PTE or FTE
4	CH Done	R/W	0	1: Charge complete / top-off mode
3	CH CV	R/W	0	1: Charger state in constant voltage mode
2	CH FC	R/W	0	1: Charge state in fast charge mode (constant current)
1	CH PC	R/W	0	1: Charger state in pre-charge mode
0	CH IDLE	R/W	0	1: Charge state in idle (not charging)

8 Application and Implementation

8.1 Application Information

The TSU8111 device can be used in portable device (PD) applications for interfacing the PD with external peripherals. The TSU8111 is ideal for use when a PD needs two separate USB signal paths, accessory detection, charger detection, and a battery charging IC.

8.2 Typical Application

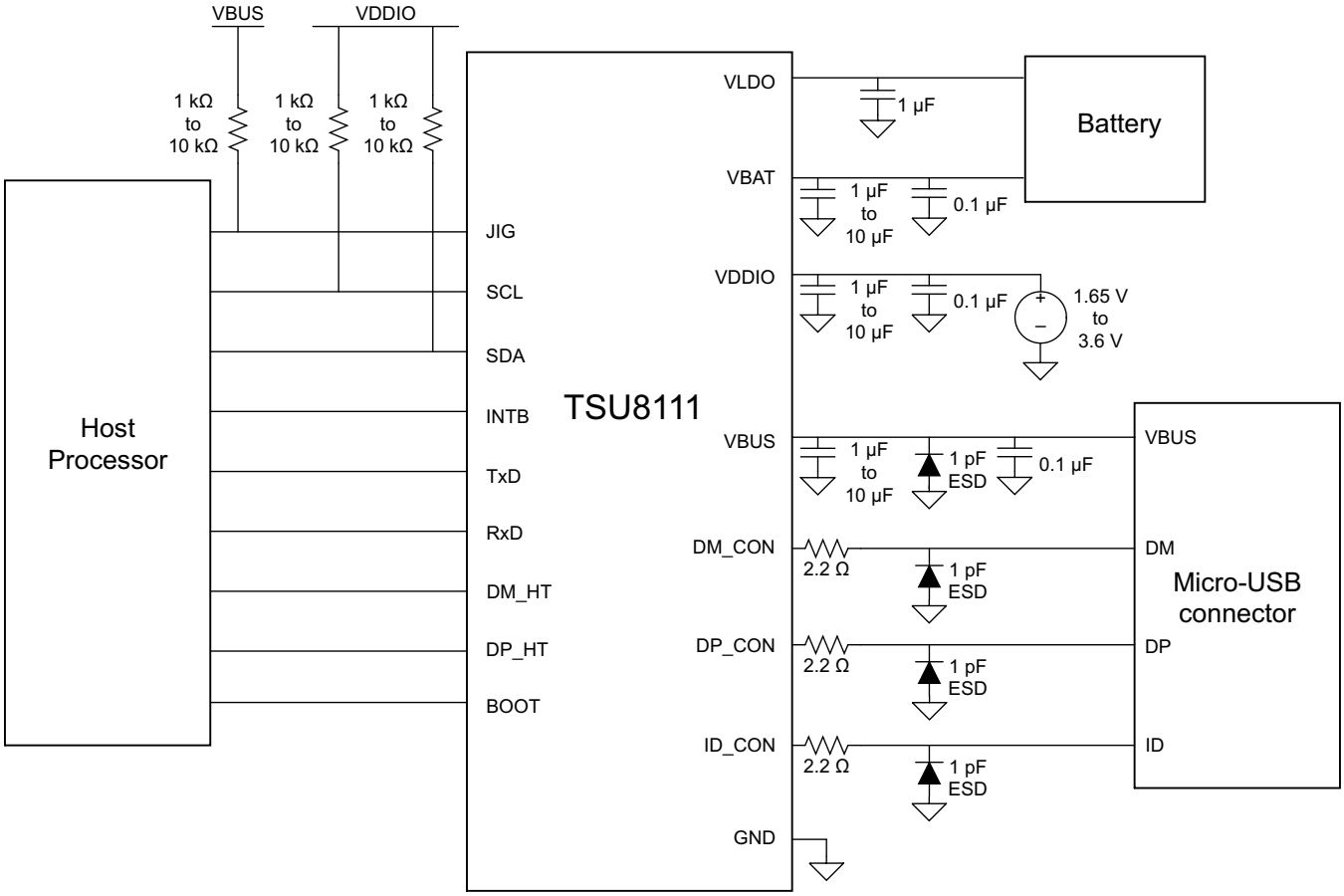


Figure 12. Interface from Host Processor to USB Connector and Battery

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 24.

Table 24. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BAT}	3 V to 4.4 V
V_{BUS}	4 V to 6.5 V
V_{DDIO}	1.65 V to 3.6 V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Desired ESD protection on micro-USB signal lines
  - Addition of optional 1-pF ESD diodes on the USB lines protects against ±8-kV IEC-61000-4-2 contact discharge. The optional 2.2-Ω resistors provide additional protection for the internal circuitry near the USB inputs.
- Output current on LDO
  - Use the charging specifications for the Li-Ion or Li-Polymer battery to determine the desired output current register setting for the TSU8111 LDO.

8.2.3 Application Curves

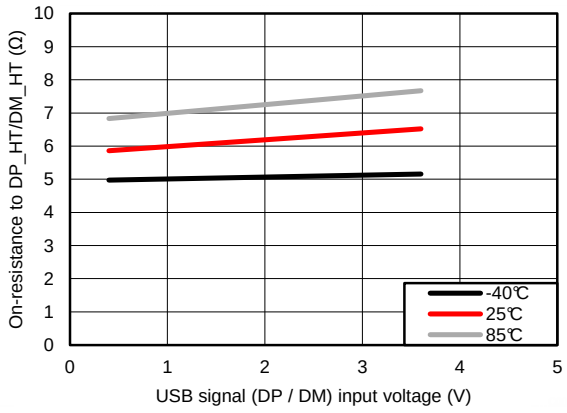


Figure 13. USB Signal vs On-resistance

9 Power Supply Recommendations

The TSU8111 has three different power supply input pins: VBAT, VBUS, and VDDIO. VBAT is the primary supply and accepts any voltage between –0.5 V and 6 V, but the operating voltage is between 3 V and 4.4 V. VBUS is the secondary power supply from the micro-USB connector and accepts any voltage between –0.5 V and 28 V, but the operating voltage is between 4 V and 6.5 V. VDDIO is the supply for I^2C communication and accepts any voltage between –0.5 V and 4.6 V, but the operating voltage is between 1.65 V and 3.6 V.

The VBAT and VBUS pins each require a 0.1-µF and a 1-µF to 10-µF decoupling capacitor. The 0.1-µF capacitor smooths out high frequency noise and has a lower series inductance. The 1-µF to 10-µF capacitor smooths out lower frequency noise and has a much higher series inductance. Placing both capacitors near each power supply input will provide better load regulation across the frequency spectrum.

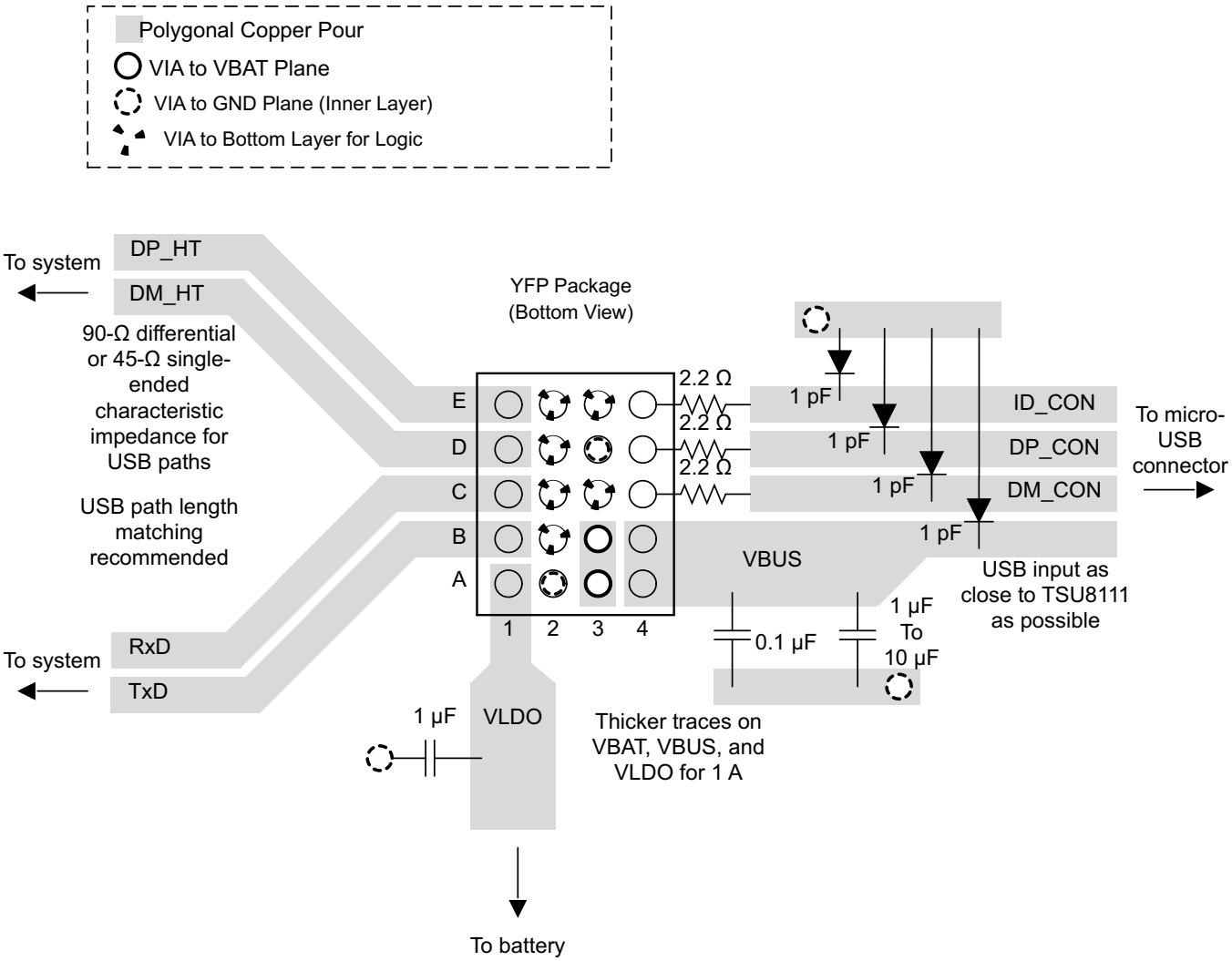
The VLDO pin requires a 1-µF load capacitor.

10 Layout

10.1 Layout Guidelines

- The TSU8111 should be placed as close to the USB connector as possible to reduce the effect of stray noise.
- Decoupling capacitors, as mentioned in Power Supply Recommendations, should be as close to the device as possible. This will also reduce the effect of ESR and ripple seen on voltages due to transient spikes.
- Lengths of all traces should be kept less than 2 inches.
- For 1-oz copper thickness, the width of the USB traces should be at least 15 mils.
- Traces to the VBAT, VBUS, and VLDO pins should be capable of carrying 1 A. This will keep routing resistance less than 100-mΩ and minimize voltage drops when charging with high currents.
- Maximize the use of vias on VBUS, VBAT, and GND. Increasing the number of vias will reduce routing resistance and improve thermal performance.
- Minimize the use of vias for USB traces to preserve USB signal integrity.
- All USB traces (DP_CON, DM_CON, DP_HT, DM_HT, TxD, and RxD) should have 45-Ω single-ended impedance and 90-Ω differential impedance to fulfill USB 2.0 requirements.

10.2 Layout Example



11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSU8111YFPR	ACTIVE	DSBGA	YFP	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

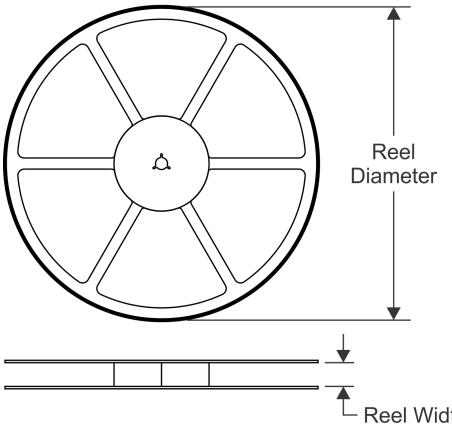
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

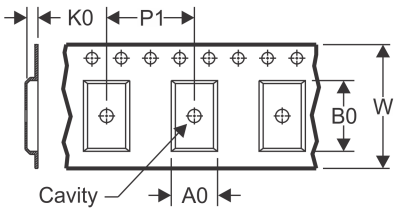
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

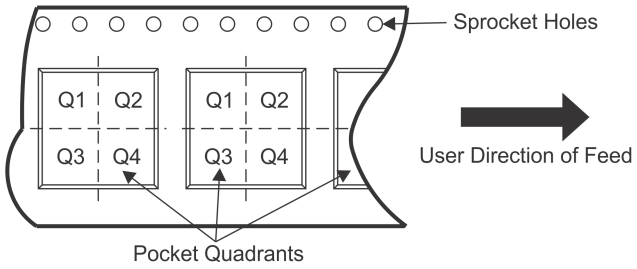


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

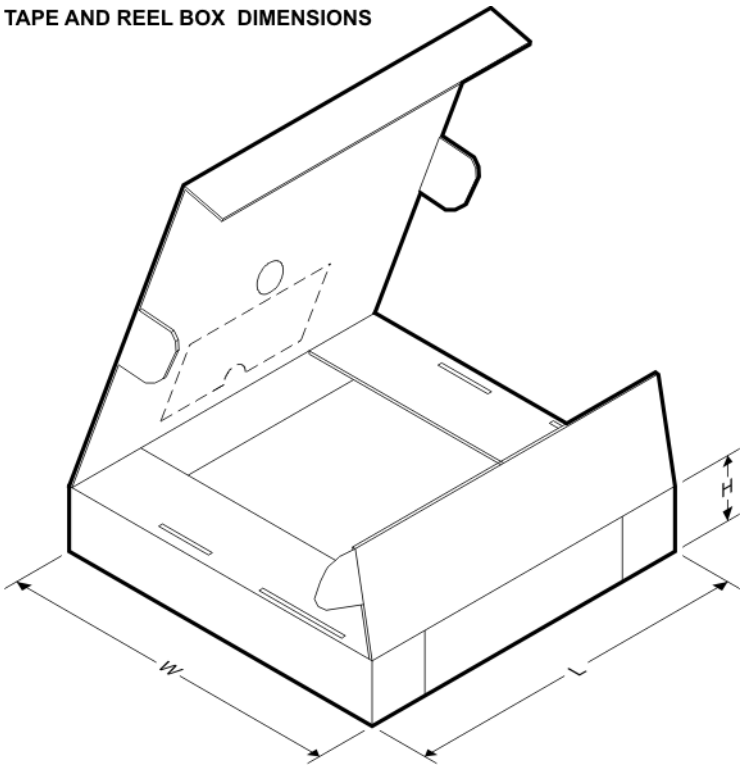
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSU8111YFPR	DSBGA	YFP	20	3000	180.0	8.4	1.92	2.3	0.56	4.0	8.0	Q1

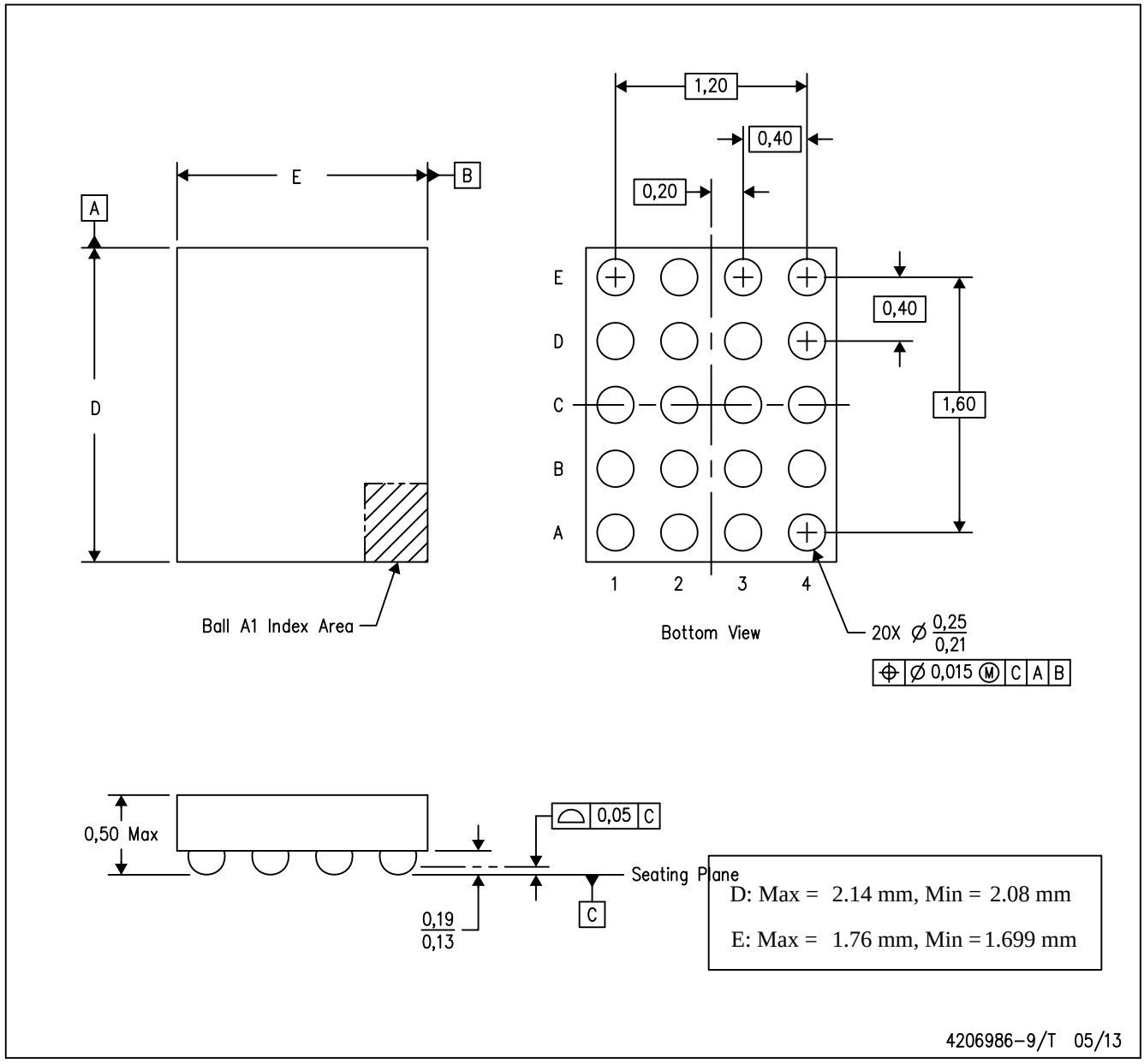
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSU8111YFPR	DSBGA	YFP	20	3000	182.0	182.0	20.0

YFP (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

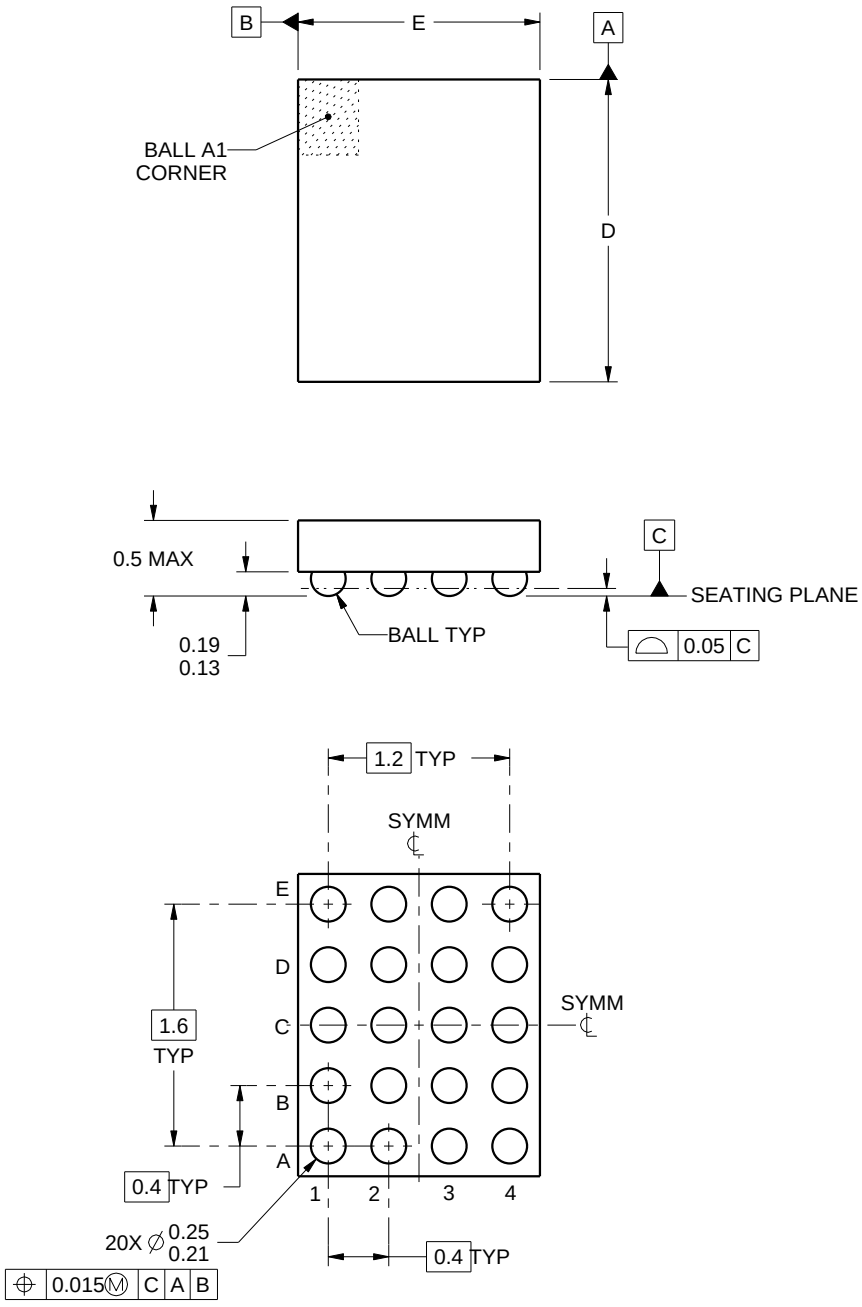
NanoFree is a trademark of Texas Instruments

PACKAGE OUTLINE

YFP0020

DSBGA - 0.5 mm max height

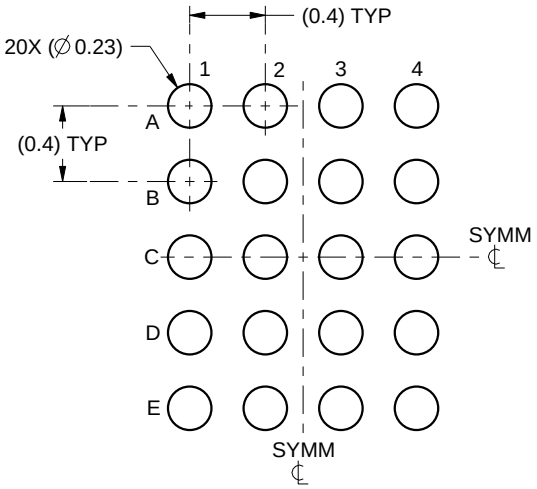
DIE SIZE BALL GRID ARRAY



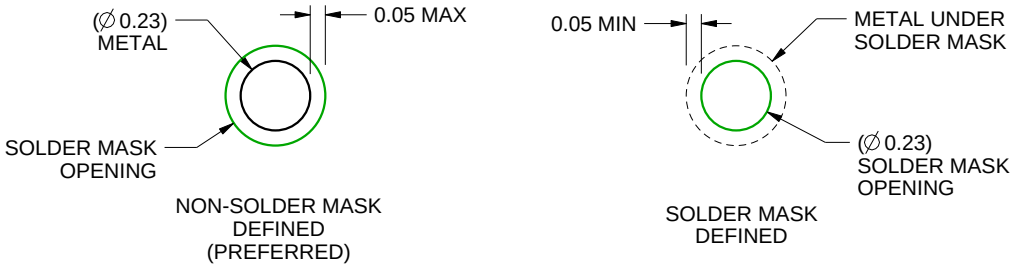
4222895/A 04/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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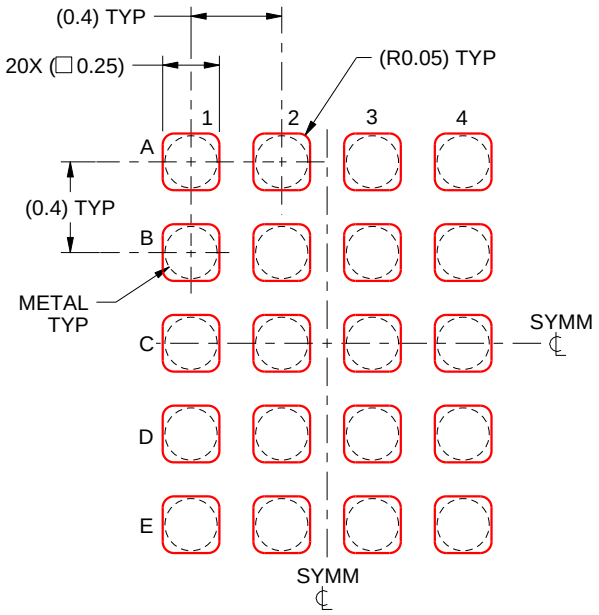
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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