TUSB2046Bx 4-Port Hub for the Universal Serial Bus With Optional Serial EEPROM Interface

1 Features

- Fully Compliant With the USB Specification as a Full-Speed Hub: TID #30220231
- 32-Pin LQFP (1) Package With a 0.8-mm Terminal Pitch or QFN Package With a 0.5-mm Pin Pitch
- 3.3-V Low-Power ASIC Logic
- Integrated USB Transceivers
- State Machine Implementation Requires No Firmware Programming
- One Upstream Port and Four Downstream Ports
- All Downstream Ports Support Full-Speed and Low-Speed Operations
- Two Power Source Modes
  - Self-Powered Mode
  - Bus-Powered Mode
- Power Switching and Overcurrent Reporting Is Provided Ganged or Per Port
- Supports Suspend and Resume Operations
- Supports Programmable Vendor ID and Product ID With External Serial EEPROM
- 3-State EEPROM Interface Allows EEPROM Sharing
- Push-Pull Outputs for $\overline{\text{PWRON}}$ Eliminate the Need for External Pullup Resistors
- Noise Filtering on $\overline{\text{OVRCUR}}$ Provides Immunity to Voltage Spikes
- Package Pinout Allows 2-Layer PCB
- Low EMI Emission Achieved by a 6-MHz Crystal Input
- Migrated From Proven TUSB2040 Hub
- Lower Cost Than the TUSB2040 Hub
- Enhanced System ESD Performance
- No Special Driver Requirements; Works Seamlessly With Any Operating System With USB Stack Support
- Supports 6-MHz Operation Through a Crystal Input or a 48-MHz Input Clock

(1) JEDEC descriptor S-PQFP-G for low-profile quad flatpack (LQFP).

2 Applications

- Computer Systems
- Docking Stations

3 Description

The TUSB2046B is a 3.3-V CMOS hub device that provides one upstream port and four downstream ports in compliance with the Universal Serial Bus (USB) specification as a full-speed hub. Because this device is implemented with a digital state machine instead of a microcontroller, no firmware programming is required. Fully compliant USB transceivers are integrated into the ASIC for all upstream and downstream ports. The downstream ports support full-speed and low-speed devices by automatically setting the slew rate according to the speed of the device attached to the ports. The configuration of the BUSPWR pin selects either the bus-powered or the self-powered mode.

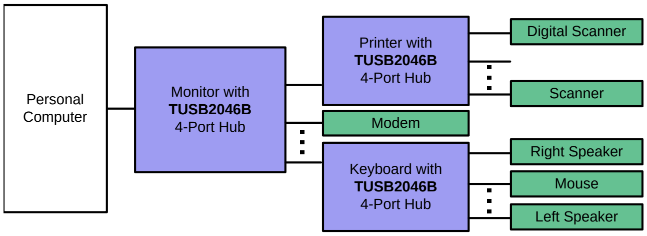
Configuring the GANGED input determines the power switching and overcurrent detection modes for the downstream ports. If GANGED is high, all $\overline{\text{PWRON}}$ outputs switch together and if any $\overline{\text{OVRCUR}}$ is activated, all ports transition to the power-off state. If GANGED is low, the $\overline{\text{PWRON}}$ outputs and $\overline{\text{OVRCUR}}$ inputs operate on a per-port basis.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB2046B	VQFN (32)	5.00 mm × 5.00 mm
	LQFP (32)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

USB-Tiered Configuration Example



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (July 2015) to Revision K	Page
• Changed the VQFN package Body Size From: 5.00 mm x 2.00 mm To: 5.00 mm x 5.00 mm	1

Changes from Revision I (September 2013) to Revision J	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

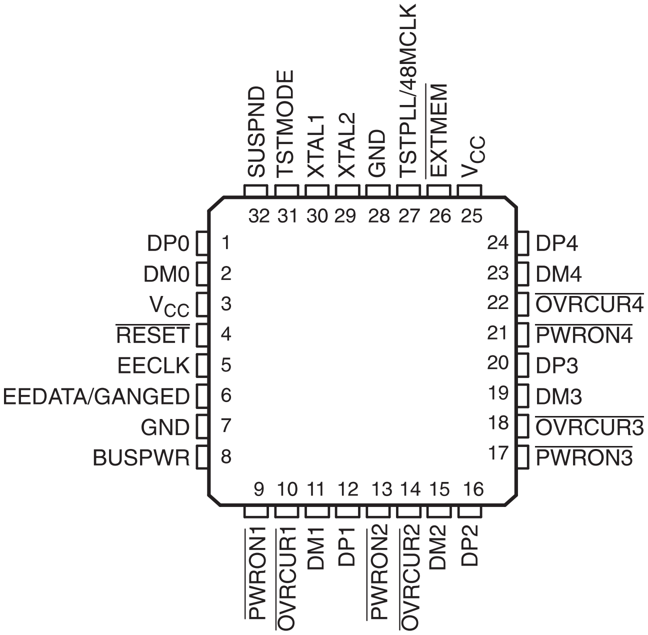
5 Description (Continued)

The TUSB2046B provides the flexibility of using a 6-MHz or a 48-MHz clock. The logic level of the TSTMODE terminal controls the selection of the clock source. When TSTMODE is low, the output of the internal APLL circuitry is selected to drive the internal core of the device. When TSTMODE is high, the TSTPLL/48MCLK input is selected as the input clock source and the APLL circuitry is powered down and bypassed. The internal oscillator cell is also powered down while TSTMODE is high. Low EMI emission is achieved because the TUSB2046B can usee a 6-MHz crystal input. Connect the crystal as shown in Figure 6. An internal PLL then generates the 48-MHz clock used to sample data from the upstream port and to synchronize the 12 MHz used for the USB clock. If low-power suspend and resume are desired, a passive crystal or resonator must be used. However, a 6-MHz oscillator may be used by connecting the output to the XTAL1 pin and leaving the XTAL2 pin open. The oscillator TTL output must not exceed 3.6 V.

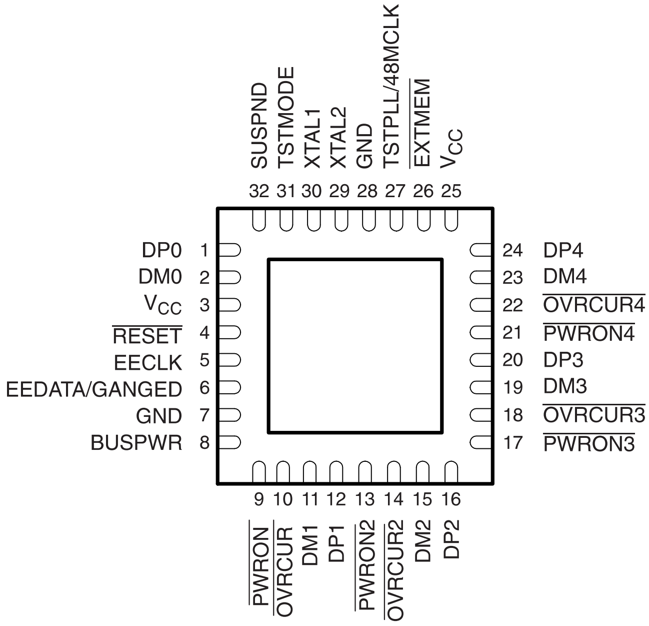
For 48-MHz operation, the clock cannot be generated with a crystal using the XTAL2 output because the internal oscillator cell supports only the fundamental frequency. Other useful features of the TUSB2046B include a package with a 0.8-mm pin pitch for easy PCB routing and assembly, push-pull outputs for the PWRON pins eliminate the need for pullup resistors required by traditional open-collector I/Os, and OVRCUR pins have noise filtering for increased immunity to voltage spikes.

6 Pin Configuration and Functions

VF Package
32-Pin LQFP
Top View



RHB Package
32-Pin VQFN With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BUSPWR	8	I	Power source indicator. BUSPWR is an active-high input that indicates whether the downstream ports source their power from the USB cable or a local power supply. For the bus-power mode, this terminal must be pulled to 3.3 V, and for the self-powered mode, this terminal must be pulled low. Input must not change dynamically during operation.
DM0	2	I/O	Root port USB differential data minus. DM0 paired with DP0 constitutes the upstream USB port.
DM1	11	I/O	USB differential data minus. DM1–DM4 paired with DP1–DP4 support up to four downstream USB ports.
DM2	15		
DM3	19		
DM4	23		
DP0	1	I/O	Root port USB differential data plus. DP0 paired with DM0 constitutes the upstream USB port.
DP1	12	I/O	USB differential data plus. DP1–DP4 paired with DM1–DM4 support up to four downstream USB ports.
DP2	16		
DP3	20		
DP4	24		
EECLK	5	O	EEPROM serial clock. When $\overline{\text{EXTMEM}}$ is high, the EEPROM interface is disabled. The EECLK terminal is disabled and must be left floating (unconnected). When $\overline{\text{EXTMEM}}$ is low, EECLK acts as a 3-state serial clock output to the EEPROM with a 100-µA internal pulldown.
EEDATA/GANGED	6	I/O	EEPROM serial data/power-management mode indicator. When $\overline{\text{EXTMEM}}$ is high, EEDATA/GANGED selects between ganged or per-port power overcurrent detection for the downstream ports. When $\overline{\text{EXTMEM}}$ is low, EEDATA/GANGED acts as a serial data I/O for the EEPROM and is internally pulled down with a 100-µA pulldown. This standard TTL input must not change dynamically during operation.
$\overline{\text{EXTMEM}}$	26	I	When $\overline{\text{EXTMEM}}$ is high, the serial EEPROM interface of the device is disabled. When $\overline{\text{EXTMEM}}$ is low, terminals 5 and 6 are configured as the clock and data terminals of the serial EEPROM interface, respectively.
GND	7, 28		GND terminals must be tied to ground for proper operation.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{OVRCUR1}}$	10	I	Overcurrent input. $\overline{\text{OVRCUR1}}$–$\overline{\text{OVRCUR4}}$ are active low. For per-port overcurrent detection, one overcurrent input is available for each of the four downstream ports. In the ganged mode, any $\overline{\text{OVRCUR}}$ input may be used and all $\overline{\text{OVRCUR}}$ terminals must be tied together. $\overline{\text{OVRCUR}}$ terminals are active low inputs with noise filtering logic.
$\overline{\text{OVRCUR2}}$	14		
$\overline{\text{OVRCUR3}}$	18		
$\overline{\text{OVRCUR4}}$	22		
$\overline{\text{PWRON1}}$	9	O	Power-on/-off control signals. $\overline{\text{PWRON1}}$–$\overline{\text{PWRON4}}$ are active low, push-pull outputs. Push-pull outputs eliminate the pullup resistors which open-drain outputs require. However, the external power switches that connect to these terminals must be able to operate with 3.3-V inputs because these outputs cannot drive 5-V signals.
$\overline{\text{PWRON2}}$	13		
$\overline{\text{PWRON3}}$	17		
$\overline{\text{PWRON4}}$	21		
$\overline{\text{RESET}}$	4	I	$\overline{\text{RESET}}$ is an active low TTL input with hysteresis and must be asserted at power up. When $\overline{\text{RESET}}$ is asserted, all logic is initialized. Generally, a reset with a pulse width between 100 μs and 1 ms is recommended after 3.3-V V_{CC} reaches its 90%. Clock signal has to be active during the last 60 μs of the reset window.
SUSPND	32	O	Suspend status. SUSPND is an active high output available for external logic power-down operations. During the suspend mode, SUSPND is high. SUSPND is low for normal operation.
TSTMODE	31	I	Test/mode terminal. TSTMODE is used as a test terminal during production testing. This terminal must be tied to ground or 3.3-V V_{CC} for normal 6-MHz or 48-MHz operation, respectively.
TSTPLL/ 48MCLK	27	I/O	Test/48-MHz clock input. TSTPLL/48MCLK is used as a test terminal during production testing. This terminal must be tied to ground for normal 6-MHz operation. If 48-MHz input clock is desired, a 48-MHz clock source (no crystal) can be connected to this input terminal.
V_{CC}	3, 25		3.3-V supply voltage
XTAL1	30	I	Crystal 1. XTAL1 is a 6-MHz crystal input with 50% duty cycle. An internal PLL generates the 48-MHz and 12-MHz clocks used internally by the ASIC logic.
XTAL2	29	O	Crystal 2. XTAL2 is a 6-MHz crystal output. This terminal must be left open when using an oscillator.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	3.6	V
V_I	Input voltage range		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ V or $V_I < V_{CC}$		±20	mA
I_{OK}	Output clamp current	$V_O < 0$ V or $V_O < V_{CC}$		±20	mA
T_A	Operating free-air temperature	TUSB2046B	0	70	°C
		TUSB2046BI	–40	85	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage levels are with respect to GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	TUSB2046B	3	3.3	3.6	V
		TUSB2046BI	3.3		3.6	
V_I	Input voltage, TTL/LVCMOS		0		V_{CC}	V
V_O	Output voltage, TTL/LVCMOS		0		V_{CC}	V
$V_{IH(REC)}$	High-level input voltage, signal-ended receiver		2		V_{CC}	V
$V_{IL(REC)}$	Low-level input voltage, signal-ended receiver				0.8	V
$V_{IH(TTL)}$	High-level input voltage, TTL/LVCMOS		2		V_{CC}	V
$V_{IL(TTL)}$	Low-level input voltage, TTL/LVCMOS		0		0.8	V
T_A	Operating free-air temperature	TUSB2046B	0		70	°C
		TUSB2046BI	–40		85	
$R_{(DRV)}$	External series, differential driver resistor		22 (–5%)		22 (5%)	Ω
$f_{(OPRH)}$	Operating (dc differential driver) high speed mode				12	Mb/s
$f_{(OPRL)}$	Operating (dc differential driver) low speed mode				1.5	Mb/s
V_{ICR}	Common mode, input range, differential receiver		0.8		2.5	V
t_t	Input transition times, TTL/LVCMOS		0		25	ns
T_J	Junction temperature range		–40		115	°C

7.4 Thermal Information

THERMAL METRIC (1)		TUSB2046BI	UNIT
		RHB (VQFN)	
		32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	35.7	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance (3)	28.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (4)	9.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter (5)	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter (6)	9.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance (7)	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL/LVCMOS	I_{OH} = –4 mA	V_{CC} – 0.5		V
		USB data lines	$R_{(DRV)}$ = 15 kΩ to GND	2.8		
			I_{OH} = –12 mA (without $R_{(DRV)}$)	V_{CC} – 0.5		
V_{OL}	Low-level output voltage	TTL/LVCMOS	I_{OL} = 4 mA		0.5	V
		USB data lines	$R_{(DRV)}$ = 1.5 kΩ to 3.6 V		0.3	
			I_{OL} = 12 mA (without $R_{(DRV)}$)		0.5	

Electrical Characteristics (continued)

over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{IT+}	Positive input threshold	TTL/LVCMOS			1.8	V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V		1.8	
V_{IT-}	Negative-input threshold	TTL/LVCMOS		0.8		V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	1		
V_{hys}	Input hysteresis (1) ($V_{T+} - V_{T-}$)	TTL/LVCMOS		0.3	0.7	mV
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	300	500	
I_{OZ}	High-impedance output current	TTL/LVCMOS	V = V_{CC} or GND (2)		±10	μA
		USB data lines	0 V ≤ V_O ≤ V_{CC}		±10	
I_{IL}	Low-level input current	TTL/LVCMOS	V_I = GND		–1	μA
I_{IH}	High-level input current	TTL/LVCMOS	V_I = V_{CC}		1	μA
$z_{0(DRV)}$	Driver output impedance	USB data lines	Static V_{OH} or V_{OL}	7.1	19.9	Ω
V_{ID}	Differential input voltage	USB data lines	0.8 V ≤ V_{ICR} ≤ 2.5 V	0.2		V
I_{CC}	Input supply current		Normal operation		40	mA
			Suspend mode		1	μA

(1) Applies for input buffers with hysteresis.
(2) Applies for open-drain buffers.

7.6 Differential Driver Switching Characteristics (Full Speed Mode)

over recommended ranges of operating free-air temperature and supply voltage, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_r	Transition rise time for DP or DM	See Figure 1 and Figure 2	4	20	ns
t_f	Transition fall time for DP or DM	See Figure 1 and Figure 2	4	20	ns
$t_{(RFM)}$	Rise/fall time matching (1)	(t_r/t_f) × 100	90%	110%	
$V_{O(CRS)}$	Signal crossover output voltage (1)		1.3	2.0	V

(1) Characterized only. Limits are approved by design and are not production tested.

7.7 Differential Driver Switching Characteristics (Low Speed Mode)

over recommended ranges of operating free-air temperature and supply voltage, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_r	Transition rise time for DP or DM (1)	C_L = 200 pF to 600 pF, See Figure 1 and Figure 2	75	300	ns
t_f	Transition fall time for DP or DM (1)	C_L = 200 pF to 600 pF, See Figure 1 and Figure 2	75	300	ns
$t_{(RFM)}$	Rise/fall time matching (1)	(t_r/t_f) × 100	80%	120%	
$V_{O(CRS)}$	Signal crossover output voltage (1)	C_L = 200 pF to 600 pF	1.3	2.0	V

(1) Characterized only. Limits are approved by design and are not production tested.

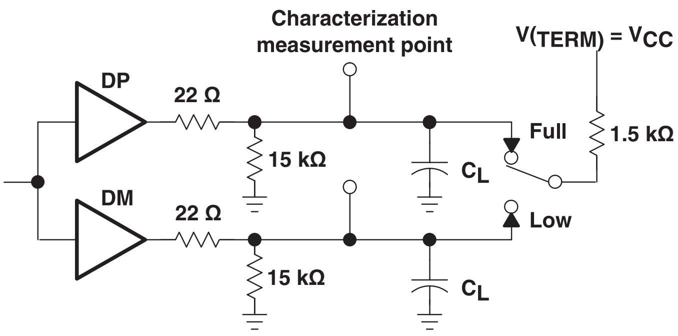
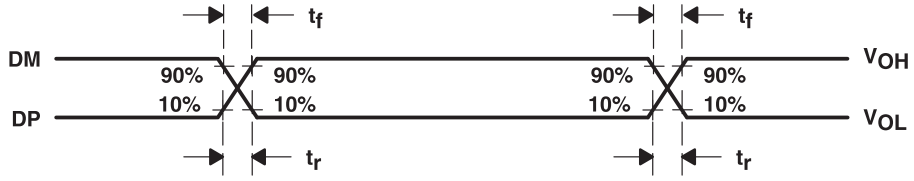


Figure 1. Differential Driver Switching Load



NOTE: The t_r/t_f ratio is measured as $t_{r(DP)}/t_{f(DM)}$ and $t_{r(DM)}/t_{f(DP)}$ at each crossover point.

Figure 2. Differential Driver Timing Waveforms

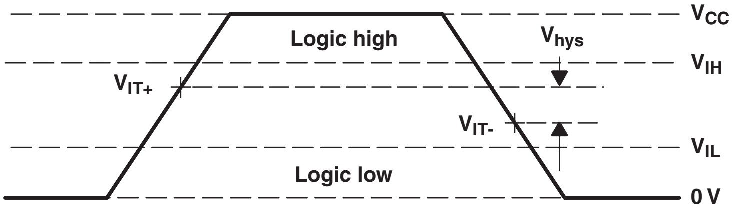


Figure 3. Single-Ended Receiver Input Signal Parameter Definitions

7.8 Typical Characteristics

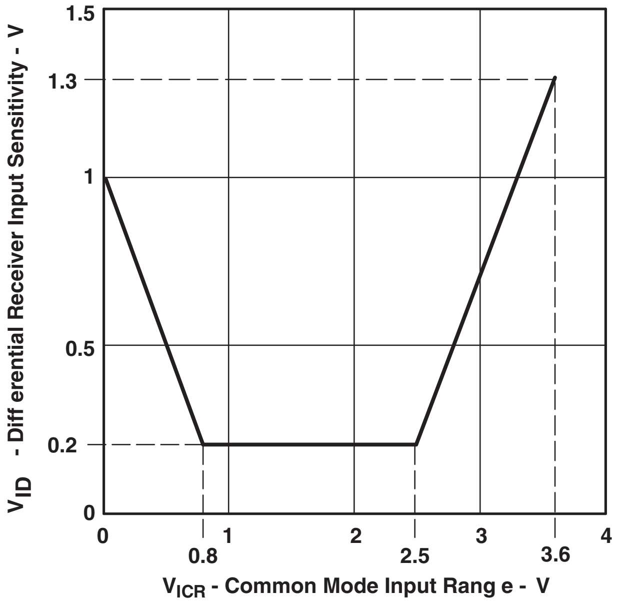


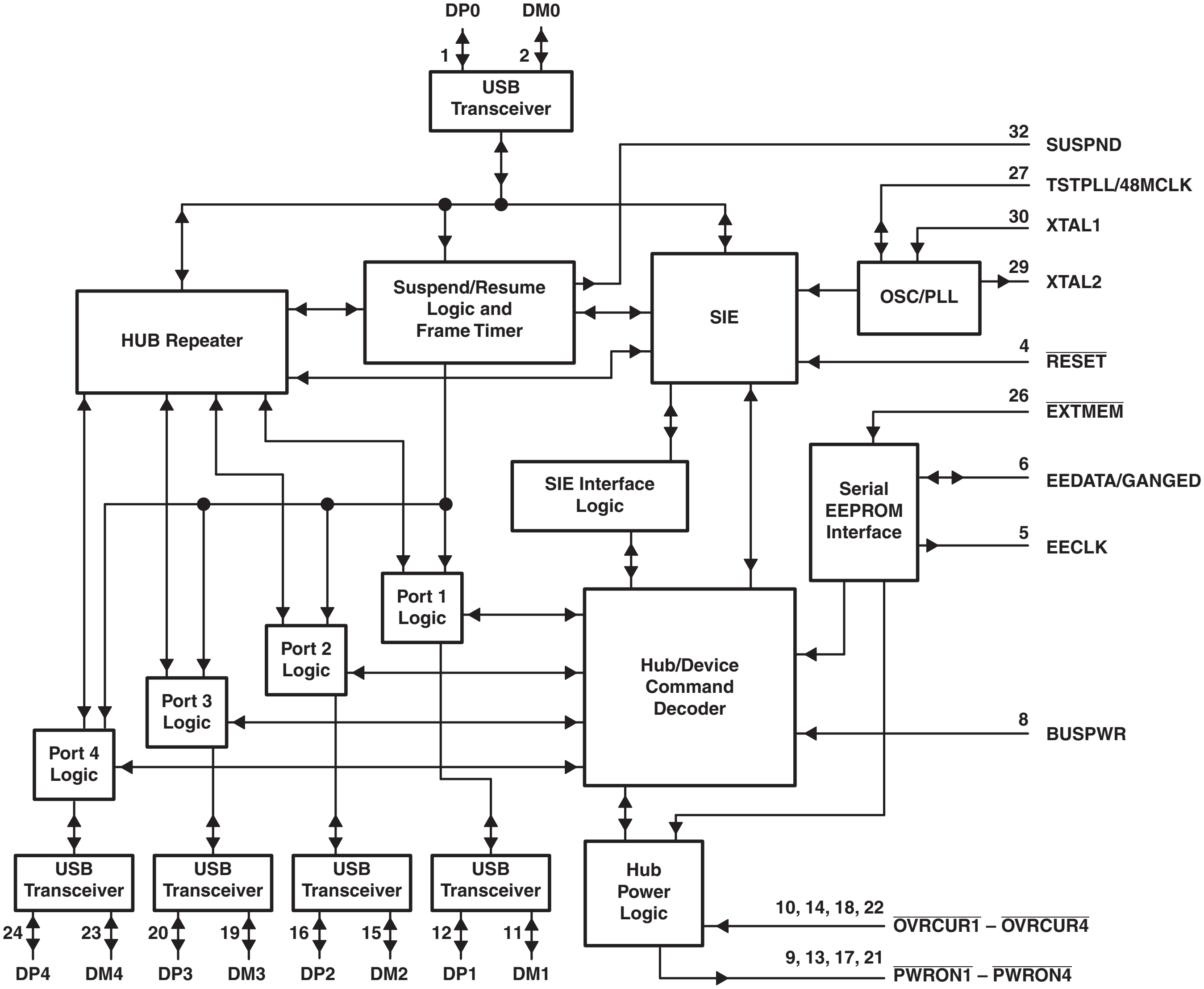
Figure 4. Differential Receiver Input Sensitivity vs Common Mode Input Range

8 Detailed Description

8.1 Overview

The TUSB2046B is a 3.3-V CMOS hub device that provides one upstream port and four downstream ports in compliance with the Universal Serial Bus (USB) specification as a full-speed hub. Because this device is implemented with a digital state machine instead of a microcontroller, no firmware programming is required. Fully compliant USB transceivers are integrated into the ASIC for all upstream and downstream ports. The downstream ports support full-speed and low-speed devices by automatically setting the slew rate according to the speed of the device attached to the ports. The configuration of the BUSPWR pin selects either the bus-powered or the self-powered mode.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 USB Power Management

External power-management devices, such as the TPS2044, are required to control the 5-V source to the downstream ports according to the corresponding values of the PWRON pin. Upon detecting any overcurrent conditions, the power-management device sets the corresponding OVRCUR pin of the TUSB2046B to a logic low. If GANGED is high, all PWRON outputs switch together and if any OVRCUR is activated, all ports transition to the power-off state. If GANGED is low, the PWRON outputs and OVRCUR inputs operate on a per-port basis.

Both bus-powered and self-powered hubs require overcurrent protection for all downstream ports. The two types of protection are individual-port management (individual-port basis) or ganged-port management (multiple-port basis). Individual-port management requires power-management devices for each individual downstream port, but adds robustness to the USB system because, in the event of an overcurrent condition, the USB host only powers down the port that has the condition. The ganged configuration uses fewer power-management devices and thus has lower system costs, but in the event of an overcurrent condition on any of the downstream ports, all the ganged ports are disabled by the USB host.

Feature Description (continued)

Using a combination of the BUSPWR and EEDATA/GANGED inputs, the TUSB2046B supports four modes of power management: bus-powered hub with either individual-port power-management or ganged-port power management, and the self-powered hub with either individual-port power management or ganged-port power management. TI supplies the complete hub solution with the TUSB2036 (2/3-port), TUSB2046B, and the TUSB2077 (7-port) hubs along with the power-management devices needed to implement a fully USB specification-compliant system.

8.3.2 Clock Generation

The input clock configuration logic of TUSB2046B is enhanced to accept a 6-MHz crystal or 48-MHz on-the-board clock source with a simple tie-off change on TSTMODE (pin 31).

- A 6-MHz input clock configuration is shown in Figure 5.

  In this mode, both TSTMODE and TSTPLL/48MCLK pins must be tied to ground. The hub is configured to use the 6-MHz clock on pins 30 and 29, which are XTAL1 and XTAL2, respectively, on the TUSB2046B. This is identical to the TUSB2046.

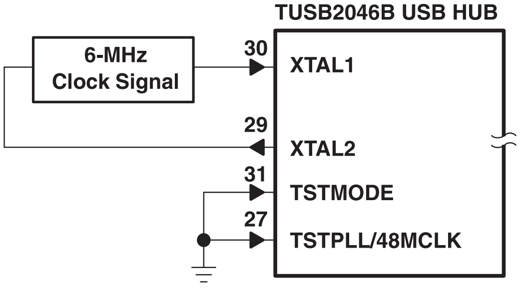
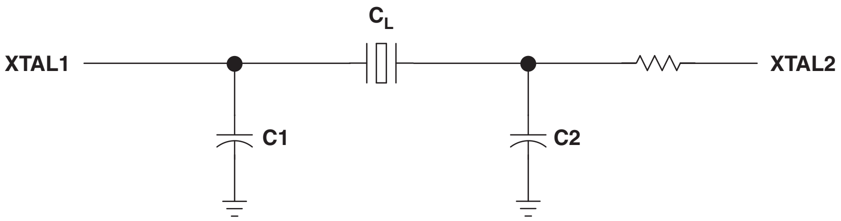


Figure 5. 6-MHz Input Clock Configuration



NOTE: This figure assumes a 6-MHz fundamental crystal that is parallel loaded. The component values of C1, C2, and R_d are determined using a crystal from Fox Electronics – part number HC49U-6.00MHz 30\50\0-70\20, which means ±30 ppm at 25°C and ±50 ppm from 0°C to 70°C. The characteristics for the crystal include a load capacitance (C_L) of 20 pF, maximum shunt capacitance (C_o) of 7 pF, and the maximum ESR of 50 Ω. In order to insure enough negative resistance, use C1 = C2 = 27 pF. The resistor R_d is used to trim the gain, and R_d = 1.5 kΩ is recommended.

Figure 6. Crystal Tuning Circuit

- A 48-MHz input clock configuration is shown in Figure 7.

  In this mode, both TSTMODE and XTAL1 pins must be tied to 3.3-V V_{CC}. The hub accepts the 48-MHz clock input on TSTPLL/48MCLK (terminal 27). XTAL2 must be left floating (open) for this configuration. Only the oscillator or the onboard clock source is accepted for this mode. A crystal cannot be used for this mode, because the internal oscillator cell of the chip only supports the fundamental frequency.

Feature Description (continued)

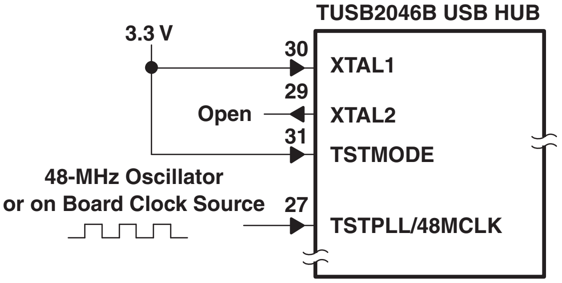


Figure 7. 48-MHz Input Clock Configuration

8.4 Device Functional Modes

8.4.1 Vendor ID and Product ID With External Serial EEPROM

The $\overline{\text{EXTMEM}}$ pin enables or disables the optional EEPROM interface. When the $\overline{\text{EXTMEM}}$ pin is high, the product ID (PID) displayed during enumeration is the general-purpose USB hub. For this default, pin 5 is disabled and pin 6 functions as the GANGED input pin. If custom product ID (PID) and vendor ID (VID) descriptors are desired, the $\overline{\text{EXTMEM}}$ pin must be low ($\overline{\text{EXTMEM}}$ = 0). For this configuration, pins 5 and 6 function as the EEPROM interface with pins 5 and 6 functioning as EECLK and EEDATA, respectively. See Table 1 for a description of the EEPROM memory map. A block diagram example of how to connect the external EEPROM if a custom PID and VID are desired is shown in Figure 8.

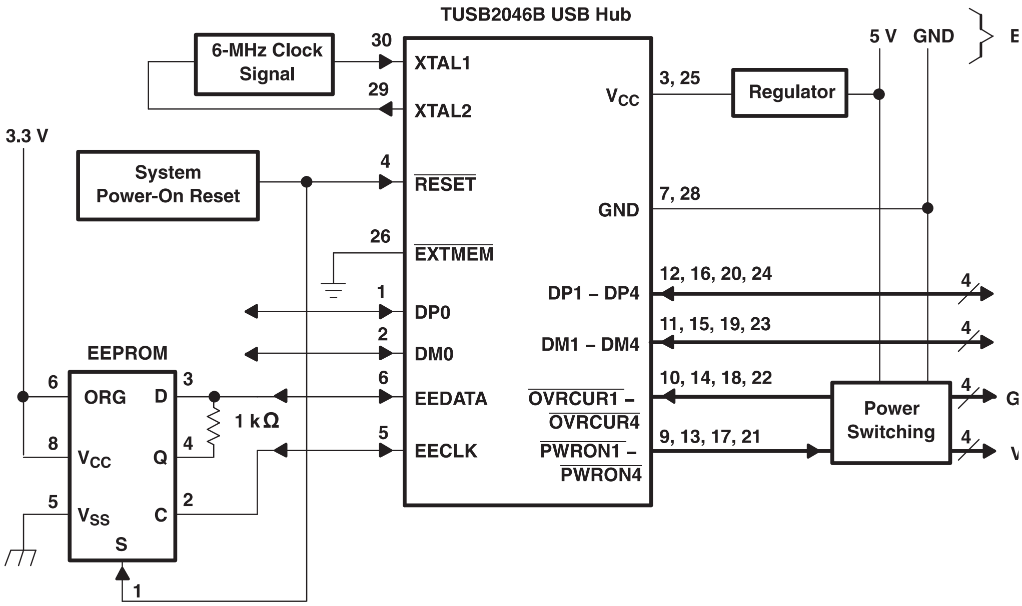


Figure 8. Typical Application of the TUSB2046B USB Hub

8.5 Programming

An SGS Thompson M93C46 EEPROM, or equivalent, stores the programmable VID and PID. When the EEPROM interface is enabled ($\overline{\text{EXTMEM}}$ = 0), the EECLK and EEDATA are internally pulled down (100 µA) inside the TUSB2046B. The internal pulldowns are disabled when the EEPROM interface is disabled ($\overline{\text{EXTMEM}}$ = 1).

The EEPROM is programmed with the three 16-bit locations as shown in Table 1. Connecting terminal 6 of the EEPROM high (ORG = 1) organizes the EEPROM memory into 64×16-bit words.

Programming (continued)

Table 1. EEPROM Memory Map

ADDRESS	D15	D14	D13	D12–D8	D7–D0
00000	0	GANGED	00000	00000	00000000
00001	VID high-byte				VID low-byte
00010	PID high-byte				PID low-byte
	XXXXXXXX				

The D and Q signals of the EEPROM must be tied together using a 1-kΩ resistor with the common I/O operations forming a single-wire bus. After system power-on reset, the TUSB2046B performs a one-time access read operation from the EEPROM if the $\overline{\text{EXTMEM}}$ terminal is pulled low and the chip select(s) of the EEPROM is connected to the system power-on reset. Initially, the EEDATA terminal is driven by the TUSB2046B to send a start bit (1) which is followed by the read instruction (10) and the starting-word address (00000). Once the read instruction is received, the instruction and address are decoded by the EEPROM, which then sends the data to the output shift register. At this point, the hub stops driving the EEDATA terminal and the EEPROM starts driving. A dummy (0) bit is then output and the first three 16-bit words in the EEPROM are output with the most significant bit (MSB) first.

The output data changes are triggered by the rising edge of the clock provided by the TUSB2046B on the EECLK terminal. The SGS-Thompson M936C46 EEPROM is recommended because it advances to the next memory location by automatically incrementing the address internally. Any EEPROM used must have the automatic internal address advance function. After reading the three words of data from the EEPROM, the TUSB2046B puts the EEPROM interface into a high-impedance condition (pulled down internally) to allow other logic to share the EEPROM. The EEPROM read operation is summarized in Figure 9. For more details on EEPROM operation, refer to *SGS-Thompson Microelectronics M93C46 Serial Microwire Bus EEPROM* data sheet.

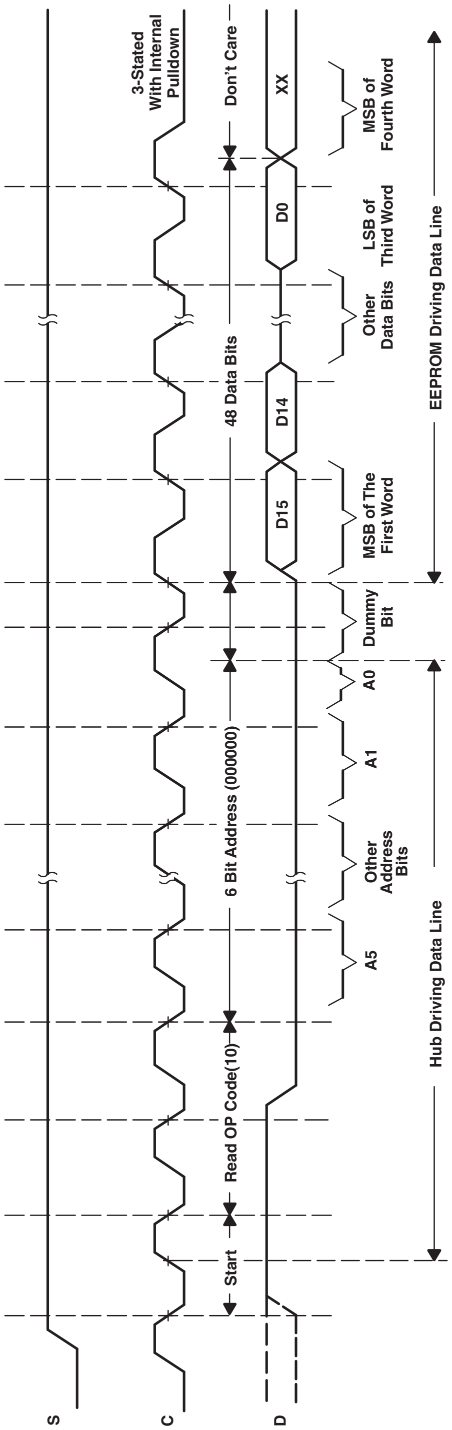


Figure 9. EEPROM Read Operation Timing Diagram

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A major advantage of USB is the ability to connect 127 functions configured in up to 6 logical layers (tiers) to a single personal computer.

Another advantage of USB is that all peripherals are connected using a standardized 4-wire cable that provides both communication and power distribution. The power configurations are bus-powered and self-powered modes. The maximum current that may be drawn from the USB 5-V line during power up is 100 mA. For the bus-powered mode, a hub can draw a maximum of 500 mA from the 5-V line of the USB cable. A bus-powered hub must always be connected downstream to a self-powered hub unless it is the only hub connected to the PC and there are no high-powered functions connected downstream. In the self-powered mode, the hub is connected to an external power supply and can supply up to 500 mA to each downstream port. High-powered functions may draw a maximum of 500 mA from each downstream port and may only be connected downstream to self-powered hubs. Per the USB specification, in the bus-powered mode, each downstream port can provide a maximum of 100 mA of current, and in the self-powered mode, each downstream port can provide a maximum of 500 mA of current.

9.2 Typical Application

A common application for the TUSB2046B is as a self powered USB hub product. The product is powered by an external 5-V DC power adapter. In this application, using a USB cable TUSB2046B's upstream port is plugged into a USB host controller. The downstream ports of the TUSB2046B are exposed to users for connecting USB cameras, keyboards, printers, and so forth.

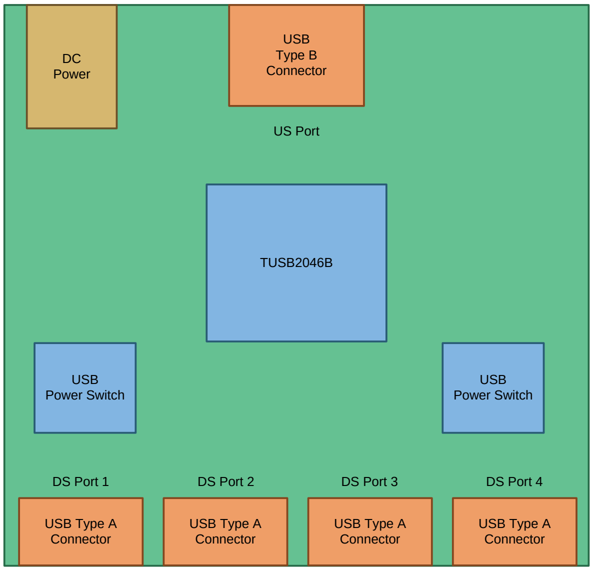


Figure 10. Self-Powered USB Hub Product

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

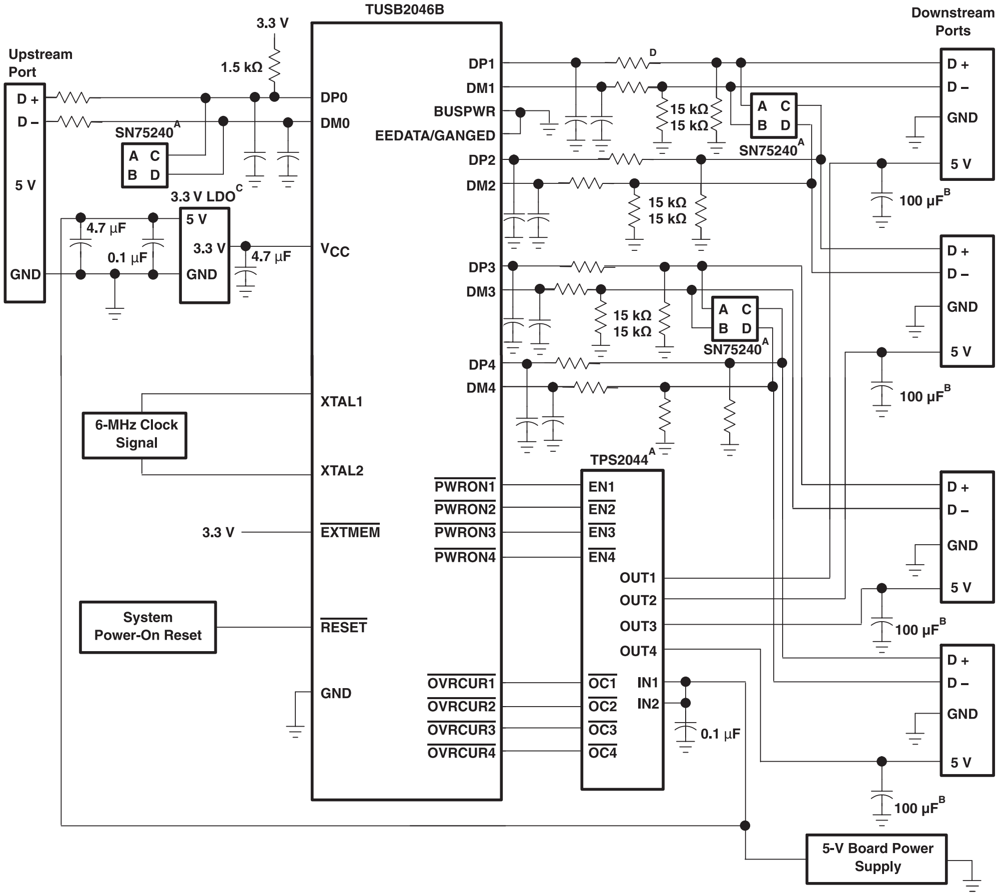
Typical Application (continued)

Table 2. Design Parameters

DESIGN PARAMETERS	VALUE
VCC Supply	3.3-V
Downstream Ports	4
Power Management	Individual-Port
Clock Source	6-MHz Crystal
External EEPROM	No
Power Source Mode	Self-Powered

9.2.2 Detailed Design Procedure

In a self-powered configuration, the TUSB2046B can be implemented for individual-port power management when used with the TPS2044 because it is capable of supplying 500 mA of current to each downstream port and can provide current limiting on a per-port basis. When the hub detects a fault on a downstream port, power is removed from only the port with the fault and the remaining ports continue to operate normally. Self-powered hubs are required to implement overcurrent protection and report overcurrent conditions. The SN75240 transient suppressors reduce inrush current and voltage spikes on the data lines.



NOTES: A. TPS2044, TPS2042, and SN75240 are Texas Instruments devices. Two TPS2042 devices can be substituted for the TPS2044. The $\overline{\text{OC}}$n outputs of the TPS204n are open drain. A 10-kΩ pullup is recommended.

B. 120 µF per hub is the minimum required per the USB specification. However, TI recommends a 100-µF, low ESR, tantalum capacitor per port for immunity to voltage droop.

C. LDO is a 5-V-to-3.3-V voltage regulator

D. All USB DP, DM signal pairs require series resistors of approximately 27Ω to ensure proper termination. An optional filter capacitor of about 22 pF is recommended for EMI suppression. This capacitor, if used, must be placed between the hub terminal and the series resistor, as per section 7.1.6 of the USB specification.

Figure 11. TUSB2046B Self-Powered Hub, Individual-Port Power-Management Application

9.2.3 Application Curve

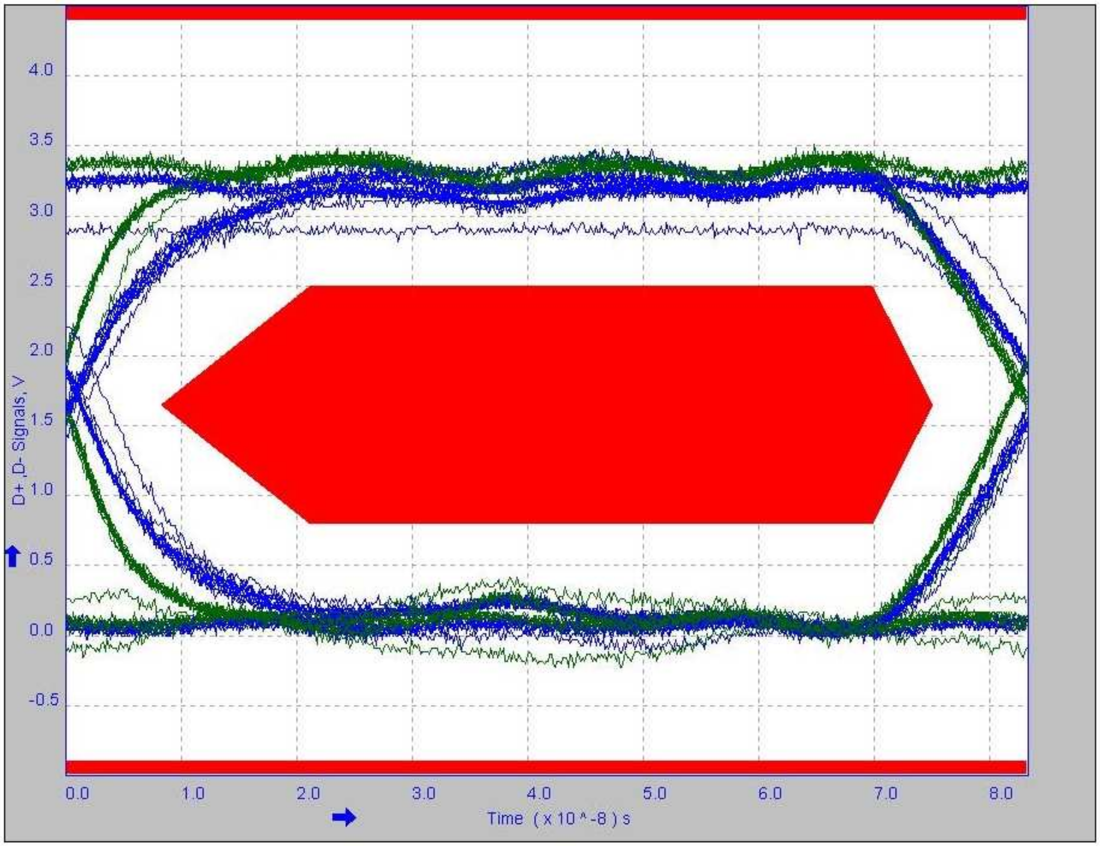


Figure 12. Downstream Port 1

10 Power Supply Recommendations

10.1 TUSB2046B Power Supply

V_{CC} should be implemented as a single power plane.

- The V_{CC} pins of the TUSB2046B supply 3.3-V power rail to the I/O of the TUSB2046B. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10-μF capacitor or 1-μF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. The smaller decoupling capacitors should be placed as close to the TUSB2046B power pins as possible with an optimal grouping of two of differing values per pin.

10.2 Downstream Port Power

- The downstream port power, VBUS, must be supplied by a source capable of supplying 5 V and up to 500 mA per port. Downstream port power switches can be controlled by the TUSB2046B signals. It is also possible to leave the downstream port power always enabled.
- A large bulk low-ESR capacitor of 22 μF or larger is required on each downstream port's VBUS to limit in-rush current.
- The ferrite beads on the VBUS pins of the downstream USB port connections are recommended for both ESD and EMI reasons. A 0.1-μF capacitor on the USB connector side of the ferrite provides a low impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

11 Layout

11.1 Layout Guidelines

11.1.1 Placement

1. A 0.1-µF should be placed as close as possible on V_{CC} power pin.
2. The ESD and EMI protection devices (if used) should also be placed as possible to the USB connector.
3. If a crystal is used, it must be placed as close as possible to the TUSB2046B's XTAL1 and XTAL2 pins.
4. Place voltage regulators as far away as possible from the TUSB2046B, the crystal, and the differential pairs.
5. In general, the large bulk capacitors associated with the power rail should be placed as close as possible to the voltage regulators.

11.1.2 Differential Pairs

1. Must be designed with a differential impedance of 90Ω ±10%.
2. Route all differential pairs on the same layer adjacent to a solid ground plane.
3. Do not route differential pairs over any plane split.
4. Adding test points will cause impedance discontinuity and will therefore negative impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
5. Avoid 90-degree turns in trace. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
6. Minimize the trace lengths of the differential pair traces. The maximum recommended trace length for USB 2.0 differential pair signals is 8 inches. Longer trace lengths require very careful routing to assure proper signal integrity.
7. Match the etch lengths of the differential pair traces. The USB 2.0 differential pairs should not exceed 50 mils relative trace length difference.
8. Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible to the TUSB2046B device.
9. Do not place power fuses across the differential pair traces.

11.1.3 Ground

TI recommends using only one board ground plane in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the TUSB2046B and any of the voltage regulators should be connected to this plane with vias. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

11.2 Layout Example

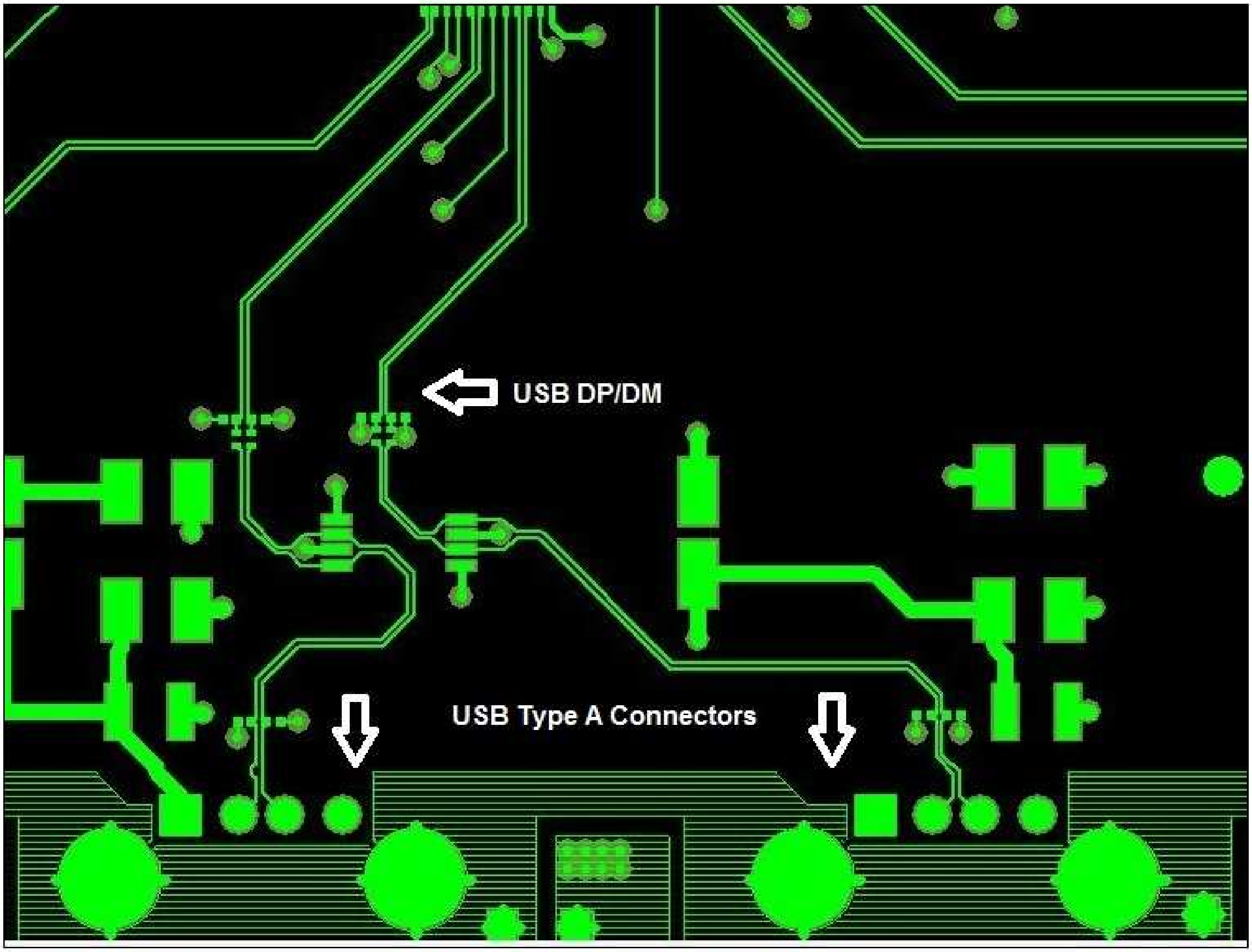


Figure 13. TUSB2046B Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TUSB2046B	Click here	Click here	Click here	Click here	Click here
TUSB2046BI	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB2046BIRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TUSB 2046BI	Samples
TUSB2046BIRHBRG4	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TUSB 2046BI	Samples
TUSB2046BIRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TUSB 2046BI	Samples
TUSB2046BIRHBTG4	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TUSB 2046BI	Samples
TUSB2046BIVFR	NRND	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	USB2046BI	
TUSB2046BIVFRG4	OBSOLETE	LQFP	VF	32		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	USB2046BI	
TUSB2046BVF	ACTIVE	LQFP	VF	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB2046B	Samples
TUSB2046BVFG4	ACTIVE	LQFP	VF	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB2046B	Samples
TUSB2046BVFR	ACTIVE	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB2046B	Samples
TUSB2046BVFRG4	ACTIVE	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB2046B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TUSB2046B :

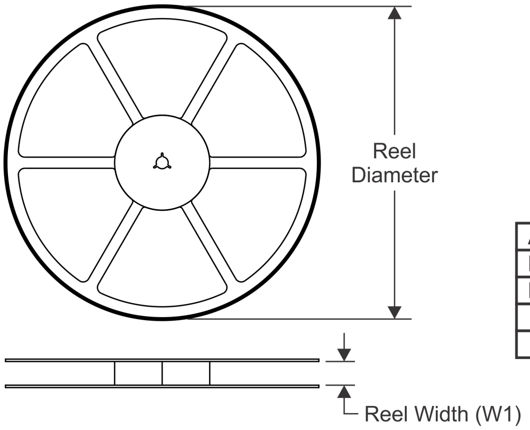
- Automotive: TUSB2046B-Q1

NOTE: Qualified Version Definitions:

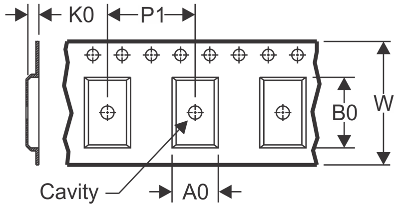
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

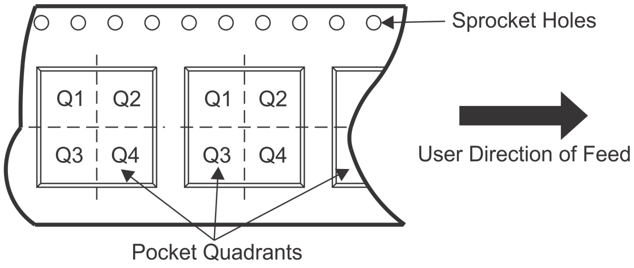


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

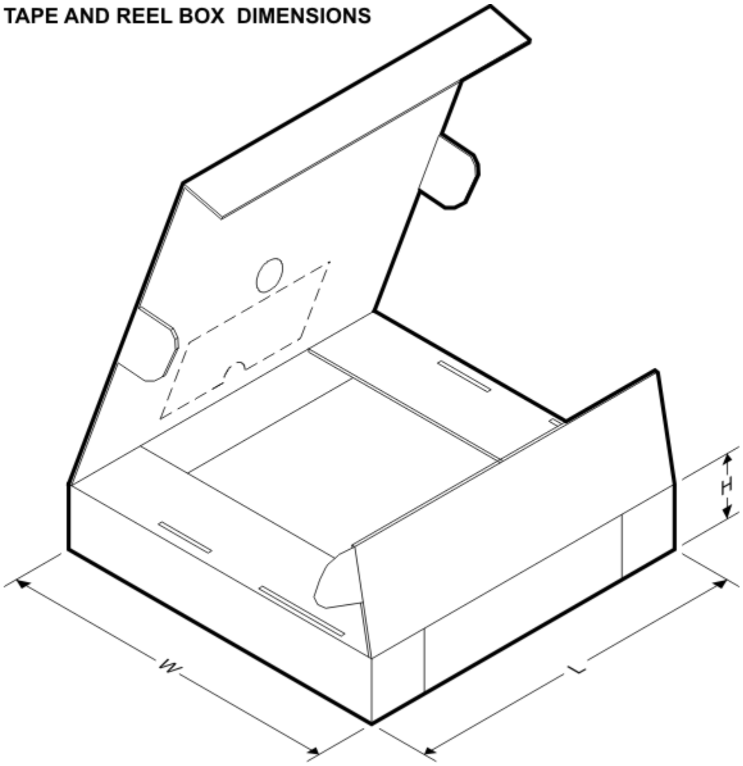
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB2046BIRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TUSB2046BIRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TUSB2046BIVFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
TUSB2046BIVFRG4	LQFP	VF	32	0	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
TUSB2046BVFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

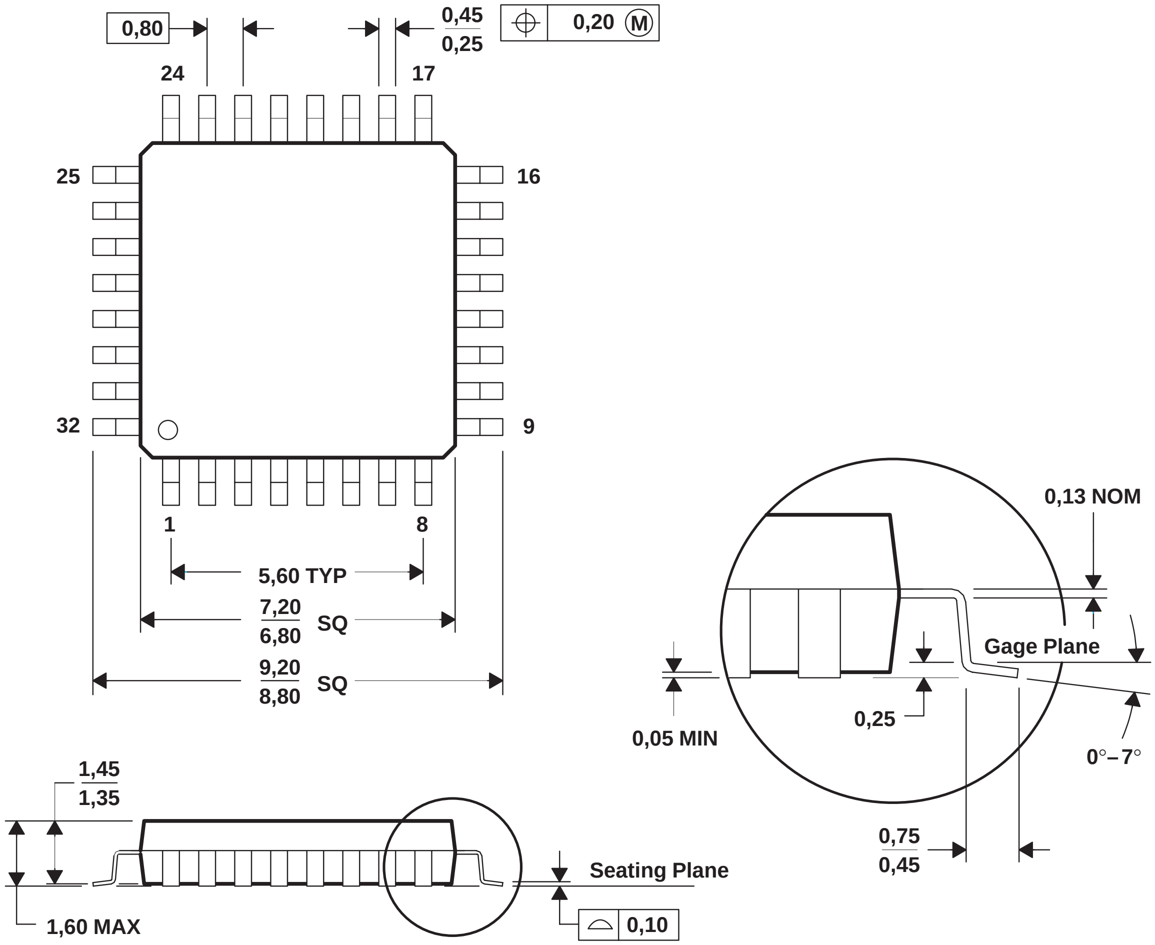
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB2046BIRHBR	VQFN	RHB	32	3000	336.6	336.6	28.6
TUSB2046BIRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
TUSB2046BIVFR	LQFP	VF	32	1000	336.6	336.6	31.8
TUSB2046BIVFRG4	LQFP	VF	32	0	336.6	336.6	31.8
TUSB2046BVFR	LQFP	VF	32	1000	336.6	336.6	31.8

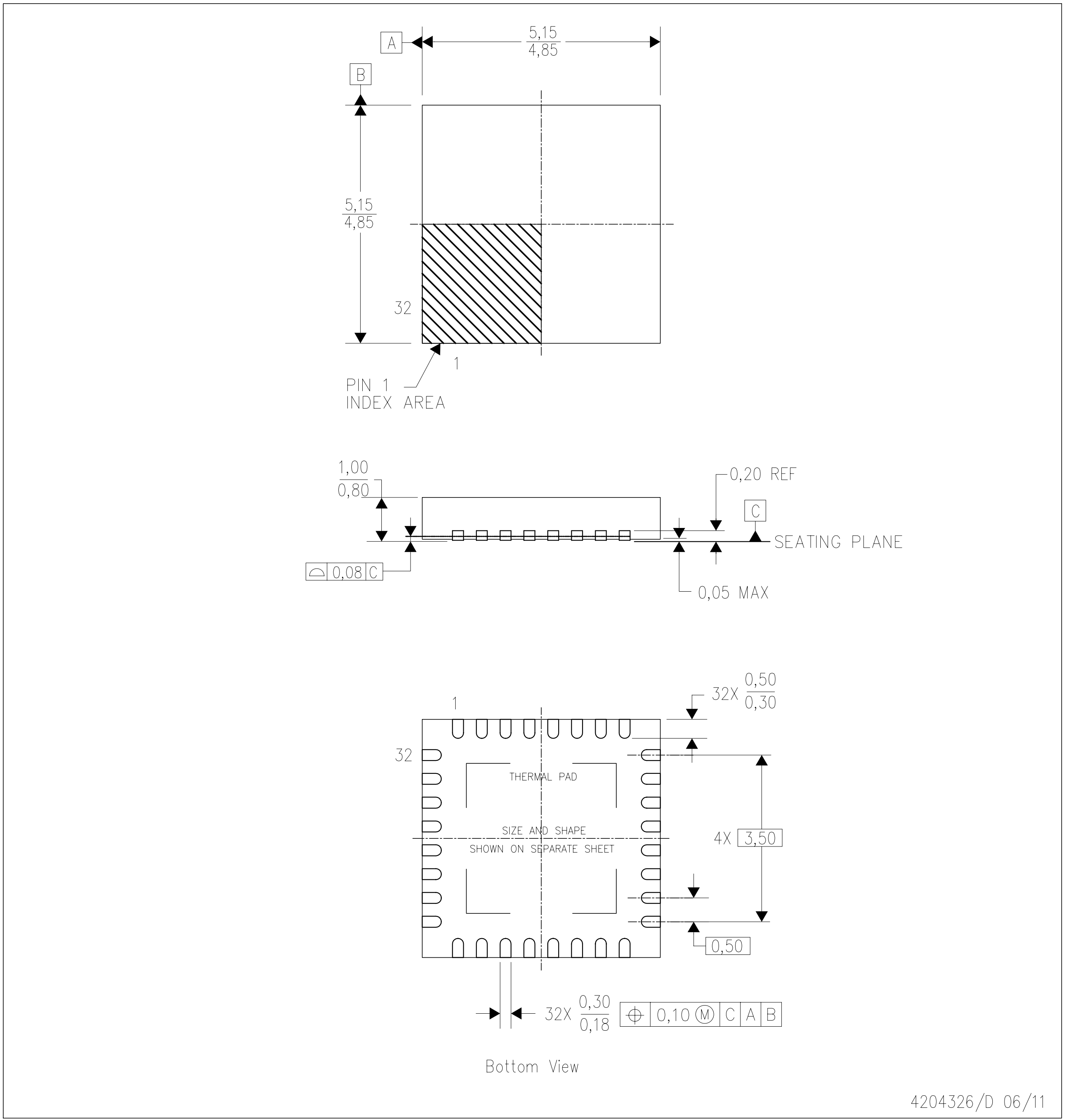
VF (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



4040172/D 04/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No−Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO−220.

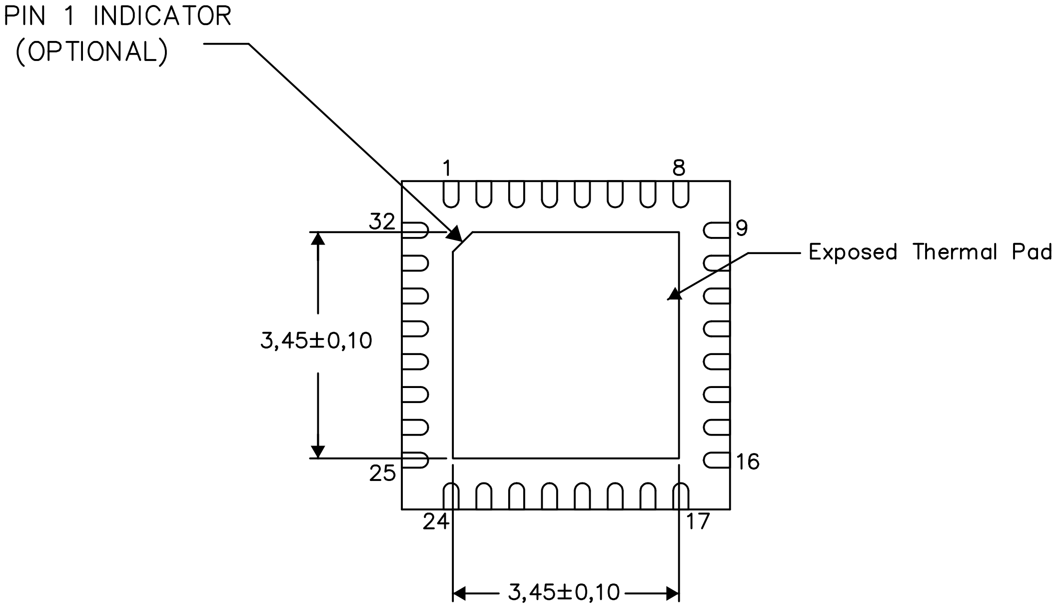
RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



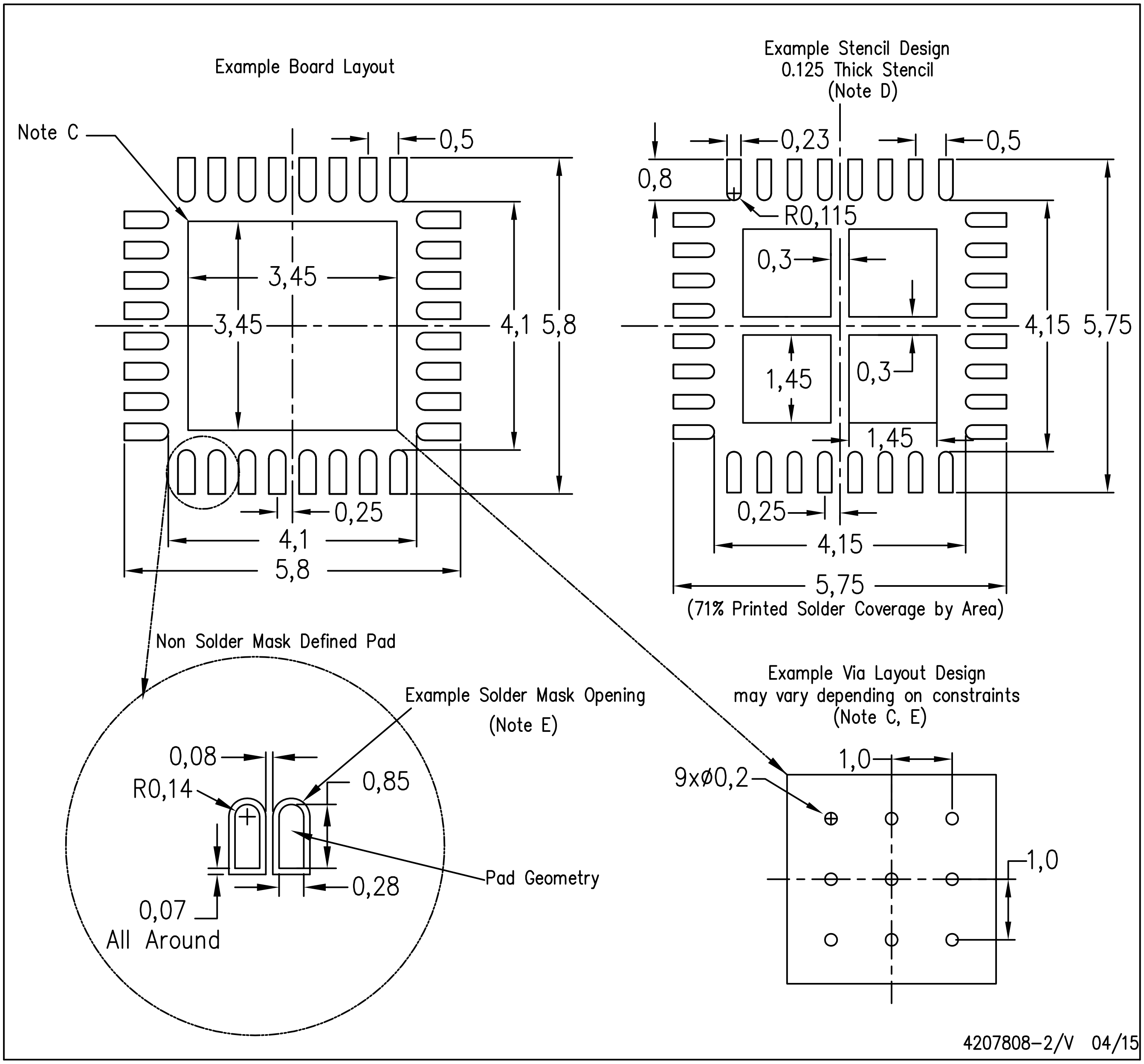
Bottom View

Exposed Thermal Pad Dimensions

4206356-2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



4207808-2/V 04/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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