TXS0101 1-Bit Bidirectional Level-Shifting, Voltage-Level Translator With Auto-Direction-Sensing for Open-Drain and Push-Pull Applications

1 Features

- No Direction-Control Signal Needed
- Maximum Data Rates
  - 24 Mbps (Push Pull)
  - 2 Mbps (Open Drain)
- Available in the Texas Instruments NanoFree™ Package
- 1.65 V to 3.6 V on A port and 2.3 V to 5.5 V on B port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- No Power-Supply Sequencing Required – Either V_{CCA} or V_{CCB} Can be Ramped First
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port
    - 2500 V Human-Body Model (A114-B)
    - 200 V Machine Model (A115-A)
    - 1500 V Charged-Device Model (C101)
  - B Port
    - 8 kV Human-Body Model (A114-B)
    - 200 V Machine Model (A115-A)
    - 1500 V Charged-Device Model (C101)

2 Applications

- Handsets
- Smartphones
- Tablets
- Desktop PCs

3 Description

This one-bit non-inverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCA} must be less than or equal to V_{CCB}. V_{CCB} accepts any supply voltage from 2.3 V to 5.5 V. This allows for low voltage bidirectional translation between any of the 1.8 V, 2.5 V, 3.3 V, and 5 V voltage nodes.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

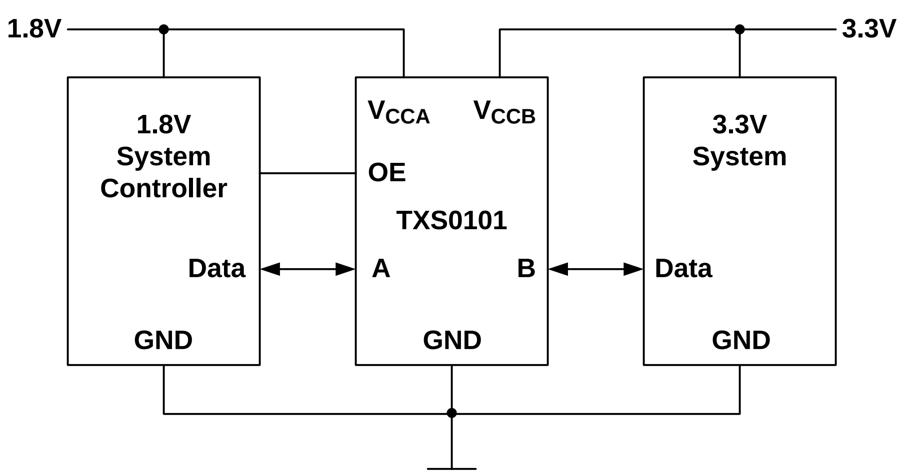
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXS0101	SOT-23 (6)	2.90 mm × 1.60 mm
	SC70 (6)	2.00 mm × 1.25 mm
	SOT (6)	1.90 mm × 1.60 mm
	DSBGA (6)	0.89 mm × 1.39 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Operating Circuit



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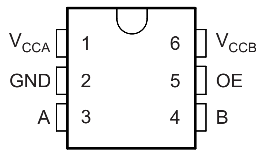
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

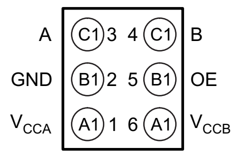
Changes from Revision B (January 2009) to Revision C	**Page**
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

DBV, DCK, and DRL Package
6-Pin SOT-23, SC70, and SOT
Top View



YZP Package
6-Pin DSBGA
Bottom View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	3	I/O	Input/output A. Referenced to V_{CCA}
B	4	I/O	Input/output B. Referenced to V_{CCB}
GND	2	G	Ground
OE	5	I	Output enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	I	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}
V_{CCB}	6	I	B-port supply voltage. 2.3 V ≤ V_{CCB} ≤ 5.5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		–0.5	4.6	V
V_{CCB}	Supply voltage		–0.5	6.5	V
V_I	Input voltage (2)	A port	–0.5	4.6	V
		B port, OE	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, A Port (1)	±2500	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, B Port (1)	±8000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, B Port(2)	±1500	
		Machine model (MM, A115-A), A Port	±200	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See(1) (2)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage(3)				1.65	3.6	V
V_{CCB}					2.3	5.5	
V_{IH}	High-level input voltage	A-port I/Os	1.65 V to 1.95 V	2.3 V to 5.5 V	V_{CCI} – 0.2	V_{CCI}	V
			2.3 V to 3.6 V		V_{CCI} – 0.4	V_{CCI}	
		B-port I/Os	1.65 V to 3.6 V	2.3 V to 5.5 V	V_{CCI} – 0.4	V_{CCI}	
		OE input			V_{CCA} × 0.65	5.5	
V_{IL}	Low-level input voltage	A-port I/Os	1.65 V to 3.6 V	2.3 V to 5.5 V	0	0.15	V
		B-port I/Os			0	0.15	
		OE input			0	V_{CCA} × 0.35	

(1) V_{CCI} is the supply associated with the input port.
(2) V_{CCO} is the supply associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

Recommended Operating Conditions (continued)

See(1) (2)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
Δt/Δv	Input transition rise or fall rate	A-port I/Os, push-pull driving	1.65 V to 3.6 V	2.3 V to 5.5 V		10	ns/V
		B-port I/Os, push-pull driving				10	
		Control Input				10	
T_A	Operating free-air temperature				–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TXS0101				UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DSBGA (YZP)	
		6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	223.9	266.9	204.2	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	185.6	80.4	76.4	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.5	99.1	38.7	10.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	63.5	1.5	3.4	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.8	98.3	38.5	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range of –40°C to 85°C (unless otherwise noted) See[(1)] [(2)] [(3)]

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –20 μA, $V_{IB} \geq V_{CCB}$ – 0.4 V	1.65 V to 3.6 V	2.3 V to 5.5 V	V_{CCA} × 0.67			V
V_{OLA}		I_{OL} = 1 mA, $V_{IB} \leq$ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V			0.4	V
V_{OHB}		I_{OH} = –20 μA, $V_{IA} \geq V_{CCA}$ – 0.2 V	1.65 V to 3.6 V	2.3 V to 5.5 V	V_{CCB} × 0.67			V
V_{OLB}		I_{OL} = 1 mA, $V_{IA} \leq$ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V			0.4	V
I_I	OE	T_A = 25°C	1.65 V to 3.6 V	1.65 V to 5.5 V			±1	μA
		–40°C to 85°C					±2	
I_{off}	A port	T_A = 25°C	0 V	0 to 5.5 V			±1	μA
		–40°C to 85°C					±2	
	B port	T_A = 25°C	0 to 3.6 V	0 V			±1	μA
		–40°C to 85°C					±2	
I_{OZ}	A or B port	T_A = 25°C	1.65 V to 3.6 V	2.3 V to 5.5 V			±1	μA
		–40°C to 85°C					±2	
I_{CCA}		$V_I = V_O$ = open, I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V			2.4	μA
			3.6 V	0 V			2.2	
			0 V	5.5 V			–1	
I_{CCB}		$V_I = V_O$ = open, I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V			12	μA
			3.6 V	0 V			–1	
			0 V	5.5 V			1	
I_{CCA} + I_{CCB}		$V_I = V_{CCI}$, I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V			14.4	μA
C_I	OE	T_A = 25°C	3.3 V	3.3 V		2.5		pF
		–40°C to 85°C					3.5	
C_{io}	A port	T_A = 25°C	3.3 V	3.3 V		5		pF
		–40°C to 85°C			6			
	B port	T_A = 25°C				6		
		–40°C to 85°C			7.5			

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

6.6 Timing Requirements: V_{CCA} = 1.8 V ± 0.15 V

					MIN	NOM	MAX	UNIT
	Data rate	Push-pull driving, Figure 4		V_{CCB} = 2.5 V, ± 0.2 V			21	Mbps
				V_{CCB} = 3.3 V, ± 0.3 V			22	
				V_{CCB} = 5 V, ± 0.5 V			24	
		Open-drain driving, Figure 5		V_{CCB} = 2.5 V, ± 0.2 V			2	
				V_{CCB} = 3.3 V, ± 0.3 V			2	
				V_{CCB} = 5 V, ± 0.5 V			2	
t_w	Pulse duration Figure 7	Push-pull driving, Figure 4	Data inputs	V_{CCB} = 2.5 V, ± 0.2 V	47			ns
				V_{CCB} = 3.3 V, ± 0.3 V	45			
				V_{CCB} = 5 V, ± 0.5 V	41			
		Open-drain driving, Figure 5		V_{CCB} = 2.5 V, ± 0.2 V	500			
				V_{CCB} = 3.3 V, ± 0.3 V	500			
				V_{CCB} = 5 V, ± 0.5 V	500			

6.7 Timing Requirements V_{CCA} = 2.5 V ± 0.2 V

					MIN	NOM	MAX	UNIT
	Data rate	Push-pull driving, Figure 4		V_{CCB} = 2.5 V, ± 0.2 V			20	Mbps
				V_{CCB} = 3.3 V, ± 0.3 V			22	
				V_{CCB} = 5 V, ± 0.5 V			24	
		Open-drain driving, Figure 5		V_{CCB} = 2.5 V, ± 0.2 V			2	
				V_{CCB} = 3.3 V, ± 0.3 V			2	
				V_{CCB} = 5 V, ± 0.5 V			1	
t_w	Pulse duration Figure 7	Push-pull driving, Figure 4	Data inputs	V_{CCB} = 2.5 V, ± 0.2 V	50			ns
				V_{CCB} = 3.3 V, ± 0.3 V	45			
				V_{CCB} = 5 V, ± 0.5 V	41			
		Open-drain driving, Figure 5		V_{CCB} = 2.5 V, ± 0.2 V	500			
				V_{CCB} = 3.3 V, ± 0.3 V	500			
				V_{CCB} = 5 V, ± 0.5 V	500			

6.8 Timing Requirements: 3.3 V ± 0.3 V

				MIN	NOM	MAX	UNIT
Data rate	Push-pull driving, Figure 4		V_{CCB} = 3.3 V, ± 0.3 V			23	Mbps
			V_{CCB} = 5 V, ± 0.5 V			24	
	Open-drain driving, Figure 5		V_{CCB} = 3.3 V, ± 0.3 V			2	
			V_{CCB} = 5 V, ± 0.5 V			2	
Pulse duration Figure 7	Push-pull driving, Figure 4	Data inputs	V_{CCB} = 3.3 V, ± 0.3 V	43			ns
			V_{CCB} = 5 V, ± 0.5 V	41			
	Open-drain driving, Figure 5		V_{CCB} = 3.3 V, ± 0.3 V	500			
			V_{CCB} = 5 V, ± 0.5 V	500			

6.9 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS (DRIVING)		MIN	MAX	UNIT
t_{PHL} Figure 8	A	B	Push-pull, Figure 4	V_{CCB} = 2.5 V ± 0.2 V		5.3	ns
				V_{CCB} = 3.3 V ± 0.3 V		5.4	
				V_{CCB} = 5 V ± 0.5 V		6.8	
			Open-drain, Figure 5	V_{CCB} = 2.5 V ± 0.2 V	2.3	8.8	
				V_{CCB} = 3.3 V ± 0.3 V	2.4	9.6	
				V_{CCB} = 5 V ± 0.5 V	2.6	10	
t_{PLH} Figure 8			Push-pull, Figure 4	V_{CCB} = 2.5 V ± 0.2 V		6.8	
				V_{CCB} = 3.3 V ± 0.3 V		7.1	
				V_{CCB} = 5 V ± 0.5 V		7.5	
			Open-drain, Figure 5	V_{CCB} = 2.5 V ± 0.2 V	45	260	
				V_{CCB} = 3.3 V ± 0.3 V	36	208	
				V_{CCB} = 5 V ± 0.5 V	27	198	
t_{PHL} Figure 8	B	A	Push-pull, Figure 4	V_{CCB} = 2.5 V ± 0.2 V		4.4	ns
				V_{CCB} = 3.3 V ± 0.3 V		4.5	
				V_{CCB} = 5 V ± 0.5 V		4.7	
			Open-drain, Figure 5	V_{CCB} = 2.5 V ± 0.2 V	1.9	5.3	
				V_{CCB} = 3.3 V ± 0.3 V	1.1	4.4	
				V_{CCB} = 5 V ± 0.5 V	1.2	4	
t_{PLH} Figure 8			Push-pull, Figure 4	V_{CCB} = 2.5 V ± 0.2 V		5.3	
				V_{CCB} = 3.3 V ± 0.3 V		4.5	
				V_{CCB} = 5 V ± 0.5 V		0.5	
			Open-drain, Figure 5	V_{CCB} = 2.5 V ± 0.2 V	45	175	
				V_{CCB} = 3.3 V ± 0.3 V	36	140	
				V_{CCB} = 5 V ± 0.5 V	27	102	
t_{en} Figure 9	OE	A or B	Push-pull, Figure 6	V_{CCB} = 2.5 V ± 0.2 V		200	ns
				V_{CCB} = 3.3 V ± 0.3 V		200	
				V_{CCB} = 5 V ± 0.5 V		200	
t_{dis} Figure 9	OE	A or B		V_{CCB} = 2.5 V ± 0.2 V		50	ns
				V_{CCB} = 3.3 V ± 0.3 V		40	
				V_{CCB} = 5 V ± 0.5 V		35	
t_{rA}	A-port rise time		Push-pull	V_{CCB} = 2.5 V ± 0.2 V	3.2	9.5	ns
				V_{CCB} = 3.3 V ± 0.3 V	2.3	9.3	
				V_{CCB} = 5 V ± 0.5 V	2	7.6	
			Open-drain	V_{CCB} = 2.5 V ± 0.2 V	38	165	
				V_{CCB} = 3.3 V ± 0.3 V	30	132	
				V_{CCB} = 5 V ± 0.5 V	22	95	
t_{rB}	B-port rise time		Push-pull	V_{CCB} = 2.5 V ± 0.2 V	1.1	10.8	ns
				V_{CCB} = 3.3 V ± 0.3 V	1	9.1	
				V_{CCB} = 5 V ± 0.5 V	1	7.6	
			Open-drain	V_{CCB} = 2.5 V ± 0.2 V	34	145	
				V_{CCB} = 3.3 V ± 0.3 V	23	106	
				V_{CCB} = 5 V ± 0.5 V	10	76	

Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V (continued)

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS (DRIVING)		MIN	MAX	UNIT
t_{fA}	A-port fall time		Push-pull	V_{CCB} = 2.5 V ± 0.2 V	1.9	5.9	ns
				V_{CCB} = 3.3 V ± 0.3 V	1.9	6	
				V_{CCB} = 5 V ± 0.5 V	1.4	13.3	
			Open-drain	V_{CCB} = 2.5 V ± 0.2 V	4.4	6.9	
				V_{CCB} = 3.3 V ± 0.3 V	4.3	6.4	
				V_{CCB} = 5 V ± 0.5 V	4.2	6.1	
t_{fB}	B-port fall time		Push-pull	V_{CCB} = 2.5 V ± 0.2 V	2.2	13.8	
				V_{CCB} = 3.3 V ± 0.3 V	2.2	16.2	
				V_{CCB} = 5 V ± 0.5 V	2.6	16.2	
			Open-drain	V_{CCB} = 2.5 V ± 0.2 V	6.9	13.8	
				V_{CCB} = 3.3 V ± 0.3 V	7.5	16.2	
				V_{CCB} = 5 V ± 0.5 V	7	16.2	
Max data rate	A or B		Push-pull	V_{CCB} = 2.5 V ± 0.2 V	21		Mbps
				V_{CCB} = 3.3 V ± 0.3 V	22		
				V_{CCB} = 5 V ± 0.5 V	24		
			Open-drain	V_{CCB} = 2.5 V ± 0.2 V	2		
				V_{CCB} = 3.3 V ± 0.3 V	2		
				V_{CCB} = 5 V ± 0.5 V	2		

6.10 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS (DRIVING)		MIN	MAX	UNIT
t_{PHL} Figure 8	A	B	Push-pull, Figure 4	V_{CCB} = 2.5 V ± 0.2 V		3.2	ns
				V_{CCB} = 3.3 V ± 0.3 V		3.7	
				V_{CCB} = 5 V ± 0.5 V		3.8	
			Open-drain, Figure 5	V_{CCB} = 2.5 V ± 0.2 V	1.7	6.3	
				V_{CCB} = 3.3 V ± 0.3 V	2	6	
				V_{CCB} = 5 V ± 0.5 V	2.1	5.8	
t_{PLH} Figure 8			Push-pull, Figure 4	V_{CCB} = 2.5 V ± 0.2 V		3.5	
				V_{CCB} = 3.3 V ± 0.3 V		4.1	
				V_{CCB} = 5 V ± 0.5 V		4.4	
			Open-drain, Figure 5	V_{CCB} = 2.5 V ± 0.2 V	43	250	
				V_{CCB} = 3.3 V ± 0.3 V	36	206	
				V_{CCB} = 5 V ± 0.5 V	27	190	

Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V (continued)

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS (DRIVING)		MIN	MAX	UNIT
t_{PHL} Figure 8	B	A	Push-pull, Figure 4	V_{CCB} = 2.5 V ± 0.2 V		3	ns
				V_{CCB} = 3.3 V ± 0.3 V		3.6	
				V_{CCB} = 5 V ± 0.5 V		4.3	
			Open-drain, Figure 5	V_{CCB} = 2.5 V ± 0.2 V	1.8	4.7	
				V_{CCB} = 3.3 V ± 0.3 V	1.6	4.2	
				V_{CCB} = 5 V ± 0.5 V	1.2	4	
t_{PLH} Figure 8			Push-pull, Figure 4	V_{CCB} = 2.5 V ± 0.2 V		2.5	
				V_{CCB} = 3.3 V ± 0.3 V		1.6	
				V_{CCB} = 5 V ± 0.5 V		1	
			Open-drain, Figure 5	V_{CCB} = 2.5 V ± 0.2 V	44	170	
				V_{CCB} = 3.3 V ± 0.3 V	37	140	
				V_{CCB} = 5 V ± 0.5 V	27	103	
t_{en} Figure 9	OE	A or B	Push-pull, Figure 6	V_{CCB} = 2.5 V ± 0.2 V		200	ns
				V_{CCB} = 3.3 V ± 0.3 V		200	
				V_{CCB} = 5 V ± 0.5 V		200	
t_{dis} Figure 9	OE	A or B		V_{CCB} = 2.5 V ± 0.2 V		50	ns
				V_{CCB} = 3.3 V ± 0.3 V		40	
				V_{CCB} = 5 V ± 0.5 V		35	
t_{rA}	A-port rise time		Push-pull	V_{CCB} = 2.5 V ± 0.2 V	2.8	7.4	ns
				V_{CCB} = 3.3 V ± 0.3 V	2.1	6.6	
				V_{CCB} = 5 V ± 0.5 V	0.9	5.6	
			Open-drain	V_{CCB} = 2.5 V ± 0.2 V	34	149	
				V_{CCB} = 3.3 V ± 0.3 V	28	121	
				V_{CCB} = 5 V ± 0.5 V	24	89	
t_{rB}	B-port rise time		Push-pull	V_{CCB} = 2.5 V ± 0.2 V	1.3	8.3	ns
				V_{CCB} = 3.3 V ± 0.3 V	0.9	7.2	
				V_{CCB} = 5 V ± 0.5 V	0.4	6.1	
			Open-drain	V_{CCB} = 2.5 V ± 0.2 V	35	151	
				V_{CCB} = 3.3 V ± 0.3 V	24	112	
				V_{CCB} = 5 V ± 0.5 V	12	81	
t_{fA}	A-port fall time		Push-pull	V_{CCB} = 2.5 V ± 0.2 V	1.9	5.7	ns
				V_{CCB} = 3.3 V ± 0.3 V	1.4	5.5	
				V_{CCB} = 5 V ± 0.5 V	0.8	5.3	
			Open-drain	V_{CCB} = 2.5 V ± 0.2 V	4.4	6.9	
				V_{CCB} = 3.3 V ± 0.3 V	4.3	6.2	
				V_{CCB} = 5 V ± 0.5 V	4.2	5.8	
t_{fB}	B-port fall time		Push-pull	V_{CCB} = 2.5 V ± 0.2 V	2.2	7.8	
				V_{CCB} = 3.3 V ± 0.3 V	2.4	6.7	
				V_{CCB} = 5 V ± 0.5 V	2.6	6.6	
			Open-drain	V_{CCB} = 2.5 V ± 0.2 V	5.1	8.8	
				V_{CCB} = 3.3 V ± 0.3 V	5.4	9.4	
				V_{CCB} = 5 V ± 0.5 V	5.4	10.4	

Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V (continued)

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

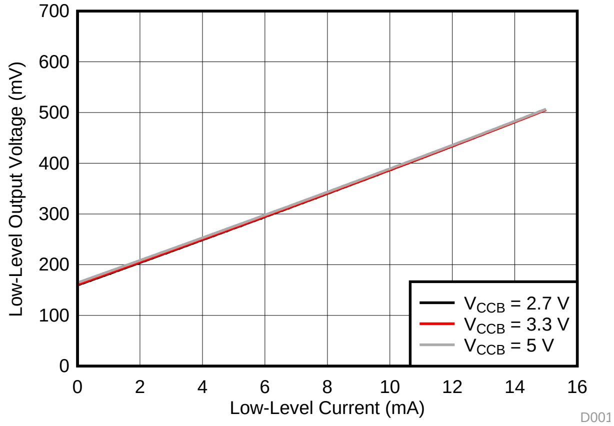
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS (DRIVING)		MIN	MAX	UNIT
Max data rate	A or B		Push-pull	V_{CCB} = 2.5 V ± 0.2 V	20		Mbps
				V_{CCB} = 3.3 V ± 0.3 V	22		
				V_{CCB} = 5 V ± 0.5 V	24		
			Open-drain	V_{CCB} = 2.5 V ± 0.2 V	2		
				V_{CCB} = 3.3 V ± 0.3 V	2		
				V_{CCB} = 5 V ± 0.5 V	2		

6.11 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

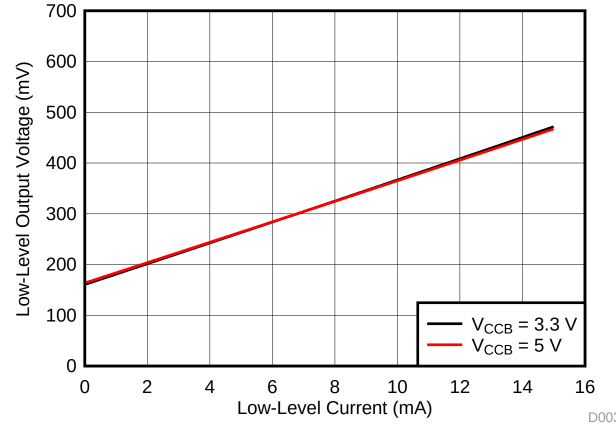
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS (DRIVING)		MIN	MAX	UNIT
t_{PHL} Figure 8	A	B	Push-pull, Figure 4	V_{CCB} = 3.3 V ± 0.3 V		2.4	ns
				V_{CCB} = 5 V ± 0.5 V		3.1	
			Open-drain, Figure 5	V_{CCB} = 3.3 V ± 0.3 V	1.3	4.2	
				V_{CCB} = 5 V ± 0.5 V	1.4	4.6	
t_{PLH} Figure 8			Push-pull, Figure 4	V_{CCB} = 3.3 V ± 0.3 V		4.2	
				V_{CCB} = 5 V ± 0.5 V		4.4	
			Open-drain, Figure 5	V_{CCB} = 3.3 V ± 0.3 V	36	204	
				V_{CCB} = 5 V ± 0.5 V	28	165	
t_{PHL} Figure 8	B	A	Push-pull, Figure 4	V_{CCB} = 3.3 V ± 0.3 V		2.5	ns
				V_{CCB} = 5 V ± 0.5 V		3.3	
			Open-drain, Figure 5	V_{CCB} = 3.3 V ± 0.3 V	1	124	
				V_{CCB} = 5 V ± 0.5 V	1	97	
t_{PLH} Figure 8			Push-pull, Figure 4	V_{CCB} = 3.3 V ± 0.3 V		2.5	
				V_{CCB} = 5 V ± 0.5 V		2.6	
			Open-drain, Figure 5	V_{CCB} = 3.3 V ± 0.3 V	3	139	
				V_{CCB} = 5 V ± 0.5 V	3	105	
t_{en} Figure 9	OE	A or B	Push-pull, Figure 6	V_{CCB} = 3.3 V ± 0.3 V		200	ns
				V_{CCB} = 5 V ± 0.5 V		200	
t_{dis} Figure 9	OE	A or B		V_{CCB} = 3.3 V ± 0.3 V		40	ns
				V_{CCB} = 5 V ± 0.5 V		9.8	
t_{rA}	A-port rise time		Push-pull	V_{CCB} = 3.3 V ± 0.3 V	2.3	5.6	ns
				V_{CCB} = 5 V ± 0.5 V	1.9	4.8	
			Open-drain	V_{CCB} = 3.3 V ± 0.3 V	25	116	
				V_{CCB} = 5 V ± 0.5 V	19	85	
t_{rB}	B-port rise time		Push-pull	V_{CCB} = 3.3 V ± 0.3 V	1.6	6.4	ns
				V_{CCB} = 5 V ± 0.5 V	0.6	7.4	
			Open-drain	V_{CCB} = 3.3 V ± 0.3 V	26	116	
				V_{CCB} = 5 V ± 0.5 V	14	72	
t_{fA}	A-port fall time		Push-pull	V_{CCB} = 3.3 V ± 0.3 V	1.4	5.4	ns
				V_{CCB} = 5 V ± 0.5 V	1	5	
			Open-drain	V_{CCB} = 3.3 V ± 0.3 V	4.3	6.1	
				V_{CCB} = 5 V ± 0.5 V	4.2	5.7	
t_{fB}	B-port fall time		Push-pull	V_{CCB} = 3.3 V ± 0.3 V	2.3	7.4	
				V_{CCB} = 5 V ± 0.5 V	2.4	7.6	
			Open-drain	V_{CCB} = 3.3 V ± 0.3 V	5	7.6	
				V_{CCB} = 5 V ± 0.5 V	4.8	8.3	
Max data rate	A or B		Push-pull	V_{CCB} = 3.3 V ± 0.3 V	23		Mbps
				V_{CCB} = 5 V ± 0.5 V	24		
			Open-drain	V_{CCB} = 3.3 V ± 0.3 V	2		
				V_{CCB} = 5 V ± 0.5 V	2		

6.12 Typical Characteristics



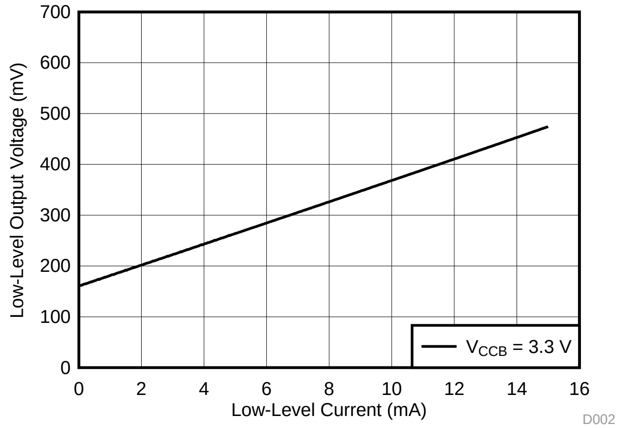
V_{CCA} = 1.8 V $V_{IL(A)}$ = 150 mV

Figure 1. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



V_{CCA} = 2.7 V $V_{IL(A)}$ = 150 mV

Figure 2. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



V_{CCA} = 3.3 V $V_{IL(A)}$ = 150 mV

Figure 3. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

7 Parameter Measurement Information

7.1 Load Circuits

Figure 4 shows the push-pull driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time. Figure 5 shows the open-drain driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time.

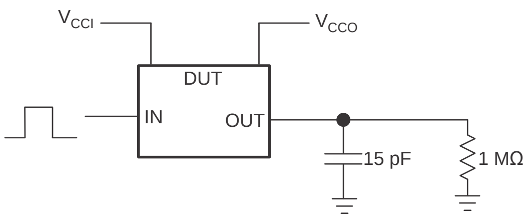


Figure 4. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver

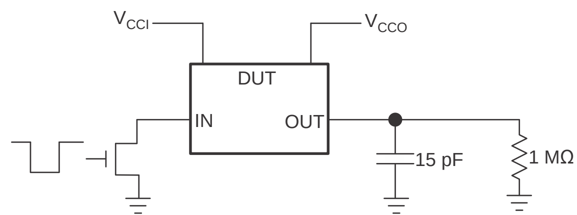


Figure 5. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver

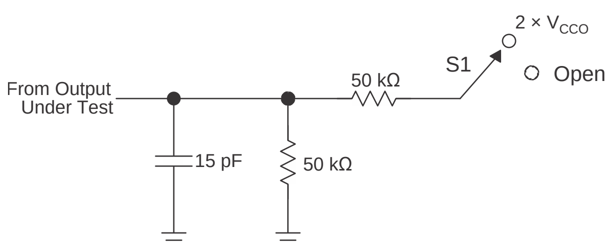


Figure 6. Load Circuit for Enable-Time and Disable-Time Measurement

TEST	S1
t_{PZL} / t_{PLZ} (t_{dis})	2 × V_{CCO}
t_{PHZ} / t_{PZH} (t_{en})	Open

1. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
2. t_{PZL} and t_{PZH} are the same as t_{en}.
3. V_{CCI} is the V_{CC} associated with the input port.
4. V_{CCO} is the V_{CC} associated with the output port.

7.2 Voltage Waveforms

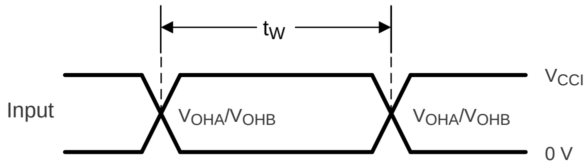


Figure 7. Pulse Duration (Push-Pull)

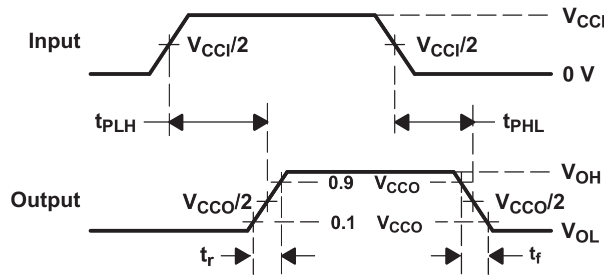
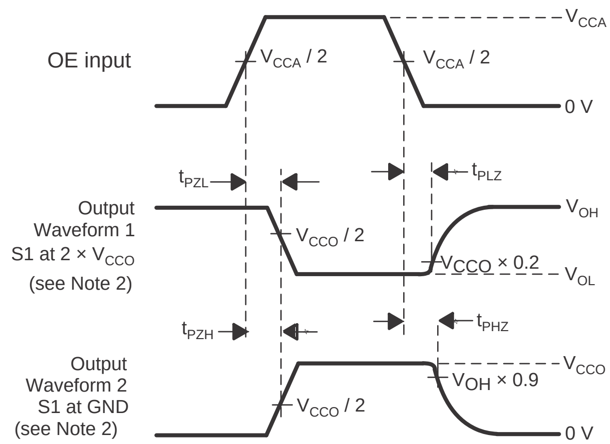


Figure 8. Propagation Delay Times



- C_L includes probe and jig capacitance.
- Waveform 1 in Figure 9 is for an output with internal such that the output is high, except when OE is high (see Figure 6). Waveform 2 in Figure 9 is for an output with conditions such that the output is low, except when OE is high.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- t_{PZL} and t_{PZH} are the same as t_{en}.
- t_{PLH} and t_{PHL} are the same as t_{pd}.
- V_{CCI} is the V_{CC} associated with the input port.
- V_{CCO} is the V_{CC} associated with the output port.

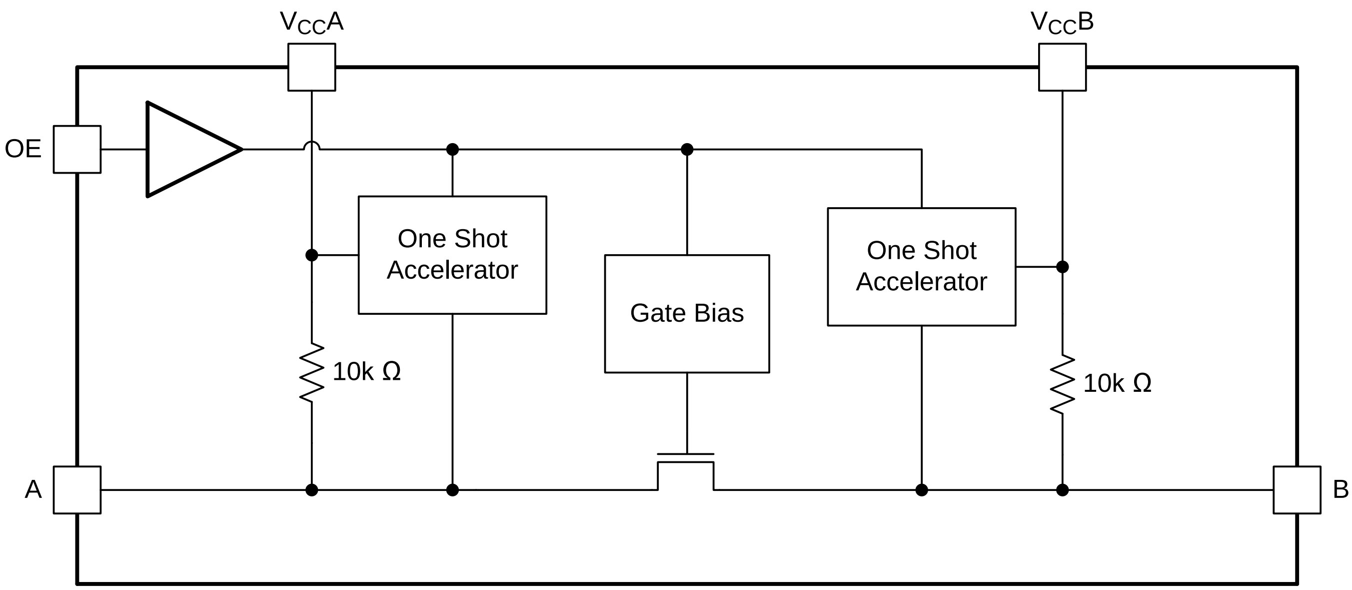
Figure 9. Enable and Disable Times

8 Detailed Description

8.1 Overview

The TXS0101 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65 V to 3.6 V, while the B port can accept I/O voltages from 2.3 V to 5.5 V. The device is a pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. 10 kΩ pullup resistors, commonly used in open drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open drain applications, the device can also translate push-pull CMOS logic outputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Architecture

The TXS0101 architecture (see Figure 10) does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

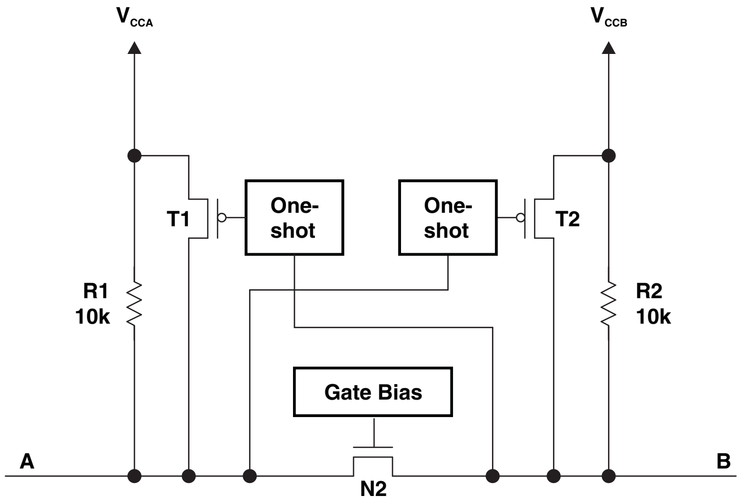


Figure 10. Architecture of a TXS01xx Cell

Each A-port I/O has an internal 10 kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10 kΩ pullup resistor to V_{CCB}. The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1,T2) for a short duration, which speeds up the low-to-high transition.

8.3.2 Input Driver Requirements

The fall time (t_{fA}, t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the TXS0101. Similarly, the t_{PHL} and max data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

8.3.3 Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first.

8.3.4 Enable and Disable

The TXS0101 has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. The disable time (t_{dis}) indicates the delay between the time when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

8.3.5 Pullup or Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10 kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10 kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10 kΩ resistors).

8.4 Device Functional Modes

The TXS0101 device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXS0101 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXS0101 is ideal for use in applications where an open-drain driver is connected to the data I/Os. The TXB0101 can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0102 might be a better option for such push-pull applications.

9.2 Typical Application

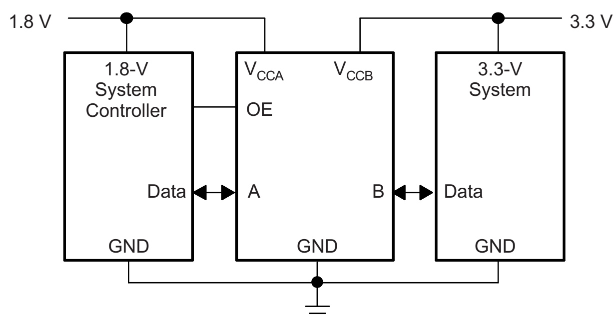


Figure 11. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6 V
Output voltage range	2.3 to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

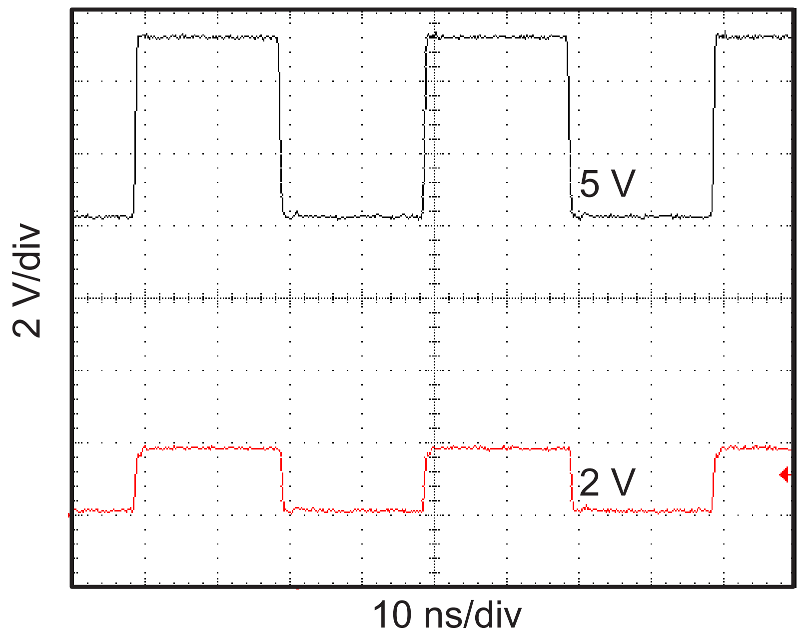
- Input voltage range
  - Use the supply voltage of the device that is driving the TXS0101 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXS0101 device is driving to determine the output voltage range.
  - The TXS0101 device has 10 kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.

- An external pull down resistor decreases the output V_{OH} and V_{OL}. Use Equation 1 to calculate the V_{OH} as a result of an external pull down resistor.

  $$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10\ k\Omega) \quad (1)$$

  where
  - V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB}
  - R_{PD} is the value of the external pull down resistor

9.2.3 Application Curve



V_{CCA} = 1.8 V V_{CCB} = 5 V

Figure 12. Level-Translation of a 2.5-MHz Signal

10 Power Supply Recommendations

The TXS0101 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCB} accepts any supply voltage from 2.3 V to 5.5 V and V_{CCA} accepts any supply voltage from 1.65 V to 3.6 V as long as Vs is less than or equal to V_{CCB}. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low voltage bidirectional translation between any of the 1.8 V, 2.5 V, 3.3 V, and 5 V voltage nodes.

The TXS0101 device does not require power sequencing between V_{CCA} and V_{CCB} during power-up so the power-supply rails can be ramped in any order. A V_{CCA} value greater than or equal to V_{CCB} ($V_{CCA} \geq V_{CCB}$) does not damage the device, but during operation, V_{CCA} must be less than or equal to V_{CCB} ($V_{CCA} \leq V_{CCB}$) at all times.

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

11.2 Layout Example

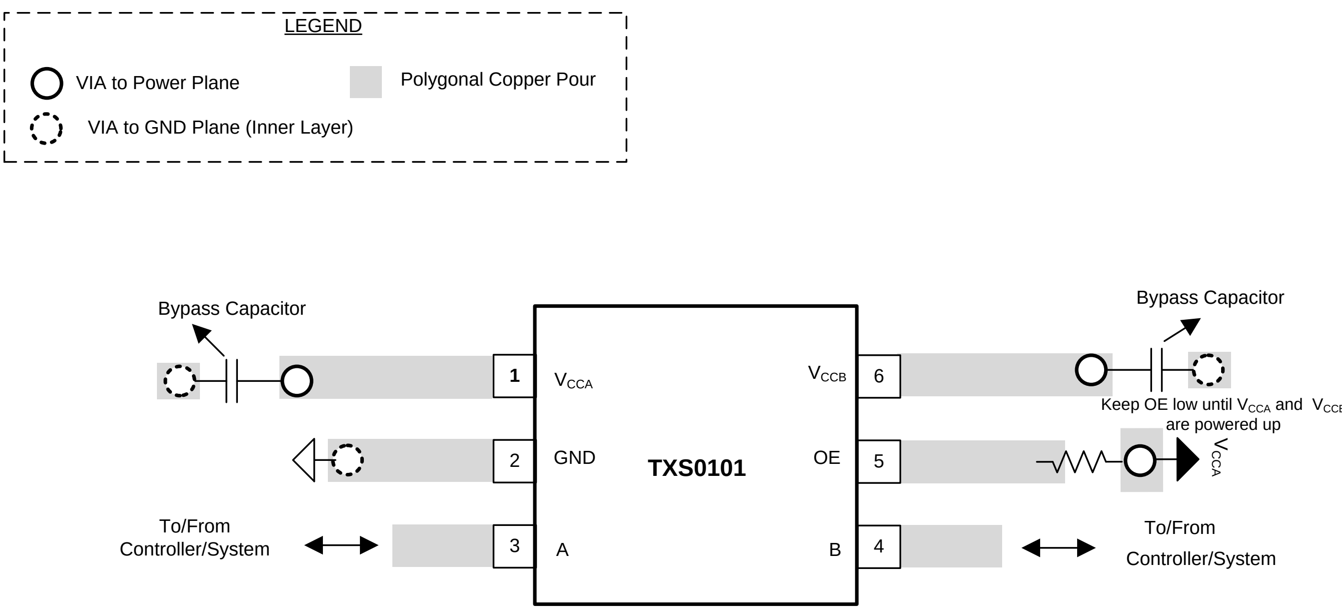


Figure 13. Typical Layout of TXS0101

12 Device and Documentation Support

12.1 Device Support

12.1.1 Related Documentation

For related documentation, see the following:

- A Guide to Voltage Translation With TXS-Type Translators, SCEA044
- Introduction to Logic, SLVA700

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS0101DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFFF ~ NFFR)	Samples
TXS0101DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFFF ~ NFFR)	Samples
TXS0101DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	NFFR	Samples
TXS0101DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFFR	Samples
TXS0101DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2GO	Samples
TXS0101DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2GO	Samples
TXS0101DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2GO	Samples
TXS0101DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2GR	Samples
TXS0101DRLRG4	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2GR	Samples
TXS0101YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(2G7 ~ 2GN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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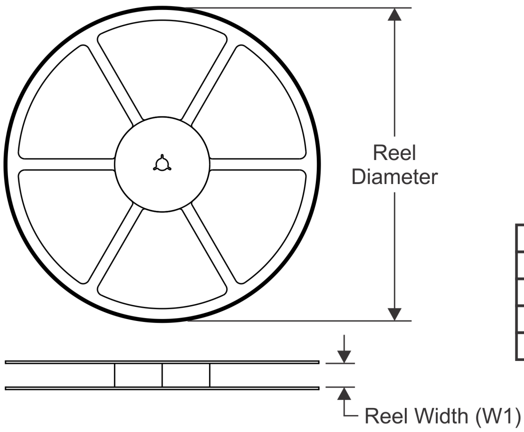
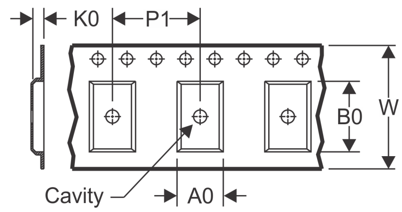
TAPE AND REEL INFORMATION

REEL DIMENSIONS

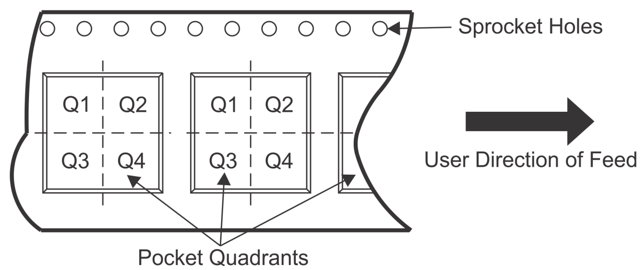


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

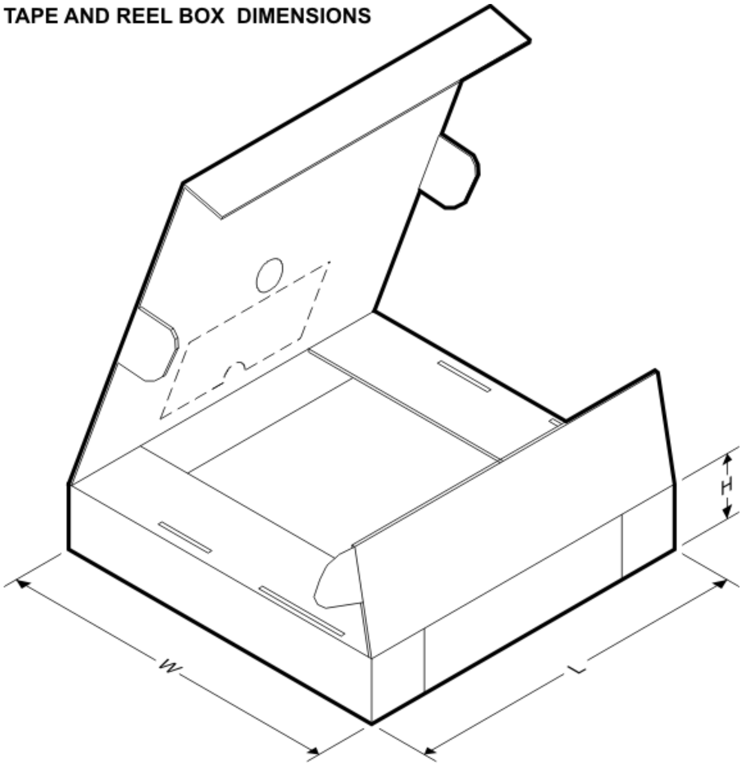
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0101DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TXS0101DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TXS0101DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TXS0101DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TXS0101DRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TXS0101YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

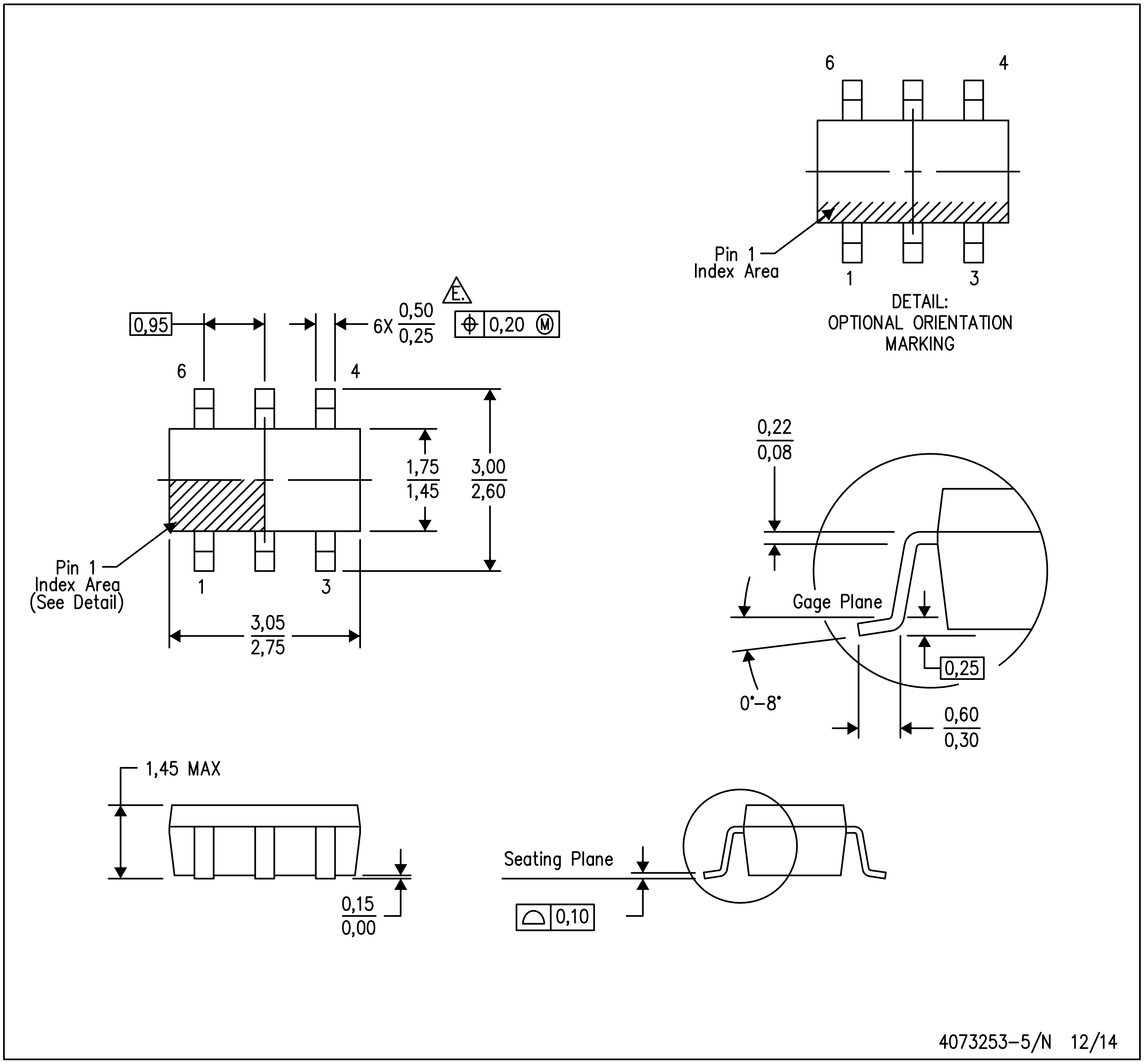
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

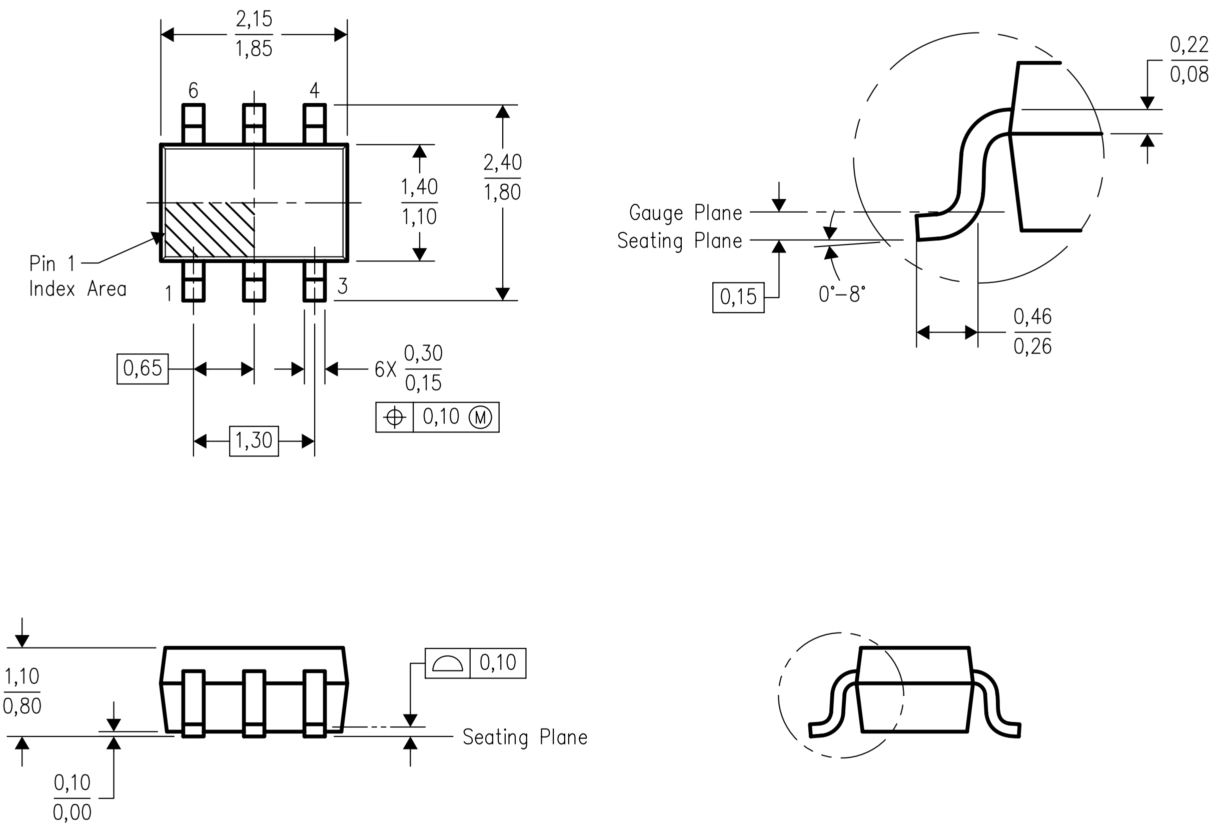
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0101DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TXS0101DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
TXS0101DCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TXS0101DCKT	SC70	DCK	6	250	203.0	203.0	35.0
TXS0101DRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TXS0101YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



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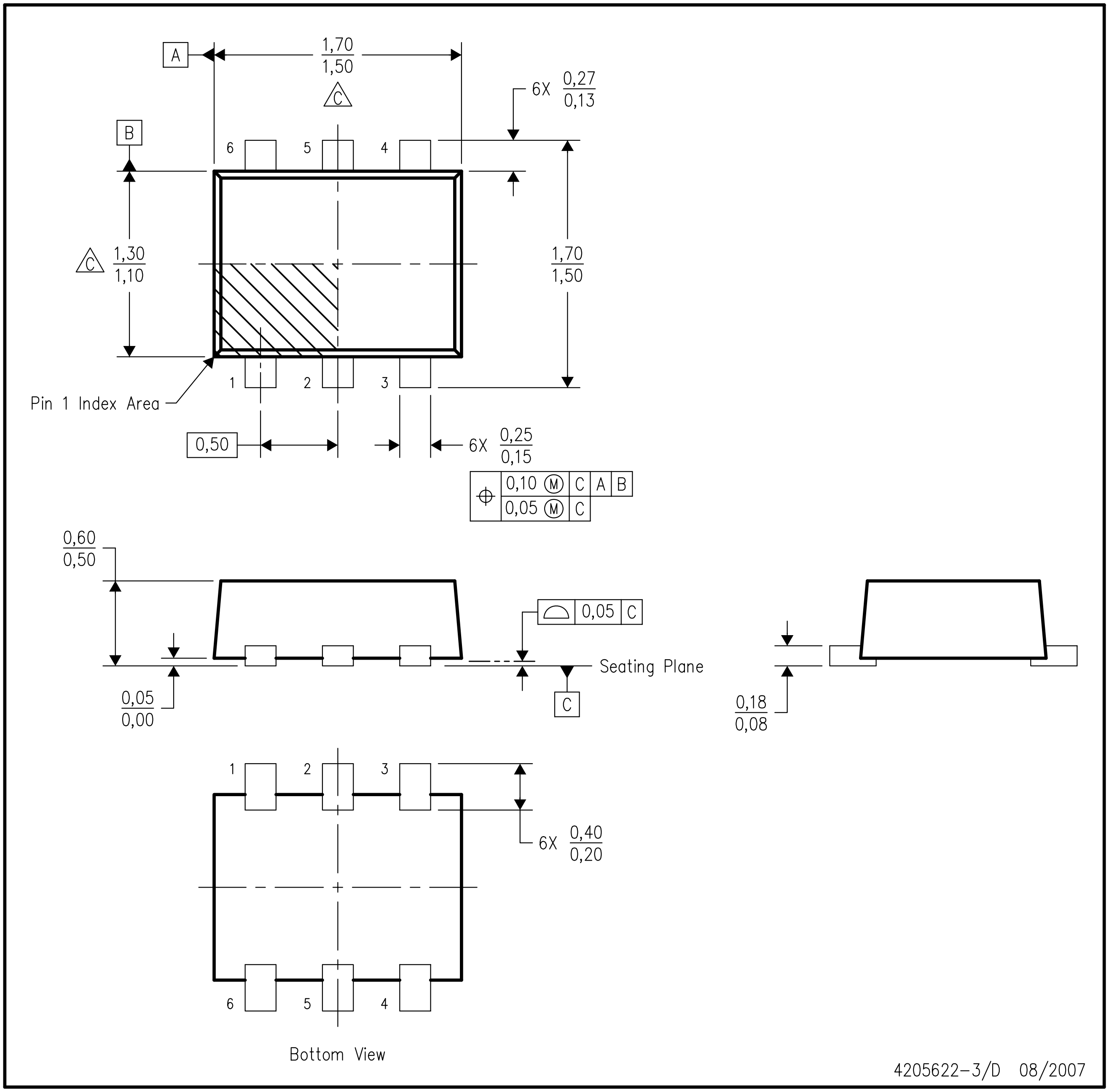
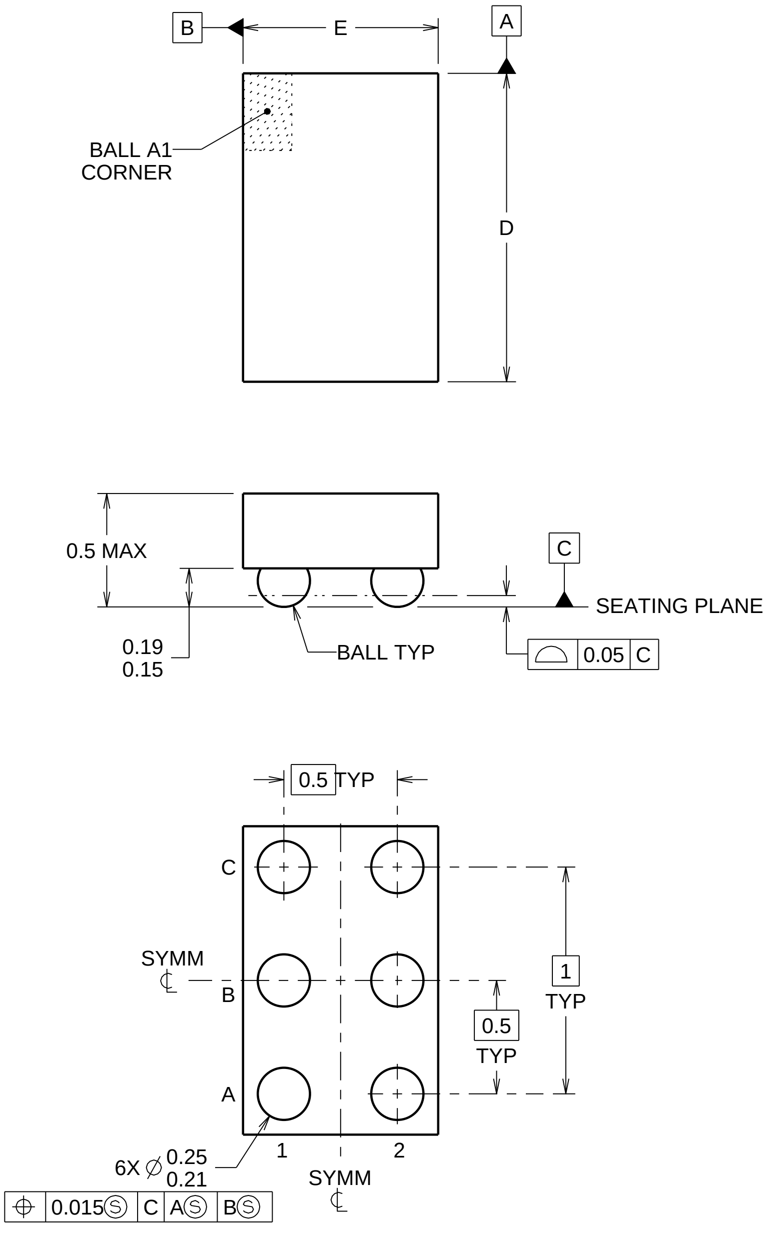
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.



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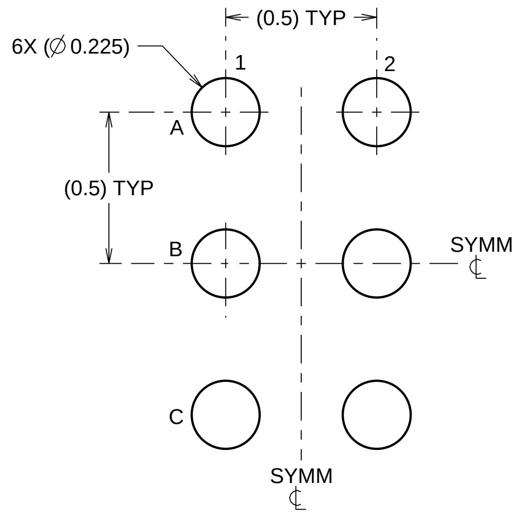
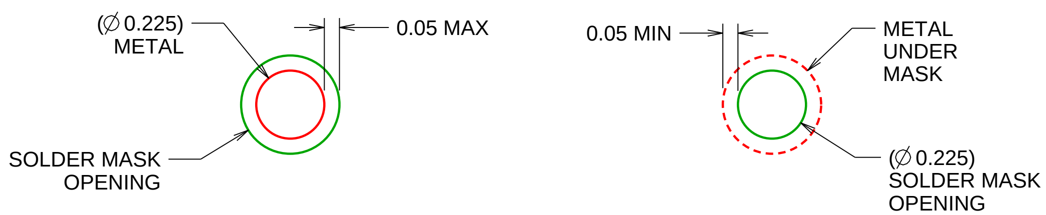
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X



NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

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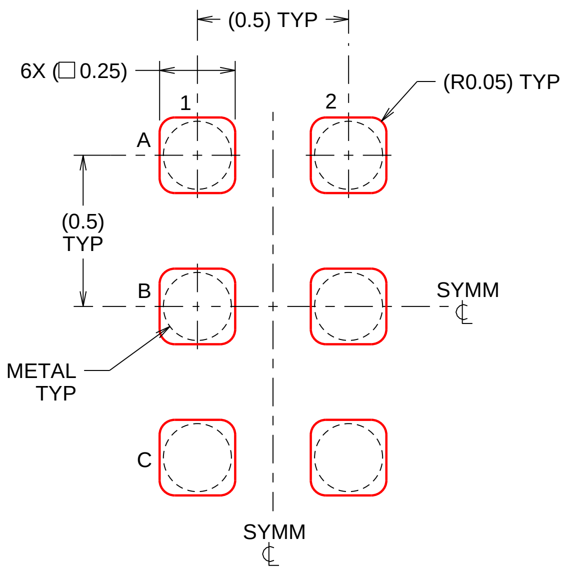
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.