TPS65290 Low-Quiescent-Current, Multi-Mode PMIC for Battery-Powered, Energy-Harvesting Applications

1 Features

- Operating Input Voltage Range: 2.2 V to 5 V
- 500-mA Buck-Boost Converter, Stand-Alone Operation or Serial-Bus Controlled
- PFM/PWM Operation With Forced PWM Option
- 150-mA LDO
- Stand-Alone or Serial-Bus (SPI or I^2C) Controlled
- Two Power Distribution Switches Powered From Buck-Boost Output
- One Power Distribution Switch Powered From the Maximum of Buck Boost or Battery Input
- Two Power Distribution Switches Powered From LDO Output
- One Power Switch Powered From Battery Input
- One Power Switch to Connect BB Output to LDO Output and Improve System Efficiency
- Automaticly Maximize System Energy Management With the internal MAX block
- Low-Power Always-On Bias Supply for Microcontroller Sleep Mode With Three Factory-Selectable Options:
  - 10-mA, 100-nA IDDQ Deep-Sleep Zero-Leakage-Current Bias Controller With Preset Voltage
  - 10-mA, 400-nA IDDQ LDO_{MINI}
  - 30-mA, 300-nA IDQQ $Buck_{MINI}$
- Input Voltage Recovery Comparator With Selectable Threshold
- Factory Selectable SPI or I^2C Interface
- –40°C to 85°C Ambient Temperature Range
- 24-Pin RHF (VQFN) Package

2 Applications

- Low-Power, Energy-Harvesting Systems
- Battery-Powered Applications

3 Description

The TPS65290 device is a power-managemant integrated circuit (PMIC) designed to operate in applications dependent on efficient power management over a wide range of system load conditions ranging from fractions of a microamp to a few hundred milliamps. The device operates over a wide 2.2-V to 5-V input-voltage range and incorporates a very low-quiescent-current always-on power supply, a 500-mA buck-and-boost converter, a 150-mA low-dropout regulator (LDO) and eight power-distribution switches. The always-on supply features three different factory selectable options: 30-mA buck converter with 300-nA quiescent current, 10-mA LDO with 400-nA quiescent current, and 10-mA zero IDDQ drop with 100-nA quiescent current. The buck-boost converter employs PFM or PWM operation with forced PWM option, for maximum overall efficiency. A designer can use the switches to support different configurations for the various loads supported by the TPS65290 device. For energy-harvesting applications, the device integrates a programmable input-voltage monitor to allow for connection and disconnection of the different power blocks and switches without the intervention of the master processor.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65290	VQFN (24)	5.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Buck-Boost Efficiency

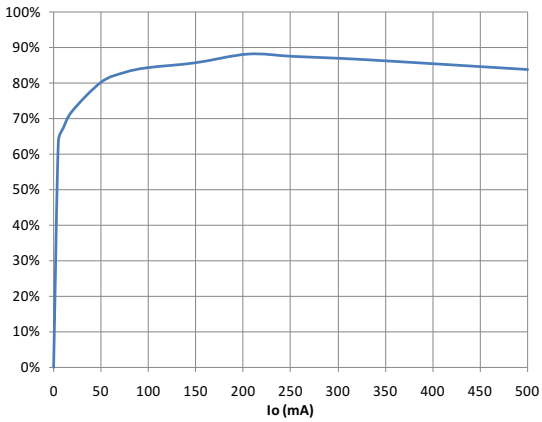


Table of Contents

4 Revision History

Changes from Revision B (June 2013) to Revision C **Page**

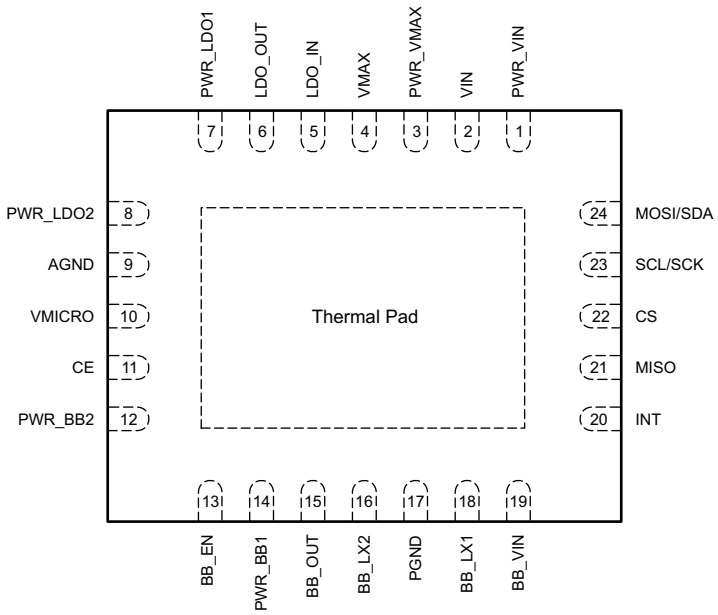
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

5 Description (Continued)

To maximize control flexibility, the TPS65290 device includes a factory-selectable choice between SPI and I^2C interfaces. To minimize PC board footprint and reduce bill of materials (BOM) components and cost, the PMIC internally includes resistive dividers (boost-buck, LDO, V_{IN} monitor), I^2C pullup resistors, SPI pulldown resistors, boost-buck compensation, and an interrupt pullup resistor. Completion of a comprehensive multi-rail solution for efficient flow meter, handheld industrial, fitness, and other long-term data-acquisition systems requires only low-cost ceramic capacitors and power inductors.

6 Pin Configuration and Functions

RHF Package
24-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	9	—	Analog ground connection. Connect to PGND and thermal pad.
BB_EN	13	I	Buck-boost converter enable pin
BB_LX1	18	O	Buck-boost boost-converter switching node
BB_LX2	16	O	Buck-boost boost-converter switching node
BB_OUT	15	O	Buck-boost converter output
BB_VIN	19	I	Input pin to buck-boost converter
CE	11	I	This is the chip enable (CE). When low the PMIC is in deep sleep, BIAS supply to the micro is enabled, and a pulldown termination disables the interrupt output. When high, the I^2C or SPI is active; the internal switches are operable, along with the interrupt logic and boost or buck.
CS	22	I	SPI bus chip select (active-high) when SPI enabled
$\overline{INT}$	20	O	Push-pull output
LDO_IN	5	I	LDO input. Decouple this pin with a 2.2-µF ceramic capacitor.
LDO_OUT	6	O	LDO output. Decouple this pin with a 2-µF ceramic capacitor.
MISO	21	O	Master input, slave output. Serial-data transmit interface
MOSI/SDA	24	I	Master output, slave input or serial-data receive interface for SPI and I^2C
PGND	17	—	Power ground connection. Connect to AGND and thermal pad.
PWR_BB1	14	O	Switch-controlled supply connected to the BB output. Decouple with a 1-µF ceramic capacitor.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PWR_BB2	12	O	Switch-controlled supply connected to the BB output. Decouple with a 1-µF ceramic capacitor.
PWR_LDO1	7	O	Switch-controlled supply connected to the LDO output. Decouple with a ceramic capacitor.
PWR_LDO2	8	O	Switch-controlled supply connected to the LDO output. Decouple with a ceramic capacitor.
PWR_VIN	1	O	Power for system output from VIN
PWR_VMAX	3	O	Switch-controlled supply connected to VMAX. Decouple with a ceramic capacitor.
SCL/SCK	23	I	Serial-data clock (SPI and I^2C)
VIN	2	I	Battery supply
VMAX	4	O	This pin shows the maximum of VIN or VBB. Decouple with a 1-µF ceramic capacitor.
VMICRO	10	O	Microcontroller supply
Thermal pad	—	—	Connect the pad to AGND, PGND and PCB GND. The thermal pad does not have electrical connections to the IC.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	BB_VIN, LDO_IN	–0.3	7	V
	BB_EN, CE, CS, MOSI/SDA, SCL/SCK, VIN	–0.3	5.5	
Output voltage	BB_LX1, BB_LX2	–1	7	V
	BB_OUT, PWR_BB2. PWR_VMAX	–0.3	7	
	INT, LDO_OUT, MISO, PWR_BB1, PWR_LDO1, PWR_LDO2, PWR_VIN, VMAX, VMICRO	–0.3	5.5	
Ground	AGND, PGND	–0.3	0.3	V
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(VIN)}$	Supply voltage	VIN	2.2		5	V
V_I	Input voltage	BB_EN	1.2			V
		BB_VIN	1.8	3.6	5	
		LDO_IN	3		5	
V_{IN_BM}	Input voltage		2.2		5	V
V_{IH}	Input high-level		0.67 × V_{MICRO}			V
V_{IL}	Input Low-level				0.33 × V_{MICRO}	V
V_{HYS}	Input hysteresis		10			mV
T_A	Operating free-air temperature		–40		125	ºC

7.4 Thermal Information

THERMAL METRIC(1)		TPS65290 RHF (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY UVLO AND INTERNAL SUPPLY						
IDD	Quiescent current always on blocks Factory configured CE = 0	Zero-bias mode		100		nA
		LDO_{MINI} mode		400		
		$BUCK_{MINI}$ mode		300		
		V_I = 3.6-V LDO enabled		5		µA
		V_I = 3.6 V, BB enabled, V_{BB_OUT} = 4.5 V, PFM mode		40		
RECOVERY VOLTAGE COMPARATOR						
$COMP_{RVLEVEL}$	Threshold voltage serial interface selectable	Rising V_I, 8 steps, 0.1-V threshold	2.4		3.1	V
		Falling V_I, 8 steps, 0.1-V threshold	1.7		2.4	
$COMP_{RVACCURACY}$	Comparator accuracy			3%		
IQQ_{COMPRV}	Quiescent Current	Buck-boost enabled		10		µA
		Buck-boost disabled		10		
ENABLE PINS (CE, BB_EN)						
V_H	Enable high	V_{MICRO} = 2.2 V to 2.8 V	1.2			V
V_L	Enable low	V_{MICRO} = 2.2 V to 2.8 V			0.4	V
BUCK-BOOST (BB)						
VIN_{START_UP}	Start-up voltage, no load BB_OUT < 4.5	T_A = –40°C to 85°C		1.8		V
	Start-up voltage, no load BB_OUT > 4.5	T_A = –40°C to 85°C		2.5		
$VIN_{SUSTAIN}$	The minimum input voltage in which the buck-boost converter sustains its operation after starting up	T_A = –40°C to 85°C		1.8		V

Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBB	DC output accuracy (PWM mode)	T_J = 25°C	–3%		3%	
	Maximum line regulation	V_I = 3 V to 3.6 V, I_O = 300 mA		0.5%		
	Maximum load regulation	I_O = 100 mA to 500 mA		0.5%		
$VBB_{OUTRANGE}$	Output voltage range	29 steps of 0.1 V from 1 V to 5 V	1		5	V
$DUTY_{BUCK\_MIN}$	Minimum duty cycle in buck mode			25%	30%	
I_{SW}	Average high-side switch-current limit	V_I = 3.6 V, T_A = 25°C		2400		mA
$VBB_{(RDSON\_HIGH)}$	High-side switch on-resistance	V_I = 3.6 V, T_A = 25°C		120		mΩ
$VBB_{(RDSON\_LOW)}$	Low-side switch on-resistance	V_I = 3.6 V, T_A = 25°C		120		mΩ
LDO						
$V_{LDO\_OUT\_RANGE}$	Output voltage range	32 steps of 0.1 V from 1 V to 4 V	1		4	V
$V_{LDO\_OUT\_ACCURACY}$	DC output accuracy	V_I = 3.6 V, V_O = 2.8 V, T_J = –40°C to 125°C, I_{Load} = 5 mA	–4%		4%	
LDO_{LINE_REG}	Line regulation	V_I = 3.3 V to 6 V, V_O = 2.8 V, I_O = 5 mA	–1%		1%	
LDO_{LOAD_REG}	Load regulation	V_I = 2.2 V to 5 V, I_O = 0 mA to 110 mA	–2%		2%	
V_{DROOP}	Dropout voltage	Allows for 5% output voltage droop, V_I = 3.6 V to 6 V, I_O = 0 mA to 150 mA			300	mV
ICL	Output current limit	V_{LDO_OUT} = 2.8 V, output voltage shorted		300		mA
PSRR	Power-supply rejection ratio at 10 kHz	V_{LDO_OUT} = 2.8 V, V_I = 3.1 V, 150-mA loading		28		dB
MICRO BIAS CIRCUIT (Different options)						
Zero Leak Adjustable Bias (TPS65290ZB)						
V_{MICRO_MIN}	Minimum output voltage			1.3		V
V_{BIAS_DROP}	Voltage difference between VIN (pin#4) and VMICRO	Nine 200-mV steps from 0.6 V to 2 V	0.6		2.0	V
V_{OUT}	DC output accuracy measured by V_{BIAS_DROP}.	T_J = 25°C, I_O = 1 µA, BAT = 3.6 V	–10%		10%	
$ZERO_{LOAD\_REG}$	Load regulation	I_O = 100 nA–10 mA , T_J = 25°C, BAT = 3.6 V, VMICRO[3:0] = 0000			15%	
LDO_{MINI} (TPS65290LM)						
V_{LDO_RANGE}		16 steps of 0.2 V from 1.8 V to 3.3 V	1.8		3.3	V
V_{OUT}	DC output accuracy	T_J = 25°C, V_I = 3.6 V, I_O = 1 µA	–5%		5%	
LDO_{LOAD_REG}	Load regulation	1 µA ≤ I_O ≤ 10 mA	–5%		5%	
V_{DROOP}	Dropout voltage– allow for 5% output voltage drop at V_{DROOP}.	V_O = 2.2 V, I_O = 10 mA			300	mV
ICL	Output current limit	V_{LDO_OUT} = 2.8 V	20		50	mA
$BUCK_{MINI}$ Internal Hysteretic Converter (TPS65290BM)						
I_{Load_BM}	Output load range		0		30	mA
f_{SW_BM}	$Buck_{MINI}$ switching frequency	L_{BM} = 33 µH, C_{BM} = 1 µF, ESR_C_{BM} = 1 Ω, No load		5		Hz
I_{PK_IND}	Peak inductor current	T_J = 25°C , L_{BM} = 33 µH, C_{BM} = 1 µF, ESR_C_{BM} = 1 Ω, V_I = 3.6 V, V_O = 2.5 V, I_O = 30 mA in high-power mode		80		mA
$I_{PK\_IND\_STARTUP}$	Peak inductor current during start-up	T_J = 25°C , L_{BM} = 33 µH, C_{BM} = 1 µF, ESR_C_{BM} = 1 Ω, V_I = 3.6 V, V_O = 2.5 V, I_O = 30 mA in high-power mode		140		mA
V_{BM_RIPPLE}	Ripple voltage	T_J = 25°C , V_I = 3.6 V, V_O = 2.5 V), L_{BM} = 33 µH, C_{BM} = 1 µF, ESR_C_{BM} = 1 Ω		5%		
POWER SWITCHES						
PWR_BB1	Distribution switch on-resistance from BB_OUT pin to PWR_BB1 pin (single P MOSFET)	V_I = 3.6 V, V_{BB} = 4.5 V, T_A = 25°C		100		mΩ
PWR_VMAX_ V_{MAX}	Distribution switch on-resistance from VMAX pin to PWR_VMAX pin (single P MOSFET)	V_I = 3.6 V, V_{BB} = 4.5 V, T_A = 25°C		600		mΩ

Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWR_BB2	Distribution switch on-resistance from BB_OUT pin to PWR_BB2 pin (single P MOSFET)	V_I = 3.6 V, V_{BB} = 4.5 V, T_A = 25°C		600		mΩ
PWR_LDO1	Distribution switch on-resistance from LDO_OUT pin to PWR_LDO1 pin (single P MOSFET)	V_I = 3.6 V, V_{LDO} = 2.8 V, T_A = 25°C		300		mΩ
PWR_LDO2	Distribution switch on-resistance from LDO_OUT pin to PWR_LDO2 pin (single P MOSFET)	V_I = 3.6 V, V_{LDO} = 2.8 V, T_A = 25°C		600		mΩ
PWR_MICRO_LDO	Distribution switch on-resistance from LDO_OUT pin to VMICRO pin (single P MOSFET)	V_I = 3.6 V, V_{LDO} = 2.8 V, T_A = 25°C		600		mΩ
PWR_VIN	Distribution switch on-resistance from VIN pin to PWR_VIN pin (single P MOSFET)	V_I = 3.6 V, T_A = 25°C		1000		mΩ
PWR_BB_LDO	Distribution switch-on resistance (internal use only) from BB_OUT pin to LDO_OUT pin (back-to-back P MOSFETs)	V_I = 3.6 V, V_{BB} = 4.5 V, T_A = 25°C		1000		mΩ
$R_{PULLDOWN}$	Pulldown resistance (connection selectable by EEPROM bit)			1.2		kΩ
LOGIC LEVEL OUTPUTS (INT, MISO)						
V_{OL}	Output level low	V_{MICRO} = 2.2 V to 2.8 V , I_{load} = 1 mA			0.4	V
V_{OH}	Output level high	V_{MICRO} = 2.2 V to 2.8 V , I_{load} = 1 mA	V_{MICRO} – 0.4			V
LOGIC LEVEL INPUT (CS, MOSI, CLK, SDA SCK)						
V_{IH}	Input high level	V_{MICRO} = 2.2 V to 2.8 V	0.67 × V_{MICRO}			V
V_{IL}	Input low level	V_{MICRO} = 2.2 V to 2.8 V			0.33 × V_{MICRO}	V
V_{HYS}	Input hysteresis		10			mV
R_{PULLUP}	Pullup resistor to VMICRO	I^2C mode enabled		10		kΩ
$R_{PULLDOWN}$	Pulldown resistor to GND	SPI mode enabled		100		kΩ
THERMAL SHUTDOWN FOR BUCK-BOOST CIRCUIT						
T_{TRIP_BB}	Buck-boost thermal protection trip point			141		°C
T_{HYST_BB}	Buck-boost thermal protection hysteresis			12		°C
CENTRAL THERMAL SHUTDOWN						
T_{TRIP_IC}	Thermal protection trip point	Rising temperature		160		°C
T_{HYST_IC}	Thermal protection hysteresis			20		°C

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{STR_BB}	Start-up time		500		µs
t_{STRLDO}	Start-up time, bandgap already enabled		200		µs

7.7 SPI Interface Timing Requirements

Minimum supply voltage is 2.2 V

			MIN	NOM	MAX	UNIT
$t_{c(SCL/SCK)}$	Cycle time, SCL/SCK	1 (see Figure 1)	100			ns
$t_{w(SCL/SCKH)}$	Pulse duration, SCL/SCK high	2 (see Figure 1)	40			ns
$t_{w(SCL/SCKL)}$	Pulse duration, SCL/SCK low	3 (see Figure 1)	40			ns
$t_{su(MISO - SCL/SCKH)}$	Delay time, MISO valid before SCL/SCK high(1)	4 (see Figure 1)			20	ns
$t_{su(MOSI - SCL/SCKH)}$	Setup time, MOSI valid before SCK high	5 (see Figure 1)	25			ns
$t_{h(SCL/SCKH - MOSI)}$	Hold time, MOSI valid after SCL/SCK high	6 (see Figure 1)	25			ns
$t_{su(CS - SCL/SCKH)}$	Setup time, CS rising to SCL/SCK high	7 (see Figure 1)	50			ns
$t_{h(CS - SCL/SCKH)}$	Hold time, CS falling after SCL/SCK high	8 (see Figure 1)	50			ns

(1) CLOAD = 20 pF

7.8 I²C Interface Timing Requirements

		MIN	MAX	UNIT
f_{MAX}	Clock frequency		400	kHz
$t_{(HIGH)}$	Clock high time	600		ns
$t_{(LOW)}$	Clock low time	1300		ns
t_r	SDA and SCL/SCK rise time		300	ns
t_f	SDA and SCL/SCK fall time		300	ns
$t_{h(STA)}$	Hold time (repeated) START condition (after this period the first clock pulse is generated)	600		ns
$t_{su(STA)}$	Setup time for repeated START condition	600		ns
$t_{h(DATA)}$	Data input hold time	0		ns
$t_{su(DATA)}$	Data input setup time	100		ns
$t_{su(STO)}$	STOP condition setup time	600		ns
$t_{(BUF)}$	Bus free time, SDA high	1300		ns

7.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f	Oscillator frequency			1600		kHz

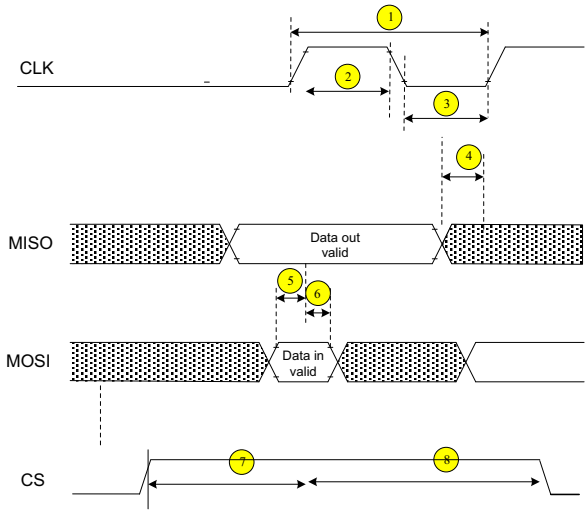


Figure 1. Timing Diagram

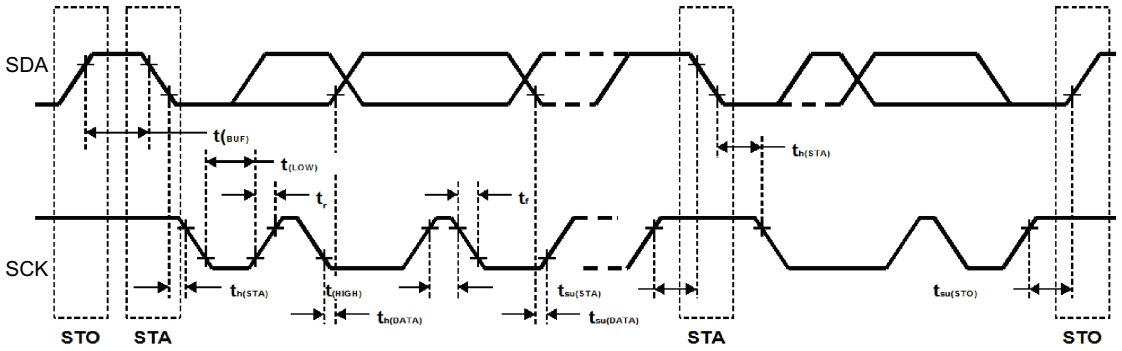
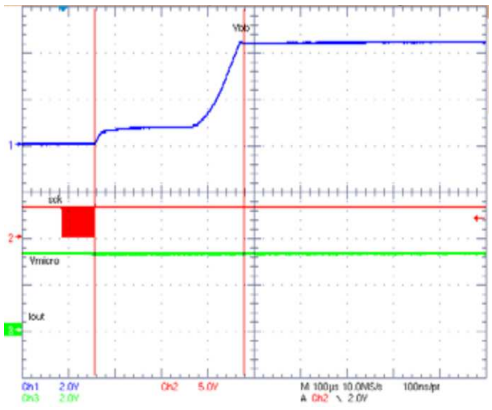


Figure 2. Serial Interface Timing Diagram

7.10 Typical Characteristics

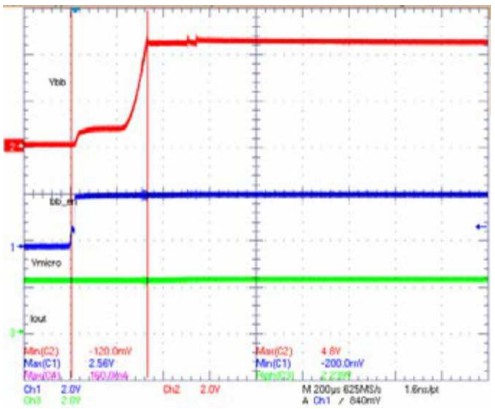
7.10.1 Typical Characteristics: Buck-Boost

T_J = 25°C (unless otherwise noted)



Ch1: BB output
Ch2: I²C SCLK turns on buck-boost
Ch3: VMICRO
Start-up time is 330 µs
Buck-Boost L and C are per application circuit

Figure 3. Buck-Boost Startup Waveform With I²C Command



Ch1: BB_EN signal
Ch2: BB output
Ch3: VMICRO
Start-up time is 330 µs
Buck-Boost L and C are per application circuit

Figure 4. Buck-Boost Start-Up Waveform With BB_EN Pin Command

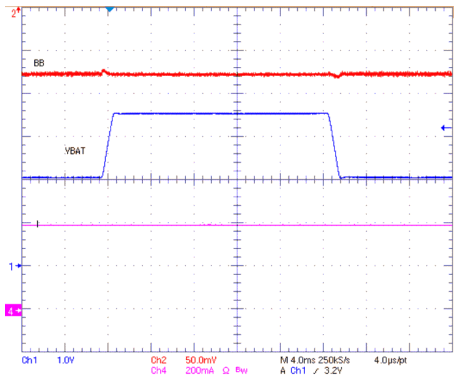
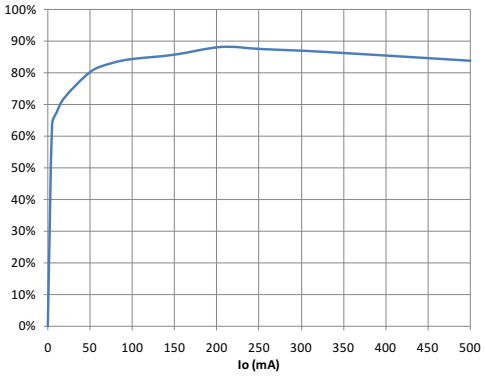
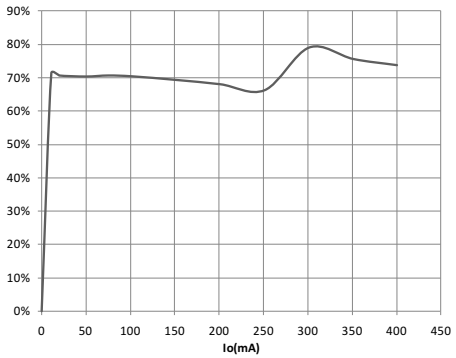


Figure 5. Buck-Boost Line Regulation, Boost Mode



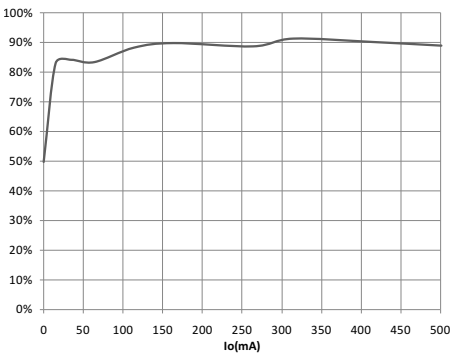
V_I = 3.6 V
V_O = 4.5 V

Figure 6. Buck-Boost Efficiency



V_I = 2.5 V
V_O = 4.5 V

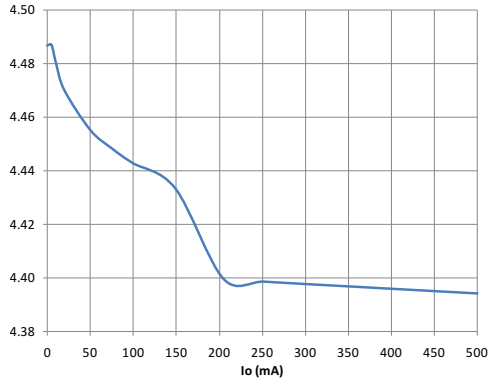
Figure 7. Buck-Boost Efficiency



V_I = 3.6 V
V_O = 2.8 V

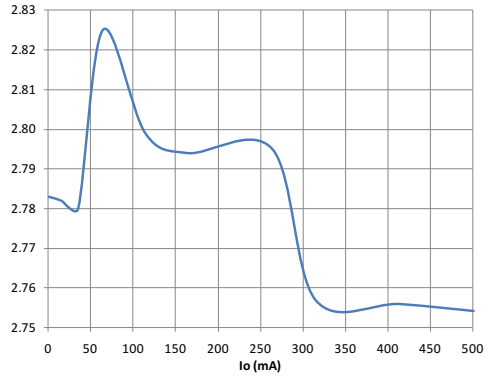
Figure 8. Buck-Boost Efficiency

Typical Characteristics: Buck-Boost (continued)



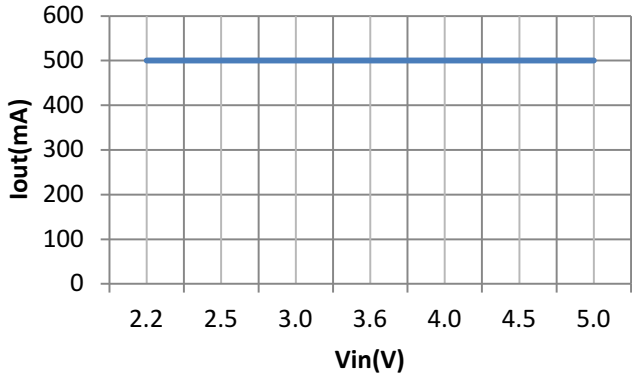
V_I = 3.6 V V_O = 4.5 V PFM mode

Figure 9. Buck-Boost Load Regulation



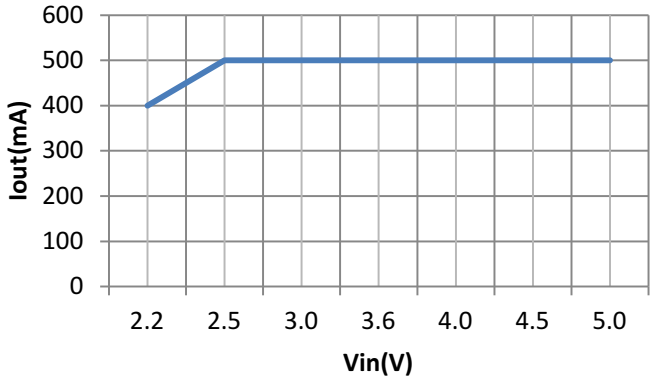
Buck-Boost Loading T_A = 85°C V_{BB} < 4.5 V
V_I = 3.6 V V_O = 2.8 V PFM mode

Figure 10. Buck-Boost Load Regulation



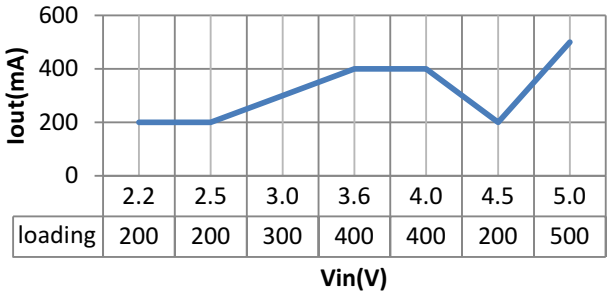
T_A = 25°C V_{BB} > 4.5 V

Figure 11. Buck-Boost Loading



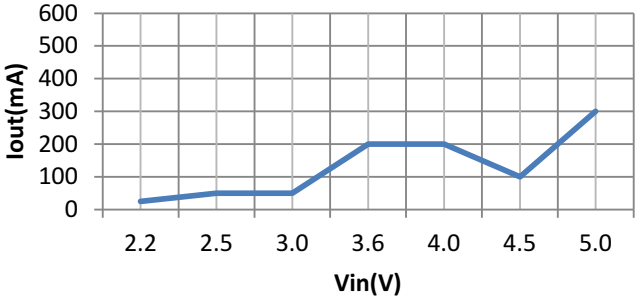
T_A = 85°C V_{BB} > 4.5 V

Figure 12. Buck-Boost Loading



T_A = –10°C V_{BB} > 4.5 V

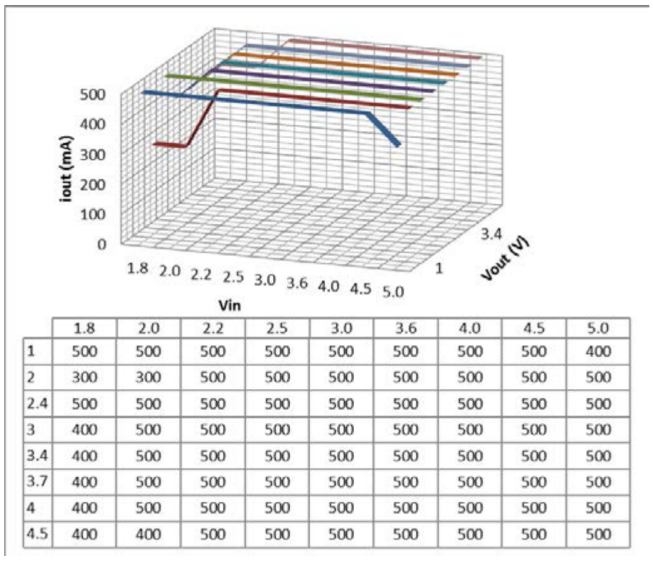
Figure 13. Buck-Boost Loading



T_A = –40°C V_{BB} > 4.5 V

Figure 14. Buck-Boost Loading

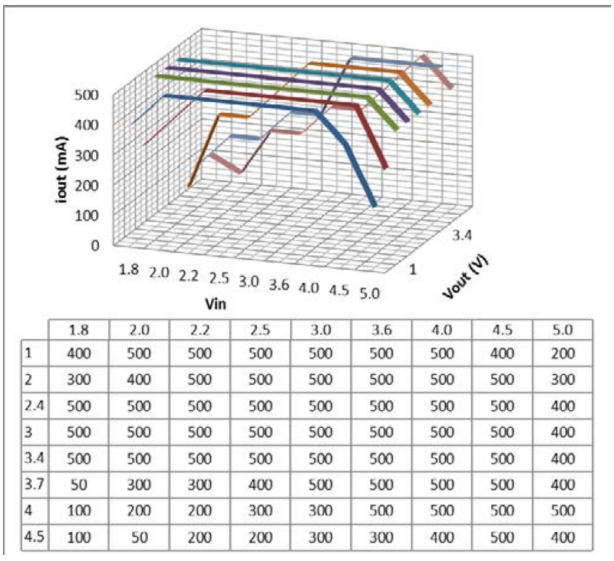
Typical Characteristics: Buck-Boost (continued)



	1.8	2.0	2.2	2.5	3.0	3.6	4.0	4.5	5.0
1	500	500	500	500	500	500	500	500	400
2	300	300	500	500	500	500	500	500	500
2.4	500	500	500	500	500	500	500	500	500
3	400	500	500	500	500	500	500	500	500
3.4	400	500	500	500	500	500	500	500	500
3.7	400	500	500	500	500	500	500	500	500
4	400	500	500	500	500	500	500	500	500
4.5	400	400	500	500	500	500	500	500	500

T_A = 25°C V_{BB} < 4.5 V

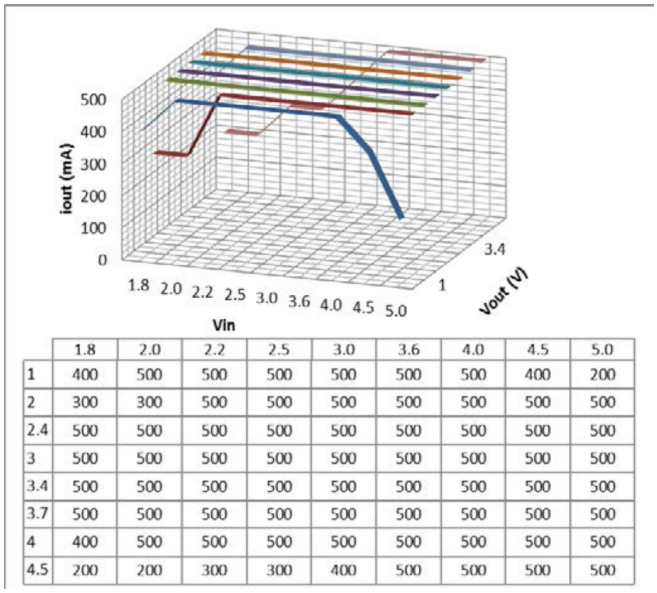
Figure 15. Buck-Boost Loading



	1.8	2.0	2.2	2.5	3.0	3.6	4.0	4.5	5.0
1	400	500	500	500	500	500	500	400	200
2	300	400	500	500	500	500	500	500	300
2.4	500	500	500	500	500	500	500	500	400
3	500	500	500	500	500	500	500	500	400
3.4	500	500	500	500	500	500	500	500	400
3.7	50	300	300	400	500	500	500	500	400
4	100	200	200	300	300	500	500	500	500
4.5	100	50	200	200	300	300	400	500	400

T_A = –40°C V_{BB} < 4.5 V

Figure 16. Buck-Boost Loading



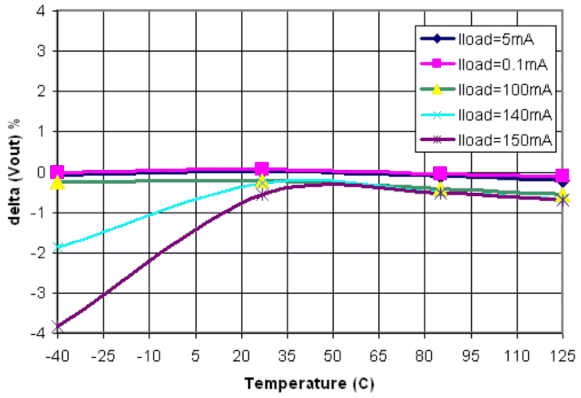
	1.8	2.0	2.2	2.5	3.0	3.6	4.0	4.5	5.0
1	400	500	500	500	500	500	500	400	200
2	300	300	500	500	500	500	500	500	500
2.4	500	500	500	500	500	500	500	500	500
3	500	500	500	500	500	500	500	500	500
3.4	500	500	500	500	500	500	500	500	500
3.7	500	500	500	500	500	500	500	500	500
4	400	500	500	500	500	500	500	500	500
4.5	200	200	300	300	400	500	500	500	500

T_A = –10°C V_{BB} < 4.5 V

Figure 17. Buck-Boost Loading

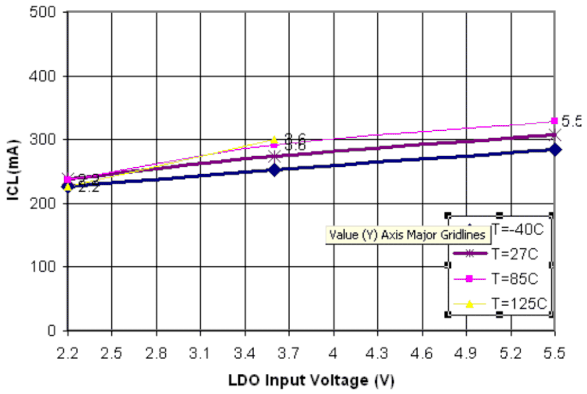
7.10.2 Typical Characteristics (LDO)

T_J = 25°C (unless otherwise noted)



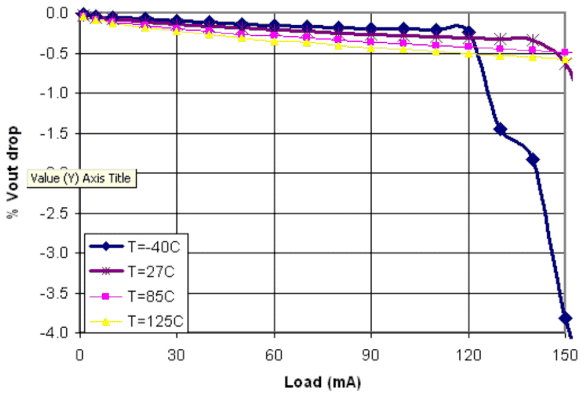
V_I = 3.6 V V_O = 2.8 V (typ)

Figure 18. LDO V_{OUT} Accuracy vs Temperature



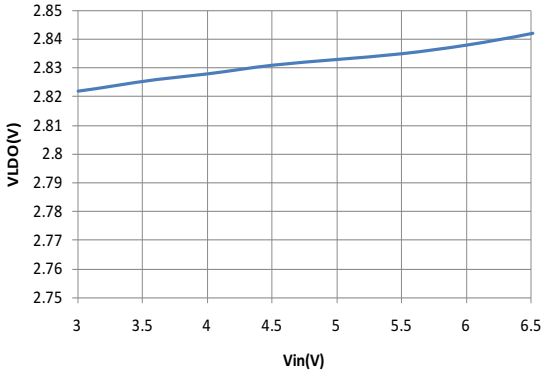
V_O = 2.8 V before short

Figure 19. LDO Short Circuit Current Limit vs V_I



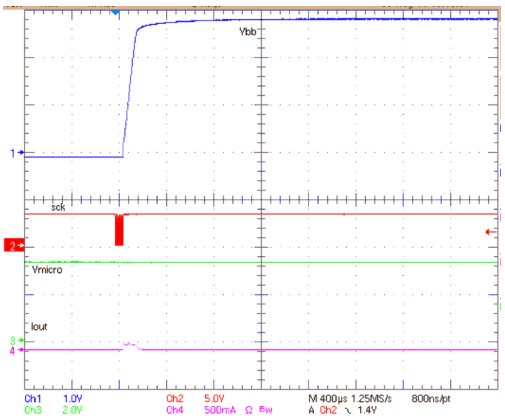
V_I = 3.6 V V_O = 2.8 V

Figure 20. Load Regulation



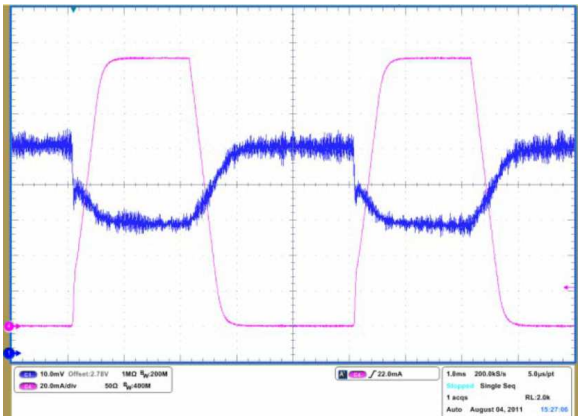
V_O = 2.8 V I_O = 5 mA

Figure 21. Line Regulation



Ch1: LDO output Ch 2: I²C SCLK Ch3: VMICRO
Ch4: VIN current Startup time is approximately 200 µs.

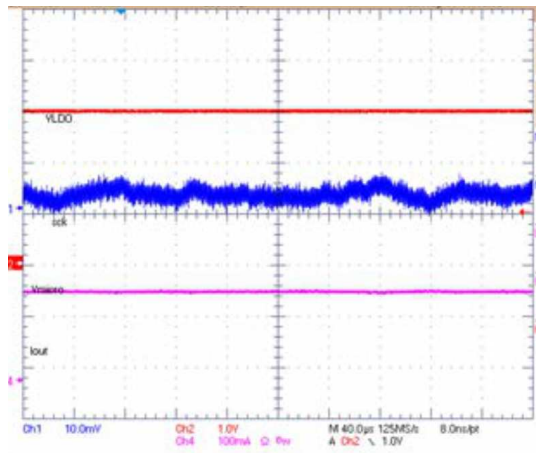
Figure 22. LDO Start-Up Waveform With I²C Command



Ch1: LDO output (10 mV/div) Ch4 load current (20 mA/div)

Figure 23. LDO Load-Transient Response (0 to 150 mA)

Typical Characteristics (LDO) (continued)



Ch1: LDO output Ch 2: LDO input Ch4: LDO current

Figure 24. LDO Input-to-Output Voltage

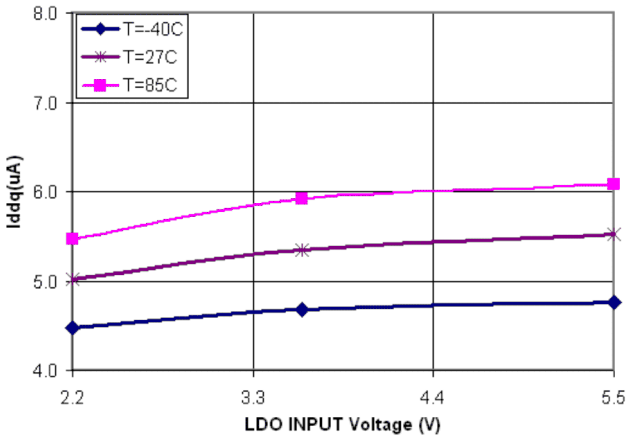
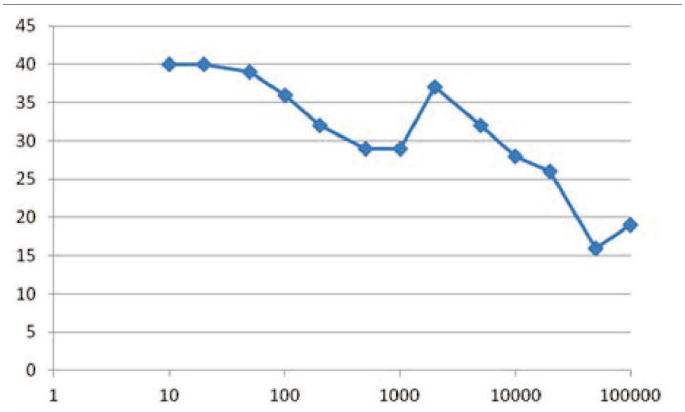


Figure 25. Main LDO IDDQ

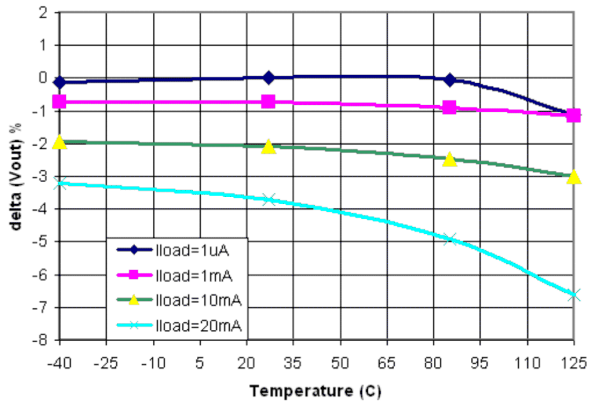


10 Hz to 100 kHz LDO output = 2.8 V LDO input = 3.1 V
150-mA loading

Figure 26. LDO PSRR (dB)

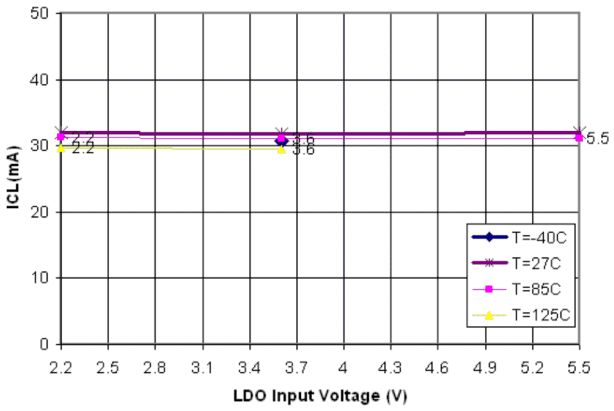
7.10.3 Typical Characteristics (LDO_{MINI})

T_J = 25°C (unless otherwise noted)



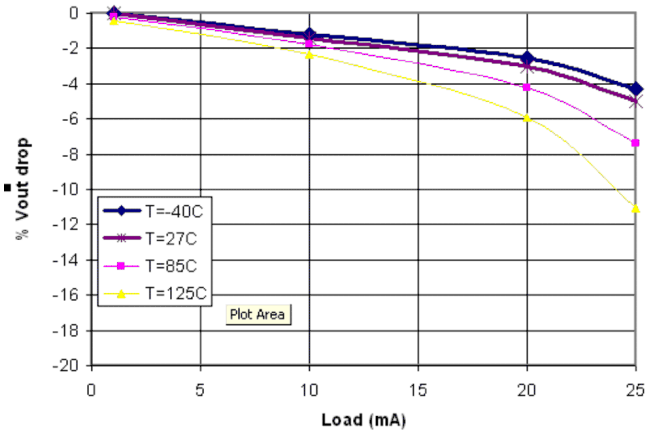
V_I = 3.6 V V_O = 2.2 V (typ)

Figure 27. LDO_{MINI} V_{OUT} Accuracy vs Temperature



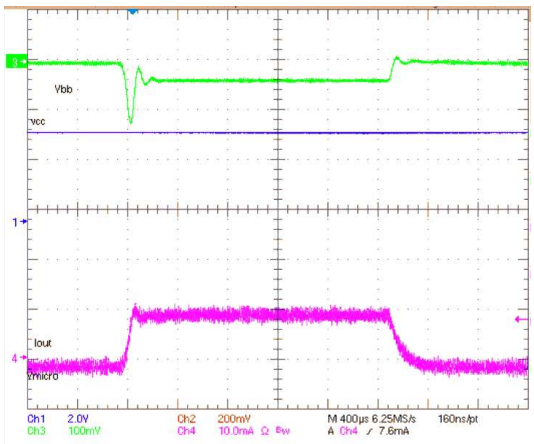
V_O = 2.2 V before short

Figure 28. LDO_{MINI} ShortCircuit Current Limit vs V_I



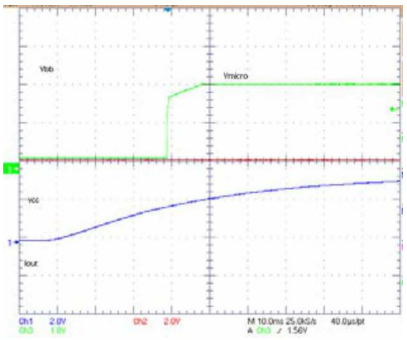
V_I = 3.6 V V_O = 2.2 V

Figure 29. LDO_{MINI} Load Regulation



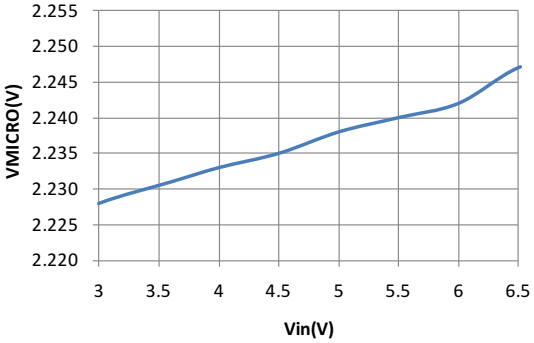
Ch1: VIN Ch3: VMICRO (LDO_{MINI} output) (100 mV/div)
Ch4: Load current (10 mA/div)

Figure 30. LDO_{MINI} Load-Transient Response (0 to 10 mA)



Ch1: VIN rising Ch 3: VMICRO (LDO_{MINI} output)
Input battery connected to 27-Ω resistor and 1000-µF capacitor

Figure 31. LDO_{MINI} Start-Up Waveform With VIN Rising

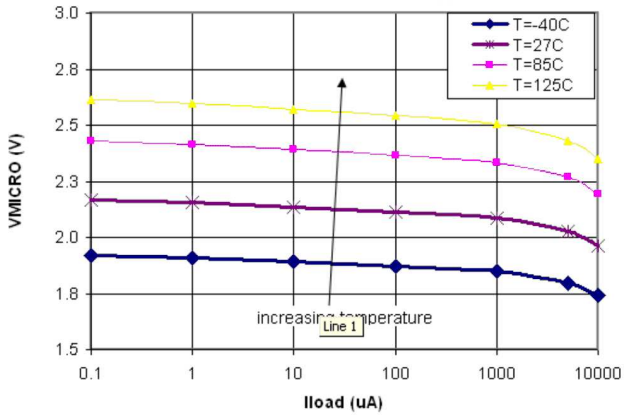


V_O = 2.2 V No load

Figure 32. Line Regulation

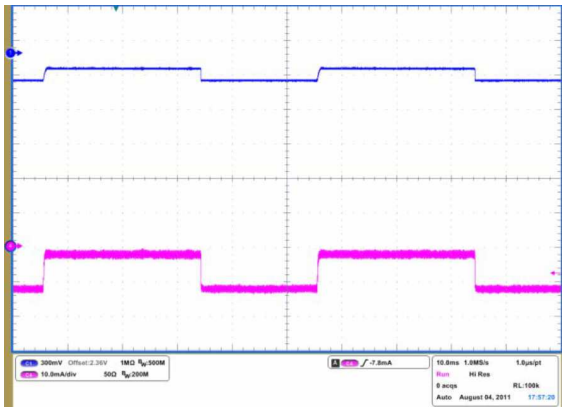
7.10.4 Typical Characteristics (Zero IDDQ)

T_J = 25°C (unless otherwise noted)



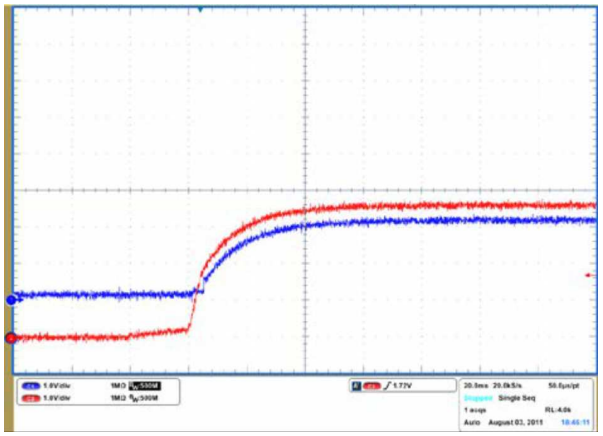
Code 4 1.4-V drop V_I = 3.6 V

Figure 33. Zero IDDQ Output Voltage vs Load



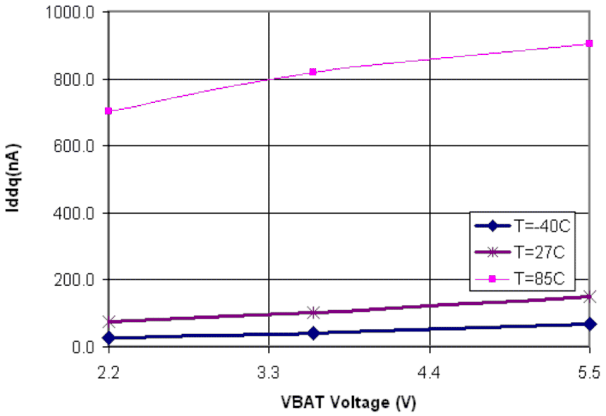
Code 4 1.4-V drop Ch1: VIN
Ch3: VMICRO (LDO_{MINI} output) (100 mV/div)
Ch4: Load current (10 mA/div)

Figure 34. Zero IDDQ Load-Transient Response (0 to 10 mA)



Code 4 1.4-V drop Ch2: VIN rising
Ch 3: VMICRO (ZERO IDDQ output)

Figure 35. ZERO IDDQ Start-Up Waveform With VIN Rising

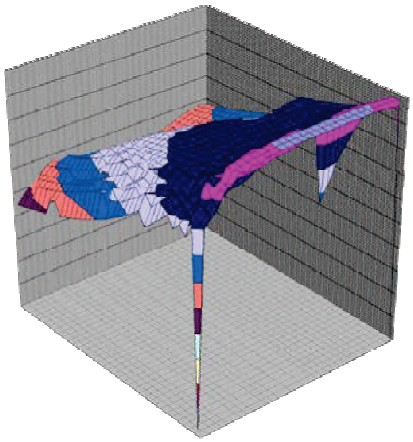


BB_EN = 0 CE = 0
ZERO IDDQ mode code 4

Figure 36. IC Leakage

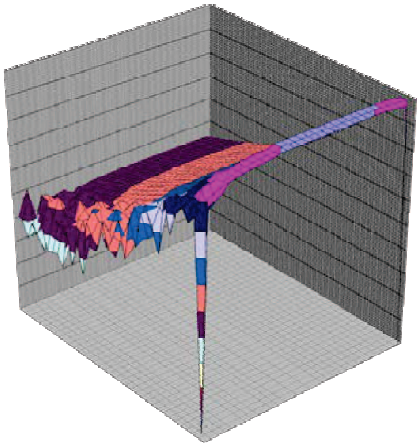
7.10.5 Typical Characteristics ($BUCK_{MINI}$)

T_J = 25°C (unless otherwise noted)



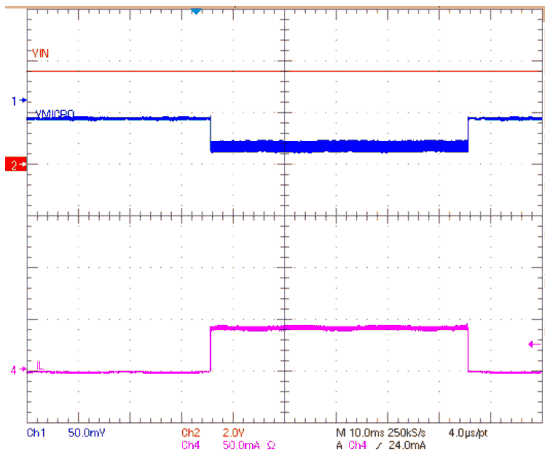
C_O = 1 µF ESR = 1Ω L = 33 µH
Automatic Mode

Figure 37. $BUCK_{MINI}$ Efficiency



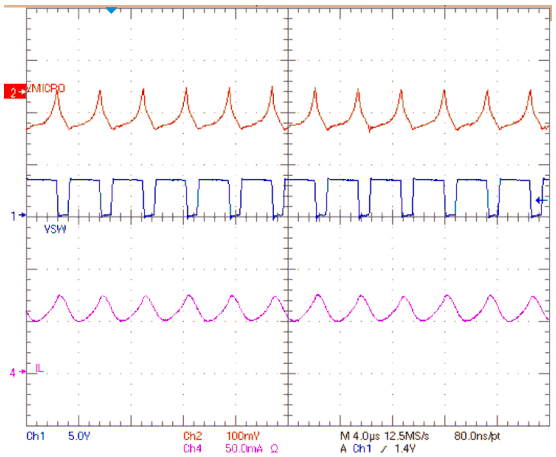
C_O = 100 µF L = 33 µH Automatic mode

Figure 38. $BUCK_{MINI}$ Efficiency



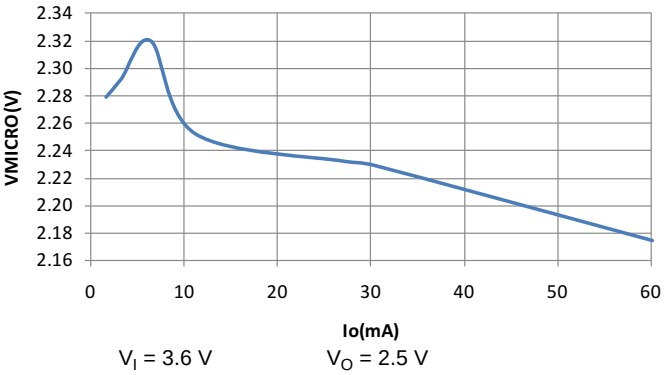
V_I = 3.6 V V_O = 2.5 V 0 to 50-mA step

Figure 39. $BUCK_{MINI}$ Transient Response



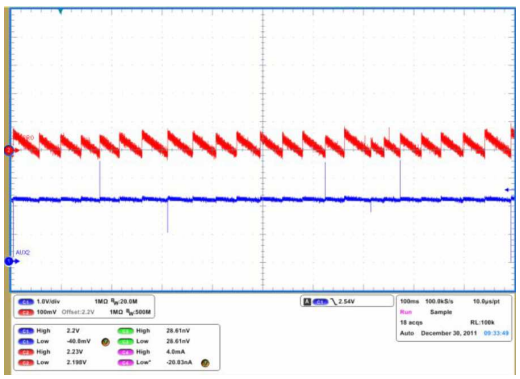
V_I = 3.6 V V_O = 2.5 V I_O = 50 mA

Figure 40. $BUCK_{MINI}$ Output Ripple



V_I = 3.6 V V_O = 2.5 V

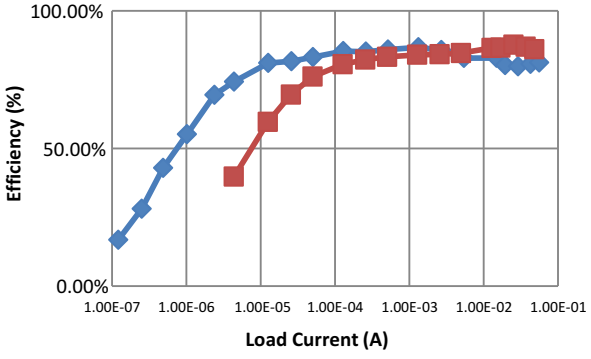
Figure 41. Load Regulation $BUCK_{MINI}$ Output Ripple



V_I = 3.6 V V_O = 2.5 V I_O = 50 mA

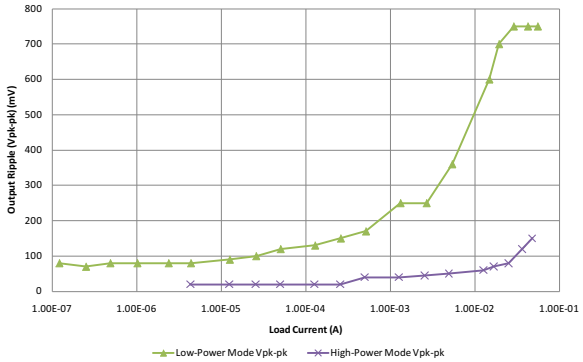
Figure 42. $BUCK_{MINI}$ Output Ripple

Typical Characteristics ($BUCK_{MINI}$) (continued)



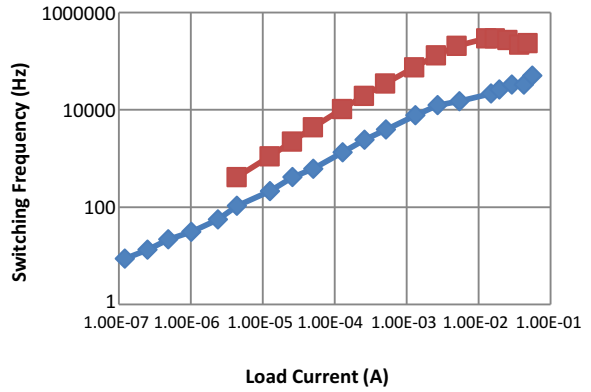
V_O = 2.5 V V_I = 3.6 V

Figure 43. $BUCK_{MINI}$ Efficiency



V_O = 2.5 V V_I = 3.6 V
Low- and high-power modes

Figure 44. $BUCK_{MINI}$ Output Ripple



V_O = 2.5 V V_I = 3.6 V
Low- and high-power modes

Figure 45. $BUCK_{MINI}$ Switching Frequency

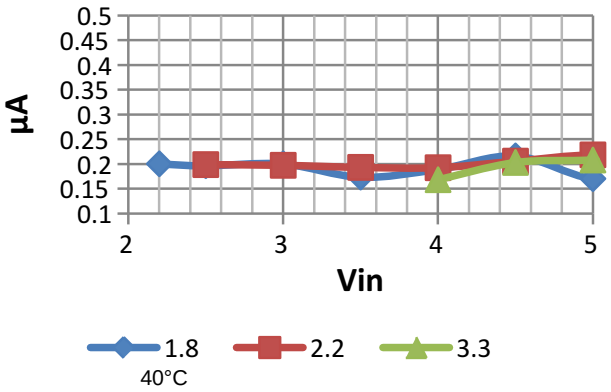


Figure 46. $Buck_{MINI}$ IDDQ

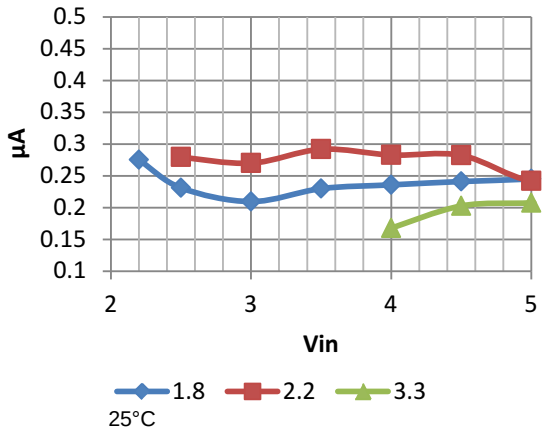


Figure 47. $Buck_{MINI}$ IDDQ

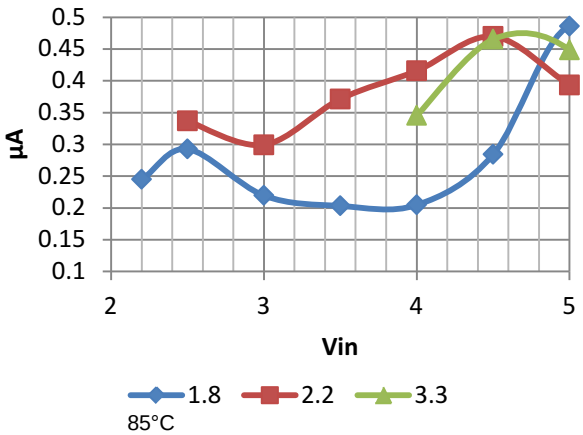
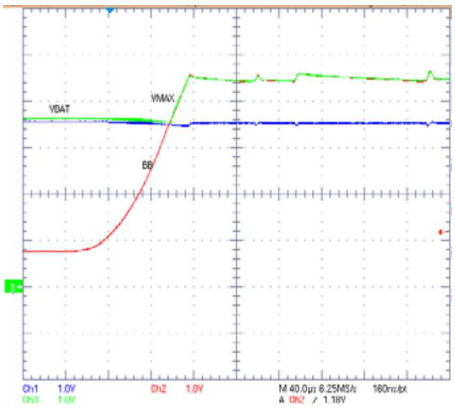


Figure 48. $Buck_{MINI}$ IDDQ

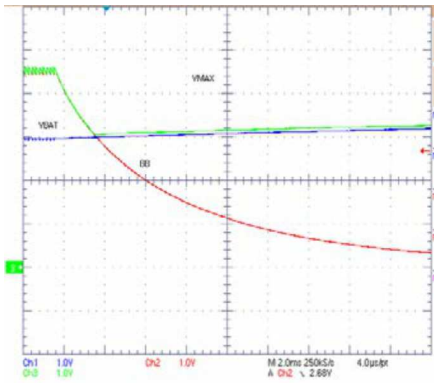
7.10.6 Typical Characteristics (VMAX)

T_J = 25°C (unless otherwise noted)



Rising BB output

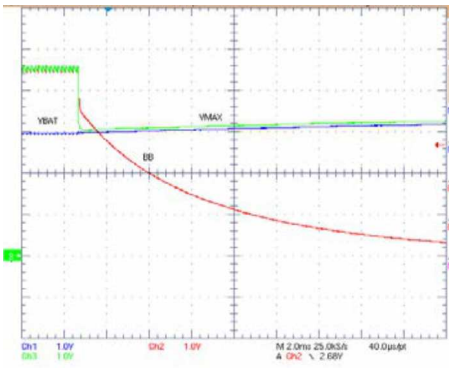
Figure 49. Typical VMAX Waveforms



Falling BB output

Switch configured for VMAX = MAX(VIN,VBBout) when BB output is disabled

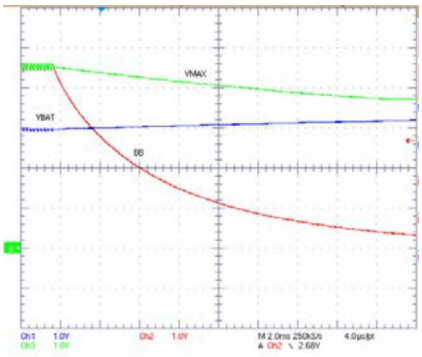
Figure 50. VMAX Waveform



Falling BB output

Switch configured for VMAX = VIN when BB output is disabled

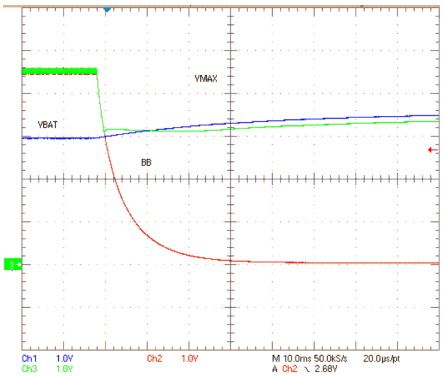
Figure 51. VMAX Waveform



Falling BB output VMAX is not loaded.

Switch configured for VMAX = MAX(VIN,VBBout) – (diode voltage drop) when BB output is disabled

Figure 52. VMAX Waveform



Falling BB output Switch is configured for VMAX = MAX(VIN,BBout).

The VMAX comparator turns off automatically when BBout falls below VIN at BB turnoff.

Figure 53. VMAX Waveform

8 Detailed Description

8.1 Overview

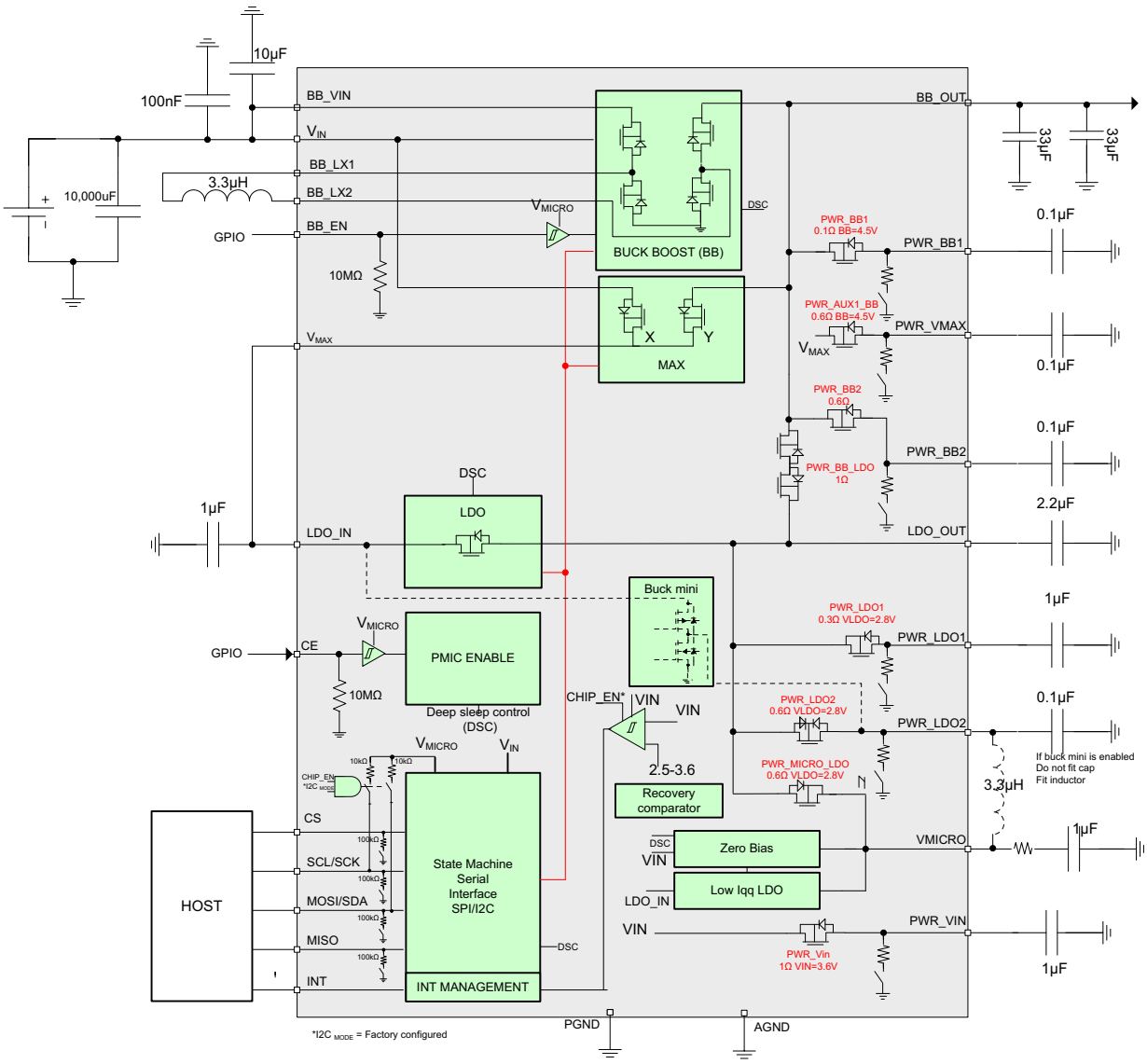
The TPS65290 provides a buck converter, buck-boost, eight power distribution switches, a low quiescent current low drop out regulator and buck converter. The system can be powered by a regulated supply or Li-ion battery between 2.2 V to 5 V. The device is characterized across –40°C to 85°C, making it suitable for portable and non-portable industrial applications.

The buck-boost converter can switch between pulse frequency mode for lighter loads and pulse width modulation mode for heavier loads to maximize efficiency or be forced into pulse width modulation for all load sizes. The power switches can be used to sustain various load configurations. The input-voltage monitor can connect and disconnect power blocks within the TPS65290 without the master processor being involved.

There are two communication protocols for the TPS65290, SPI and I^2C. SPI is the default communication for this device, but can be configured to use I^2C as well.

The buck converter and low-dropout regulator have three default settings to choose from, these resources are intended to provide a low-power, always-on bias supply for the microcontroller in sleep mode.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Serial Interface

Table 1 lists pins that are allocated to the serial interface.

Table 1. Serial Interface

PIN		SPI INTERFACE	I²C INTERFACE	COMMENT
NO.	NAME			
1	SCL/SCK	Clock	Clock	Can be pulled down to ground with 100 kΩ Setting Bit 1, Register 5
2	MOSI/SDA	Master-to-slave data	Data	Can be pulled down to ground with 100 kΩ Setting Bit 1, Register 5
22	INT	Interruption pin	Interruption pin	Push-pull interruption output, powered from VMICRO
23	MISO	Slave-to-master data	Not used. Connect to ground	1 mA output drive. Can be pulled down to ground with 100 kΩ Setting Bit 1, Register 5
24	CS	Slave select (active-high)	Not used. Connect to ground	Can be pulled down to ground with 100 kΩ Setting Bit 1, Register 5

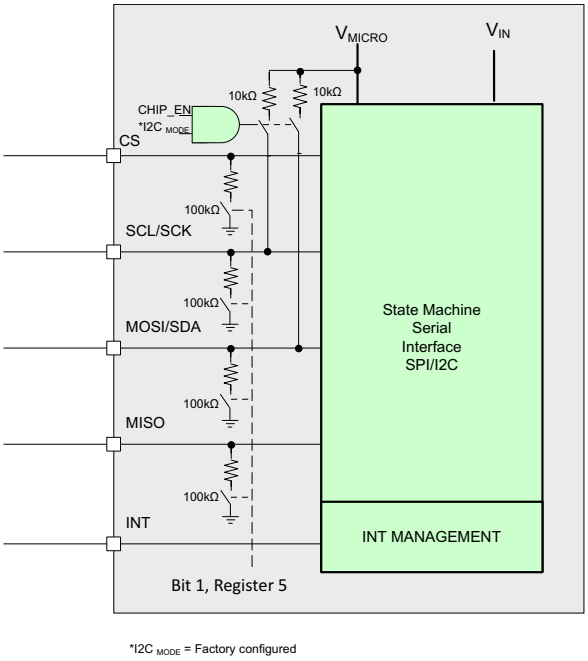


Figure 54. State Machine Serial Interface

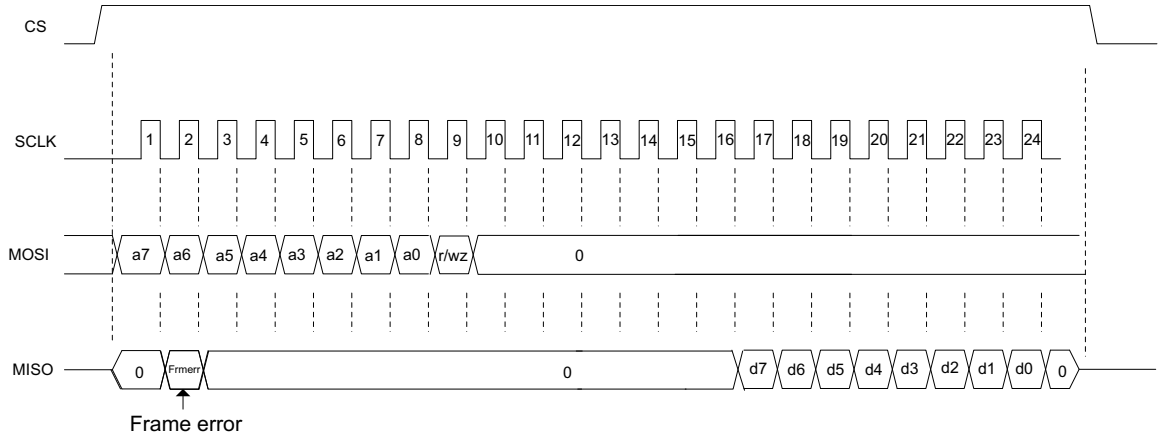
NOTE

The CS level must be low when powering the device up. When using SPI, power the interface with VMICRO to avoid level-shifting issues.

8.3.1.1 SPI Interface

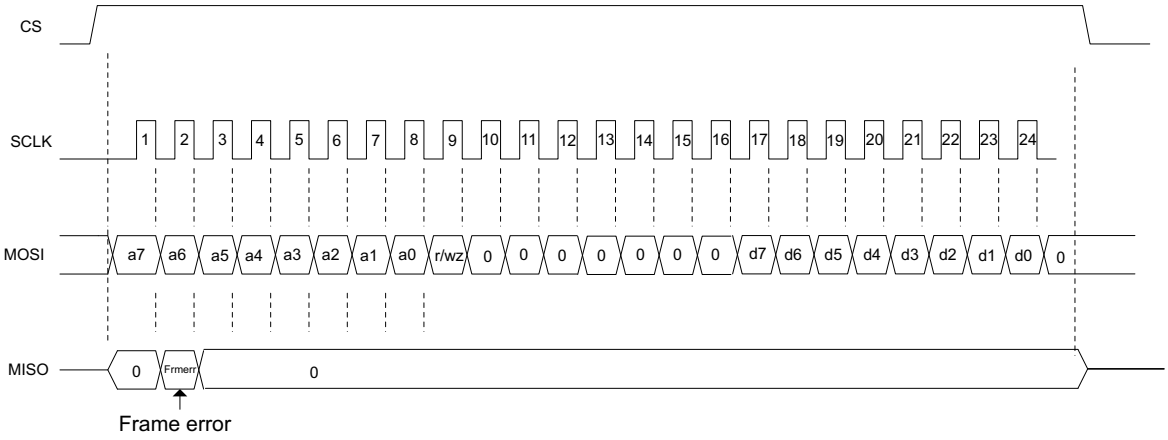
The SPI frequency range is from 32 kHz to 10 MHz with a minimum voltage of 2.2 V. Operation at 1.8 V requires a maximum clock frequency of 5 MHz.

The following figures show SPI write and read transaction timing diagrams. SPI assumes that a SPI master drives CS and MOSI at the falling edge of the SCK clock and a SPI slave drives MOSI at the falling edge of SCK. SPI requires a CS idle time of at least four SPI clock cycles between transactions. CS idle time means the time CS is low. CS is the chip select, which is active-high. The SPI master drives CS and MISO at the falling edge of SCK, and the SPI slave samples MISO data at the rising edge of SCK during the address phase and data phase of a write transaction. The SPI host samples MOSI data at the rising edge of SCK. If a transaction does not contain exactly 24 clock cycles a frame error has occurred. This is indicated by Frmerr, which will be 1. The write data is ignored if a frame error occurs.



SPI read transaction timing diagram
r/wz= 1 to read data
MOSI when reading 0x02 register
0000 // 0010 // 1 000 // 0000 // 0000 // 0000

Figure 55. SPI Read Transaction



SPI write transaction timing diagram
r/wz=0 to write data
MOSI when writing 0xA5 date to 0x02 register to iridium
0000 // 0010 // 0 000 // 0000 // 1010 // 0101

Figure 56. SPI Write Transaction

8.3.1.2 I^2C Interface

The serial interface is compatible with the standard and fast mode I^2C specifications, allowing transfers at up to 400 kHz. The device has a 7-bit address: 0x56h. Attempting to read data from register addresses not listed in this section results in 00h being read out. Requirements for normal data transfer allow SDA to change only when SCK is low. Changes when SCK is high are exclusively for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. The data transfer begins with a start condition and terminates with a stop condition. When addressed, the device generates an acknowledge bit after the reception of the byte. The master device (microprocessor) must generate an extra clock pulse in association with the acknowledge bit. The device must pull down the SDA line during the acknowledge clock pulse so that the SDA line is a stable low during the high period of the acknowledge clock pulse. The SDA line is a stable low during the high period of the acknowledge-related clock pulse. Take setup and hold times into count. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte clocked out of the slave. In this case, the slave device must leave the data line high to enable the master to generate the stop condition.

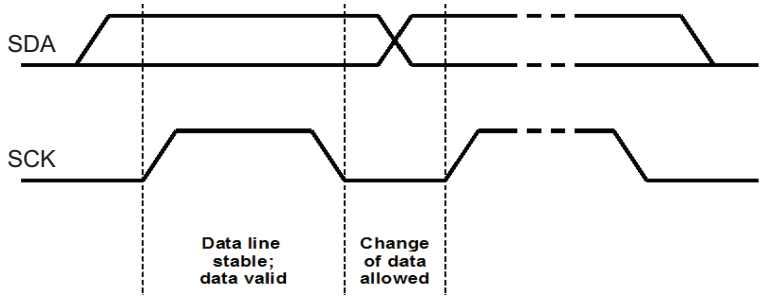


Figure 57. Bit Transfer on the Serial Interface

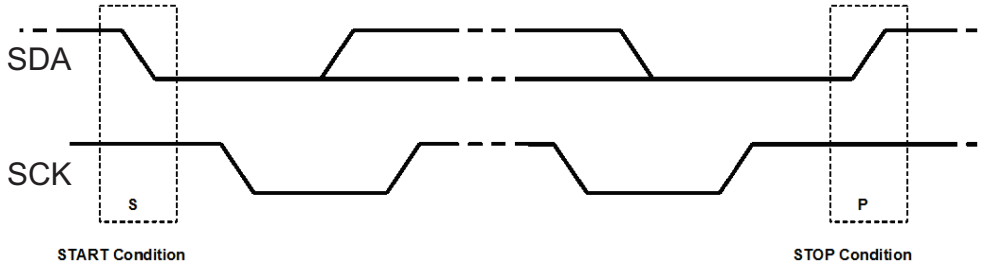


Figure 58. START and STOP Conditions

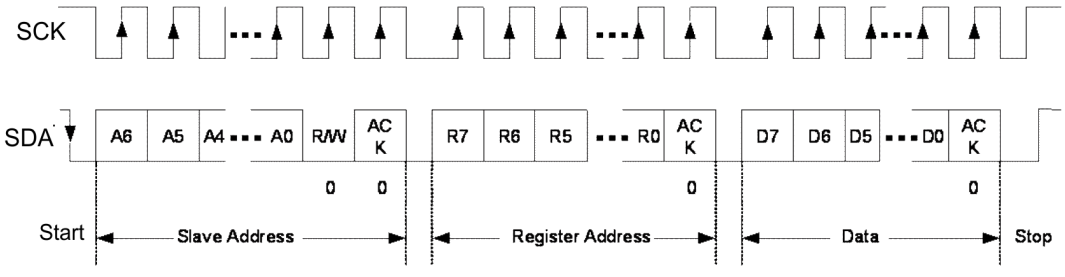


Figure 59. Serial Interface WRITE to Device

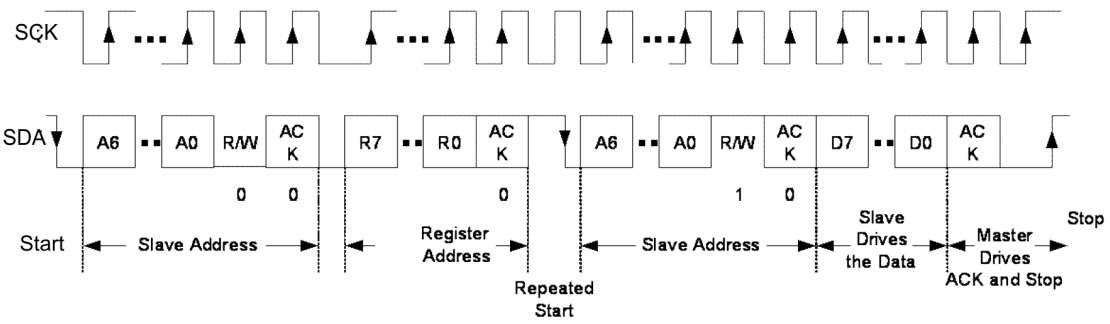


Figure 60. Serial Interface READ Protocol A

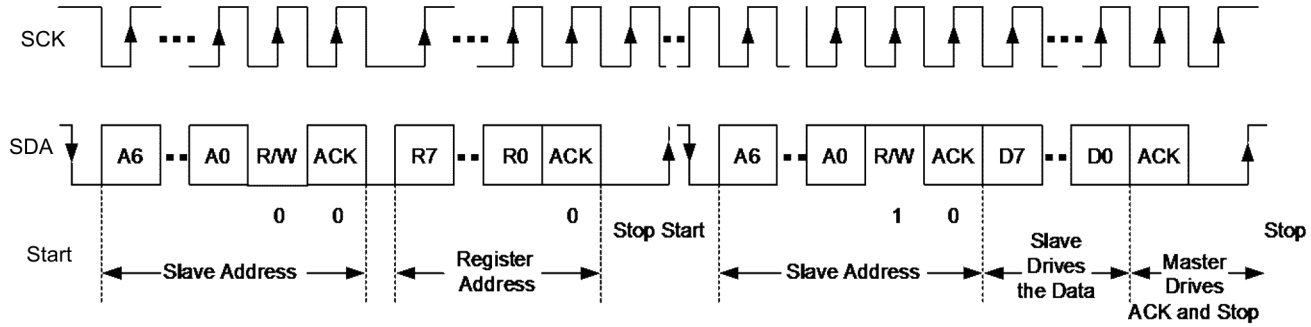


Figure 61. Serial Interface READ Protocol B

8.3.2 Thermal Shutdown

TPS65290 has two overtemperature sensors. The buck-boost temperature sensor is close to the buck-boost power FETs and monitors the power and heat going into the buck-boost block. The central temperature sensor monitors the rest of the chip, and its shutdown threshold is set at a higher temperature. At the digital core level, outputs of both temperature sensors are ORed together. Figure 62 show the logic for buck-boost enable (BB_EN) and power switches. The following example shows the diagram for the BB_PWR_PA switch. The same diagram applies to the 1Wire, SEI, AUX1, AUX2, RF, and LDOBB switches.

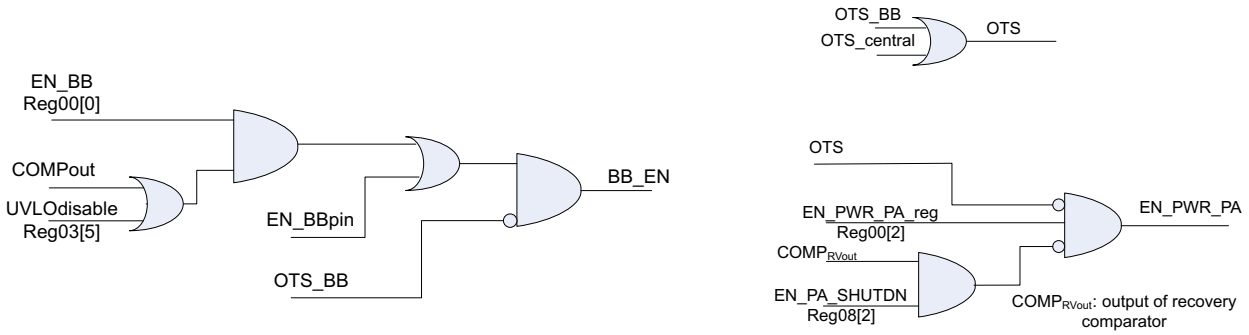


Figure 62. Thermal Shutdown Diagrams

8.3.3 Recovery Comparator (EEPROM Setting)

Design of the recovery comparator is for tracking the operation of a high-output-impedance battery. On application of a load, the battery voltage collapses and the input voltage monitor detects the falling edge and issues an interruption when the programmable falling edge threshold an interruption is generated and the PMIC switches are automatically disabled as per the choice set in register 8. Once the switches are disabled, the loading on the battery collapses and its voltage rises. The recovery comparator monitors this rising edge (as per the programmed setting) and automatically restarts the switches disabled when the battery voltage collapsed.

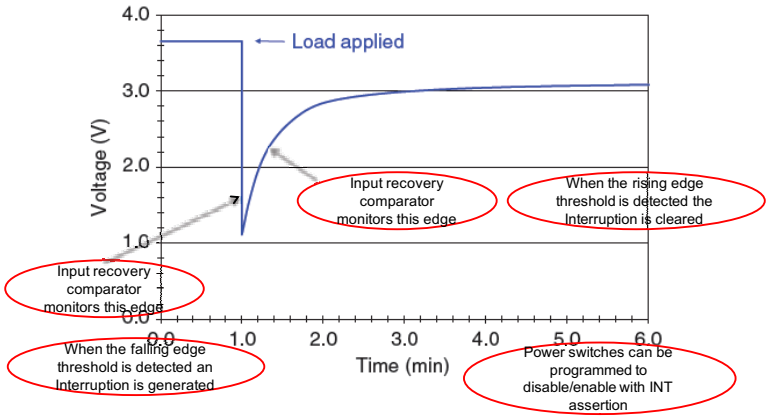


Figure 63. Recovery Comparator (EEPROM Setting)

8.4 Device Functional Modes

8.4.1 State Machine

Figure 64 shows the operational states of the TPS65290, and how to move between each state.

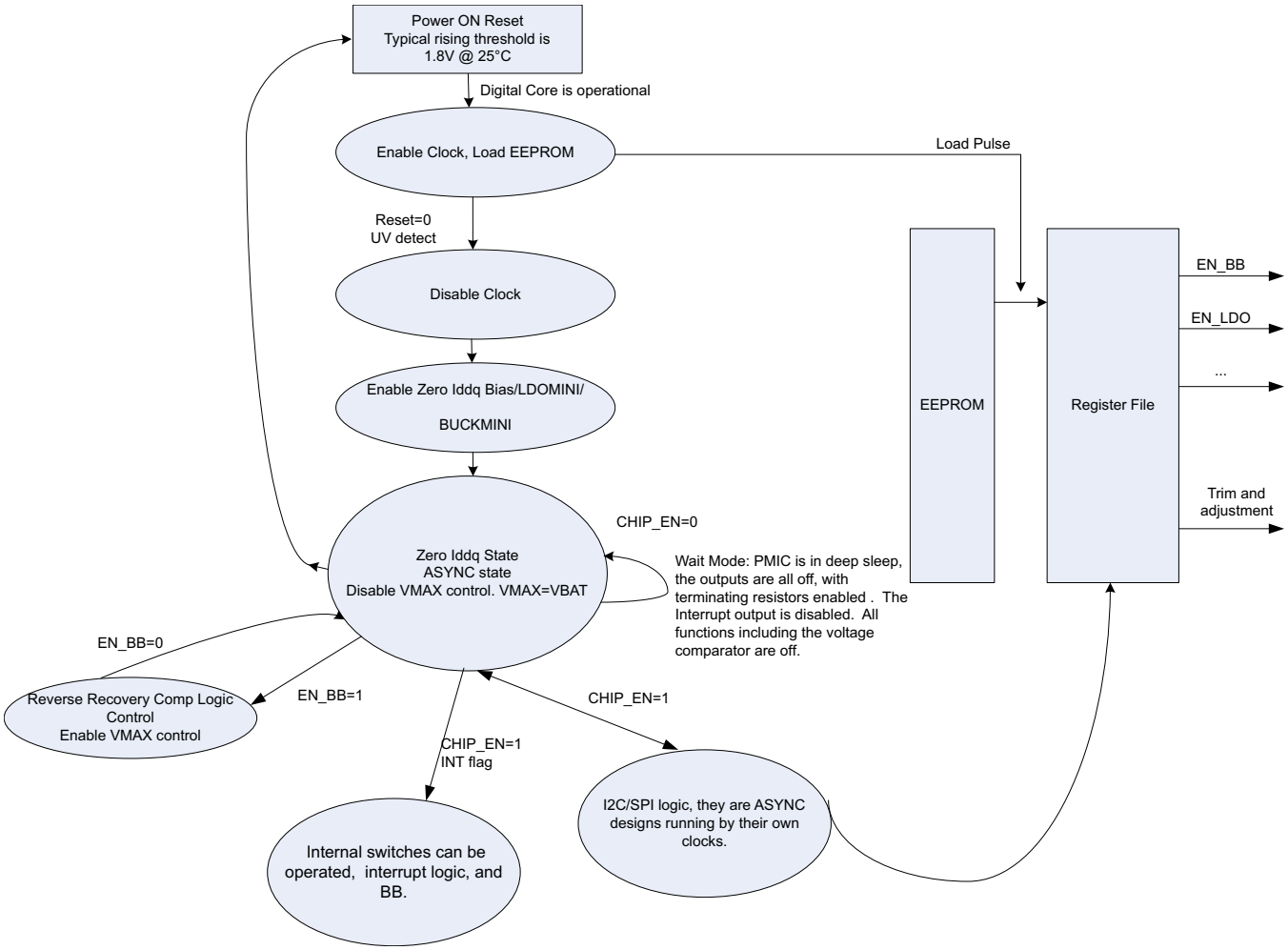


Figure 64. State Machine Schematic

Device Functional Modes (continued)

8.4.2 Power Up and Enabling the IC

There are two ways of enabling the PMIC, by setting the CE or BB_EN pins. If CE IS disabled, only the always-on blocks (as per default) and pulldown resistors are enabled by default.

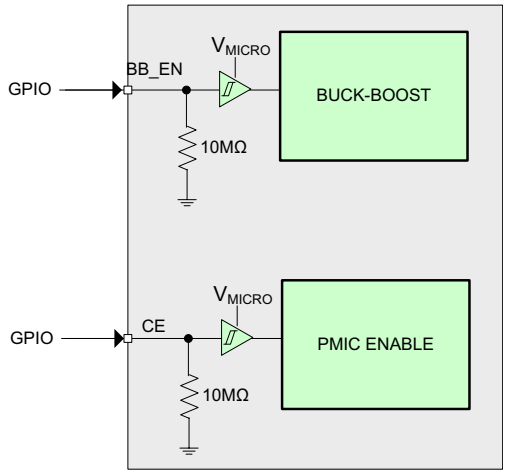


Figure 65. Power Up and Enabling the IC

When CE and BB_EN is low, the PMIC is in deep sleep, and BIAS supply to the micro is enabled. When CE is set high, the I^2C or SPI is active; the internal switches can be operated, along with the interrupt logic, boost, and buck. The buck-boost is enabled either by BB_EN (high) or EN_BB bit (1). BB_EN can be used to enable the buck-boost converter without need of the serial interface.

With the serial interface active, it is possible to enable, disable, and change settings for the power blocks. All changes on registers are kept as long as the input supply is higher than 1.8 V. If power is cycled. the registers are re-loaded with the programmed factory defaults.

8.4.3 Bandgap Enable (Non-EEPROM Setting)

The LDO bandgap is normally disabled to reduce consumption, and it is enabled when any of the of LDO, LDO_{MINI}, or $BUCK_{MINI}$ blocks is enabled. However, to speed up the power-up time of the LDO, the bandgap can be enabled in advance (register 4, bit 5).

8.4.4 $BUCK_{MINI}$ Operation (Non-EEPROM Setting)

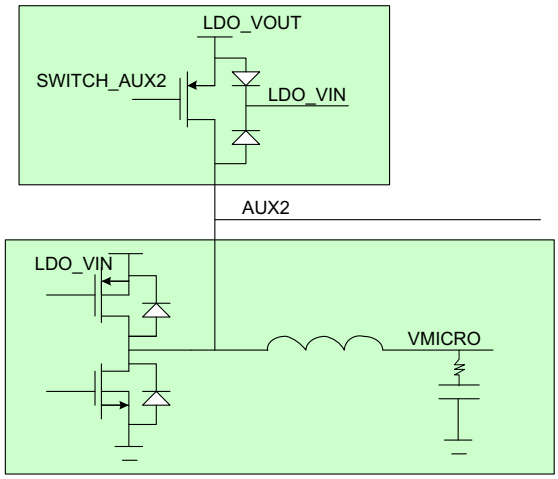


Figure 66. $Buck_{MINI}$ Functional Block Diagram

Device Functional Modes (continued)

$BUCK_{MINI}$ is a hysteretic buck converter that can deliver up to 30 mA and therefore can be used beyond the sleep-mode operation of the microprocessor. When using this block, is important to keep the following in mind:

- The AUX2 output is not available, as this pin connects to the external inductor required by the converter.
- If VMICRO has a ceramic capacitor, it is recommend to add a small resistor (0.5 Ω to 1 Ω) to obtain a fixed ripple value at the output.
- $BUCK_{MINI}$ does not feature a current-limit circuit. Provide overcurrent protection (if needed) externally.
- When used to support loads between 100 µA to 1 mA, there is trade-off between input quiescent current and output ripple. It is suggested to use the settings for low- and high-power mode (register 2, bits [5,4]) to determine which power mode is most suitable for the application. Plots on the characteristics section show the typical trade-off between efficiency and ripple.
- $BUCK_{MINI}$ starts at automatic power selection mode. If loading higher than 100 µA to 1 mA is required, set the $BUCK_{MINI}$ setting to (register 2, bits [5,4]) to reduce ripple.
- Once the loading is removed, set (register 2, bits [5,4]) to reduce power consumption.

8.4.5 Setting V_{MAX} (Non EEPROM Setting)

The operation of V_{MAX} is not set on EEPROM and the switches inside the block can be programmed for specific conditions such as

- Diode drops
- To connect to VIN
- To follow the maximum voltage with its logic enabled
- To follow the maximum voltage and to connect to VIN when VBB is lower than VIN and to disconnect the V_{MAX} logic. Table 2 shows the options available.

Table 2. Setting V_{MAX} (Non EEPROM Setting)

REG6_BIT6	REG6_BIT7	REG3_BIT7	OPERATION	FIGURE
VMAXx_DIS	VMAXx_EN	VMAX_LATCH		
0	0	0	V_{MAX} switch comparator is enabled when BB is enabled. When BB is disabled, the switch that connects V_{MAX} to V_{BAT} turns on.	Figure 67
1	0	0	V_{MAX} switch comparator is enabled when BB is enabled. When BB is disabled, the V_{MAX} switches both turn off.	Figure 68
0	0	1	V_{MAX}switch comparator is enabled when BB is enabled. When BB is disabled, the comparator remains on until BB_OUT goes below V_{MAX}. V_{MAX}follows BB output until BB output voltage goes below V_{BAT} voltage. At that point, V_{MAX} switch comparator is disabled, and V_{MAX} is connected to V_{BAT} with 0 Iddq static logic.	Figure 69
1	0	1	V_{MAX} switch comparator is enabled when BB is enabled. When BB is disabled and BB_OUT drops below V_{BAT}, both switches in V_{MAX} block are disabled and V_{MAX} becomes the diode drope from the diode below V_{BAT} when BB is turned off.	Figure 70
X	1	X	When VMAX_EN = 1 regardless of the status of other bits, V_{MAX} logic is always ON and monitors VIN vs BB_OUT voltage and connects to the maximum voltage. The comparator consumes about 25 µA. VMAX_EN can be set to 1 before the transmission phase and then set to zero at the end of the transmission phase when chip goes into sleep mode.	Figure 71

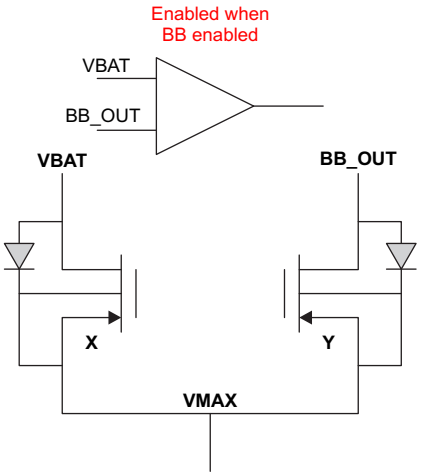


Figure 67. VMAXx_DIS: 0, VMAXx_EN: 0, VMAX_LATCH: 0

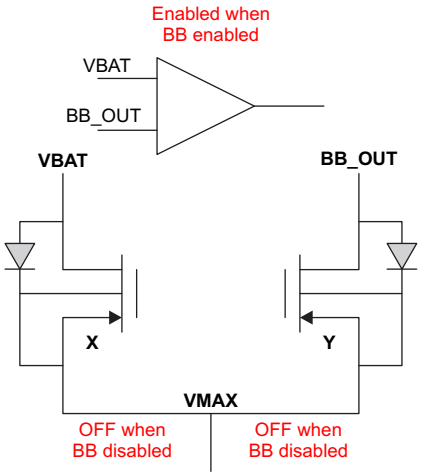


Figure 68. VMAXx_DIS: 1, VMAXx_EN: 0, VMAX_LATCH: 0

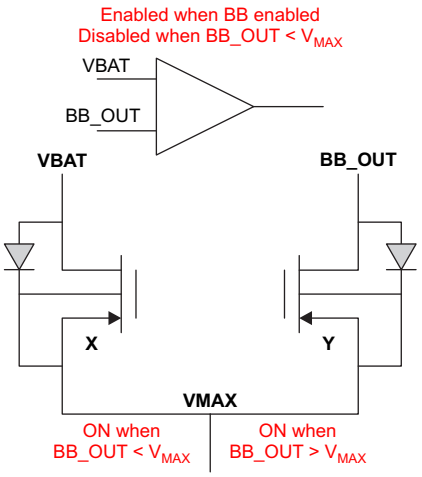


Figure 69. VMAXx_DIS: 0, VMAXx_EN: 0, VMAX_LATCH: 1

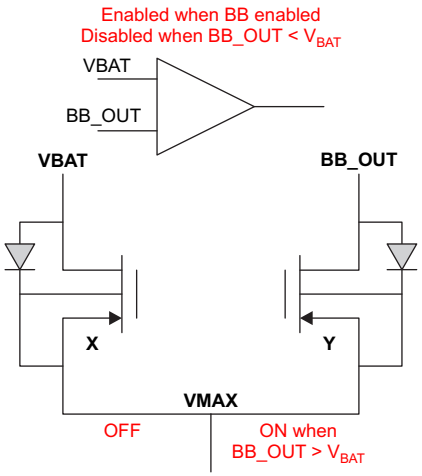


Figure 70. VMAXx_DIS: 1, VMAXx_EN: 0, VMAX_LATCH: 1

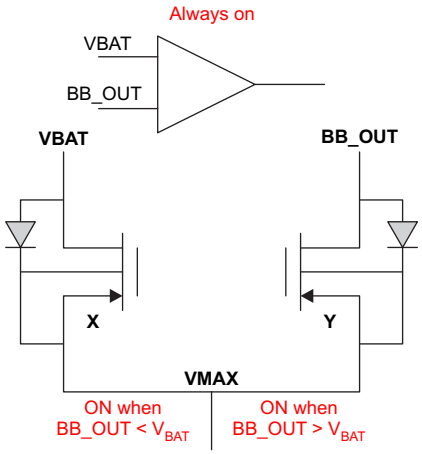


Figure 71. VMAXx_DIS: X, VMAXx_EN: 1, VMAX_LATCH: X

8.5 Register Maps

NOTE

To access registers: write 1 to bit 7, register 1

To lock registers: write 0 to bit 7, register 1

8.5.1 Register 0, Block Enable, Address 00h

This register enables the buck-boost converter, the main LDO, and most of the power switches. All options can be preset with EEPROM bits. The enable logic for all switches and power blocks is:

0: Disabled

1: Enabled

Note that either a register setting or a high on the BB_EN pin (15) can enable the buck-boost block.

Table 3. Register 0, Block Enable, Address 00h Field Descriptions

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
EN_PWR_VIN_VIN	7	PWR_ON	R/W	Y	0	Enables switch from VIN to 1WIRE power
EN_PWR_MICRO_LDO	6	PWR_ON	R/W	Y	0	Enables switch from LDO output to VMICRO
EN_PWR_LDO2_LDO	5	PWR_ON	R/W	Y	0	Enables switch from LDO to AUX2
EN_PWR_LDO1_LDO	4	PWR_ON	R/W	Y	0	Enables switch from LDO output to RF
EN_PWR_VMAX_VMAX	3	PWR_ON	R/W	Y	0	Enables switch from VMAX output to AUX1
EN_PWR_BB2_BB	2	PWR_ON	R/W	Y	0	Enables switch from BB output to power amplifier
EN_LDO	1	PWR_ON	R/W	Y	0	Enables LDO
EN_BB	0	PWR_ON	R/W	Y	0	Enables buck-boost converter

8.5.2 Register 1, Rev ID and write protect, Address 01h

Bit 7 must be set to 1 before any other register can be read or written. If set to 0, all registers are locked. Bits 0 to 3 are for TI internal usage to track IC revisions.

Table 4. Register 1, Rev ID and write protect, Address 01h Field Descriptions

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
WRITE_EN	7	GLOBAL	R/W	N	N/A	If 1, allows access to TI internal registers
Revision[3]	3	GLOBAL	R	N	0	Revision ID
Revision[2]	2	GLOBAL	R	N	1	Revision ID
Revision[1]	1	GLOBAL	R	N	1	Revision ID
Revision[0]	0	GLOBAL	R	N	0	Revision ID
Reserved	4, 5, 6	—	—	—	NA	Reserved

8.5.3 Register 2, VMICRO_VOUT, Address 02h

Depending on the factory setting, this register sets the voltage drop from battery to V_{MICRO} for the zero-leak bias or the V_{MICRO} set voltage (LDO_{MINI}, $BUCK_{MINI}$ options).

Table 5. Register 2, VMICRO_VOUT, Address 02h Field Descriptions

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION		
BMINI[1]	7	$BUCK_{MINI}$	R/W	N	0	BMINI[1]	BMINI[0]	Low-power mode
						1	0	
BMINI[0]	6	$BUCK_{MINI}$	R/W	N	0	1	1	High-power mode
RESERVED	5	RESERVED	R/W	N	0			
RESERVED	4	RESERVED	R/W	N	0			
VMICRO[3]	3	VMICRO	R/W	Y	0	Zero-leak bias, LDO_{MINI} (only one is set to work as per factory setting)		
VMICRO[2]	2	VMICRO	R/W	Y	1			
VMICRO[1]	1	VMICRO	R/W	Y	0			
VMICRO[0]	0	VMICRO	R/W	Y	0			

Table 6. Register 2, VMICRO_VOUT, Address 02h

SETTING	VMICRO[3]	VMICRO[2]	VMICRO[1]	VMICRO[0]	LDO_{MINI} (V)	$BUCK_{MINI}$ (V)	ZERO LEAK BIAS (V)
0	0	0	0	0	1.806	1.806	V_I – 0.6
1	0	0	0	1	1.903	1.903	V_I – 0.8
2	0	0	1	0	1.998	1.998	V_I – 1
3	0	0	1	1	2.101	2.101	V_I – 1.2
4	0	1	0	0	2.194	2.194	V_I – 1.4
5	0	1	0	1	2.295	2.295	V_I – 1.6
6	0	1	1	0	2.407	2.407	V_I – 1.8
7	0	1	1	1	2.496	2.496	V_I – 2
8	1	0	0	0	2.592	2.592	V_I
9	1	0	0	1	2.696	2.696	V_I
10	1	0	1	0	2.806	2.806	V_I
11	1	0	1	1	2.885	2.885	V_I
12	1	1	0	0	2.969	2.969	V_I
13	1	1	0	1	3.058	3.058	V_I
14	1	1	1	0	3.152	3.152	N/A
15	1	1	1	1	3.254	3.254	Disconnect

8.5.4 Register 3, BUCK-BOOST_VOUT, Address 03h

The buck-boost voltage is set with this register (bits 0 to 4) which can be set by EEPROM.

UVLO operation on the buck-boost can be enabled or disabled by setting bit 5.

Forced PWM operation can be set with bit 6.

Table 7. Register 3, BUCK-BOOST_VOUT, Address 03h Field Descriptions

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
VMAX_LATCH	7	VMAX	R/W	Y	0	0: VMAX switches off instantaneously when disabled. 1: VMAX Switches off when VBB goes below VIN
BB_FORCE_PWM	6	BUCK_BOOST	R/W	Y	0	0:, automatic PWM/PFM. 1: is forced PWM.
UVLO disable	5	BUCK_BOOST	R/W	Y	1	If 1, UVLO comparator does NOT shut down BB. INT is still generated.
VBB_VOUT[4]	4	BUCK_BOOST	R/W	Y	1	
VBB_VOUT[3]	3	BUCK_BOOST	R/W	Y	0	
VBB_VOUT[2]	2	BUCK_BOOST	R/W	Y	0	
VBB_VOUT[1]	1	BUCK_BOOST	R/W	Y	1	
VBB_VOUT[0]	0	BUCK_BOOST	R/W	Y	1	

Table 8. Register 3, BUCK-BOOST_VOUT, Address 03h

SETTING	VBUCK_BOOST[4]	VBUCK_BOOST[3]	VBUCK_BOOST[2]	VBUCK_BOOST[1]	VBUCK_BOOST[0]	VBB
0	0	0	0	0	0	0.995
1	0	0	0	0	1	1.194
2	0	0	0	1	0	1.394
3	0	0	0	1	1	1.594
4	0	0	1	0	0	1.784
5	0	0	1	0	1	1.985
6	0	0	1	1	0	2.189
7	0	0	1	1	1	2.381
8	0	1	0	0	0	2.587
9	0	1	0	0	1	2.779
10	0	1	0	1	0	2.972
11	0	1	0	1	1	3.161
12	0	1	1	0	0	3.374
13	0	1	1	0	1	3.452
14	0	1	1	1	0	3.576
15	0	1	1	1	1	3.664
16	1	0	0	0	0	3.756
17	1	0	0	0	1	3.853
18	1	0	0	1	0	3.954
19	1	0	0	1	1	4.062
20	1	0	1	0	0	4.176
21	1	0	1	0	1	4.235
22	1	0	1	1	0	4.359
23	1	0	1	1	1	4.424
24	1	1	0	0	0	4.559
25	1	1	0	0	1	4.779
26	1	1	0	1	0	4.857
27	1	1	0	1	1	4.938
28	1	1	1	0	0	5.022
29						Reserved
30						Reserved
31						Reserved

8.5.5 Register 4, LDO_VOUT, Bandgap, Address 04h

The LDO voltage is set with this register (bits 0 to 4) which can be set by EEPROM.

To speed up system start-up the internal bandgap can be enabled before the LDO and switches are enabled.

Table 9. Register 4, LDO_VOUT, Bandgap, Address 04h Field Descriptions

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
Reserved	7					
Reserved	6					
BGLP_EN	5	Bandgap	R/W	N		When 1, enables internal bandgap.
LDO_VOUT[4]	4	LDO	R/W	Y	1	See Table 10
LDO_VOUT[3]	3	LDO	R/W	Y	0	See Table 10
LDO_VOUT[2]	2	LDO	R/W	Y	0	See Table 10
LDO_VOUT[1]	1	LDO	R/W	Y	1	See Table 10
LDO_VOUT[0]	0	LDO	R/W	Y	0	See Table 10

Table 10. Register 4, LDO_VOUT, Bandgap, Address 04h

SETTING	VLDO[4]	VLDO[3]	VLDO[2]	VLDO[1]	VLDO[0]	VLDO
0	0	0	0	0	0	1.001
1	0	0	0	0	1	1.103
2	0	0	0	1	0	1.202
3	0	0	0	1	1	1.303
4	0	0	1	0	0	1.399
5	0	0	1	0	1	1.506
6	0	0	1	1	0	1.606
7	0	0	1	1	1	1.712
8	0	1	0	0	0	1.81
9	0	1	0	0	1	1.921
10	0	1	0	1	0	2.019
11	0	1	0	1	1	2.127
12	0	1	1	0	0	2.23
13	0	1	1	0	1	2.33
14	0	1	1	1	0	2.438
15	0	1	1	1	1	2.534
16	1	0	0	0	0	2.637
17	1	0	0	0	1	2.725
18	1	0	0	1	0	2.845
19	1	0	0	1	1	2.948
20	1	0	1	0	0	3.031
21	1	0	1	0	1	3.148
22	1	0	1	1	0	3.243
23	1	0	1	1	1	3.343
24	1	1	0	0	0	3.449
25	1	1	0	0	1	3.563
26	1	1	0	1	0	3.643
27	1	1	0	1	1	3.769
28	1	1	1	0	0	3.858
29	1	1	1	0	1	3.952
30	1	1	1	1	0	4.05
31	1	1	1	1	1	0.803 (1)

(1) Do not use

8.5.6 Register 5, Pulldown Resistors, Address 05h

The power switches can be pulled down when disabled using bits 1 to 7.

The enable logic for all pulldowns is:

0: Disable

1: Enable

Bit 0 is used to increase the turnon speed of the switches.

Table 11. Register 5, Pulldown Resistors, Address 05h Field Descriptions

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
EN_PWR_VIN_VIN	7	PWR_ON	R/W	Y	1	Enable pulldown resistor from VIN to PWR_VIN
EN_PWR_BB1_BB	6	PWR_ON	R/W	Y	1	Enable pulldown resistor from Buck-Boost (BB). BB output to switch
EN_PWR_LDO2_LDO	5	PWR_ON	R/W	Y	0	Enable pulldown resistor from LDO to switch
EN_PWR_LDO1_LDO	4	PWR_ON	R/W	Y	0	Enable pulldown resistor from LDO output to switch
EN_PWR_VMAX_VMAX	3	PWR_ON	R/W	Y	0	Enable pulldown resistor from BB output to switch
EN_PWR_BB2_BB	2	PWR_ON	R/W	Y	0	Enable pulldown resistor from BB output to switch
SPI	1	PWR_ON	R/W	Y	1	Enable pulldown resistor for serial interface pins
FAST	0	PWR_ON	R/W	Y	0	If 1, makes switch turn on 10× faster.

8.5.7 Register 6, VMAX Control and Recovery Comparator, Address 06h

Bits 5 to 3 set the threshold for falling voltage on the recovery comparator.

Bits 2 to 0 set the threshold for rising voltage on the recovery comparator.

Bits 7 and 6 set VMAX operation (see V_{MAX} options section).

Table 12. Register 6, VMAX Control and Recovery Comparator, Address 06h Field Descriptions

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
VMAX_DIS	7	VMAX	R/W	N	0	See *Setting V_{MAX} (Non EEPROM Setting)*
VMAX_EN	6	VMAX	R/W	N	0	
VRECOVERY[2]_FALLING	5	VINPUT	R/W	Y	0	INT pin is asserted when VIN reaches the falling threshold voltage, and is cleared when VIN recovers to the rising threshold voltage. See following table
VRECOVERY[1]_FALLIING	4	VINPUT	R/W	Y	1	
VRECOVERY[0]_FALLIING	3	VINPUT	R/W	Y	1	
VRECOVERY[2]_RISING	2	VINPUT	R/W	Y	0	See Table 13
VRECOVERY[1]_RISING	1	VINPUT	R/W	Y	0	
VRECOVERY[0]_RISING	0	VINPUT	R/W	Y	0	

Table 13. Register 6, VMAX Control and Recovery Comparator Falling, Address 06h

SETTING	VRECOVERY_FALLING[2]	VRECOVERY_FALLING[1]	VRECOVERY_FALLING[0]	VRECOVERY COMPARATOR
0	0	0	0	1.7
1	0	0	1	1.8
2	0	1	0	1.9
3	0	1	1	2
4	1	0	0	2.1
5	1	0	1	2.2
6	0	1	1	2.3
7	1	1	1	2.4

Table 14. Register 6, VMAX Control and Recovery Comparator Rising, Address 06h

SETTING	VRECOVERY_RISING[2]	VRECOVERY_RISING[1]	VRECOVERY_RISING[0]	VRECOVERY COMPARATOR
0	0	0	0	2.4
1	0	0	1	2.5
2	0	1	0	2.6
3	0	1	1	2.7
4	1	0	0	2.8
5	1	0	1	2.9
6	0	1	1	3
7	1	1	1	3.1

8.5.8 Register 7, PWR_BB_LDO Switch Control and Interruption Management, Address 07h

The alarm status of the device can be verified with this register.

Bits 7 and 3 report on the UVLO comparator status. Bit 5 masks this alarm.

Bits 6 and 2 report on the overtemperature status. Bit 4 masks this alarm.

Bits 1 and 0 are used to control the switches associated with the internal connection between the LDO and the buck-boost converter.

The enable logic for the switches is:

0: Disabled

1: Enabled

Table 15. Register 7, PWR_BB_LDO Switch Control and Interruption Management, Address 07h Field Descriptions

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
UVLO_INT	7	INT	R	N	0	Set to 1 when recovery comparator is asserted (falling edge), cleared to 0 when register is read by serial interface.
OTS_INT	6	INT	R	N	0	Set to 1 when over temperature is asserted, cleared to 0 when the serial interface reads the register.
UVLO_MASK	5	INT	R/W	N	0	Masks the recovery comparator assertion (falling edge). Reported to the INT pin
OTS_MASK	4	INT	R/W	N	1	Masks the over temperature assertion. Reported to the INT pin
UVLO_STATUS	3	INT	R	N	0	Status report of recovery comparator fault
OTS_STATUS	2	INT	R	N	0	Status report of an overt temperature fault
EN_PWR_SEL_BB	1	PWR_ON	R/W	Y	0	Enable switch to SEL from Buck-Boost (BB) BB output OR LDO
EN_PWR_BB_LDO	0	PWR_ON	R/W	Y	0	Enables the back to back switch from Ldo output to BB output

8.5.9 Register 8, Interruption Block Disable, Address 08h

Bits 7 to 1 can be used to disable the power switches automatically when an interruption is asserted.

Bit 0 disables the recovery comparator to reduce power consumption.

Table 16. Register 8, Interruption Block Disable, Address 08h Field Descriptions

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
EN_VIN_SHUTDN	7	Pulldown	R/W	Y	1	If 1, switch turns off at interruption.
EN_BB2_SHUTDN	6	Pulldown	R/W	Y	0	If 1, switch turns off at interruption.
EN_LDO2_SHUTDN	5	Pulldown	R/W	Y	1	If 1, switch turns off at interruption.
EN_LDO1_SHUTDN	4	Pulldown	R/W	Y	1	If 1, switch turns off at interruption.
EN_AUX1_SHUTDN	3	Pulldown	R/W	Y	1	If 1, switch turns off at interruption.
EN_BB1_SHUTDN	2	Pulldown	R/W	Y	0	If 1, switch turns off at interruption.
EN_LDOBBbb_SHUTDN	1	Pulldown	R/W	Y	1	If 1, PWR_BB_LDO switch turns off at interruption
COMPrv_ENmask	0	Pulldown	R/W	Y	1	If 1, COMPrv is disabled

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65290 is intended for portable and non-portable industrial applications such as energy-harvesting and water meter applications.

9.2 Typical Application

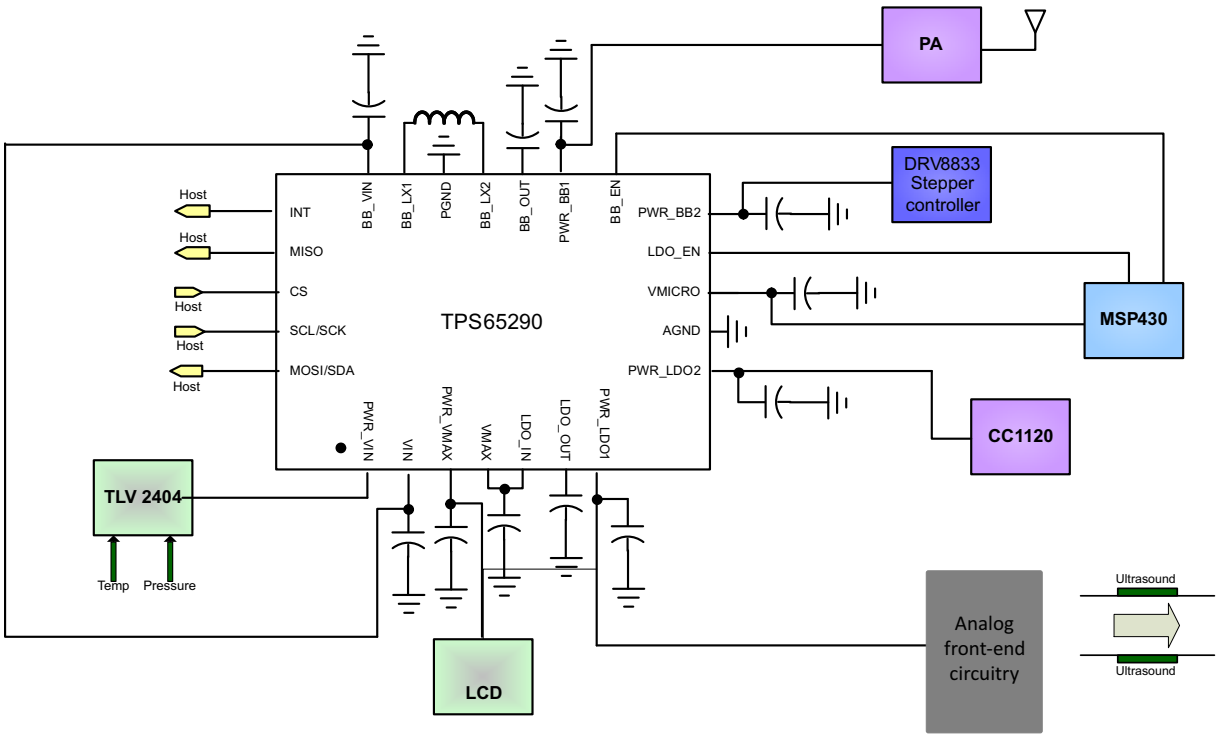


Figure 72. Typical Flow Meter Application

Typical Application (continued)

9.2.1 Design Requirements

For this design example, follow the design requirements in Table 17 and Table 18.

Table 17. TPS65290 Design Requirements

BLOCK	FUNCTIONALITY			POWER SAVING OPTIONS		
		Reg	Bit		Reg	Bit
Buck-boost	Enable	[0]	[0]	PFM or PWM mode	[3]	[6]
	Set voltage	[3]	[0,5]			
	UVLO disable	[3]	[5]			
LDO	Enable	[0]	[1]			
	Set voltage	[4]	[0,4]			
Zero drop, LDO_{MINI}, $BUCK_{MINI}$	Set voltage	[2]	[0,3]			
$BUCK_{MINI}$ low and high current mode	Operation mode	[2]	[5,4]	Low-current mode (for standby operation)	[2]	[5,4]
MAX	Latch-on turnoff	[3]	[7]	See V_{MAX} options section		
	Turnon options	[6]	[6,7]			
Recovery comparator	Set falling voltage	[6]	[5,3]	Enable or disable	[8]	[0]
	Set rising voltage	[6]	[0,2]			
Power switches	Enable (BB, LDO, BAT, V_{MAX})	[0]	[2,7]	Enable or disable pulldown	[5]	[1,7]
		[7]	[1]	Fast or slow turnon	[5]	[0]
	Enable (PWR_BB_LDO)	[7]	[0]			
Interruption management (INT)	INT status and masking	[7]	[2,7]	Power switches automatic disable when INT asserted	[8]	[1,7]
Bandgap				Enable or disable	[4]	[5]

Table 18. Outputs and Operational Range

TYPE	V_O (V)	DEFAULT	I_O MAX (mA)	SET ACCURACY	FEATURES
Buck-boost	1 V–5 V, approximately 200-mV steps	4.06 V	500	3%	
LDO	0.8 V for external divider 1 V–4 V, approximately 100-mV steps	2.8 V	150	4%	
Low bias supply	0.6-V–2-V selective drop from battery voltage, 8 adjustment steps	V_I – 1.4	10	10% at 25°C	No IDQQ
	1.8 V–3.3 V, 200-mV steps	2.2 V	10	5%	Low Iqq LDO
	1.8 V–3.3 V, 200-mV steps	2.2 V	30	5%	Low Iqq buck
Power switches powered from BB output	PWR_BB1	Disabled	800	100-mΩ switch	1-kΩ pulldown, single P MOSFET
	PWR_BB2		350	600-mΩ switch	
Power switches powered from VMAX	PWR_VMAX	Disabled	250	600-mΩ switch	1-kΩ pulldown single P MOSFET
Power switches powered from LDO output	PWR_LDO2	Disabled	250	600-mΩ switch	1-kΩ pulldown single P MOSFET
	PWR_MICRO_LDO		N/A		
	PWR_LDO1	Disabled	250	300 mΩ	1-kΩ pulldown single P MOSFET
Power switch connecting output of BB to LDO	PWR_BB_LDO	Disabled	250	1 Ω	1-kΩ pulldown back-to-back P MOSFETS
Power switch powered from battery	PWR_VIN	Disabled	100	1 Ω	1-kΩ pulldown single P mosfet
Recovery comparator	1.7–2.4V 100-mV steps falling edge	2 V	NA	3%	
	2.4–3.1V 100mV steps rising edge	2.4 V			
MAX (analog multiplexer)	Highest of BB and LDO	NA	150	NA	Configurable for turnon and turnoff operation
INT (maskable)		All switches disabled by interruption			

9.2.2 Detailed Design Procedure

9.2.2.1 Factory Programmed Settings

The following blocks are programmed in the factory.

Buck-boost

- Can be enabled or disabled when IC is enabled (can also be enabled with pin 15 high)
- Voltage can be set to:
  - 1 V to 3.4 V, 200-mV steps
  - 3.5 V to 4.7 V, 100-mV steps
  - 4.9 V, 5 V
- Forced PWM or PFM (low-power mode)
- Input UVLO comparator enabled or disabled. If disabled, BB will turn on with any input voltage higher than 1.8 V LDO
  - Can be disabled or enabled when IC is enabled
- Output voltage can be set from 1 V to 4 V in 100-mV steps

Recovery comparator

- Can be enabled or disabled when IC is enabled
- Falling edge can be set from 1.7 V to 2.4 V in 100-mV steps. An interruption is generated.
- Rising edge can be set from 2.4 V to 3.1 V in 100-mV steps. The interruption is released.

Power switches

- Can be enabled or disabled when IC is enabled
- Pulldown resistance can be connected or disconnected when IC is enabled
- Power switches can be disabled when an interruption is generated
- Switches can be turned on at slow or fast speed

9.2.2.2 Functional Block Setup and Serial Interface Selection

Once a voltage higher than 2.2 V is applied to VIN, the always-on supply starts according to the factory default setting. This is the only block available within the device and always stays on as long as the input supply does not drop below 2.2 V.

There are three possible choices of always-on supply. The main parameter to consider is the efficiency of the supply during sleep mode.

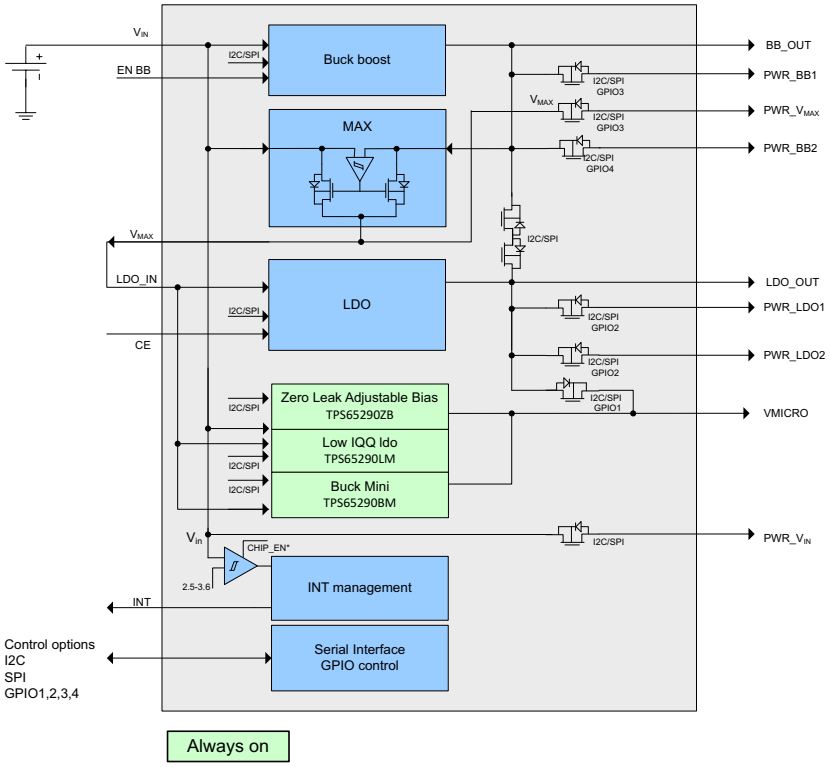


Figure 73. Always-On Supply Selection Diagram

Zero Bias set to V_I – 1.4

- Takes the least amount of quiescent current
- Provides voltage drops from 0.6 V to 2 V in 200-mV steps
- Is not a regulated output
- Programmable to zero drop or to open circuit
- 10 mA maximum

LDO_{MINI} set to 2.2 V

- Provides a regulated output
- Programmable from 1.8 V to 3.3 V in 100-mV steps
- 10 mA maximum

$BUCK_{MINI}$ set to 2.2 V

- Provides a regulated output
- Can be programmed from 1.8 V to 3.3V in 100-mV steps
- 30 mA maximum
- Output has a ripple content
- Requires additional inductor (0603) and resistor. (0402) PWR_AUX2 switch is disabled (pin becomes switching node).

The default serial interface for the device is SPI, The I^2C lines are open-drain lines with internal 20-kΩ pullup resistors that are capable of 400-kHz operation, but also create power losses when any of the bus lines are low. The expectation is that operation with SPI produces less average current consumption when compared to I^2C. For I^2C or GPIO operation, please check with the factory.

9.2.2.3 Inductor Selection

To estimate the inductance of the buck-boost converter, use equations Equation 1 and Equation 2:

$$L_1 = (V_{IN\_MAX} - V_{OUT}) \times 0.5\ (\mu s/A) \quad (1)$$

$$L_2 = V_{OUT} \times 0.5\ (\mu s/A) \quad (2)$$

L_1 is used for the stepdown mode of operation. VIN is the maximum input voltage. L_2 is used for boost mode operation is calculated. The recommended minimum inductor value is either L_1 or L_2, whichever is higher. As an example, a suitable inductor for generating 3.3 V from a Li-ion battery with a battery voltage range from 2.5 V up to 4.2 V is 2.2 µH. The recommended inductor range is between 1.5 µH and 4.7 µH. In general, this means that at high voltage conversion rates, higher inductor values offer better performance.

The table below shows the recommended inductance for input and output voltage combinations. The highest inductance among the region of interest is recommended.

Table 19. Recommended Inductance (µH) for Input- and Output-Voltage Combinations

	V_I	1.8	1.9	2	2.2	2.5	3	3.6	4	4.5	5
V_O											
1		0.4	0.45	0.5	0.6	0.75	1	1.3	1.5	1.75	2
2		1	1	1	0.1	0.25	0.5	0.8	1	1.25	1.5
2.4		1.2	1.2	1.2	1.2	0.05	0.3	0.6	0.8	1.05	1.3
3		1.5	1.5	1.5	1.5	1.5	1.5	0.3	0.5	0.75	1
3.4		1.7	1.7	1.7	1.7	1.7	1.7	0.1	0.3	0.55	0.8
4		2	2	2	2	2	2	2	2	0.25	0.5
4.5		2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	0.25
5		2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 3 shows how to calculate the peak current I_1 in step down mode operation and Equation 4 show how to calculate the peak current I_2 in boost mode operation.

$$I_1 = \frac{I_{OUT}}{0.8} + \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{2 \times V_{OUT} \times f \times L} \quad (3)$$

$$I_2 = \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN\_MIN}} + \frac{V_{IN\_MIN} \times (V_{OUT} - V_{IN\_MIN})}{2 \times V_{OUT} \times f \times L} \quad (4)$$

In both equations f is the switching frequency. The critical current value for selecting the right inductor is the higher value of I_1 and I_2. It also needs to be taken into account that load transient and error conditions may cause higher inductor currents. This also needs to be taken into account when selecting an appropriate inductor.

The table below shows the recommended inductor current rating for input and output voltage combinations with assumption of 1.6-MHz switching frequency, 500-mA loading, 3.3-µH inductance. The highest current rating among the region of interest is recommended.

Table 20. Recommended Inductor Current Rating (A) for Input and Output Voltage Combination With 3.3-µH Inductor, 1.6-MHz Switching Frequency, and 500-mA Load

	V_I	1.8	1.9	2	2.2	2.5	3	3.6	4	4.5	5
V_O											
1		0.79	0.79	0.8	0.8	0.81	0.81	0.82	0.82	0.82	0.82
2		0.85	0.8	0.75	0.77	0.79	0.81	0.83	0.84	0.85	0.86
2.4		1.04	0.98	0.93	0.84	0.76	0.79	0.82	0.84	0.85	0.86
3		1.32	1.25	1.19	1.08	0.94	0.75	0.8	0.82	0.84	0.86
3.4		1.49	1.42	1.35	1.23	1.08	0.88	0.77	0.8	0.83	0.85
4		1.76	1.67	1.59	1.45	1.29	1.07	0.87	0.75	0.79	0.82
4.5		1.97	1.88	1.79	1.64	1.45	1.22	1	0.88	0.75	0.79
5		2.19	2.08	1.99	1.82	1.61	1.36	1.13	1.01	0.87	0.75

9.2.2.4 Buck-Boost Input-Capacitor Selection

A 10-µF ceramic capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the buck-boost input pin and power ground of the IC is recommended.

9.2.2.5 Battery Input Pin Capacitor Selection

To make sure that the internal control circuits are supplied with a stable low-noise supply voltage, a capacitor can be connected between VIN and AGND. Using a ceramic capacitor with a value of 0.1 µF is recommended. The value of this capacitor should not be higher than 0.22 µF.

9.2.2.6 Buck-Boost Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the BB_OUT and PGND. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the BB_OUT and PGND pins of the IC.

There are no additional requirements regarding minimum ESR. There is also no upper limit for the output capacitor value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

9.2.2.7 LDO Output Capacitor

A 2.2-µH capacitor is recommended to be placed as close as possible to the LDO output pin and AGND. In particular, a good ground plane for the TPS65290 and the LDO output capacitor is highly recommended to prevent LDO overshoot during buck-boost converter operation.

9.2.2.8 Operation of the IC During RF Transmission at Full Power

For high-power output transmission, the BB output voltage powers up the power amplifier with a voltage set to 3 V to 5 V at the buck-boost output. Pulse currents of tens to hundreds of mA are common in wireless sensor systems during transmit and receive modes. These high-current pulses place special demands on batteries. Repeated delivery of pulse currents exceeding the recommended load current of a given chemistry diminishes the useful life of the cell. The effects can be severe, depending on the amplitude of the current and the particular cell chemistry and construction. Also, the internal impedance of the cell often results in an internal voltage drop that precludes the cell from delivering the pulse current at the voltage necessary to operate the external circuit.

One method of mitigating these effects is to place a capacitor with low equivalent series resistance (ESR) across the battery. The battery charges the capacitor between discharge pulses, and the capacitor delivers the pulse current to the load. Determination of the necessary capacitance requires the following parameters:

- Battery impedance (at temperature and state-of-charge)
- Battery voltage (as a function of state-of-charge)
- Operating temperatures
- Pulse current amplitude
- Pulse current duration
- Allowable voltage drop during pulse discharge

Use the following equations to calculate the output capacitance needed to deliver the specified pulse current of a known duration and the latency time that required between pulses to allow the battery to recharge the capacitor. Both formulas assume that the capacitor ESR is sufficiently low to result in negligible internal voltage drop while delivering the specified pulse current; consequently, only the battery resistance is considered in the formula used to compute capacitor charging time, and only the load resistance is considered when computing the capacitance needed to deliver the discharge current.

The first step in creating a battery-capacitor couple for pulse-current applications is to size the capacitance using the discharge formula in Equation 5.

$$C = t / R \times [-\ln (V_{MIN} / V_{MAX})]$$

where

- C = output capacitance in parallel with battery
- t = pulse duration
- R = load resistance = V_O(average) / Ipulse

(5)

V_{MIN} and V_{MAX} are determined by the combination of the battery voltage at a given state-of-charge and the operating voltage requirement of the external circuit. Once the capacitance has been determined, the capacitor charging time can be calculated using the charge formula in Equation 6.

$$t = R \times C \times [-\ln (1 - V_{MIN} / V_{MAX})]$$

where

- t = capacitor charging time from V_{MIN} to V_{MAX}
- R = battery resistance
- C = output capacitance in parallel with battery

(6)

Again, V_{MIN} and V_{MAX} are functions of the battery voltage and the circuit operating specifications. Battery resistance varies according to temperature and state-of-charge as described previously. Worst-case conditions are often applied to the calculations to ensure proper system operation over temperature extremes, battery condition, capacitance tolerance, etc.

Due to the high input impedance of the battery used, a high-value input capacitor on the order of thousands of microfarads is therefore placed at the battery input to store charge. During the RF transmission phase that takes on the order of 5 ms to10 m, the storage capacitor provides power for transition. The input voltage, V_I, drops from 3.6 V at the beginning of the operation to about 2 V at the receive time. The main LDO is powered by VMAX, which would be at the buck-boost output during this transition. The blocks that would see low-voltage operation of VIN are buck-boost and digital logic. The buck-boost is designed to work down to 1.8 V of typical falling input voltage. This is for when buck-boost was enabled at a higher input voltage, started up successfully, and then its input voltage falls. If buck-boost starts from a disabled mode, rising VIN voltage is higher.

Digital reset (nPUC) is designed for a rising VIN voltage of 1.76 V and falling voltage of 1.25 V. To prevent digital logic from reset, the recovery voltage comparator levels should be set higher than falling voltage (that is, 1.9 V).

If the recovery voltage is lower, or the feature is disabled, PMIC can be reset. When reset happens, PMIC disables both the main LDO, the BB block (if BB_EN = 0), and all switches. However, VMICRO function will be still provided. After digital reset and when all blocks are disabled, the input voltage will rise again, and PMIC starts again with default register values.

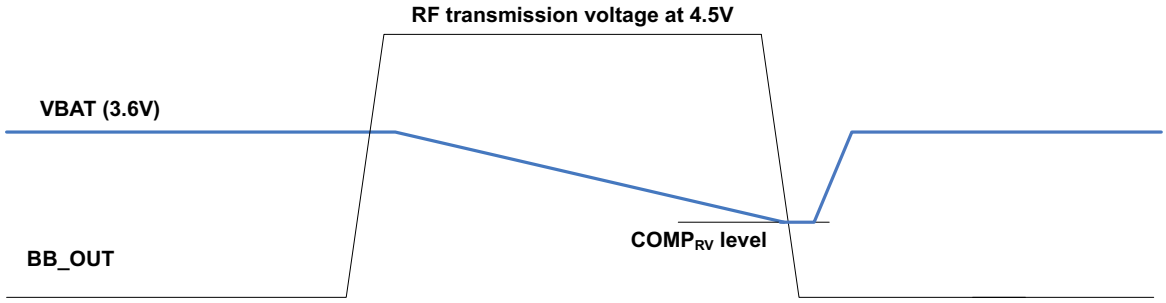
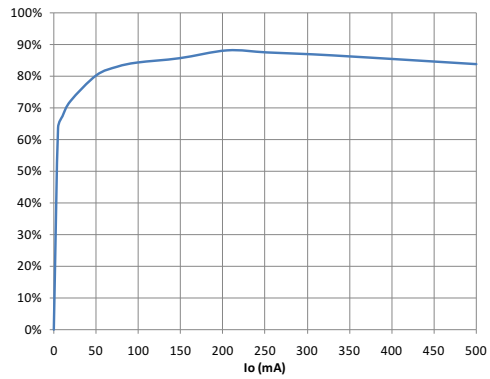


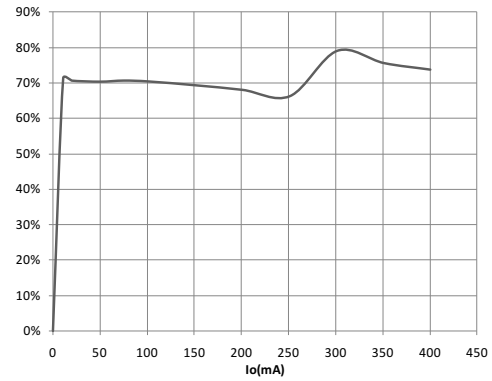
Figure 74. Operation of the IC During RF Transmission at Full Power

9.2.3 Application Curves



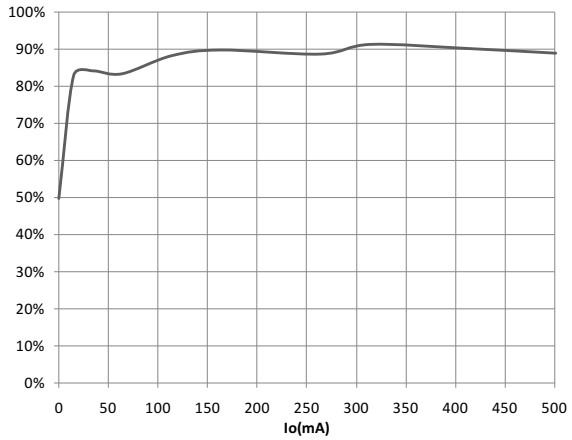
V_I = 3.6 V V_O = 4.5 V

Figure 75. Buck-Boost Efficiency



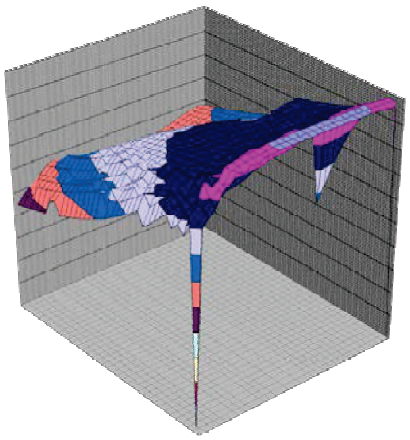
V_I = 2.5 V V_O = 4.5 V

Figure 76. Buck-Boost Efficiency



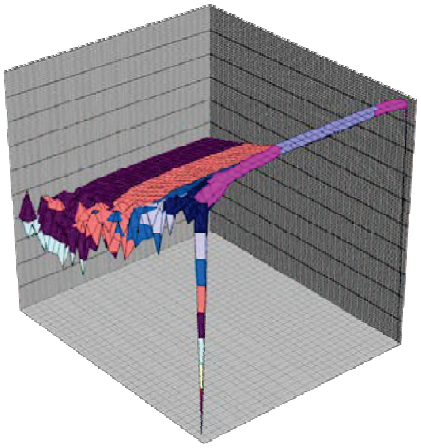
V_I = 3.6 V V_O = 2.8 V

Figure 77. Buck-Boost Efficiency



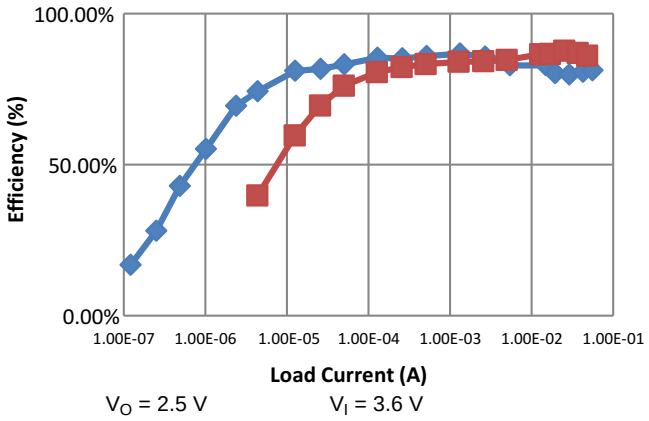
C_O = 1 µF ESR = 1Ω L = 33 µH
Automatic Mode

Figure 78. $BUCK_{MINI}$ Efficiency



C_O = 100 µF L = 33 µH Automatic mode

Figure 79. BUCK$_{MINI}$ Efficiency



V_O = 2.5 V V_I = 3.6 V

Figure 80. BUCK$_{MINI}$ Efficiency

10 Power Supply Recommendations

The device is designed to operate with an input voltage supply range between 2.2 V and 5.0 V. This input supply can be from a single-cell Li-ion, Li-Polymer batteries, or other externally regulated supply. If the input supply is located more than a few inches from the TPS65290, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

This section provides the recommendation of the TPS65290 board layout based on TI evaluation board. Close placement to the chip and to the ground plane is required for power components including C21, C2, C6, C15, C15a, L1, C10 and C4. The priority among the components is C21 → C2 → C8 → C6 → C15 → C15A → L1 → C10 → C4. In particular, a good ground plane for the TPS65290 and the LDO output capacitor (C6) is highly recommended to prevent LDO overshoot during the buck-boost converter operation. A good ground connection for C21 and C2 is also required for the high performance of the buck-boost converter. The pin is regarded as a noise generator because of the buck-boost converter switching operation. Therefore, do not tap the trace to pin2 from the trace from C21. Use star connection for two inputs of pin 19 and pin 4 from the power supply.

11.2 Layout Example

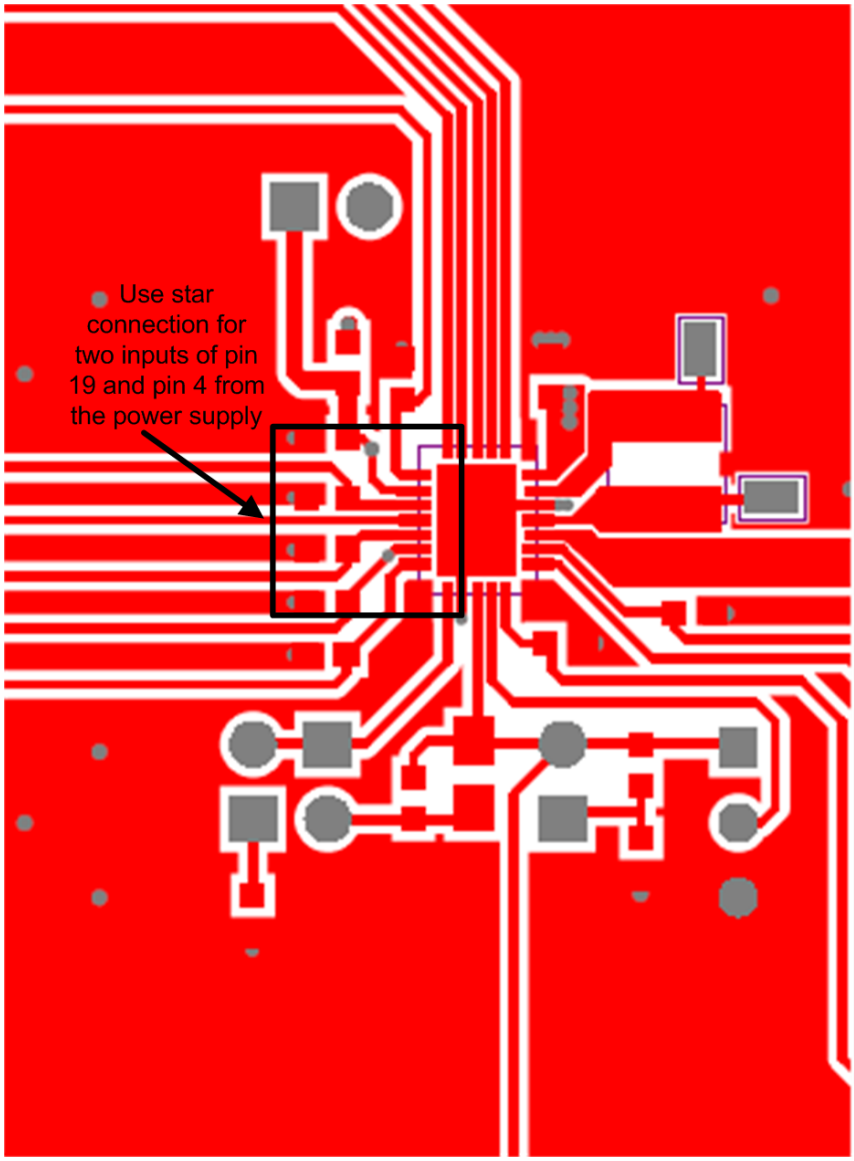


Figure 81. TPS65290 Board Layout

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65290BMRHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290BM	Samples
TPS65290BMRHFT	ACTIVE	VQFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290BM	Samples
TPS65290LMRHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290LM	Samples
TPS65290LMRHFT	ACTIVE	VQFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290LM	Samples
TPS65290ZBRHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290ZB	Samples
TPS65290ZBRHFT	ACTIVE	VQFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290ZB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

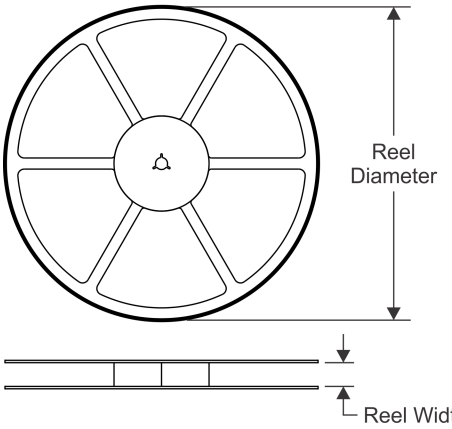
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

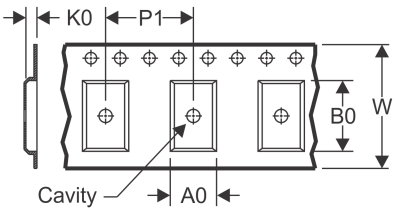
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

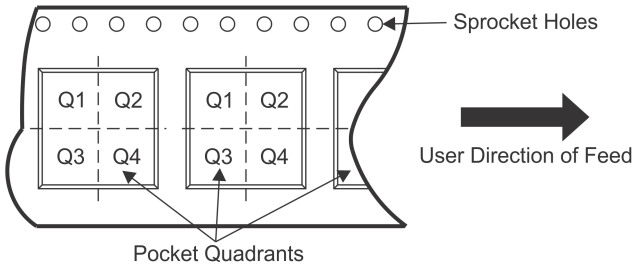


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

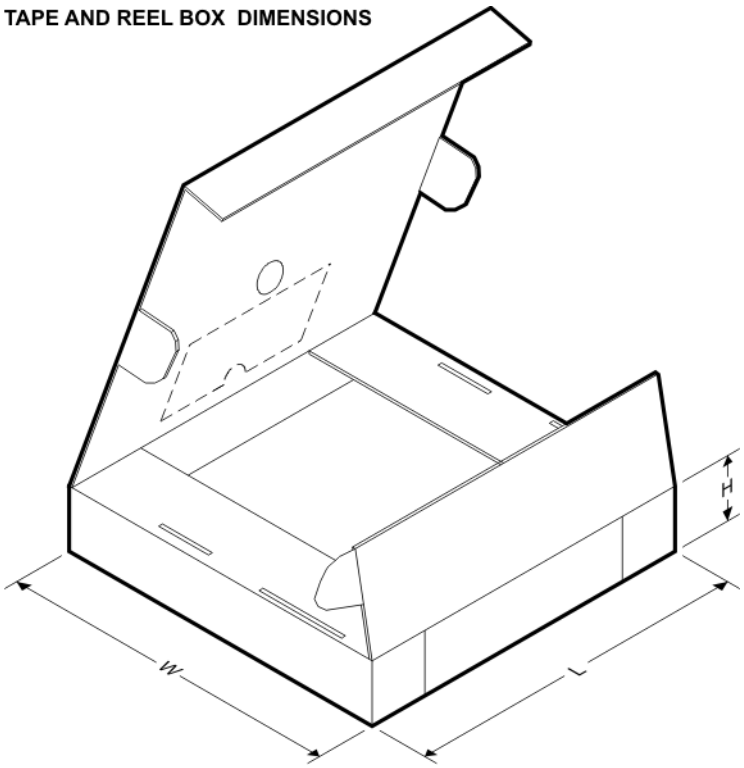
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65290BMRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
TPS65290BMRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
TPS65290LMRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
TPS65290LMRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
TPS65290ZBRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
TPS65290ZBRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

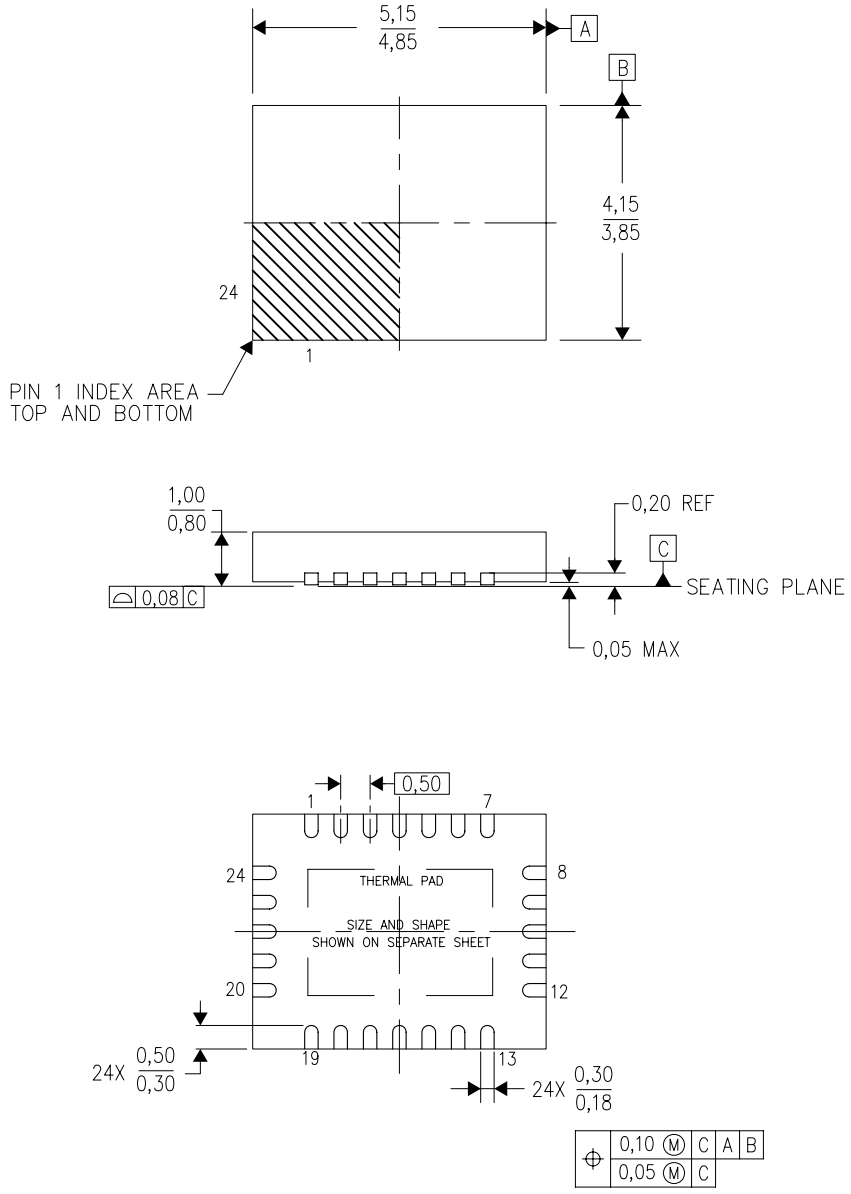
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65290BMRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
TPS65290BMRHFT	VQFN	RHF	24	250	210.0	185.0	35.0
TPS65290LMRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
TPS65290LMRHFT	VQFN	RHF	24	250	210.0	185.0	35.0
TPS65290ZBRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
TPS65290ZBRHFT	VQFN	RHF	24	250	210.0	185.0	35.0

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



4204845–2/H 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

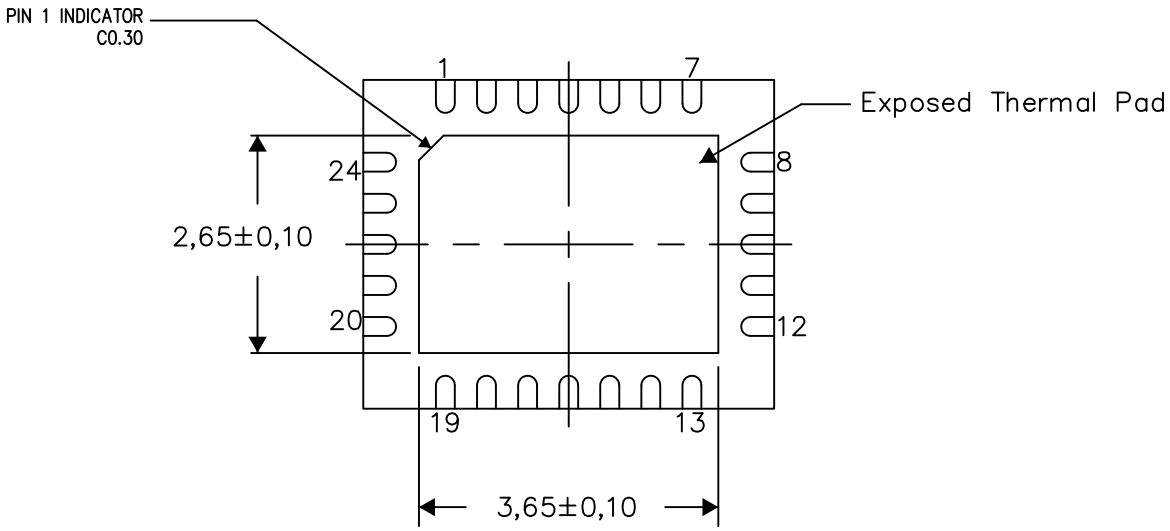
RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



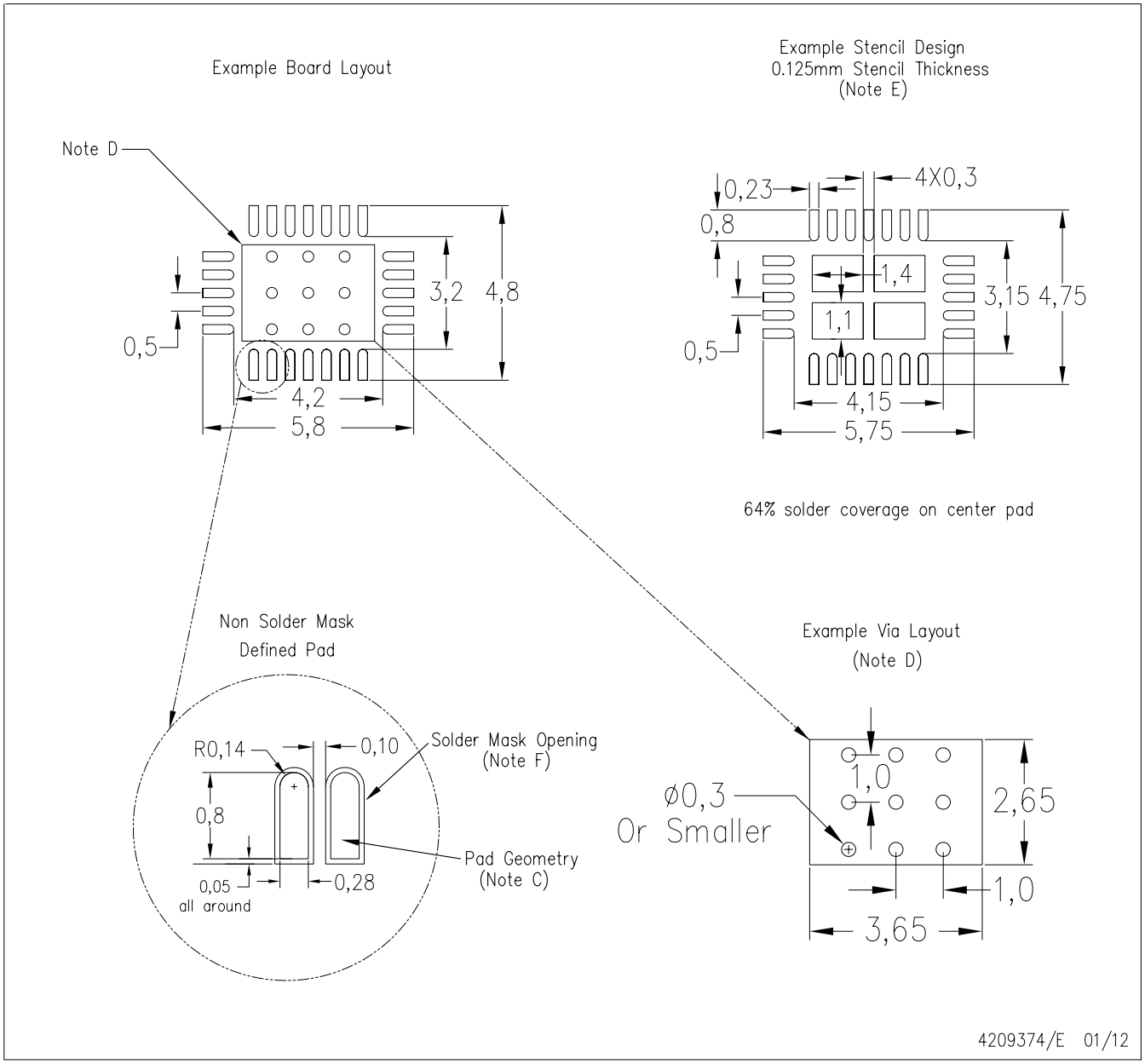
Bottom View

Exposed Thermal Pad Dimensions

4206360–3/K 02/14

NOTE: All linear dimensions are in millimeters

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265