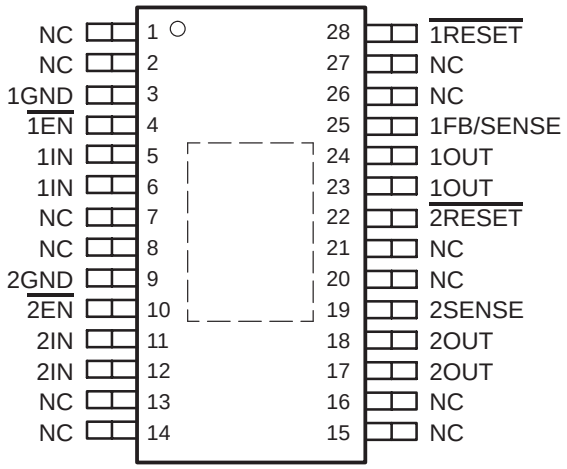
- **Dual Output Voltages for Split-Supply Applications**
- **3.3-V/Adjustable Output, 3.3 V/1.8 V, and 3.3 V/2.5**
- **Dropout Voltage < 80 mV Max at I_O = 100 mA (3.3-V option)**
- **Low Quiescent Current, Independent of Load . . . 340 μA Typ Per Regulator**
- **Ultra-Low-Current Sleep State . . . 2 μA Max**
- **Dual Active-Low Reset Signals with 200-ms Pulse Width**
- **Output Current Range of 0 mA to 750 mA Per Regulator**
- **28-Pin PowerPAD™ TSSOP Package**

PWP PACKAGE
(TOP VIEW)



NC − No internal connection

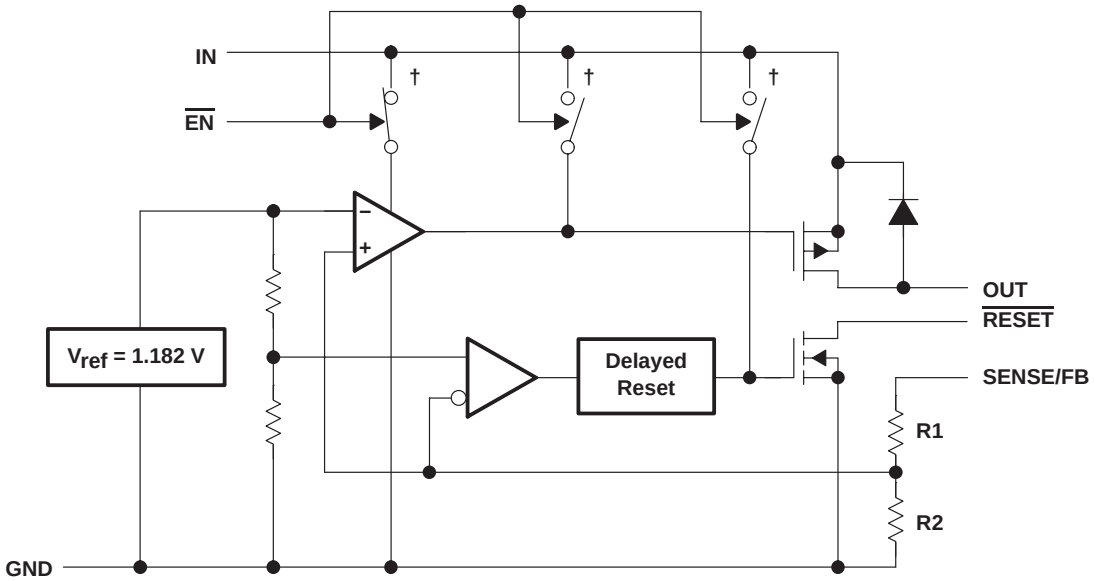
description

The TPS73HD3xx family of dual voltage regulators offers very low dropout voltages and dual outputs in a compact package. Designed primarily for DSP applications, these devices can be used in any mixed-output voltage application with each regulator supporting up to 750 mA. Output current can be allocated as desired between the two regulators and used to power many of todays DSPs. Low quiescent current and very low dropout voltage assure maximum power usage in battery-powered applications. Texas Instruments PowerPAD TSSOP package allows use of these devices with any voltage/current combination within the range of the listed specifications without thermal problems, provided proper device mounting procedures are followed. Separate inputs allow the designer to configure the source power as desired. Dual active-low reset signals allow resetting of core-logic and I/O separately. Remote sense/feedback terminals provide regulation at the load. The TPS73HD3xx are available in 28-pin PowerPAD TSSOP. They operate over a free-air temperature range of −40°C to 125°C.

AVAILABLE OPTIONS

T_A	REGULATOR 1 V_O (V)	REGULATOR 2 V_O (V)	TSSOP (PWP)
−40°C to 125°C	Adj (1.2 − 9.75 V)	3.3 V	TPS73HD301PWPR
	1.8 V	3.3 V	TPS73HD318PWPR
	2.5 V	3.3 V	TPS73HD325PWPR

functional block diagram



† Switch positions shown with $\overline{EN}$ low (active).

OUTPUT VOLTAGE	R1	R2	UNIT
Adjustable	0	∞	Ω
1.8 V	122	233	kΩ
2.5 V	260	233	kΩ
3.3 V	420	233	kΩ

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
NC	1, 2, 7, 8, 13−16, 20, 21, 26, 27		No connection
1GND	3		Regulator #1 ground
$\overline{1EN}$	4	I	Regulator #1 enable, low = enable
1IN	5, 6	I	Regulator #1 input supply voltage
2GND	9		Regulator #2 ground
$\overline{2EN}$	10	I	Regulator #2 enable, low = enable
2IN	11, 12	I	Regulator #2 input supply voltage
2OUT	17, 18	O	Regulator #2 output voltage
2SENSE	19	I	Regulator #2 output voltage sense (fixed output)
$\overline{2RESET}$	22	O	Regulator #2 reset signal, low = reset
1OUT	23, 24	O	Regulator #1 output voltage
1FB/SENSE	25	I	Regulator #1 output voltage feedback (adjustable output)
$\overline{1RESET}$	28	O	Regulator #1 reset signal, low = reset

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range, V_I (xIN, $\overline{\text{xRESET}}$, xSENSE, $\overline{\text{xEN}}$) . . . . . −0.3 V to 11 V
Differential input voltage,V_{ID} (1GND to 2GND) . . . . . 2 V
Output current, I_O (1OUT, 2OUT) . . . . . 2 A
Continuous total power dissipation . . . . . See Dissipation Rating Tables
Operating free-air temperature range, T_A . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE 1 − FREE-AIR TEMPERATURES‡

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PWP‡	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP§	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

‡ This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in^2).

§ This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2).

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I†	Adjustable output (regulator #1)	2.97	10	V
Input voltage, V_I†	3.3−V output (regulator #2)	3.97	10	V
High-level input voltage at $\overline{\text{EN}}$, V_{IH}		2		V
Low-level input voltage at $\overline{\text{EN}}$, V_{IL}			0.5	V
Total output current range (per regulator), I_O		0	750	mA
Operating virtual junction temperature range, T_J		−40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage, V_{DO}, at the maximum specified load range (750 mA). Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

Because regulator 1 of the TPS373HD301 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 3 in the TPS73HD301 electrical characteristics table. The minimum value of 3.5 V is the absolute lower limit for the recommended input voltage range for the TPS73HD301. With 2.97-V input voltage, the LDO may be in dropout and will not meet the 3% regulaotr output or 750-mA load current specification.

electrical characteristics, $V_{I(IN)}$ = 4.3 V, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR‡ = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	T_J	MIN	TYP	MAX	UNIT
	Quiescent current (active mode), each regulator	$\overline{EN}$ ≤ 0.5 V, 0 mA ≤ I_O ≤ 750 mA, See NOTE 2	25°C		340	415	μA
			−40°C to 125°C			550	
I_{CC}	Supply current (standby mode), each regulator	$\overline{EN}$ = V_I, NOTE 2	25°C		0.01	0.5	μA
			−40°C to 125°C			2	
I_O	Output current limit, each regulator	V_O = 0, V_I = 10 V	25°C	0.8	1.2	2	A
			−40°C to 125°C			2	
I_{lkg}	Pass-element leakage current (standby mode)	$\overline{EN}$ = V_I, See NOTE 2	25°C		0.01	0.5	μA
			−40°C to 125°C			1	
	Output voltage temperature coefficient		−40°C to 125°C		61	75	ppm/°C
	Thermal shutdown junction temperature				165		°C
	Logic high ($\overline{EN}$) (standby mode)	2.5 V ≤ V_I ≤ 6 V, 6 V ≤ V_I ≤ 10 V	−40°C to 125°C	2			V
				2.7			
	Logic low ($\overline{EN}$) (active mode)	See NOTE 2	25°C			0.5	V
			−40°C to 125°C			0.5	
V_{hys}	Hysteresis voltage ($\overline{EN}$)		25°C		50		mV
I_I	Input current ($\overline{EN}$)	0 V ≤ V_I ≤ 10 V	25°C	−0.5	0.001	0.5	μA
			−40°C to 125°C	−0.5		0.5	
	Minimum input voltage, for active pass element		25°C		2.05	2.5	V
			−40°C to 125°C			2.5	
	Minimum input voltage, for valid $\overline{RESET}$	$I_{O(RESET)}$ = −300 μA	25°C		1	1.5	V
			−40°C to 125°C			1.9	

‡ CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

§ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

NOTE 2: Minimum input voltage is 3.5V or Vo(typ) + 1V whichever is greater.

The minimum value of 3.5 V is the absolute lower limit for the recommended input voltage range for the TPS73HD301.

electrical characteristics, $V_{I(IN)}$ = 4.3 V, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted) (continued)

adjustable regulator

PARAMETER		TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
	Reference voltage (1FB)	5 mA ≤ I_O ≤ 750 mA, See NOTE 2		25°C		1.182		V
				−40°C to 125°C	1.147		1.217	
	Reference voltage temperature coefficient			−40°C to 125°C		61	75	ppm/°C
	Pass-element series resistance (see Note 3)	50 μA ≤ I_O ≤ 750 mA, See NOTE 2		25°C		0.52	1	Ω
				−40°C to 125°C			1	
		V_I = 3.9 V, 50 μA ≤ I_O ≤ 750 mA		25°C		0.32		
		V_I = 5.9 V, 50 μA ≤ I_O ≤ 750 mA		25°C		0.23		
	Input regulation	V_I = 3.5 V, 50 μA ≤ I_O ≤ 750 mA		25°C		3		mV
	Output regulation	I_O = 5 mA to 750 mA, See NOTE 2		25°C		7		mV
		I_O = 50 μA to 750 mA, See NOTE 2		25°C		10		mV
	Ripple rejection	f = 120 Hz,	I_O = 50 μA	25°C		59		dB
		f = 120 Hz,	I_O = 500 mA	25°C		54		
	Output noise-spectral density	f = 120 Hz		25°C		2		mV/√Hz
	Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C_L = 4.7 μF	25°C		95		μV/rms
			C_L = 10 μF	25°C		89		
			C_L = 100 μF	25°C		74		
$V_{(TO)}$	Trip-threshold voltage ($\overline{RESET}$)§	$V_{O(FB)}$ decreasing		−40°C to 125°C	1.101		1.145	V
V_{hys}	Hysteresis voltage ($\overline{RESET}$)§	Measured at $V_{O(ER)}$		25°C		12		mV
V_{OL}	Low-level output voltage ($\overline{RESET}$)§	V_I = 2.13 V,	$I_{O(RESET)}$ = 400 μA	25°C		0.1	0.4	V
				−40°C to 125°C			0.4	
I_I	Input current (1FB)			25°C	−10	0.1	10	nA
				−40°C to 125°C	−20		20	

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_L.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information)

NOTE 3: To calculate dropout voltage, use equation:

$$V_{DO} = I_O \times r_{DS(ON)}$$

$r_{DS(ON)}$ is a function of both output current and input voltage. This parametric table lists $r_{DS(ON)}$ for V_I = 3.9 V and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 4 V and 6 V respectively. For other programmed values, refer to Figure 29.

electrical characteristics, $V_{I(IN)}$ = 4.3 V, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted) (continued)

1.8-V regulator (TPS73HD318)

PARAMETER		TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
V_O	Output voltage	4.3 V ≤ V_I ≤ 10 V		25°C	1.746	1.8	1.854	V
				−40°C to 125°C	1.728		1.872	
	Pass-element series resistance	(3.5 V − V_O)/I_O, I_O = 750 mA,	V_I = 3.5 V, V_{2SENSE} = 0 V§	25°C		0.5	1	Ω
				−40°C to 125°C			1.2	
	Input regulation	50 μA ≤ I_O ≤ 750 mA,	See NOTE 2	25°C		6		mV
	Output regulation	I_O = 5 mA to 750 mA,	See NOTE 2	25°C		14		mV
		I_O = 50 μA to 750 mA,	See NOTE 2	25°C		18		
	Ripple rejection	f = 120 Hz,	I_O = 50 μA	25°C		51		dB
		f = 120 Hz,	I_O = 500 mA	25°C		49		
	Output noise-spectral density	f = 120 Hz		25°C		2		mV/√Hz
	Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C_L = 4.7 μF	25°C		274		μV/rms
			C_L = 10 μF	25°C		228		
			C_L = 100 μF	25°C		159		

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_L.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Pass-element series resistance measured with sense pin disconnected from output to allow output voltge to rise to full saturation.

electrical characteristics, $V_{I(IN)}$ = 4.3 V, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted) (continued)

2.5-V regulator (TPS73HD325)

PARAMETER		TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
V_O	Output voltage	4.3 V ≤ V_I ≤ 10 V		25°C	2.45	2.5	2.55	V
				−40°C to 125°C	2.425		2.575	
	Dropout voltage	I_O = 750 mA,	V_I = 3.5 V	−40°C to 125°C			800	mV
	Input regulation	50 μA ≤ I_O ≤ 750 mA,	See NOTE 2	25°C		6		mV
	Output regulation	I_O = 5 mA to 750 mA,	See NOTE 2	25°C		20		mV
		I_O = 50 μA to 750 mA,	See NOTE 2	25°C		25		mV
	Ripple rejection	f = 120 Hz,	I_O = 50 μA	25°C		51		dB
		f = 120 Hz,	I_O = 500 mA	25°C		49		
	Output noise-spectral density	f = 120 Hz		25°C		2		mV/√Hz
	Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C_L = 4.7 μF	25°C		274		μV/rms
			C_L = 10 μF	25°C		228		
			C_L = 100 μF	25°C		159		
$V_{(TO)}$	Trip-threshold voltage ($\overline{RESET}$)	V_O decreasing		−40°C to 125°C	2.172			V
V_{hys}	Hysteresis voltage ($\overline{RESET}$)			25°C		18		mV
V_{OL}	Low-level output voltage ($\overline{RESET}$)	V_I = 2.8 V,	$I_{O(RESET)}$ = −1 mA	25°C		0.17	0.4	V
				−40°C to 125°C			0.4	

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_L.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Pass-element series resistance measured with sense pin disconnected from output to allow output voltge to rise to full saturation.

switching characteristics

PARAMETER	TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
Time-out delay ($\overline{RESET}$)	See Figure 3	25°C	140	200	260	ms
		−40°C to 125°C	100		300	

electrical characteristics, $V_{I(IN)}$ = 4.3 V, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted) (continued)

3.3-V regulator (TPS73HD301)

PARAMETER		TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
V_O	Output voltage	4.3 V ≤ V_I ≤ 10 V		25°C		3.3		V
				−40°C to 125°C	3.23		3.37	
	Dropout voltage	I_O = 10 mA,	V_I = 3.23 V	25°C		4.5	10	mV
		I_O = 100 mA,	V_I = 3.23 V	25°C		44	100	
		I_O = 750 mA,	V_I = 3.23 V	25°C		353	750	
				−40°C to 125°C			800	
	Pass-element series resistance	(3.23 V − V_O)/I_O, I_O = 750 mA	V_I = 3.23 V,	25°C		0.44	1	Ω
				−40°C to 125°C			1.07	
	Input regulation	50 μA ≤ I_O ≤ 750 mA,	See NOTE 2	25°C		6		mV
	Output regulation	I_O = 5 mA to 750 mA,	See NOTE 2	25°C		30		mV
		I_O = 50 μA to 750 mA,	See NOTE 2	25°C		37		mV
	Ripple rejection	f = 120 Hz,	I_O = 50 μA	25°C		51		dB
		f = 120 Hz,	I_O = 500 mA	25°C		49		
	Output noise-spectral density	f = 120 Hz		25°C		2		mV/√Hz
	Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C_L = 4.7 μF	25°C		274		μV/rms
			C_L = 10 μF	25°C		228		
			C_L = 100 μF	25°C		159		
$V_{(TO)}$	Trip-threshold voltage ($\overline{RESET}$)	V_O decreasing		−40°C to 125°C	2.868			V
V_{hys}	Hysteresis voltage ($\overline{RESET}$)			25°C		18		mV
V_{OL}	Low-level output voltage ($\overline{RESET}$)	V_I = 2.8 V,	$I_{O(RESET)}$ = −1 mA	25°C		0.17	0.4	V
				−40°C to 125°C			0.4	

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_L.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

switching characteristics

PARAMETER	TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
Time-out delay ($\overline{RESET}$)	See Figure 3	25°C	140	200	260	ms
		−40°C to 125°C	100		300	

PARAMETER MEASUREMENT INFORMATION

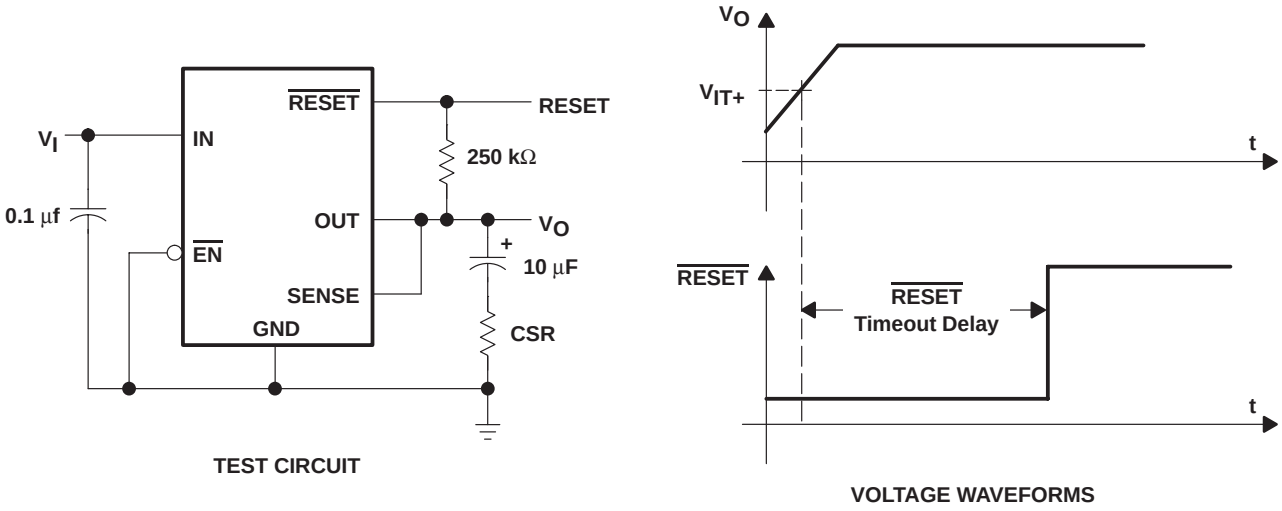


Figure 1. Test Circuit and Voltage Waveforms

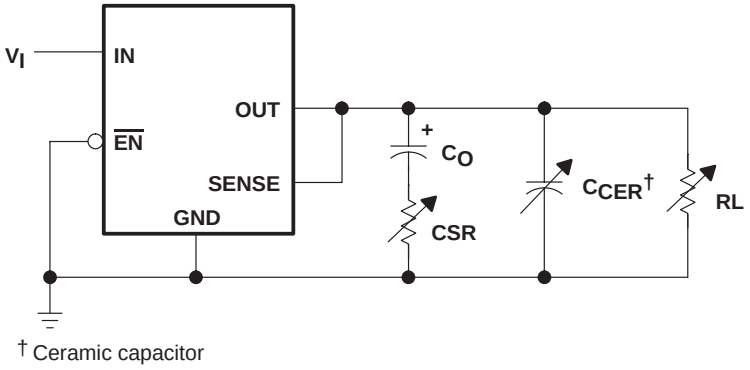


Figure 2. Test Circuit for Typical Regions of Stability (Refer to Figures 29 through 32)

TYPICAL CHARACTERISTICS

Table of Graphs

I_Q	Quiescent current		vs Load current	5
			vs Input voltage	6
V_{DO}	Dropout voltage	Adjustable regulator	vs Load current	7
		3.3-V regulator	vs Load current	8
ΔV_{DO}	Change in dropout voltage		vs Free-air temperature	9
V_{DO}	Dropout voltage		vs Output current	10
ΔV_O	Change in output voltage		vs Free-air temperature	11
V_O	Output voltage		vs Input voltage	12
	Line regulation			13
V_O	Output voltage		vs Output current	14, 15
	Output voltage response from enable ($\overline{EN}$)			16
	Load transient response	Adjustable regulator		17
		3.3-V regulator		18
	Line transient response	Adjustable regulator		19
		3.3-V regulator		20
	Ripple rejection		vs Frequency	21
	Output spectral noise density		vs Frequency	22
	Compensation series resistance (CSR)	Adjustable regulator	vs Output current	23
			vs Added ceramic capacitance	24
			vs Output current	25
		3.3-V regulator	vs Output current	26
		Adjustable regulator	vs Added ceramic capacitance	27
		3.3-V regulator	vs Added ceramic capacitance	28
$r_{DS(on)}$	Pass-element resistance		vs Input voltage	29
V_I	Minimum input voltage for valid $\overline{RESET}$		vs Free-air temperature	30
V_{IT-}	Negative-going reset threshold		vs Free-air temperature	31
$I_{OL(RESET)}$	$\overline{RESET}$ output current	3.3-V regulato	vs Input voltage	32
t_d	Reset time delay		vs Free-air temperature	33
t_d	Distribution for reset delay			34

TYPICAL CHARACTERISTICS

QUEISCENT CURRENT
vs
LOAD CURRENT

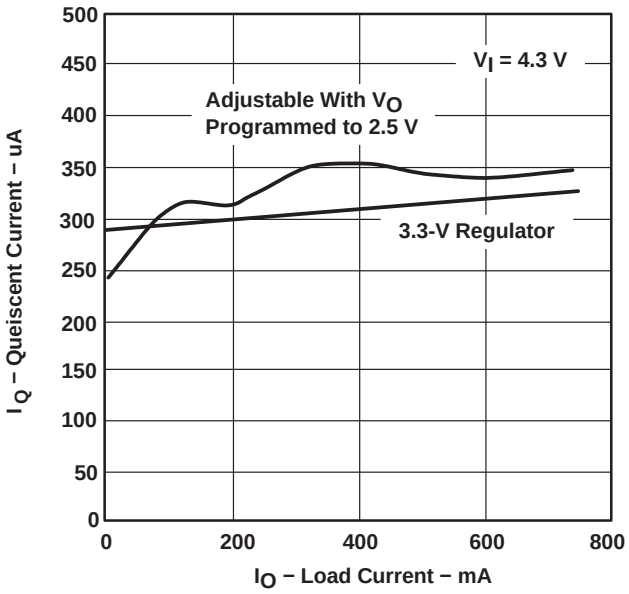


Figure 3

QUIESCENT CURRENT
vs
INPUT VOLTAGE

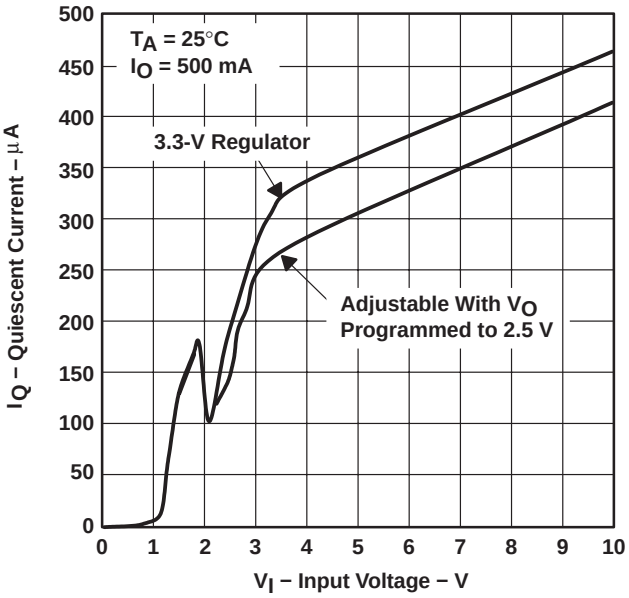


Figure 4

ADJUSTABLE REGULATOR DROPOUT VOLTAGE
vs
LOAD CURRENT

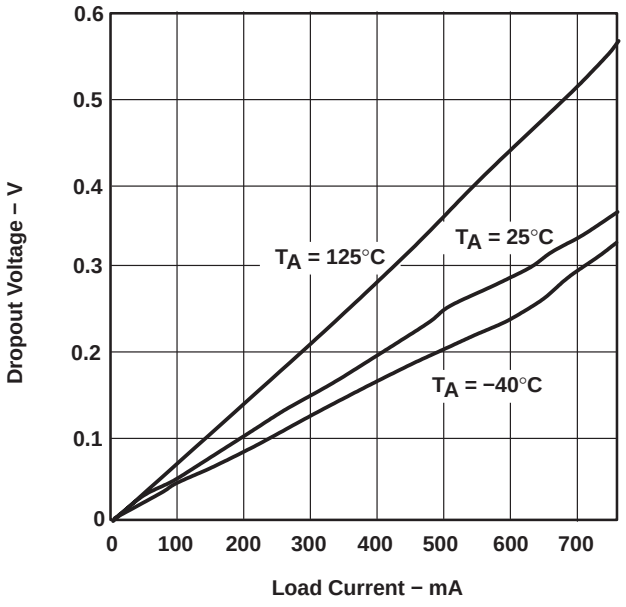


Figure 5

3.3−V REGULATOR DROPOUT VOLTAGE
vs
LOAD CURRENT

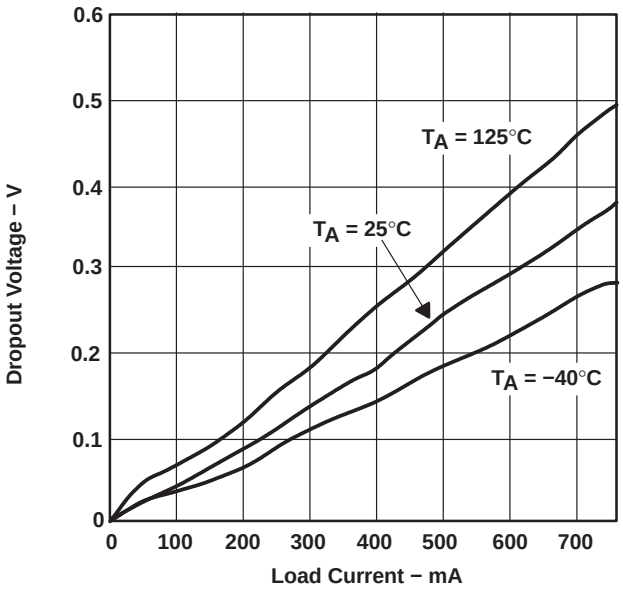


Figure 6

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

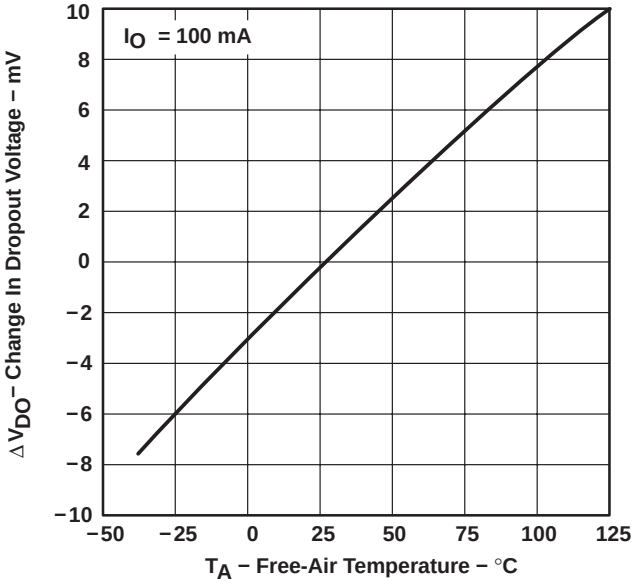


Figure 7

DROPOUT VOLTAGE vs OUTPUT CURRENT

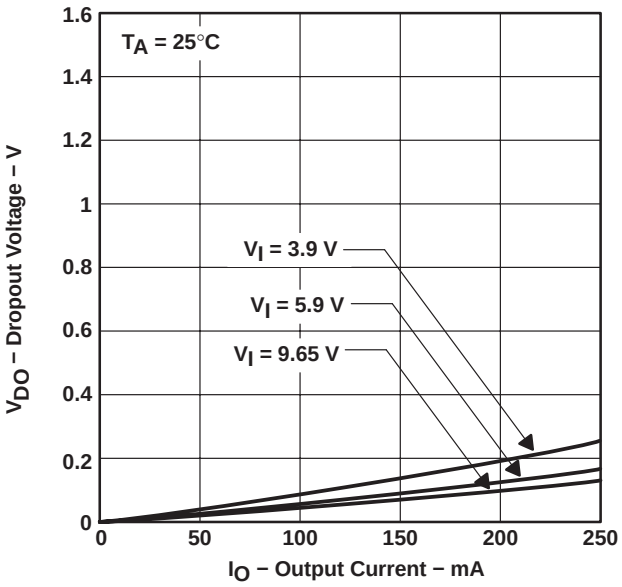


Figure 8

CHANGE IN OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

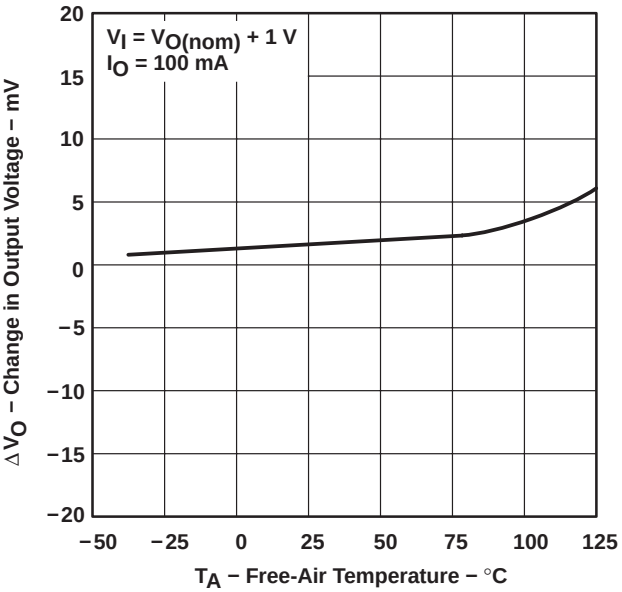


Figure 9

OUTPUT VOLTAGE vs INPUT VOLTAGE

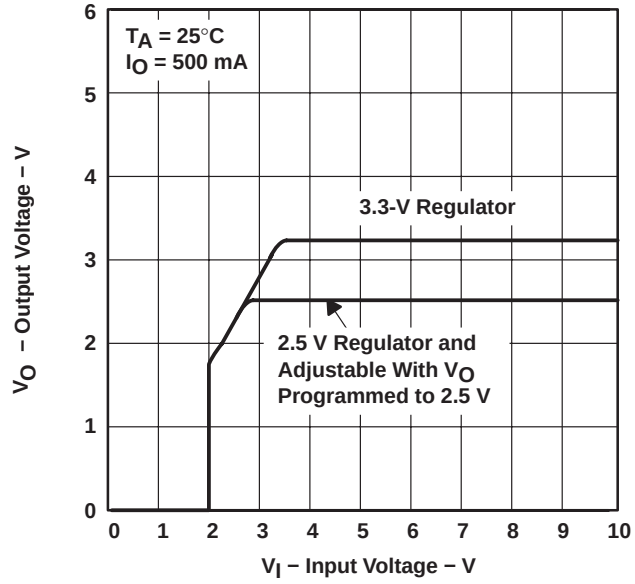


Figure 10

TYPICAL CHARACTERISTICS

LINE REGULATION

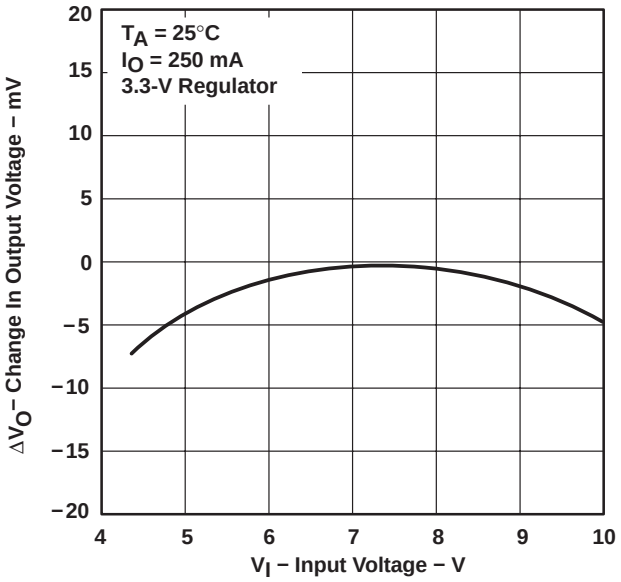


Figure 11

OUTPUT VOLTAGE vs OUTPUT CURRENT

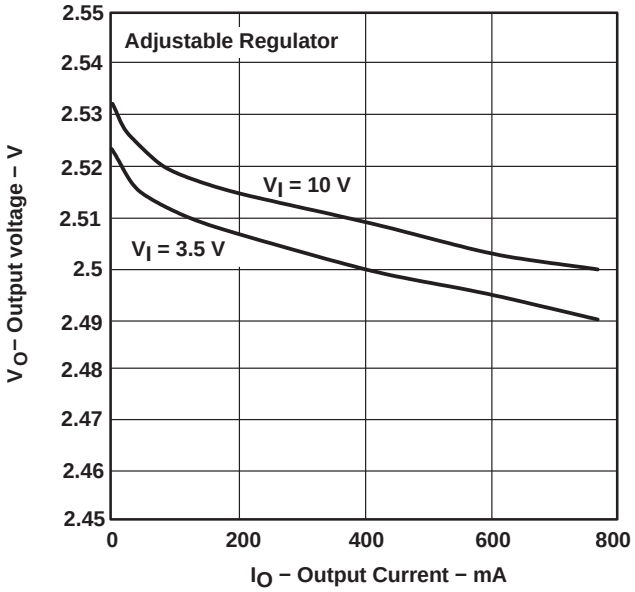


Figure 12

OUTPUT VOLTAGE vs OUTPUT CURRENT

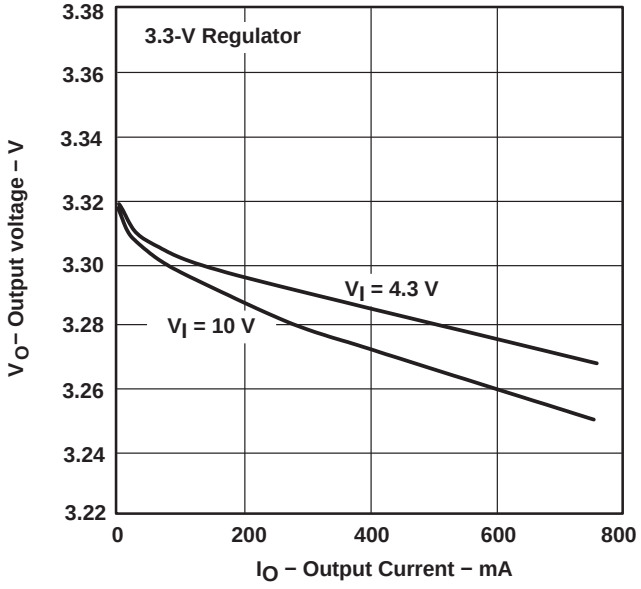


Figure 13

TYPICAL CHARACTERISTICS

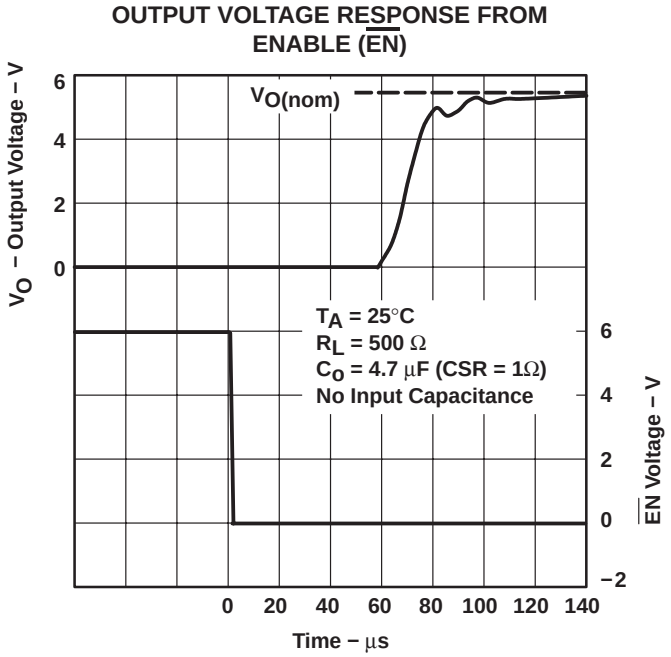


Figure 14

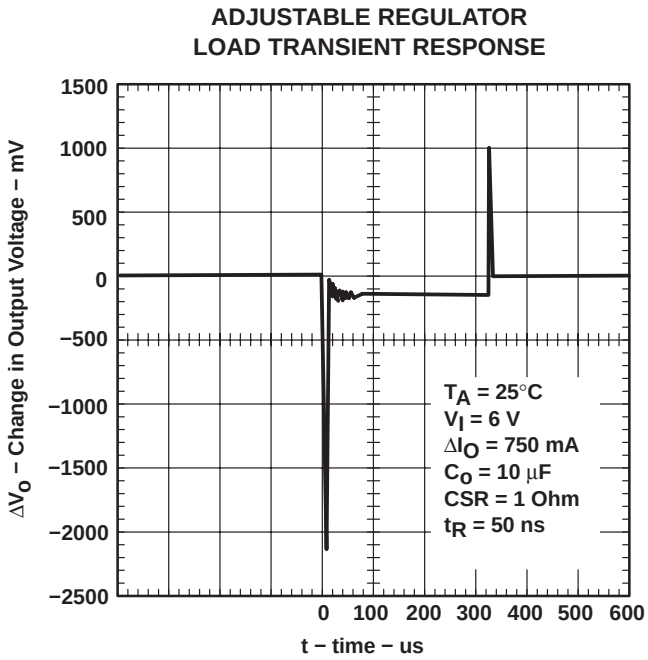


Figure 15

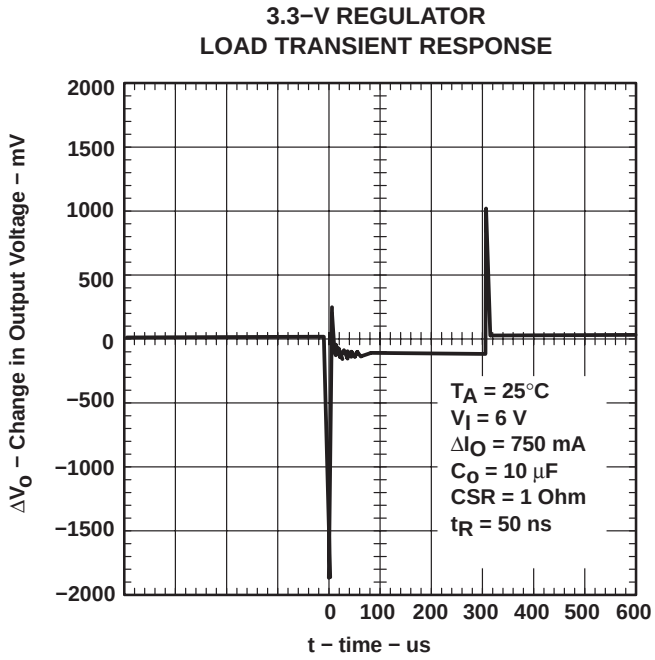


Figure 16

TYPICAL CHARACTERISTICS

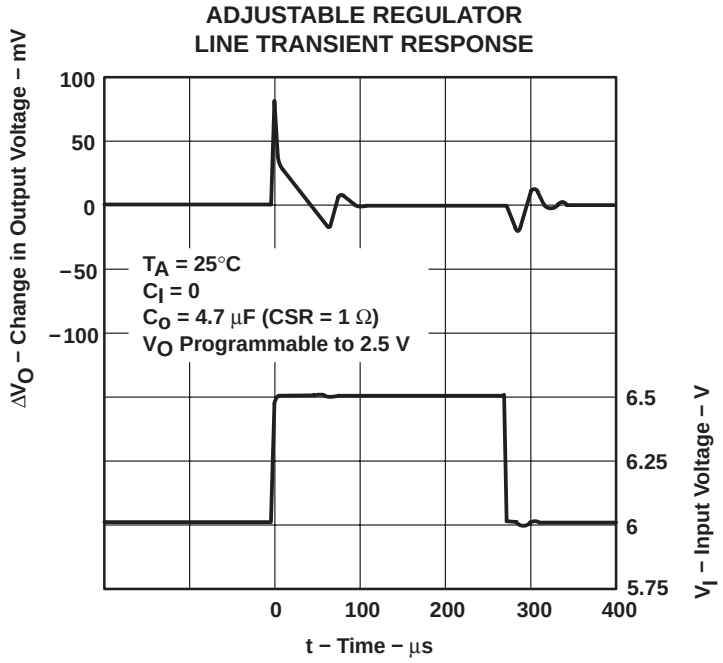


Figure 17

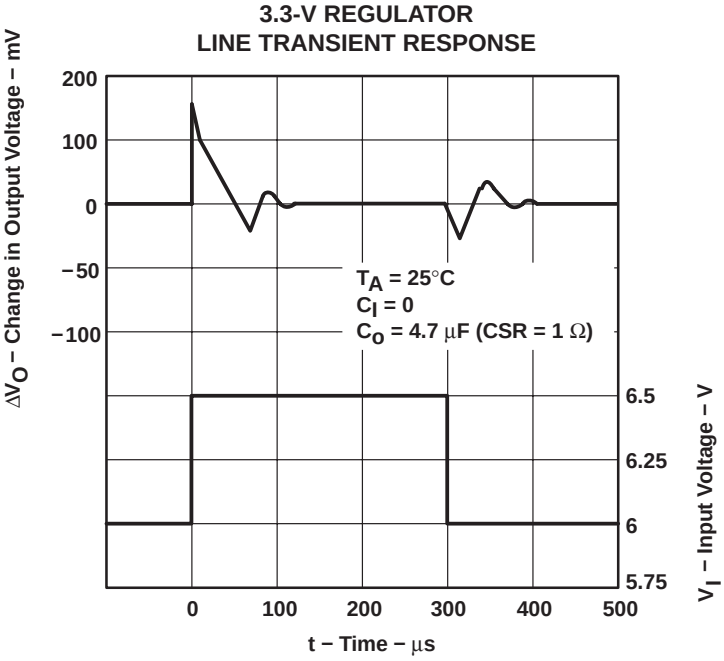


Figure 18

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
FREQUENCY

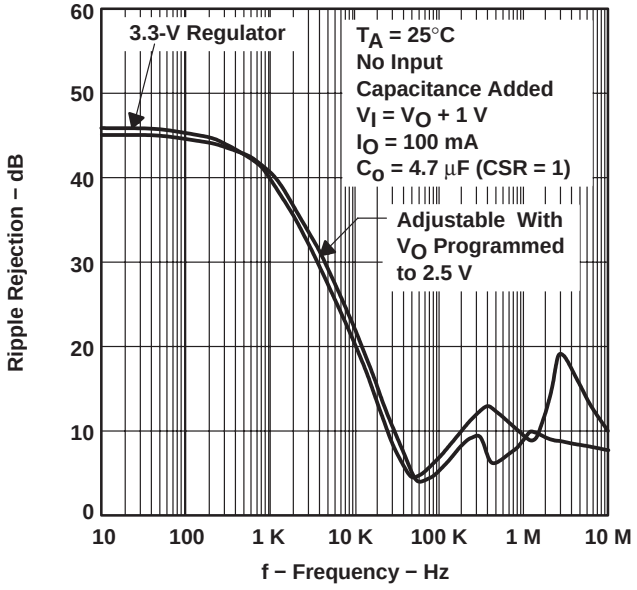


Figure 19

OUTPUT SPECTRAL-NOISE DENSITY
vs
FREQUENCY

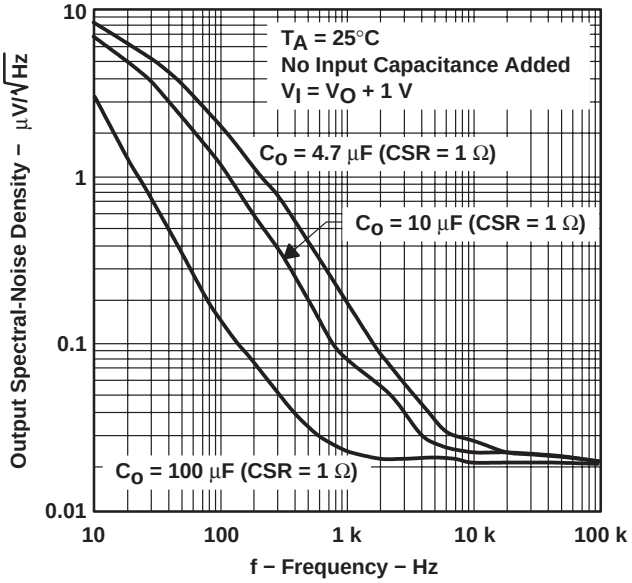


Figure 20

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
OUTPUT CURRENT

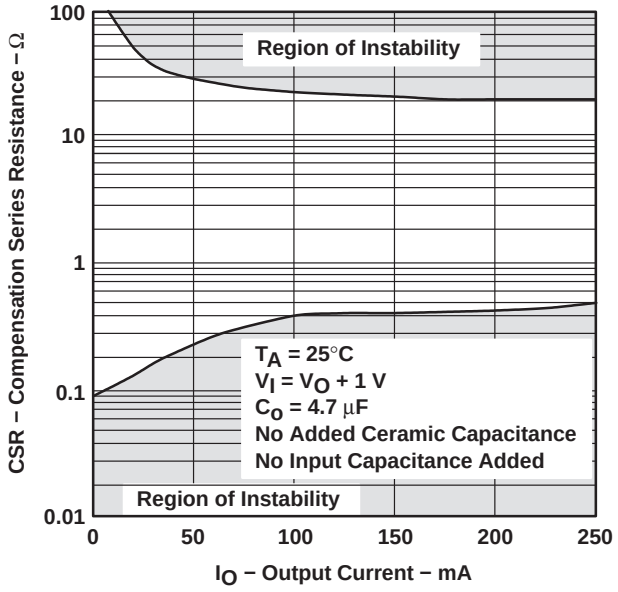


Figure 21

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
ADDED CERAMIC CAPACITANCE

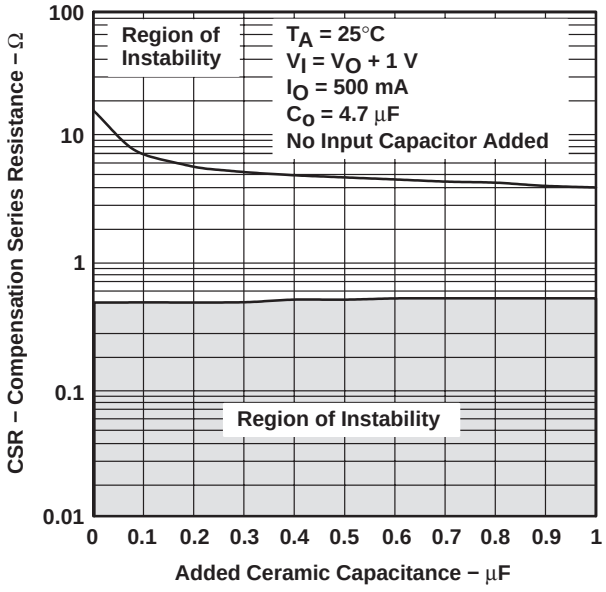


Figure 22

TYPICAL CHARACTERISTICS

ADJUSTABLE REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

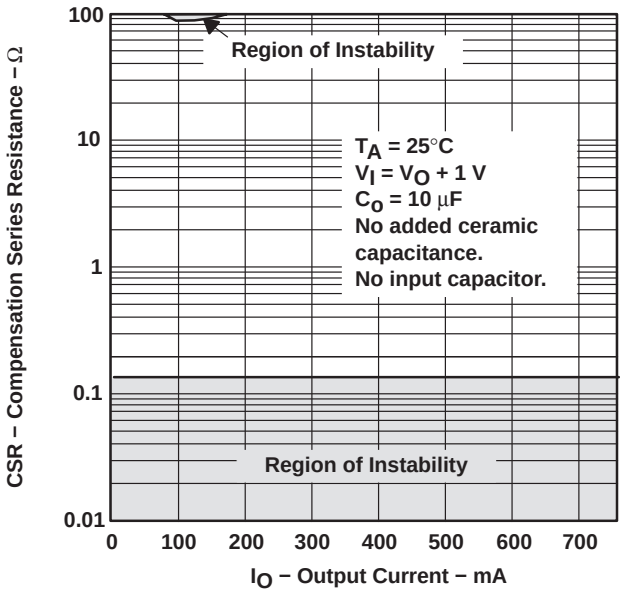


Figure 23

3.3−V REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

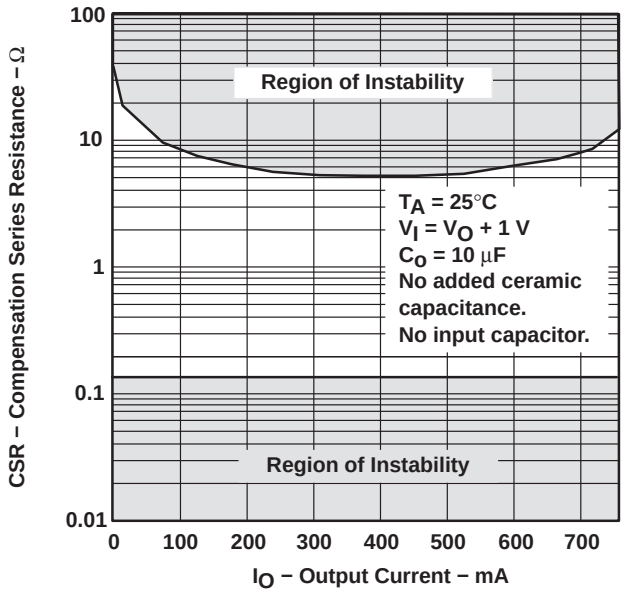


Figure 24

ADJUSTABLE REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

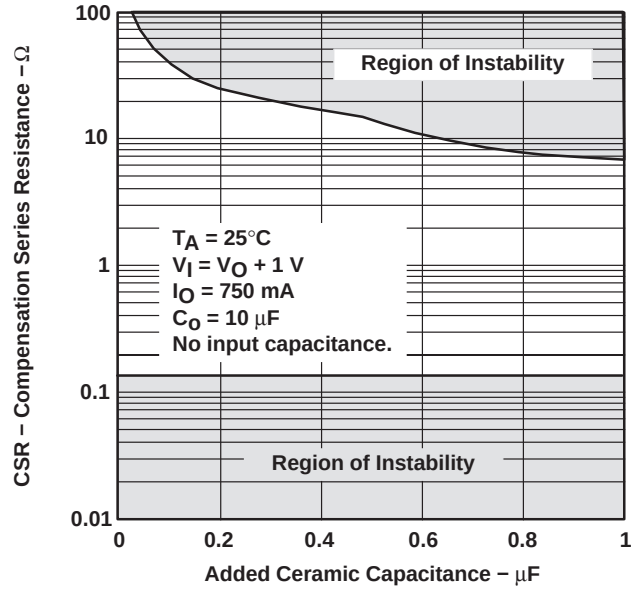


Figure 25

3.3-V REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

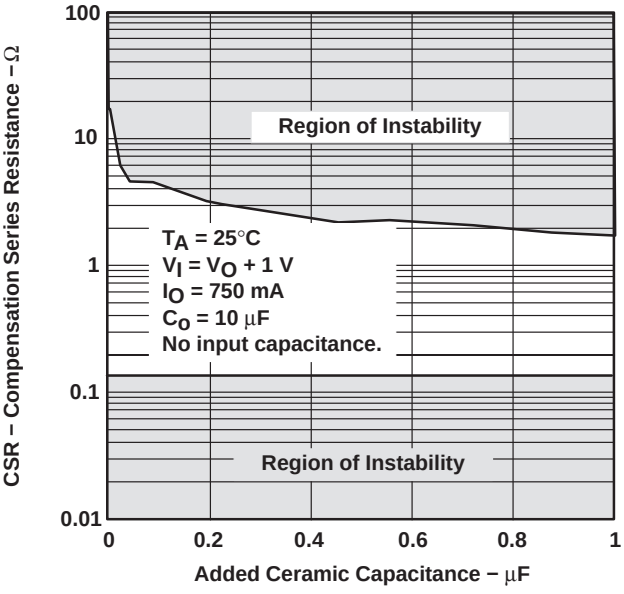


Figure 26

TYPICAL CHARACTERISTICS

PASS-ELEMENT RESISTANCE vs INPUT VOLTAGE

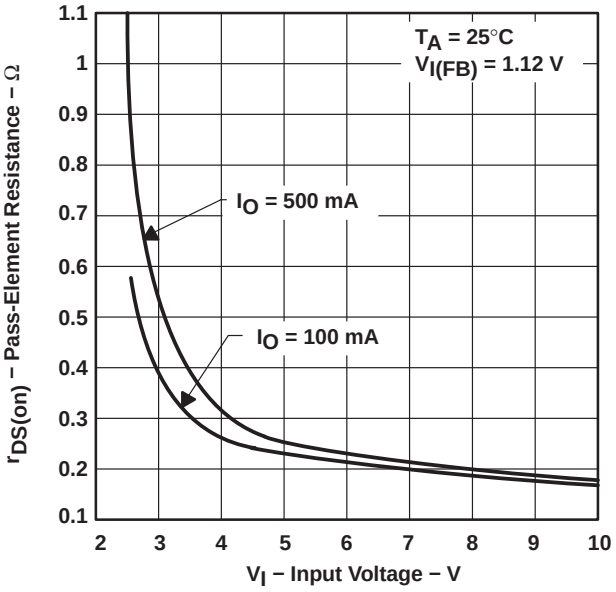


Figure 27

MINIMUM INPUT VOLTAGE FOR VALID $\overline{\text{RESET}}$ vs FREE-AIR TEMPERATURE

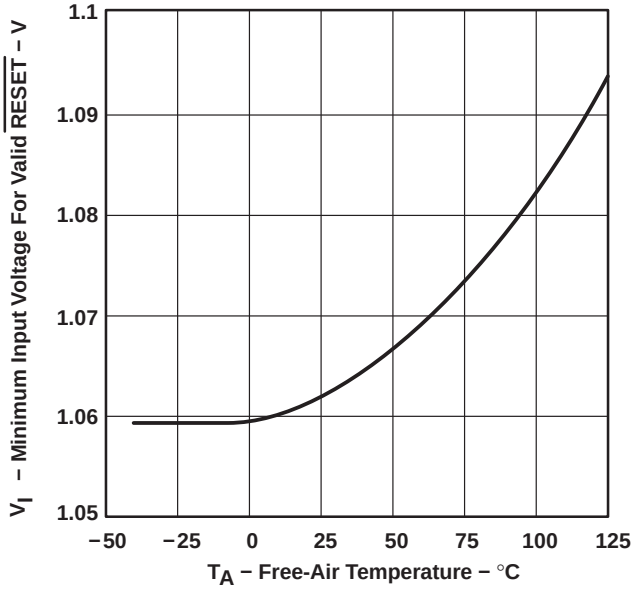


Figure 28

NEGATIVE-GOING RESET THRESHOLD vs FREE-AIR TEMPERATURE

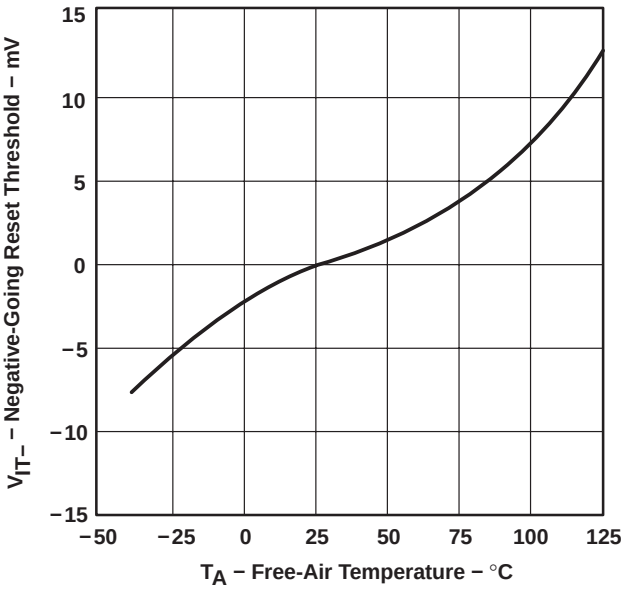


Figure 29

$\overline{\text{RESET}}$ OUTPUT CURRENT vs INPUT VOLTAGE

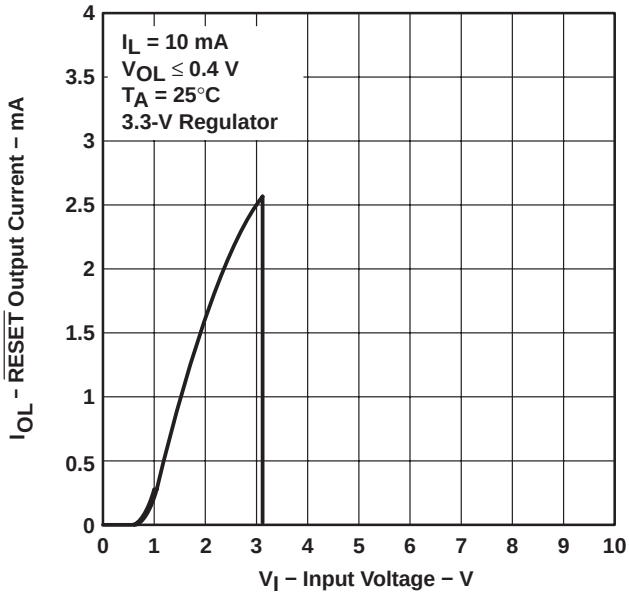


Figure 30

TYPICAL CHARACTERISTICS

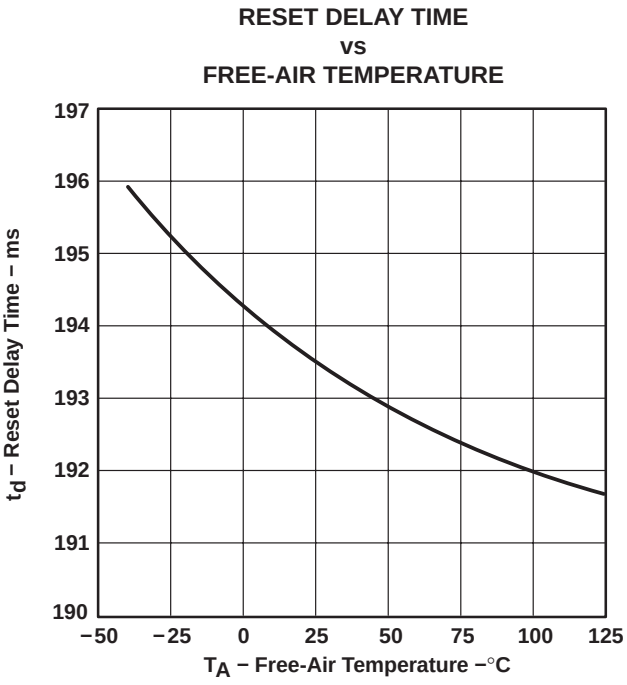


Figure 31

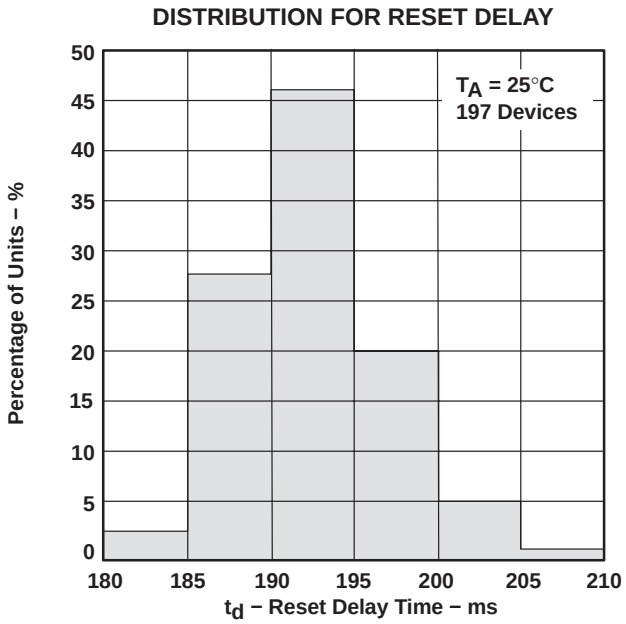


Figure 32

THERMAL INFORMATION

The TPS73HD3xx is packaged in a high-power dissipation downset lead frame for optimal power handling. with proper heat dissipation techniques, the full power soutput of these devices can be safely handled over the full temperture range. The Texas Instruments technical brief, *PowerPAD Thermally Enhanced Package* (literature number SLMA002), goes into considerable detail into techniques for properly mounting this type of package for maximum thermal performance. A thermal conduction plane of approximately 3″ y 3″ will give a power dissipatio level of 4.5 W.

Power dissipation within the device can be calculated with the following equation:

$$P_D = P_{IN} - P_{OUT} = V_I\left(I_{O1} + I_{O2}\right) - \left(V_{O1} \times I_{O1} + V_{O2} \times I_{O2}\right)$$

APPLICATION INFORMATION

thermal considerations

DISSIPATION RATING TABLE

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PWP‡	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP§	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

† This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in^2).

‡ This parameter is measured with the recommended copper heat sink pattern on an 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2).

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM and 300 CFM data from the dissipation rating table, the derating factor for the PWP package with 6.9 in^2 of copper area on a multilayer PCB is 24 mW/°C and 58 mW/°C respectively. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}}$$

For 0 CFM :

$$= \frac{1}{0.0235}$$

$$= 42.6°C/W$$

For 300 CFM :

$$= \frac{1}{0.0579}$$

$$= 17.3°C/W$$

Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPS73HD3xx is 150 °C.

$$T_A\,\text{Max} = T_J\,\text{Max} - \left(\Theta_{JA} \times P_D\right)$$

The maximum power dissipation limit is determined using the following equation:

$$T_{D(max)} = \frac{T_J\,\text{max} - T_A}{R_{\theta JA}}$$

Where:

$T_J$max is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-free-air for the package (i.e., 285°C/W for the 5-terminal SOT-23 package.

T_A is the free-air temperautre

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times 1_O$$

Power dissipation resulting from quiescent current is negligible.

APPLICATION INFORMATION

Capitalizing upon the features of the TPS73xx family (low-dropout voltage, low quiescent current, power-saving shutdown mode, and a supply-voltage supervisor) and the power-dissipation properties of the TSSOP PowerPAD package has enabled the integration of the TPS73HD3xx dual LDO regulator with high output current for use in DSP and other multiple voltage applications. Figure 35 shows a typical dual-voltage DSP application.

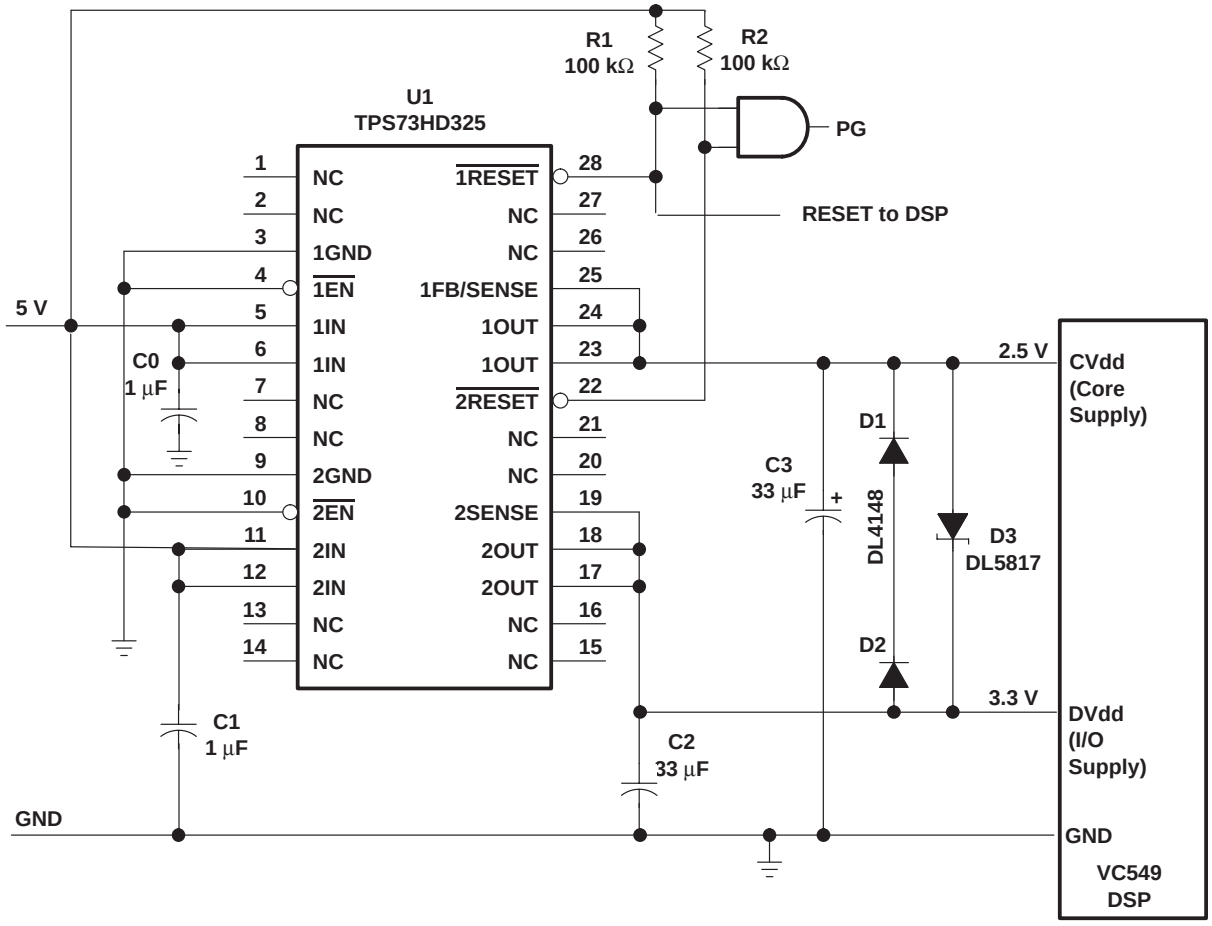


Figure 33. Dual-Voltage DSP Application

DSP power requirements include very high transient currents that must be considered in the initial design. This design uses higher-valued output capacitors to handle the large transient currents. Details of this type of design are shown in the application report, *Designing Power Supplies for TMS320VC549 DSP Systems.*

minimum load requirements

The TPS73HD3xx is stable even at zero load; no minimum load is required for operation.

APPLICATION INFORMATION

SENSE connection

The SENSE terminal of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way as to minimize/avoid noise pickup. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μF) improves load transient response and noise rejection when the TPS73HD3xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

As with most LDO regulators, the TPS73HD3xx requires an output capacitor for stability. A low-ESR 10-μF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 44). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106M035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to −40°C). Where component height and/or mounting area is a problem, physically smaller, 10-μF devices can be screened for ESR. Figures 23 through 28 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

Due to the reduced stability range available when using output capacitors smaller than 10 μF, capacitors in this range are not recommended. Larger capacitors provide a wider range of stability and better load transient response. Because capacitor minimum ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As shown in the CSR graphs (Figures 23 through 28), minimum ESR is not a problem when using 10-μF or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS73HD3xx. This information, along with the CSR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

APPLICATION INFORMATION

external capacitor requirements (continued)

All load and temperature conditions with up to 1 µF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 µF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 µF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 µF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 µF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 µF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 µF, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 µF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 µF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 µF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 µF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 µF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 µF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.

APPLICATION INFORMATION

programming the adjustable LDO regulator output

Programming the adjustable regulator is done using an external resistor divider as shown in Figure 44. The equation governing the output voltage is:

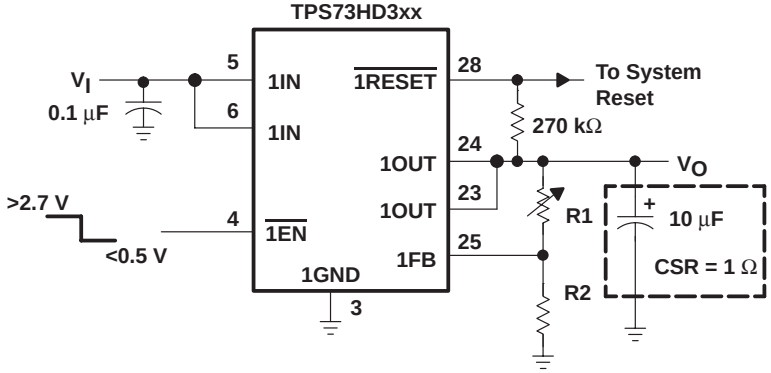
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right)$$

Where

V_{ref} = reference voltage, 1.182 V typ

Resistors R1 and R2 should be chosen for approximately 7-μA divider current. A recommended value for R2 is 169 kΩ with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	RESET VOLTAGE	R1	R2	UNIT
1.5 V	−†	45.3	169	kΩ
1.8 V	−†	88.7	169	kΩ
2.5 V	2.37 V	191	169	kΩ
3.3 V	3.13 V	309	169	kΩ
3.6 V	3.42 V	348	169	kΩ
4 V	3.80 V	402	169	kΩ
5 V	4.75 V	549	169	kΩ
6.4 V	6.08 V	750	169	kΩ

† Non-operational below 1.9 V

Figure 34. TPS7301 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

undervoltage supervisor function

The $\overline{\text{RESET}}$ outputs of the TPS73HD3xx initiate a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS73HD3xx monitors the output voltage of the regulator to detect the undervoltage condition. When that occurs, the $\overline{\text{RESET}}$ output transistor turns on, taking the $\overline{\text{RESET}}$ signal low.

At programmed output voltages below 1.9 V (on the adjustable regulator only) and on the 1.8 V regulator the reset function becomes unusable. With a minimum output voltage requirement for a valid $\overline{\text{RESET}}$ signal (over temperature) being 1.9 V, $\overline{\text{RESET}}$ will not operate reliably in this range.

On power up, the output voltage tracks the input voltage. The $\overline{\text{RESET}}$ output becomes active (low) as V_I approaches the minimum required for a valid $\overline{\text{RESET}}$ signal (specified at 1.5 V for 25°C and 1.9 V over full recommended operating temperature range). When the output voltage reaches the appropriate positive-going input threshold (V_{IT+}), a 200-ms (typical) timeout period begins during which the $\overline{\text{RESET}}$ output remains low. Once the timeout has expired, the $\overline{\text{RESET}}$ output becomes inactive. Since the $\overline{\text{RESET}}$ output is an open-drain NMOS, a pullup resistor should be used to ensure that a logic-high signal is indicated.

The supply-voltage-supervisor function is also activated during power down. As the input voltage decays and after the dropout voltage is reached, the output voltage tracks linearly with the decaying input voltage. When the output voltage drops below the specified negative-going input threshold (V_{IT-} — see electrical characteristics tables), the $\overline{\text{RESET}}$ output becomes active (low). It is important to note that if the input voltage decays below the minimum required for a valid $\overline{\text{RESET}}$, the $\overline{\text{RESET}}$ is undefined.

Since the circuit is monitoring the regulator output voltage, the $\overline{\text{RESET}}$ output can also be triggered by disabling the regulator or by any fault condition that causes the output to drop below V_{IT-}. Examples of fault conditions include a short circuit on the output and a low input voltage. Once the output voltage is reestablished, either by reenabling the regulator or removing the fault condition, then the internal timer is initiated, which holds the $\overline{\text{RESET}}$ signal active during the 200-ms (typical) timeout period.

Transient loads or line pulses can also cause a reset to occur if proper care is not taken in selecting the input and output capacitors. Load transients that are faster than 5 μs can cause a reset if high-ESR output capacitors (greater than approximately 7 Ω) are used. A 1-μs transient causes a reset when using an output capacitor with greater than 3.5 Ω of ESR. Note that the output-voltage spike during the transient can drop well below the reset threshold and still not trip if the transient duration is short. A 1-μs transient must drop at least 500 mV below the threshold before tripping the reset circuit. A 2-μs transient trips $\overline{\text{RESET}}$ at just 400 mV below the threshold. Lower-ESR output capacitors help by reducing the drop in output voltage during a transient and should be used when fast transients are expected.

NOTE:

$V_{IT+} = V_{IT-}$ +Hysteresis

output noise

The TPS73HD3xx has very low output noise, with a spectral noise density < 2 μV/$\sqrt{\text{Hz}}$. This is important when noise-susceptible systems, such as audio amplifiers, are powered by the regulator.

APPLICATION INFORMATION

regulator protection

The TPS73HD3xx PMOS-pass transistors have built-in back diodes that safely conduct reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS73HD3xx also features internal current limiting and thermal protection. During normal operation, the TPS73HD3xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73HD301PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73HD301	Samples
TPS73HD301PWPG4	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73HD301	Samples
TPS73HD301PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73HD301	Samples
TPS73HD318PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73HD318	Samples
TPS73HD318PWPG4	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73HD318	Samples
TPS73HD318PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73HD318	Samples
TPS73HD325PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73HD325	Samples
TPS73HD325PWPG4	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73HD325	Samples
TPS73HD325PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73HD325	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

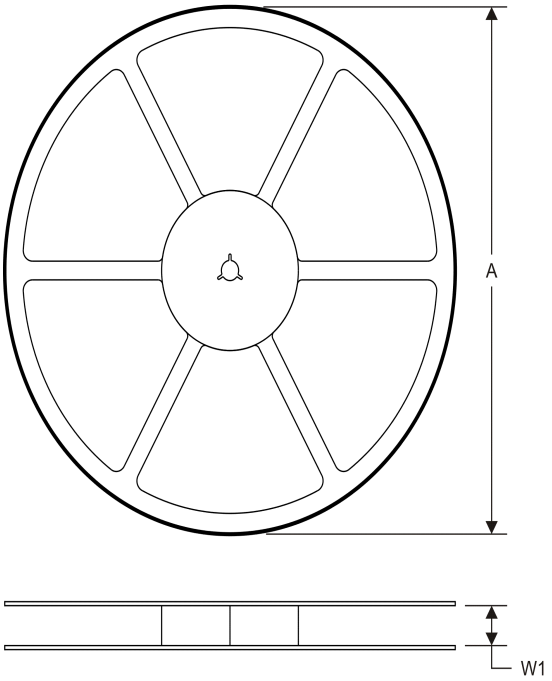
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

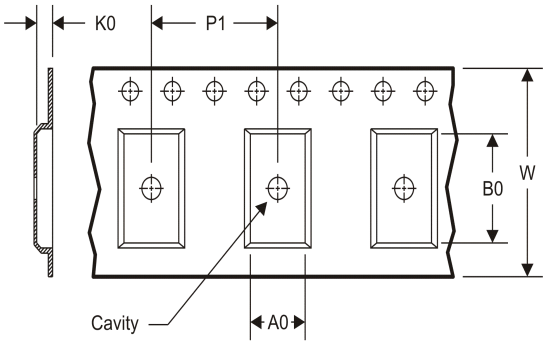
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



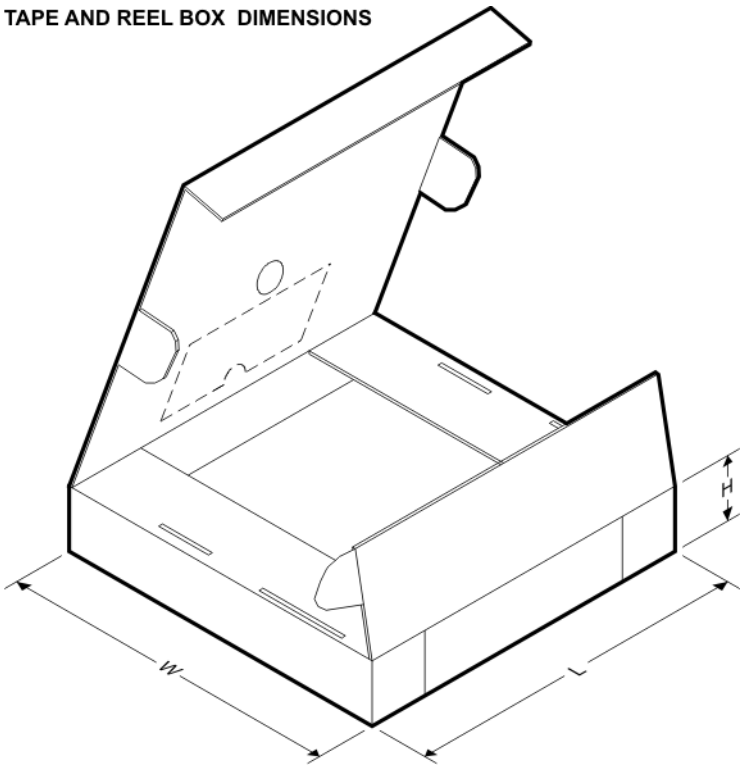
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73HD301PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPS73HD318PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPS73HD325PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

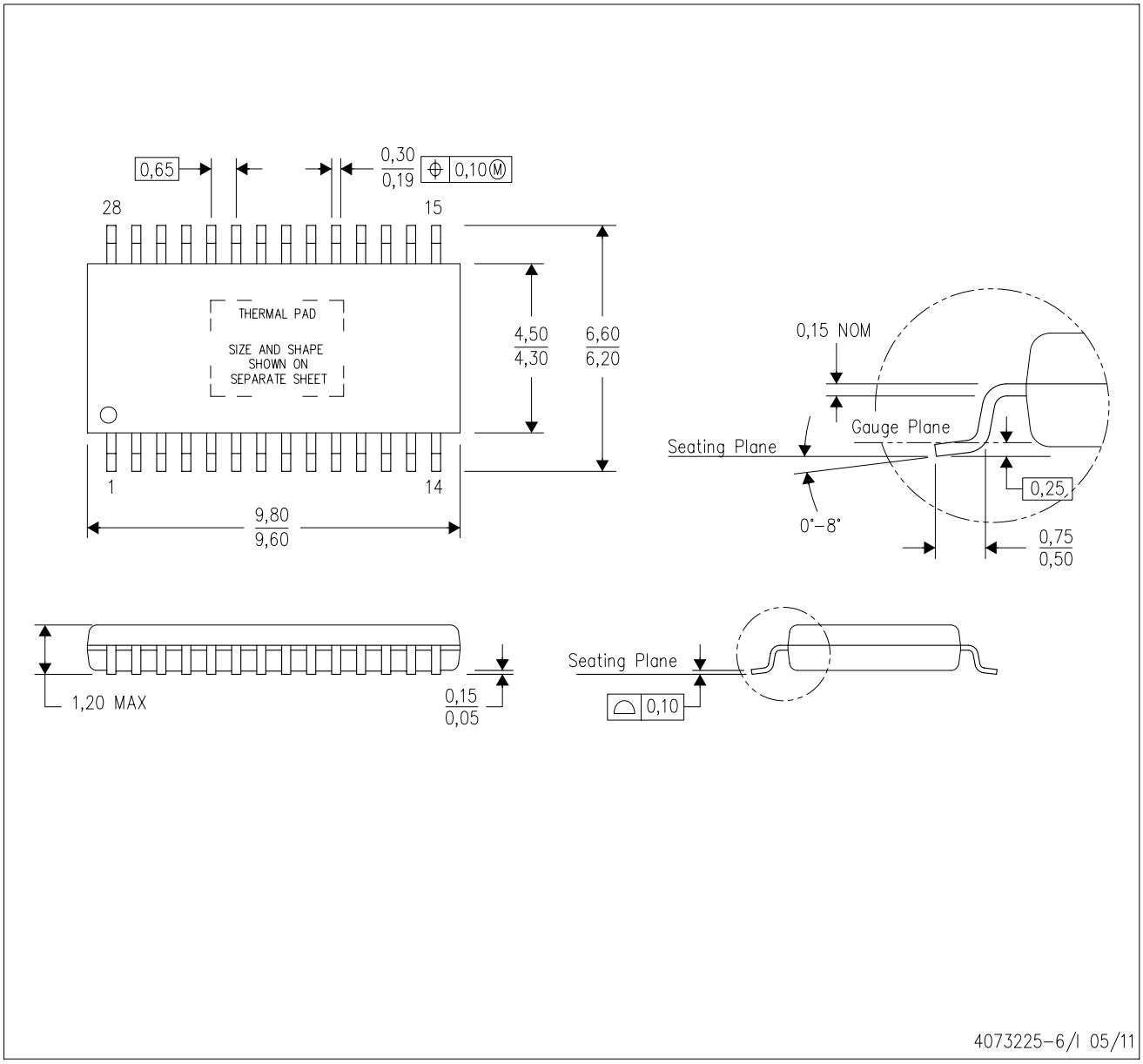
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73HD301PWPR	HTSSOP	PWP	28	2000	367.0	367.0	38.0
TPS73HD318PWPR	HTSSOP	PWP	28	2000	367.0	367.0	38.0
TPS73HD325PWPR	HTSSOP	PWP	28	2000	367.0	367.0	38.0

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

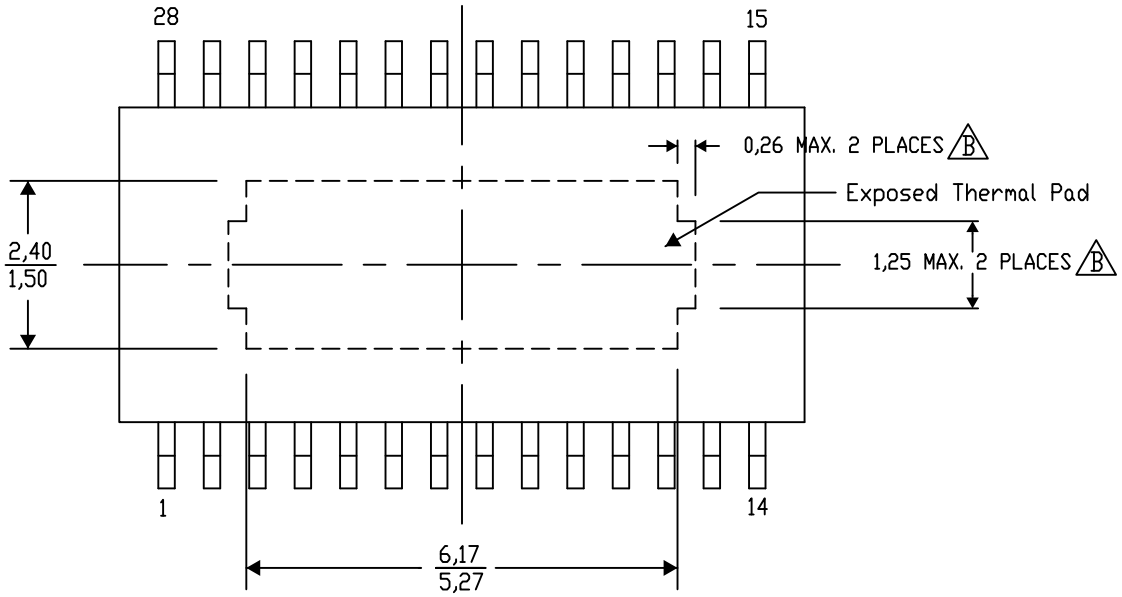
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

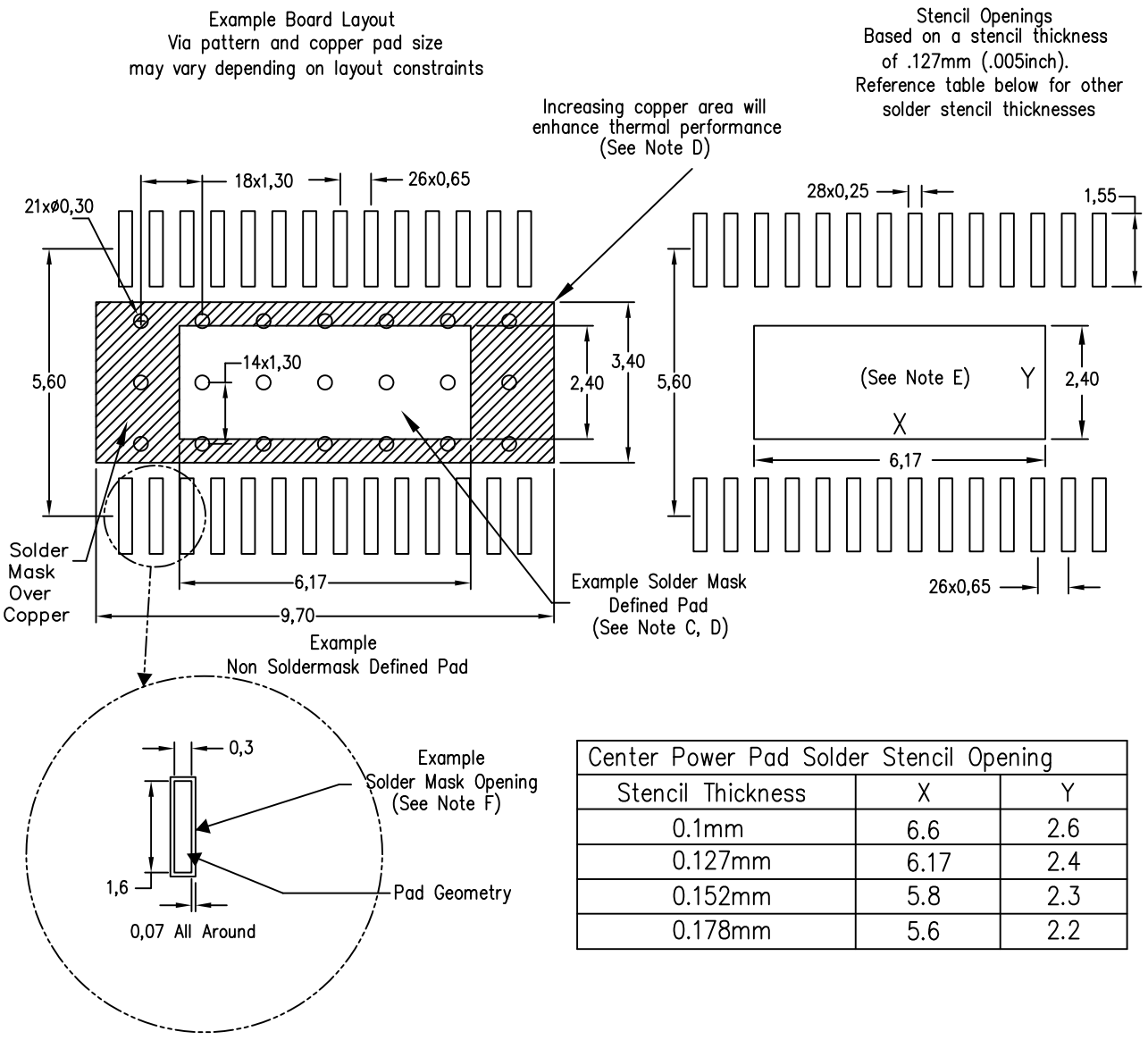
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609–19/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

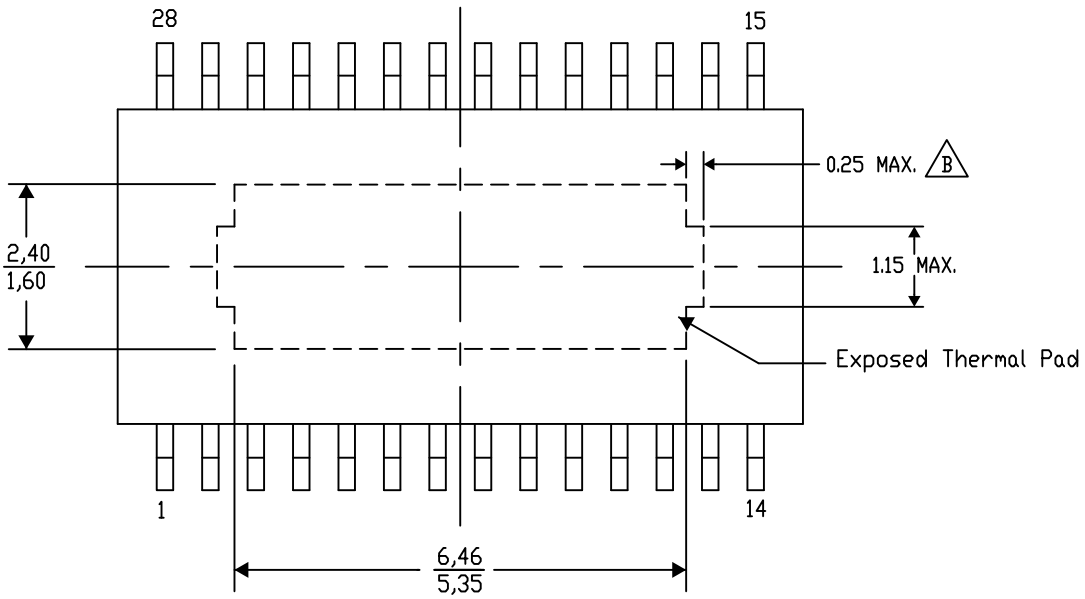
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

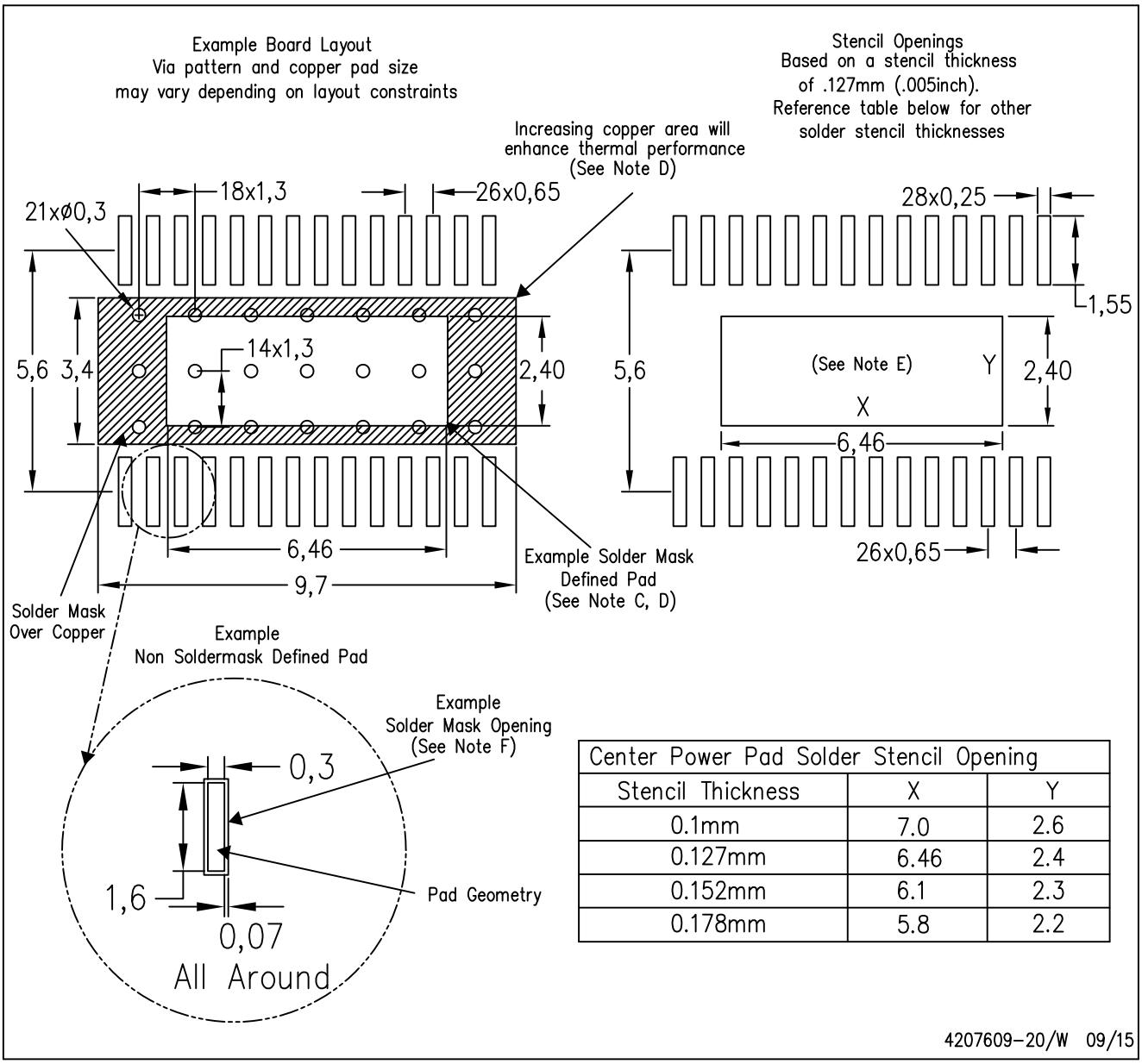
4206332–34/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.0	2.6
0.127mm	6.46	2.4
0.152mm	6.1	2.3
0.178mm	5.8	2.2

4207609–20/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
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F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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