bq2431x Overvoltage and Overcurrent Protection IC and Li+ Charger Front-End Protection IC

1 Features

- Provides Protection for Three Variables:
  - Input Overvoltage, With Rapid Response in < 1 µs
  - User-Programmable Overcurrent With Current Limiting
  - Battery Overvoltage
- 30-V Maximum Input Voltage
- Supports up to 1.5-A Input Current
- Robust Against False Triggering Due to Current Transients
- Thermal Shutdown
- Enable Input
- Status Indication – Fault Condition
- Available in Space-Saving Small 8-Pin 2 × 2 SON and 12-Pin 4 × 3 SON Packages

2 Applications

- Mobile Phones and Smart Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices
- Bluetooth™ Headsets

3 Description

The bq24314 and bq24316 devices are highly integrated circuits designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current, and the battery voltage. In case of an input overvoltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. Additionally, the IC also monitors its own die temperature and switches off if it becomes too hot. The input overcurrent threshold is user-programmable.

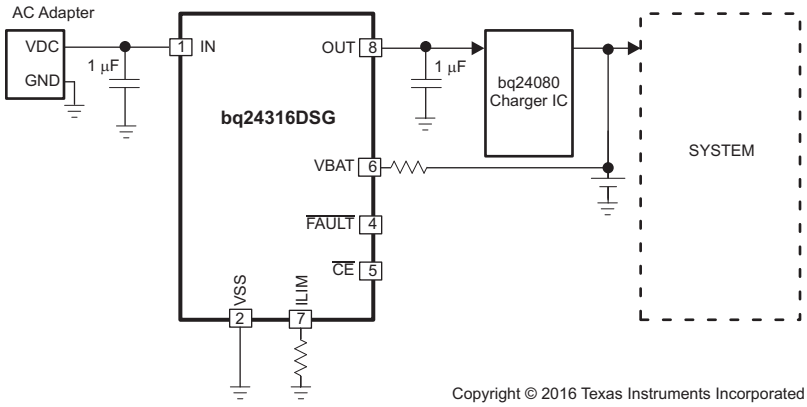
The IC can be controlled by a processor and also provides status information about fault conditions to the host.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24314 bq24316	WSON (8)	2.00 mm × 2.00 mm
	VSON (8)	3.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2007) to Revision D — **Page**

- Added *Device Information* table, *ESD Rating* table, *Thermal Information* table, *Timing Requirements* table, *Overview* section, *Feature Description*, *Device Functional Modes* section, *Application and Implementations* section, *Power Supply Recommendations* section, *Layout* section, *Device Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Replaced the *ORDERING INFORMATION* table with the *Device Information* table ... 1

Changes from Revision B (September 2007) to Revision C — **Page**

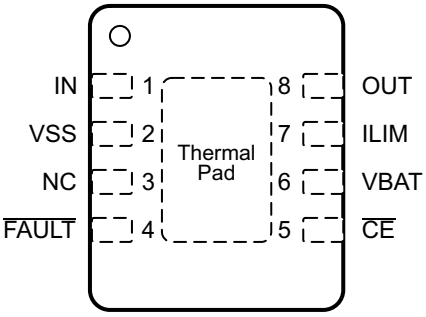
- Changed the MARKING column of the *ORDERING INFORMATION* table ... 1

Changes from Revision A (September 2007) to Revision B — **Page**

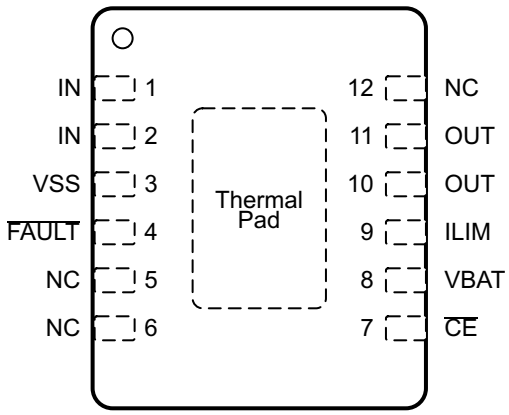
- Changed *Electrical Characteristics*: operating current typ value from 500 µA to 400 µA ... 5
- Changed *Electrical Characteristics*: bq24314 input overvoltage protection threshold min value from 5.67 V to 5.71 V. ... 5

5 Pin Configuration and Functions

DSG Package
8-Pin WSON
Top View



DSJ Package
8-Pin VSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	VSON	WSON		
$\overline{CE}$	7	5	I	Chip enable input. Active low. When $\overline{CE}$ = High, the input FET is off. Internally pulled down.
$\overline{FAULT}$	4	4	O	Open-drain output, device status. $\overline{FAULT}$ = Low indicates that the input FET Q1 has been turned off due to input overvoltage, input overcurrent, battery overvoltage, or thermal shutdown.
ILIM	9	7	I/O	Input overcurrent threshold programming. Connect a resistor to VSS to set the overcurrent threshold.
IN	1, 2	1	I	Input power, connect to external DC supply. Connect external 1-µF ceramic capacitor (minimum) to VSS. For the 12-pin (DSJ-suffix) device, ensure that pins 1 and 2 are connected together on the PCB at the device.
NC	5, 6, 12	3	—	These pins may have internal circuits used for test purposes. Do not make any external connections at these pins for normal operation.
OUT	10, 11	8	O	Output terminal to the charging system. Connect external 1-µF ceramic capacitor (minimum) to VSS.
Thermal PAD	—	—	—	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed-circuit board. Do not use the thermal pad as the primary ground input for the device. The VSS pin must be connected to ground at all times.
VBAT	8	6	I	Battery voltage sense input. Connect to pack positive terminal through a resistor.
VSS	3	2	—	Ground terminal

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN (with respect to VSS)	–0.3	30	V
	OUT (with respect to VSS)	–0.3	12	
	ILIM, $\overline{\text{FAULT}}$, $\overline{\text{CE}}$, VBAT (with respect to VSS)	–0.3	7	
Input current	IN		2	A
Output current	OUT		2	A
Output sink current	$\overline{\text{FAULT}}$		15	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	3.3	26	V
I_{IN}	Input current, IN pin		1.5	A
I_{OUT}	Output current, OUT pin		1.5	A
R_{ILIM}	OCP programming resistor	15	90	kΩ
T_J	Junction temperature	0	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		bq24314, bq24316		UNIT
		DSG (WSON)	DSJ (VSON)	
		8 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.6	49.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.9	60.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.7	24.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.3	24.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.6	11.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over junction temperature range –40°C to 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN							
UVLO	Undervoltage lockout, input power detected threshold		$\overline{CE}$ = Low, V_{IN} increasing from 0 V to 3 V	2.6	2.7	2.8	V
$V_{HYS-UVLO}$	Hysteresis on UVLO		$\overline{CE}$ = Low, V_{IN} decreasing from 3 V to 0 V	200	260	300	mV
$T_{DGL(PGOOD)}$	Deglitch time, input power detected status		$\overline{CE}$ = Low. Time measured from V_{IN} 0 V → 5 V, 1-µs rise-time, to output turning ON		8		ms
I_{DD}	Operating current		$\overline{CE}$ = Low, No load on OUT pin, V_{IN} = 5 V, R_{ILIM} = 25 kΩ		400	600	µA
I_{STDBY}	Standby current		$\overline{CE}$ = High, V_{IN} = 5 V		65	95	µA
INPUT TO OUTPUT CHARACTERISTICS							
VDO	Drop-out voltage IN to OUT		$\overline{CE}$ = Low, V_{IN} = 5 V, I_{OUT} = 1 A		170	280	mV
INPUT OVERVOLTAGE PROTECTION							
V_{OVP}	Input overvoltage protection threshold	bq24314	$\overline{CE}$ = Low, V_{IN} increasing from 5 V to 7.5 V	5.71	5.85	6	V
		bq24316		6.6	6.8	7	V
$V_{HYS-OVP}$	Hysteresis on OVP		$\overline{CE}$ = Low, V_{IN} decreasing from 7.5 V to 5 V	25	60	110	mV
INPUT OVERCURRENT PROTECTION							
I_{OCP}	Input overcurrent protection threshold range			300		1500	mA
I_{OCP}	Input overcurrent protection threshold		$\overline{CE}$ = Low, R_{ILIM} = 25 kΩ,	930	1000	1070	mA
BATTERY OVERVOLTAGE PROTECTION							
BV_{OVP}	Battery overvoltage protection threshold		$\overline{CE}$ = Low, V_{IN} > 4.4 V	4.30	4.35	4.4	V
$V_{HYS-BOVP}$	Hysteresis on BV_{OVP}		$\overline{CE}$ = Low, V_{IN} > 4.4 V	200	275	320	mV
I_{VBAT}	Input bias current on VBAT pin	DSG Package	V_{BAT} = 4.4 V, T_J = 25°C			10	nA
		DSJ Package	V_{BAT} = 4.4 V, T_J = 85°C			10	
THERMAL PROTECTION							
$T_{J(OFF)}$	Thermal shutdown temperature				140	150	°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis				20		°C
LOGIC LEVELS ON $\overline{CE}$							
V_{IL}	Low-level input voltage			0		0.4	V
V_{IH}	High-level input voltage			1.4			V
I_{IL}	Low-level input current		V_{CE} = 0 V			1	µA
I_{IH}	High-level input current		V_{CE} = 1.8 V			15	µA
LOGIC LEVELS ON $\overline{FAULT}$							
V_{OL}	Output low voltage		I_{SINK} = 5 mA			0.2	V
I_{HI-Z}	Leakage current, $\overline{FAULT}$ pin HI-Z		V_{FAULT} = 5 V			10	µA

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
IN						
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	$\overline{CE}$ = Low. Time measured from V_{IN} 0 V → 5 V, 1-µs rise-time, to output turning ON		8		ms
INPUT OVERVOLTAGE PROTECTION						
$t_{PD(OVP)}$	Input OV propagation delay(1)	$\overline{CE}$ = Low			1	µs
$t_{ON(OVP)}$	Recovery time from input overvoltage condition	$\overline{CE}$ = Low, Time measured from V_{IN} 7.5 V → 5 V, 1-µs fall-time		8		ms
INPUT OVERCURRENT PROTECTION						
$t_{BLANK(OCP)}$	Blanking time, input overcurrent detected			176		µs
$t_{REC(OCP)}$	Recovery time from input overcurrent condition			64		ms
BATTERY OVERVOLTAGE PROTECTION						
$t_{DGL(BOVP)}$	Deglitch time, battery overvoltage detected	$\overline{CE}$ = Low, V_{IN} > 4.4 V. Time measured from V_{VBAT} rising from 4.1 V to 4.4 V to $\overline{FAULT}$ going low.		176		µs

(1) Not tested in production. Specified by design.

6.7 Typical Characteristics

Test conditions (unless otherwise noted) for typical operating performance: V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, R_{ILIM} = 25 kΩ, R_{BAT} = 100 kΩ, T_A = 25°C, V_{PU} = 3.3 V (see Figure 11 for the Typical Application Circuit)

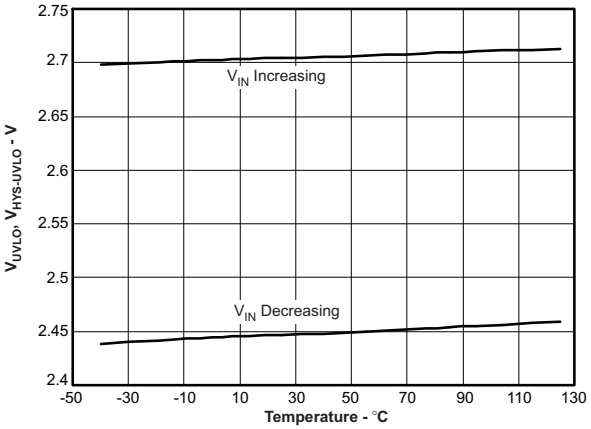


Figure 1. Undervoltage Lockout vs Free-Air Temperature

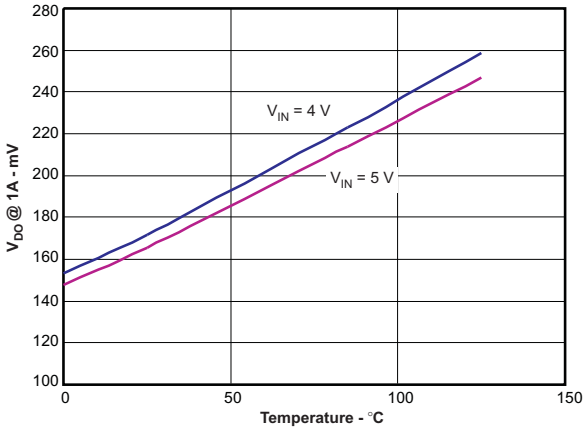


Figure 2. Dropout Voltage (IN to OUT) vs Free-Air Temperature

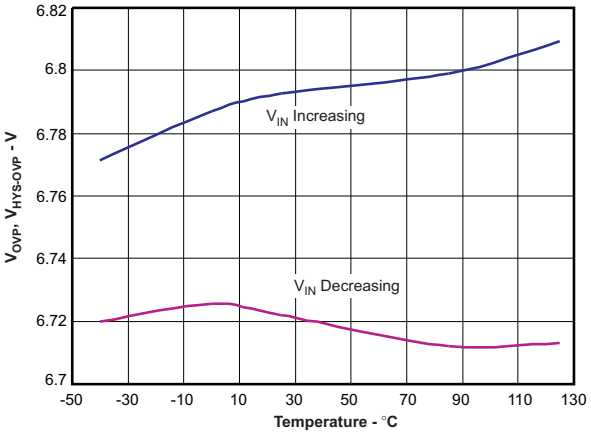


Figure 3. Overvoltage Threshold Protection (bq24316) vs Free-Air Temperature

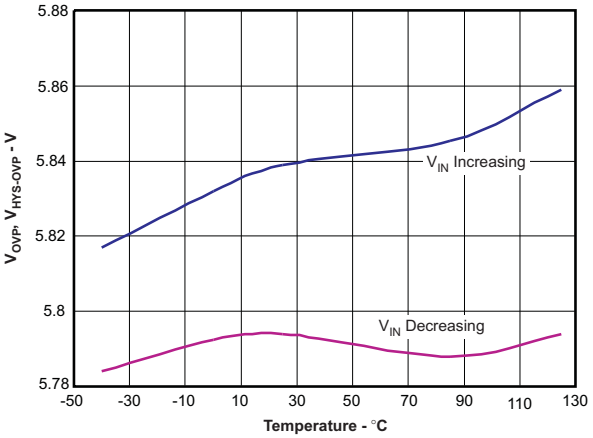


Figure 4. Overvoltage Threshold Protection (bq24314) vs Free-Air Temperature

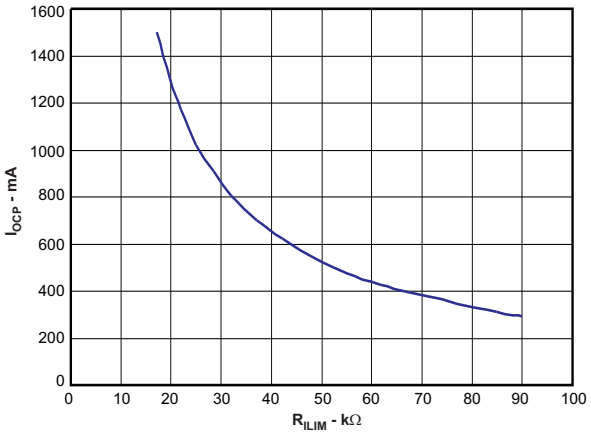


Figure 5. Input Overcurrent Protection vs ILIM Resistance

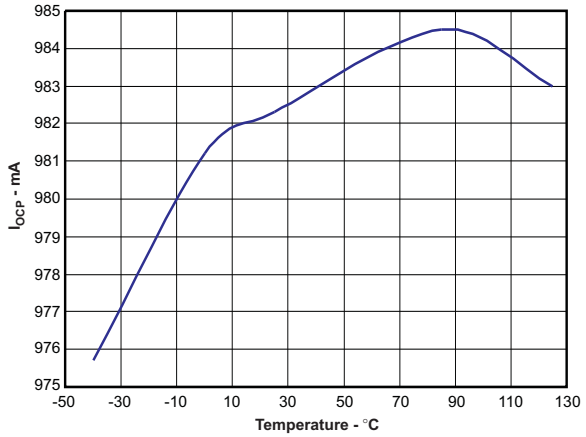


Figure 6. Input Overcurrent Protection vs Free-Air Temperature

Typical Characteristics (continued)

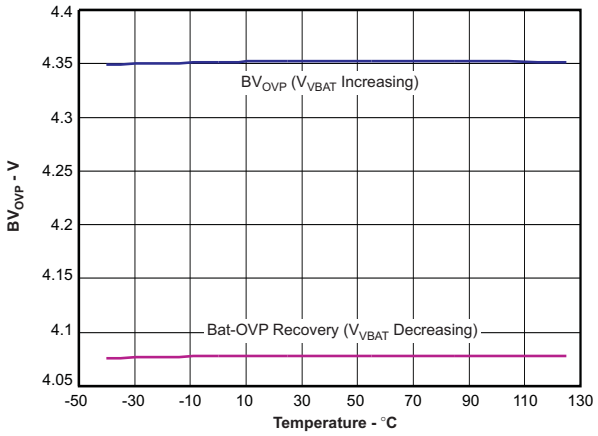


Figure 7. Battery Overvoltage Protection vs Free-Air Temperature

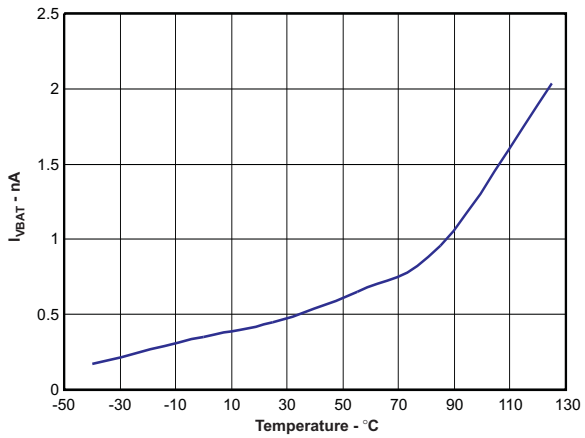


Figure 8. Leakage Current (VBAT Pin) vs Free-Air Temperature

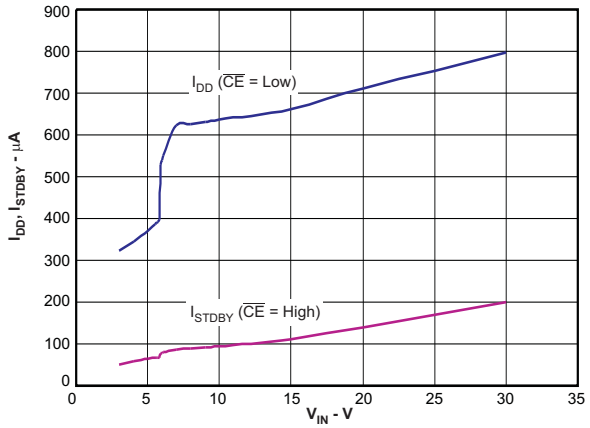


Figure 9. Supply Current (bq24314) vs Input Voltage

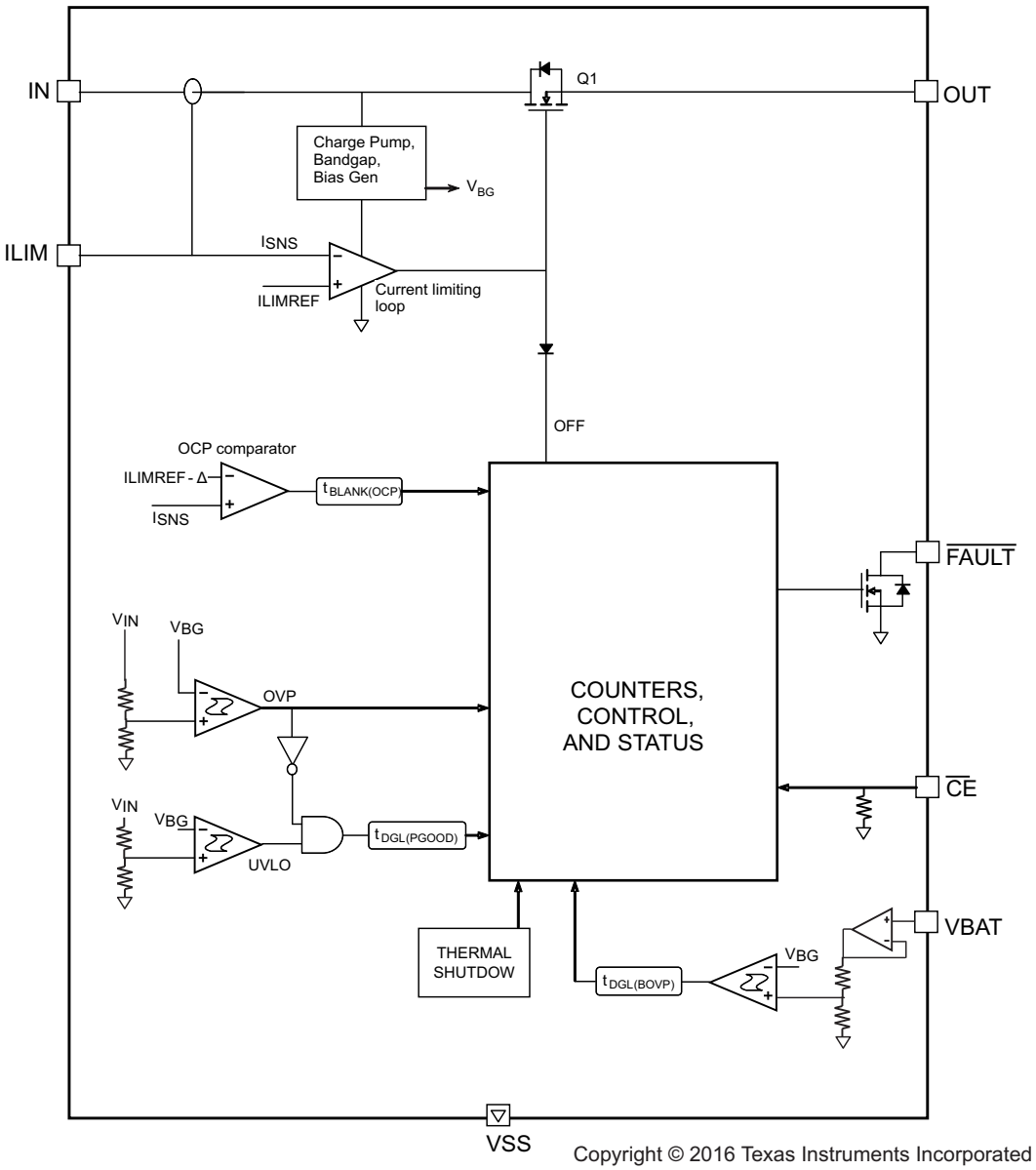
7 Detailed Description

7.1 Overview

The bq24314 and bq24316 devices monitor the input voltage, input current, and the battery voltage to protect the charging system of a Li-Ion battery. The protection features can be enabled through the /CE pin.

When enabled, the system is protected against input overvoltage by turning off an internal switch, immediately removing power from the charging circuit. The system is protected against an overcurrent condition by limiting the input current to a safe value for a blanking duration before disconnecting the input from the output by turning the switch off. The overcurrent threshold is user-programmable. Additionally, the device also monitors its own die temperature and switches off if it becomes too hot.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Down

The device remains in power-down mode when the input voltage at the IN pin is below the undervoltage threshold V_{UVLO}. The FET Q1 connected between IN and OUT pins is off, and the status output, $\overline{FAULT}$, is set to Hi-Z.

7.3.2 Power-On Reset

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. All internal counters and other circuit blocks are reset. The IC then waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are safe, FET Q1 is turned ON. The IC has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). Figure 12 shows the power-up behavior of the device. Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, instead it will go into protection mode and indicate a fault on the $\overline{FAULT}$ pin, as shown in Figure 13.

7.3.3 Operation

The device continuously monitors the input voltage, the input current, and the battery voltage as described in detail in the following sections.

7.3.3.1 Input Overvoltage Protection

If the input voltage rises above V_{OVP}, the internal FET Q1 is turned off, removing power from the circuit. As shown in Figure 14 to Figure 17, the response is very rapid, with the FET turning off in less than a microsecond. The $\overline{FAULT}$ pin is driven low. When the input voltage returns below $V_{OVP} – V_{HYS-OVP}$ (but is still above V_{UVLO}), the FET Q1 is turned on again after a deglitch time of $t_{ON(OVP)}$ to ensure that the input supply has stabilized. Figure 18 shows the recovery from input OVP.

7.3.3.2 Input Overcurrent Protection

The overcurrent threshold is programmed by a resistor R_{ILIM} connected from the ILIM pin to VSS. Figure 5 shows the OCP threshold as a function of R_{ILIM}, and may be approximated by Equation 1:

$$I_{OCP} = 25 \div R_{ILIM} \quad (1)$$

where

- current is in A
- and resistance is in kΩ

If the load current tries to exceed the I_{OCP} threshold, the device limits the current for a blanking duration of $t_{BLANK(OCP)}$. If the load current returns to less than I_{OCP} before $t_{BLANK(OCP)}$ times out, the device continues to operate. However, if the overcurrent situation persists for $t_{BLANK(OCP)}$, the FET Q1 is turned off for a duration of $t_{REC(OCP)}$, and the $\overline{FAULT}$ pin is driven low. The FET is then turned on again after $t_{REC(OCP)}$ and the current is monitored all over again. Each time an OCP fault occurs, an internal counter is incremented. If 15 OCP faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the $\overline{CE}$ pin. Figure 19 to Figure 21 show what happens in an overcurrent fault.

To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is turned off slowly, resulting in a *soft-stop*, as shown in Figure 21.

7.3.3.3 Battery Overvoltage Protection

The battery overvoltage threshold BV_{OVP} is internally set to 4.35 V. If the battery voltage exceeds the BV_{OVP} threshold, the FET Q1 is turned off, and the $\overline{FAULT}$ pin is driven low. The FET is turned back on once the battery voltage drops to $BV_{OVP} – V_{HYS-BOVP}$ (see Figure 22 and Figure 23). Each time a battery overvoltage fault occurs, an internal counter is incremented. If 15 such faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the $\overline{CE}$ pin. In the case of a battery overvoltage fault, Q1 is switched OFF gradually (see Figure 22).

Feature Description (continued)

7.3.3.4 Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the FET Q1 is turned off, and the $\overline{FAULT}$ pin is driven low. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

7.3.3.5 Enable Function

The IC has an enable pin which can be used to enable or disable the device. When the $\overline{CE}$ pin is driven high, the internal FET is turned off. When the $\overline{CE}$ pin is low, the FET is turned on if other conditions are safe. The OCP counter and the Bat-OVP counter are both reset when the device is disabled and re-enabled. The $\overline{CE}$ pin has an internal pulldown resistor and can be left floating.

NOTE

The $\overline{FAULT}$ pin functionality is also disabled when the $\overline{CE}$ pin is high.

7.3.3.6 Fault Indication

The $\overline{FAULT}$ pin is an active-low open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting $\overline{CE}$ high. With $\overline{CE}$ low, the $\overline{FAULT}$ pin goes low whenever any of these events occurs:

- Input overvoltage
- Input overcurrent
- Battery overvoltage
- IC Overtemperature

Feature Description (continued)

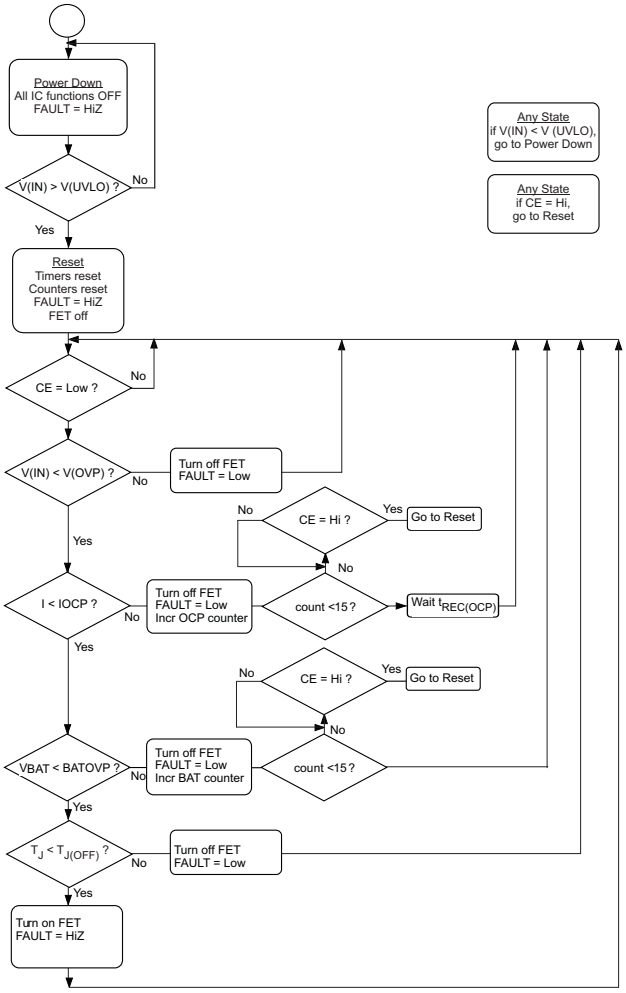


Figure 10. Flow Diagram

7.4 Device Functional Modes

7.4.1 OPERATION Mode

The bq2431x device continuously monitors the input voltage, the input current, and the battery voltage. As long as the input voltage is less than VOVP, the output voltage tracks the input voltage (less the drop caused by RDSON of Q1). During fault conditions, the internal FET is turned off and the output is isolated from the input source.

7.4.2 POWER-DOWN Mode

The device remains in POWER-DOWN mode when the input voltage at the IN pin is below the undervoltage lock-out threshold, VUVLO. The FET Q1 (see *Functional Block Diagram*) connected between IN and OUT pins is off. See Figure 10.

Device Functional Modes (continued)

7.4.3 POWER-ON RESET Mode

The device resets all internal timers when the input voltage at the IN pin exceeds the UVLO threshold. The gate driver for the external P-FET is enabled. The device then waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are safe, FET Q1 is turned ON. The device has a soft-start feature to control the inrush current. This soft-start minimizes voltage ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). Figure 12 shows the power-up behavior of the device. Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, as shown in Figure 13.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq2431x device protects against overvoltage, overcurrent, and battery overvoltage events that occur due to faulty adapter or other input sources. If any of these faults occur, the bq24308 device isolates the downstream devices from the input source.

8.2 Typical Application

V_{OVP} = 6.8 V, I_{OCP} = 1000 mA, BV_{OVP} = 4.35 V (Terminal numbers shown are for the 2 × 2 DSG package)

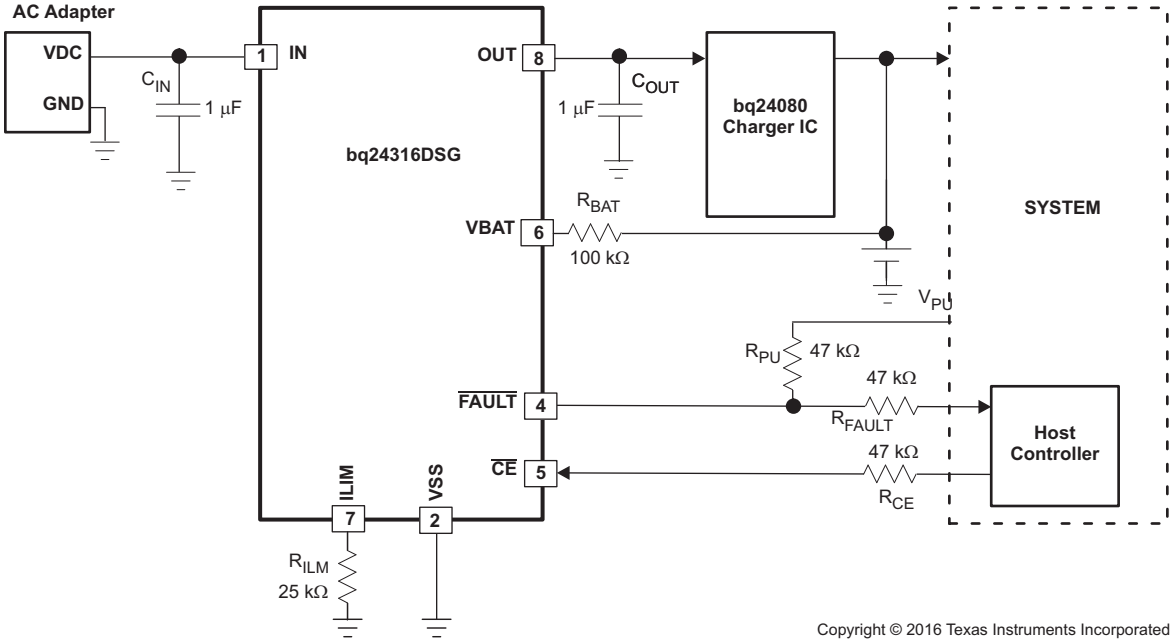


Figure 11. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters shown in Table 1.

Table 1. Design Parameters

PARAMETER	VALUE
Supply voltage	5 V
INILIM	1 A

8.2.2 Detailed Design Procedure

8.2.2.1 Selection of R_{BAT}

TI strongly recommends that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30 V, and applying 30 V to the battery in case of the failure of the bq2431x can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in case of a failure of the IC. In the interests of safety, R_{BAT} should have a very high value. The problem with a large R_{BAT} is that the voltage drop across this resistor because of the VBAT bias current I_{VBAT} causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.35-V BV_{OVP} threshold.

Choosing R_{BAT} in the range 100 kΩ to 470 kΩ is a good compromise. In the case of an IC failure, with R_{BAT} equal to 100 kΩ, the maximum current flowing into the battery would be (30 V – 3 V) ÷ 100 kΩ = 246 µA, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 100 kΩ would result in a worst-case voltage drop of $R_{BAT} \times I_{VBAT}$ = 1mV. This is negligible to compared to the internal tolerance of 50 mV on BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin must be connected to VSS.

8.2.2.2 Selection of R_{CE}, R_{FAULT}, and R_{PU}

The $\overline{CE}$ pin can be used to enable and disable the IC. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left unconnected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As in the case of the VBAT pin, the $\overline{CE}$ pin must be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor must be greater than V_{IH} of the bq2431× $\overline{CE}$ pin. The drop across the resistor is given by $R_{CE} \times I_{IH}$.

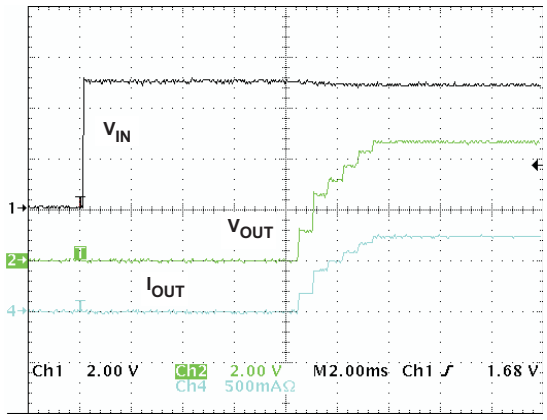
The $\overline{FAULT}$ pin is an open-drain output that goes low during OV, OC, battery-OV, and OT events. If the application does not require monitoring of the $\overline{FAULT}$ pin, it can be left unconnected. But if the $\overline{FAULT}$ pin has to be monitored, it must be pulled high externally through R_{PU}, and connected to the host through R_{FAULT}. R_{FAULT} prevents damage to the host controller if the bq2431x fails. The resistors should be of high value, in practice values between 22 kΩ and 100 kΩ should be sufficient.

8.2.2.3 Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in Figure 11 is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. TI strongly recommends that a ceramic capacitor of at least 1 µF be used at the input of the device. It must be located in close proximity to the IN pin.

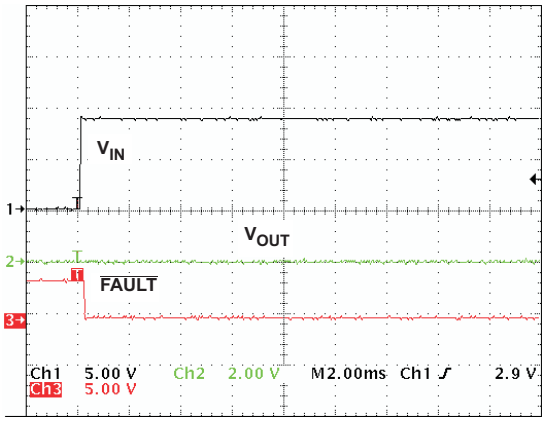
C_{OUT} in Figure 11 is also important: If a very fast (< 1-µs rise time) overvoltage transient occurs at the input, the current that charges C_{OUT} causes the current-limiting loop of the device to kick in, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection. C_{OUT} must also be a ceramic capacitor of at least 1 µF, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

8.2.3 Application Curves



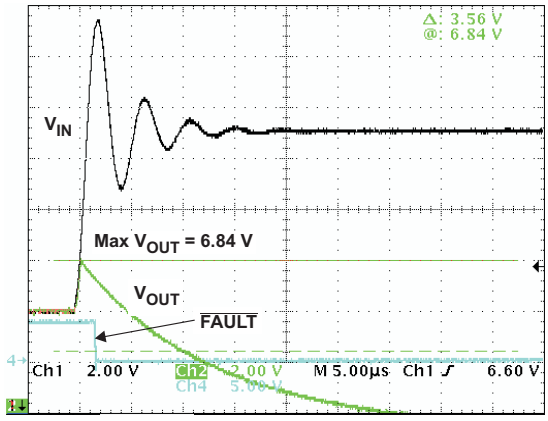
R_{OUT} = 6.6 Ω

Figure 12. Normal Power-On Showing Soft-Start



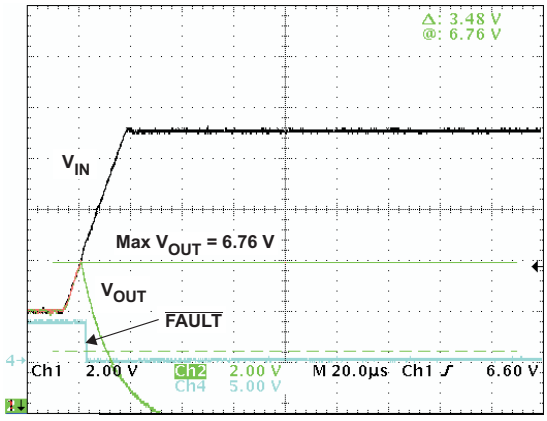
V_{IN} = 0 V to 9 V t_r = 50 µs

Figure 13. OVP at Power-On



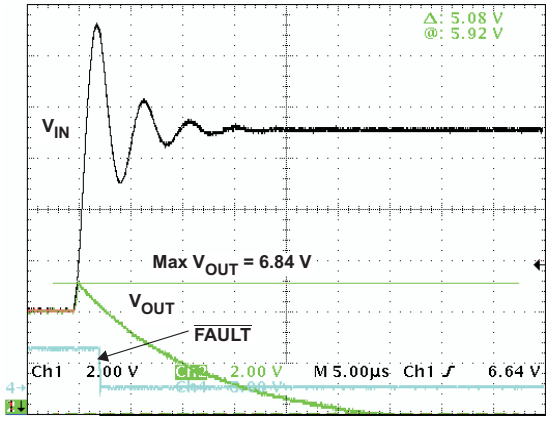
V_{IN} = 5 V to 12 V t_r = 1 µs

Figure 14. bq24316 OVP Response for Input Step



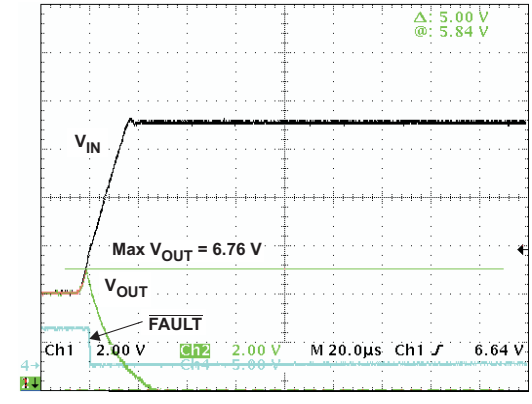
V_{IN} = 5 V to 12 V t_r = 20 µs

Figure 15. bq24316 OVP Response for Input Step



V_{IN} = 5 V to 12 V t_r = 1 µs

Figure 16. bq24314 OVP Response for Input Step



V_{IN} = 5 V to 12 V t_r = 20 µs

Figure 17. bq24314 OVP Response for Input Step

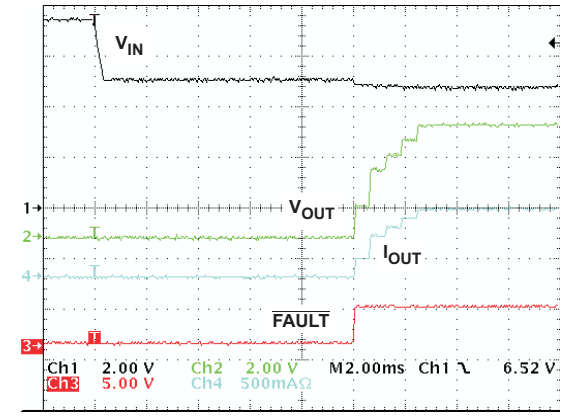


Figure 18. Recovery from OVP

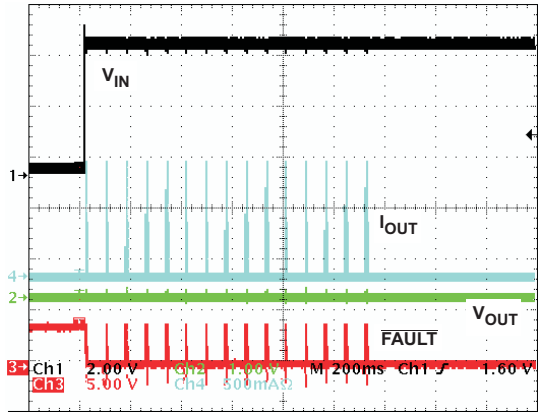


Figure 19. OCP, Powering Up into a Short Circuit on OUT Pin, OCP Counter Counts to 15 Before Switching OFF the Device

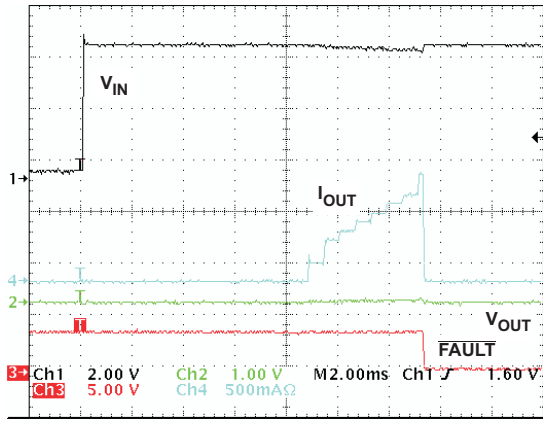


Figure 20. OCP, Zoom-in on the First Cycle of Figure 19

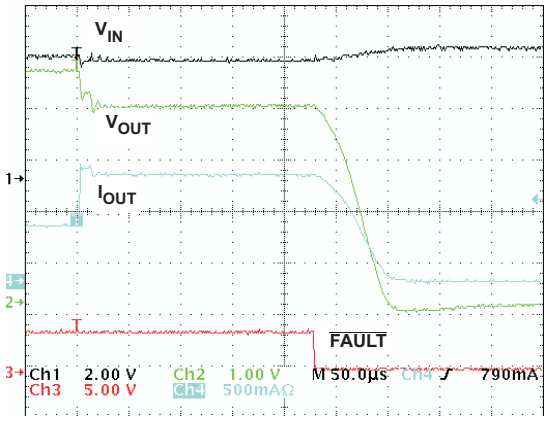


Figure 21. OCP, R_{OUT} Switches from 6.6 Ω to 3.3 Ω, Shows Current Limiting and Soft-Stop

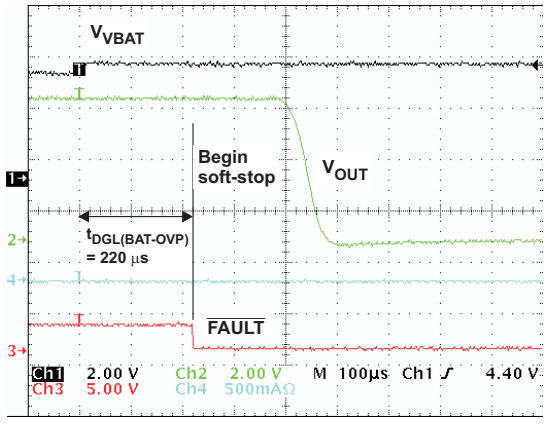


Figure 22. BAT-OVP, V_{VBAT} Steps from 4.2 V to 4.4 V, Shows $t_{DGL(BAT-OVP)}$ and Soft-Stop

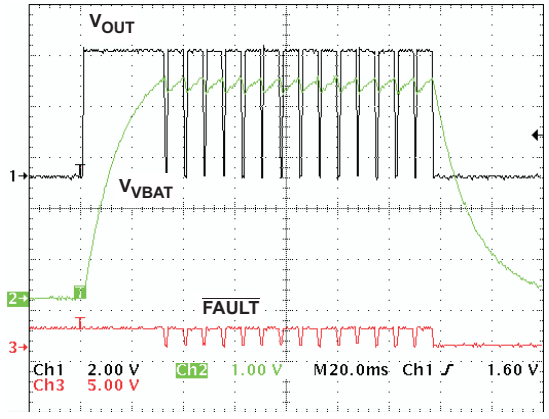


Figure 23. BAT-OVP, V_{VBAT} Cycles Between 4.1 V and 4.4 V, Shows BAT-OVP Counter

9 Power Supply Recommendations

9.1 Powering Accessories

In some applications, the equipment that the protection IC resides in may be required to provide power to an accessory (for example, a cellphone may power a headset or an external memory card) through the same connector pins that are used by the adapter for charging. Figure 24 and Figure 25 illustrate typical charging and accessory-powering scenarios:

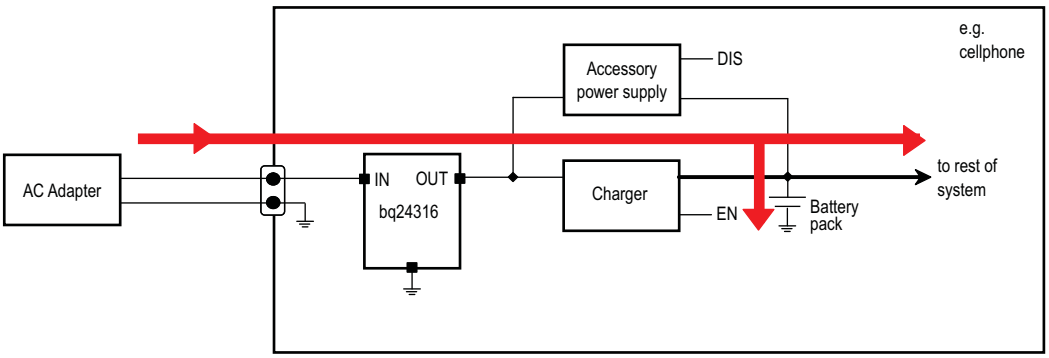


Figure 24. Charging – the Red Arrows Show the Direction of Current Flow

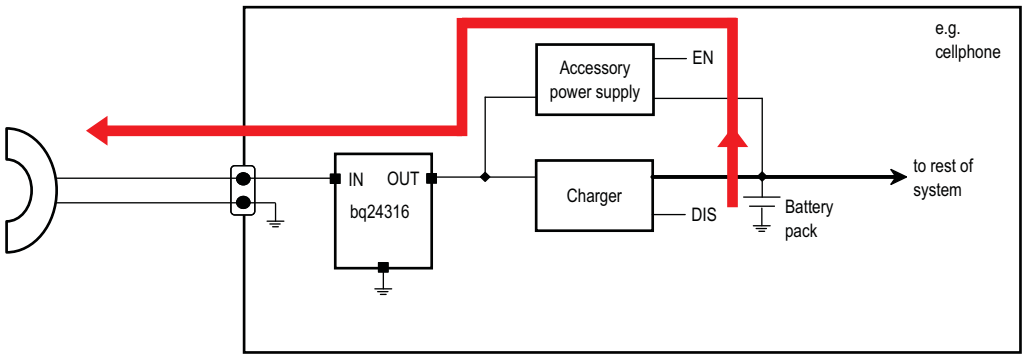


Figure 25. Powering an Accessory – the Red Arrows Show the Direction of Current Flow

In the second case, when power is being delivered to an accessory, the bq24314 and bq24316 devices are required to support current flow from the OUT pin to the IN pin.

If $V_{OUT} > V_{UVLO} + 0.7$ V, FET Q1 is turned on, and the reverse current does not flow through the diode but through Q1 (see Figure 26). Q1 will then remain ON as long as $V_{OUT} > V_{UVLO} – V_{HYS-UVLO} + R_{DS}ON \times I_{ACCESSORY}$. Within this voltage range, the reverse current capability is the same as the forward capability, 1.5 A.

NOTE

There is no overcurrent protection in this direction.

Powering Accessories (continued)

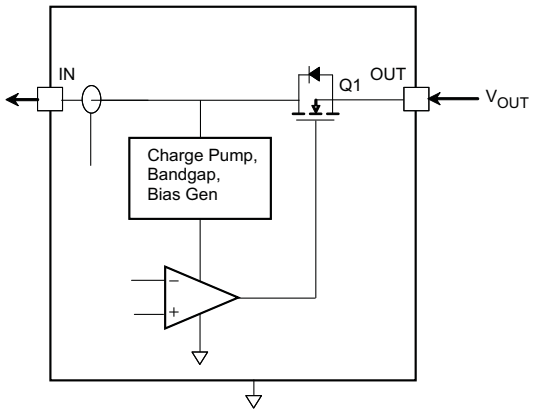


Figure 26. Powering an Accessory – Internal Power Path

10 Layout

10.1 Layout Guidelines

- This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for high voltages.
- The device uses SON packages with a PowerPAD™. For good thermal performance, the PowerPAD must be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the IC. This copper pad must be connected to the ground plane with an array of thermal vias.
- C_{IN} and C_{OUT} must be located close to the IC. Other components like R_{ILIM} and R_{BAT} should also be located close to the IC.

10.2 Layout Example

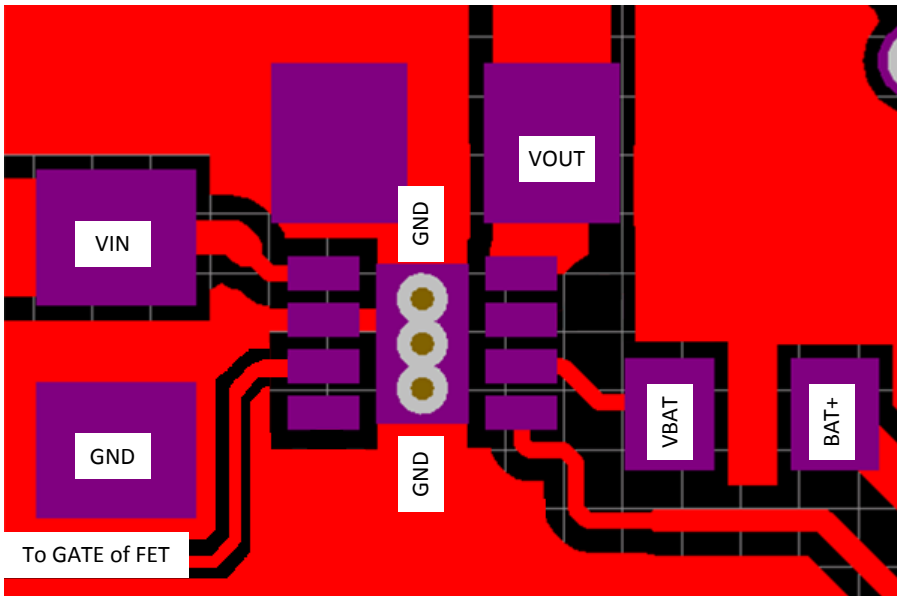


Figure 27. Recommended Layout

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq24314	Click here	Click here	Click here	Click here	Click here
bq24316	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
Bluetooth is a trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24314DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBV	Samples
BQ24314DSGRG4	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBV	Samples
BQ24314DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBV	Samples
BQ24314DSJR	ACTIVE	VSON	DSJ	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBX	Samples
BQ24314DSJT	ACTIVE	VSON	DSJ	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBX	Samples
BQ24316DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBW	Samples
BQ24316DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBW	Samples
BQ24316DSGTG4	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBW	Samples
BQ24316DSJR	ACTIVE	VSON	DSJ	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZC	Samples
BQ24316DSJT	ACTIVE	VSON	DSJ	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

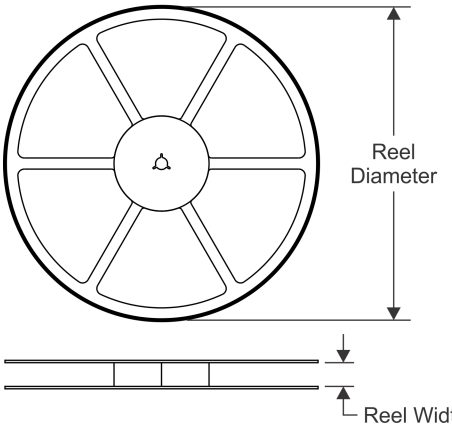
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

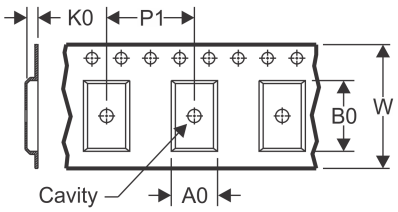
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

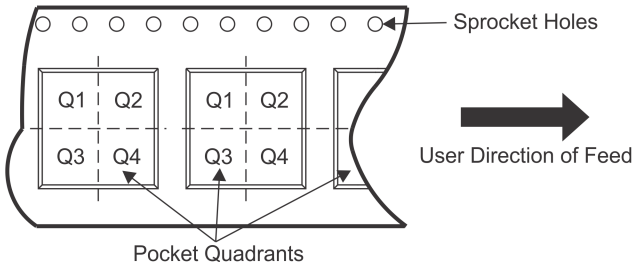


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

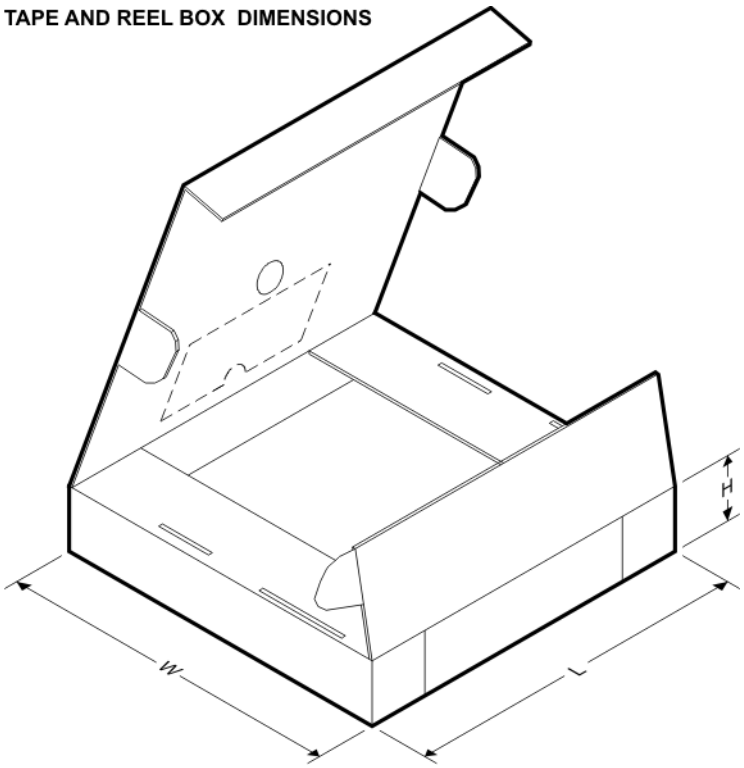
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24314DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24314DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24314DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
BQ24314DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
BQ24314DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24314DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24314DSJR	VSON	DSJ	12	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
BQ24314DSJT	VSON	DSJ	12	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
BQ24316DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
BQ24316DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24316DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
BQ24316DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24316DSJR	VSON	DSJ	12	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
BQ24316DSJT	VSON	DSJ	12	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1

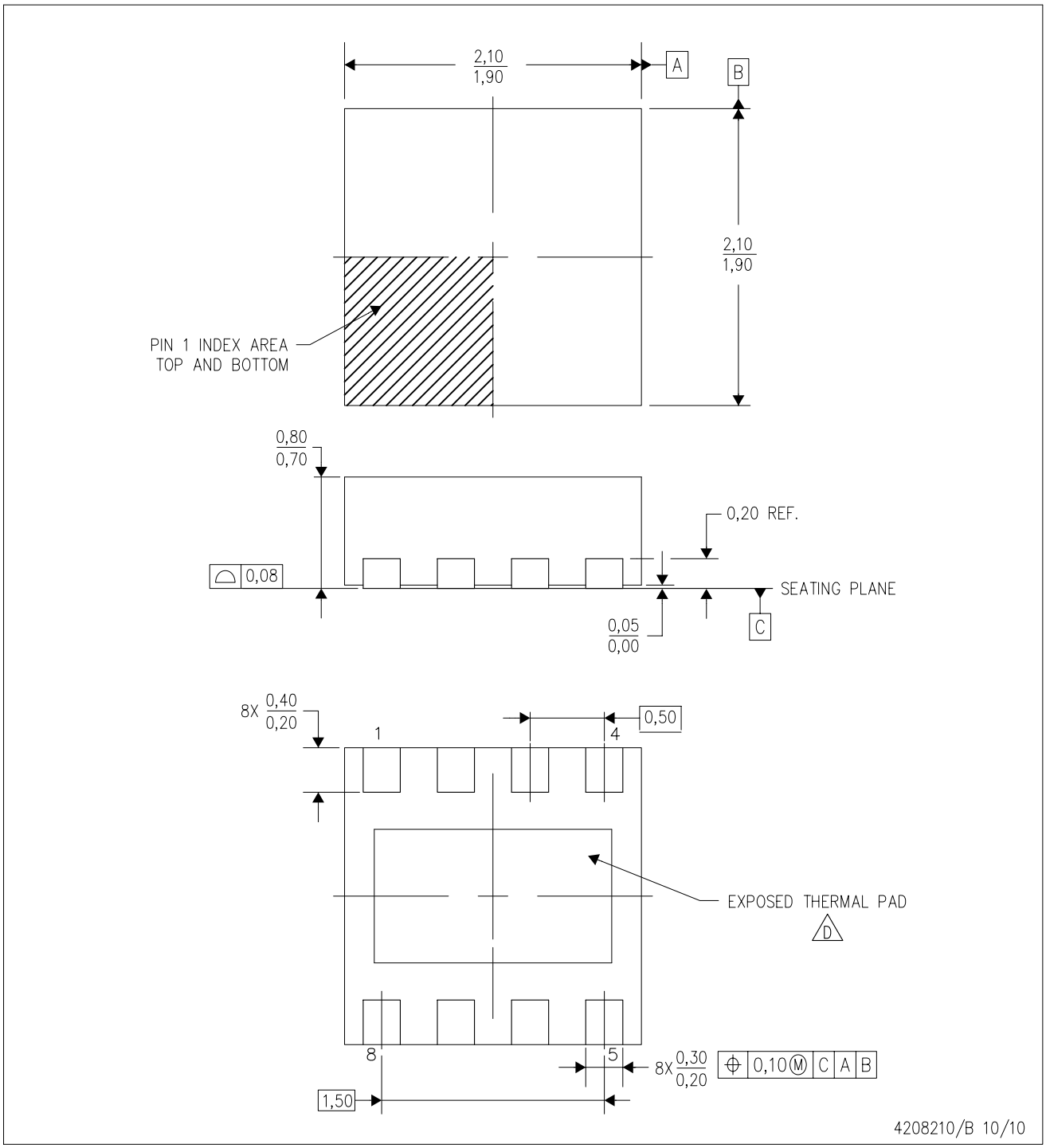
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24314DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
BQ24314DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ24314DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
BQ24314DSGT	WSON	DSG	8	250	205.0	200.0	33.0
BQ24314DSGT	WSON	DSG	8	250	195.0	200.0	45.0
BQ24314DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ24314DSJR	VSON	DSJ	12	3000	367.0	367.0	35.0
BQ24314DSJT	VSON	DSJ	12	250	210.0	185.0	35.0
BQ24316DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
BQ24316DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
BQ24316DSGT	WSON	DSG	8	250	205.0	200.0	33.0
BQ24316DSGT	WSON	DSG	8	250	195.0	200.0	45.0
BQ24316DSJR	VSON	DSJ	12	3000	367.0	367.0	35.0
BQ24316DSJT	VSON	DSJ	12	250	210.0	185.0	35.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

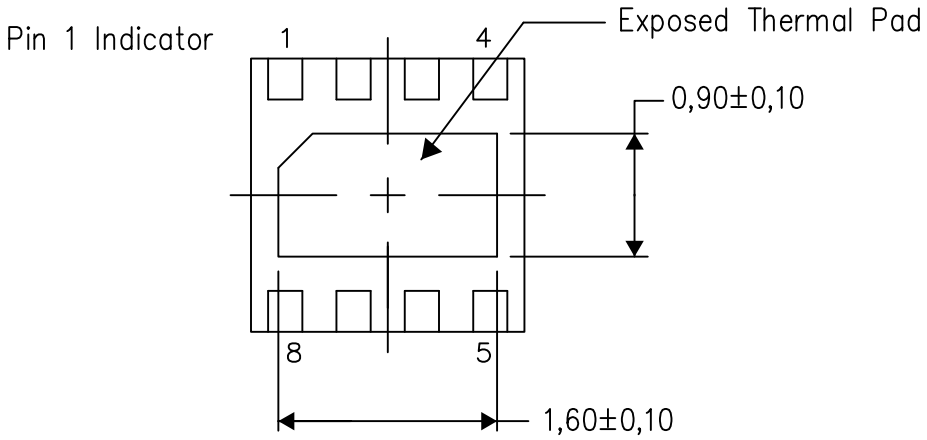
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



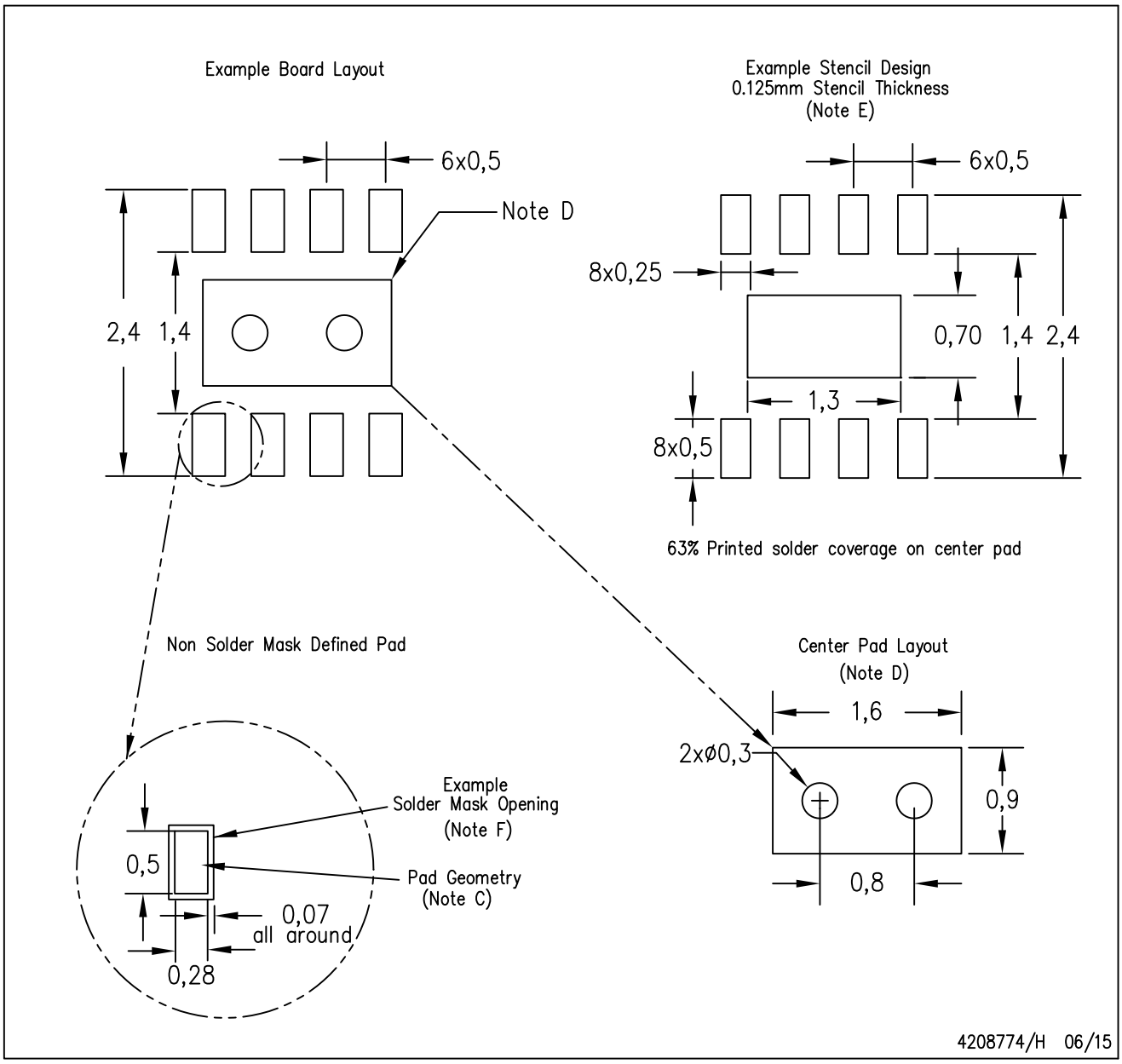
Bottom View

Exposed Thermal Pad Dimensions

4208347/I 06/15

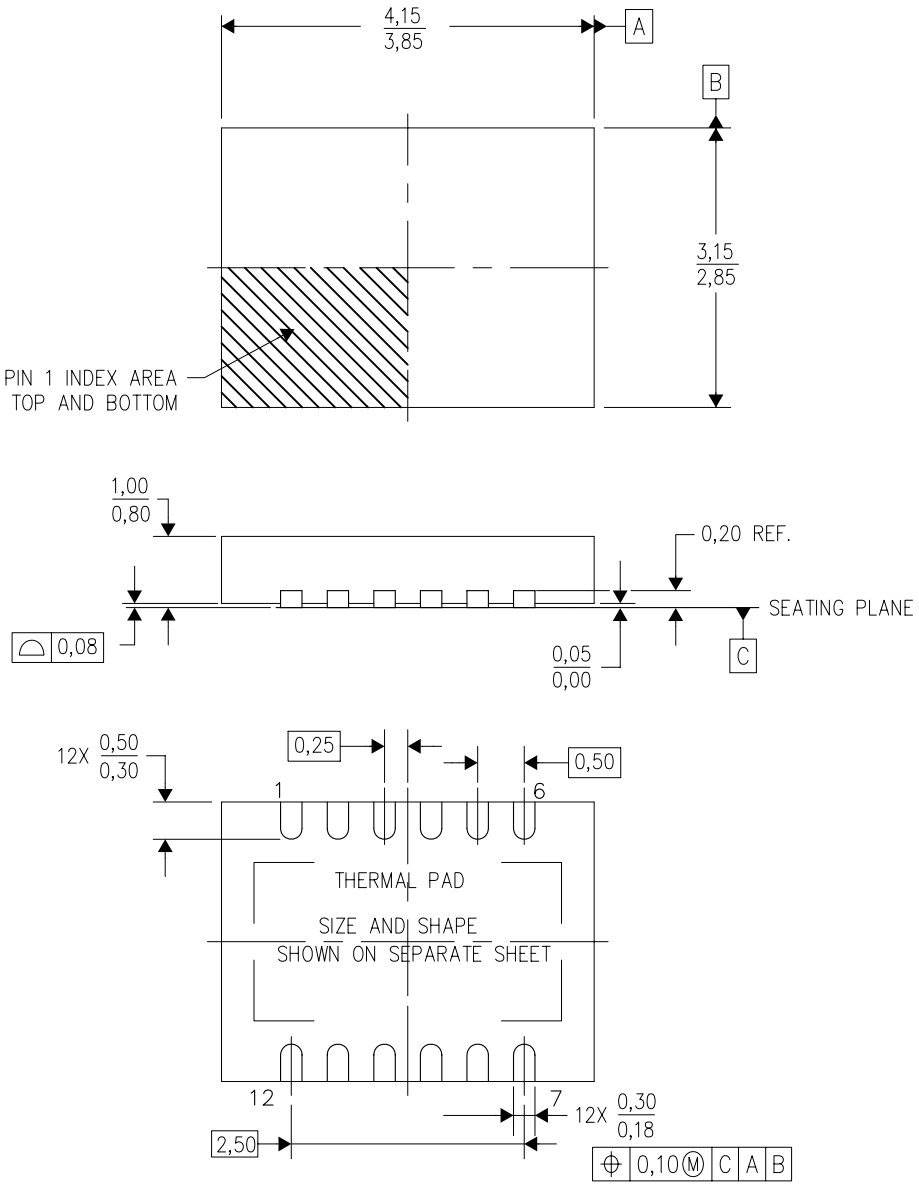
NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

DSJ (R–PVSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



4208212-2/C 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–229.

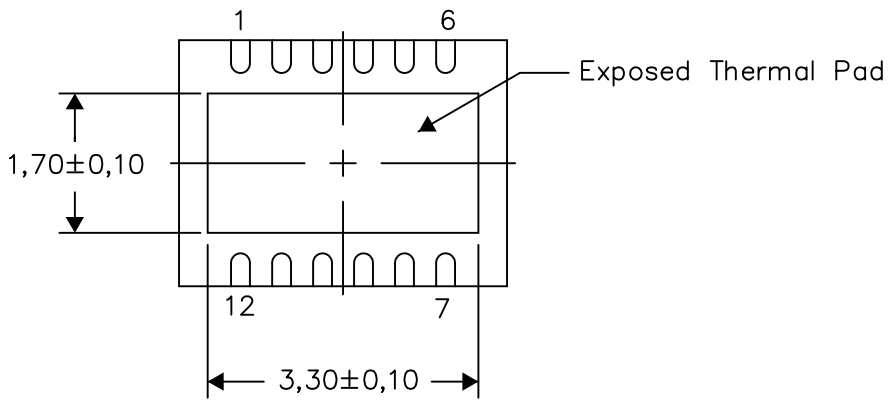
DSJ (R–PVSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



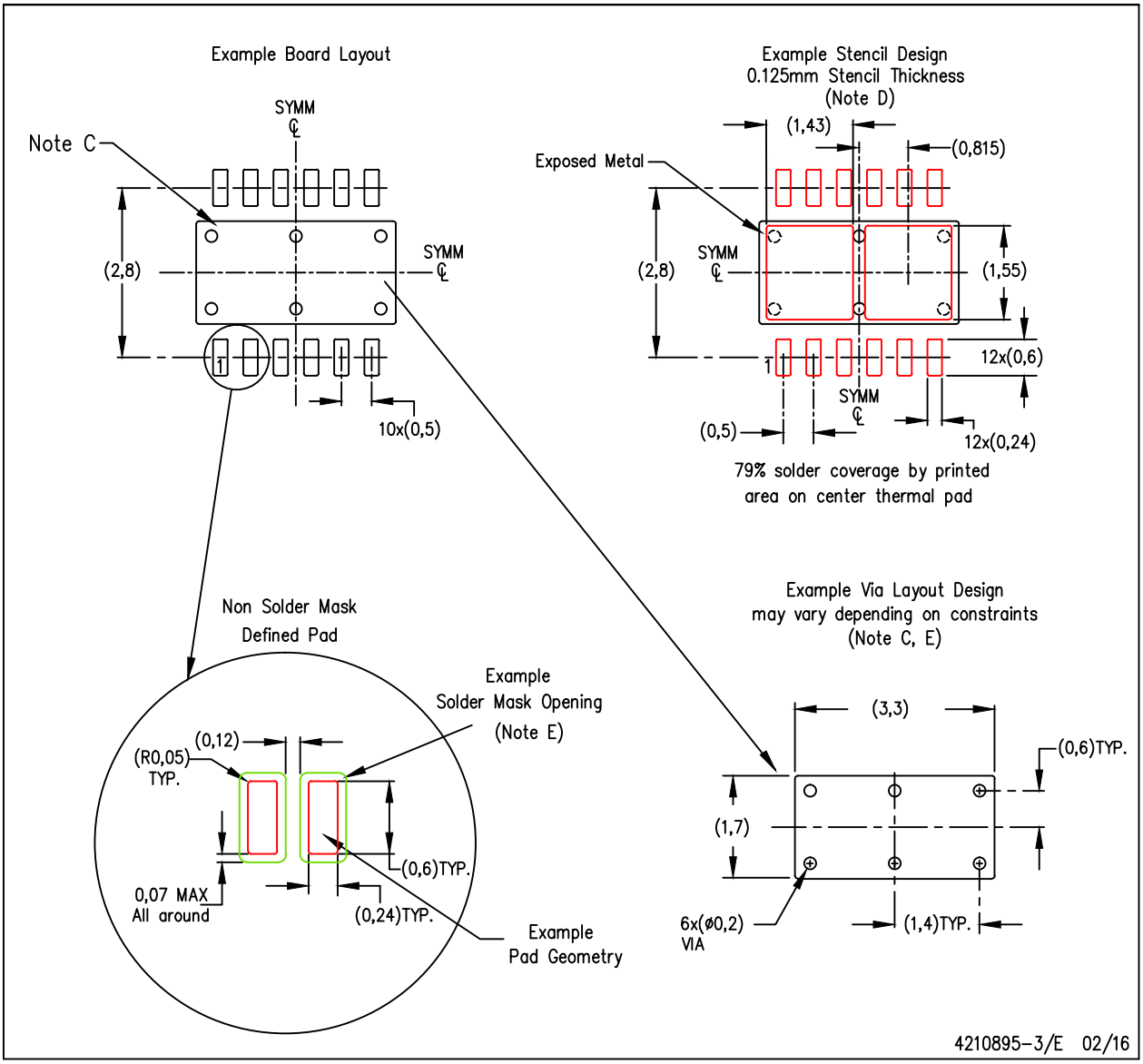
Bottom View

Exposed Thermal Pad Dimensions

4208549–2/G 04/15

NOTE: All linear dimensions are in millimeters

DSJ (R–PVSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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