CSD87384M Synchronous Buck NexFET™ Power Block II

1 Features

- Half-Bridge Power Block
- 90.5% System Efficiency at 25 A
- Up to 30 A Operation
- High Density – 5 mm x 3.5 mm LGA Footprint
- Double-Side Cooling Capability
- Ultra-Low Profile – 0.48 mm Max
- Optimized for 5 V Gate Drive
- Low Switching Losses
- Ultra-Low Inductance Package
- RoHS Compliant
- Halogen Free
- Pb-Free

2 Applications

- Synchronous Buck Converters
  - High Frequency Applications
  - High Current, Low Duty Cycle Applications
- Multiphase Synchronous Buck Converters
- POL DC-DC Converters

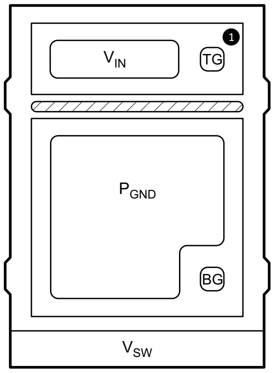
3 Description

The CSD87384M NexFET™ Power Block II is a highly optimized design for synchronous buck applications offering high current and high efficiency capability in a small 5.0 mm × 3.5 mm outline. Optimized for 5 V gate drive applications, this product offers an efficient and flexible solution capable of providing a high density power supply when paired with any 5 V gate drive from an external controller or driver.

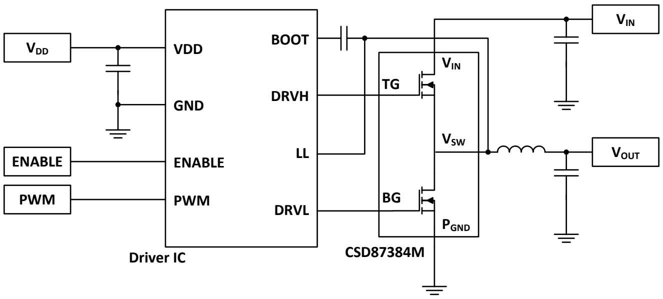
Ordering Information(1)

Device	Media	Qty	Package	Ship
CSD87384M	13-Inch Reel	2500	5 × 3.5 LGA	Tape and Reel
CSD87384MT	7-Inch Reel	250		

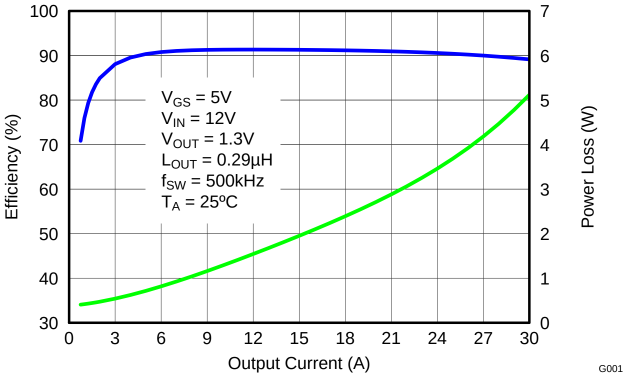
(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Circuit



Typical Power Block Efficiency and Power Loss



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2014) to Revision D	Page
• Changed capacitance units to read pF in Figure 15	8
• Changed capacitance units to read pF in Figure 16	8

Changes from Revision A (September 2013) to Revision B	Page
• Added small reel info	1
• Changed Figure 16	8

Changes from Original (September 2013) to Revision A	Page
• Changed $V_{GS(th)}$ from 1.0 V to 1.1 V in the Electrical Characteristics table	4

5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage		V_{IN} to P_{GND}	–0.8	30	V
		V_{SW} to P_{GND}		30	
		V_{SW} to P_{GND} (10 ns)		32	
		T_G to V_{SW}	–8	10	
		B_G to P_{GND}	–8	10	
I_{DM}	Pulsed Current Rating (2)			95	A
P_D	Power Dissipation (3)			8	W
E_{AS}	Avalanche Energy	Sync FET, I_D = 68, L = 0.1 mH		231	mJ
		Control FET, I_D = 31, L = 0.1 mH		48	
T_J	Operating Junction		–55	150	°C
T_{stg}	Storage Temperature Range		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Pulse Duration ≤50 µs, duty cycle ≤0.01

(3) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2) Cu

5.2 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{GS}	Gate Drive Voltage		4.5	8	V
V_{IN}	Input Supply Voltage			24	V
f_{SW}	Switching Frequency	C_{BST} = 0.1 µF (min)	200	1500	kHz
Operating Current		No Airflow		30	A
		With Airflow (200 LFM)		35	A
		With Airflow + Heat Sink		40	A
T_J	Operating Temperature			125	°C

5.3 Power Block Performance

T_A = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}	Power Loss (1)	V_{IN} = 12 V, V_{GS} = 5 V V_{OUT} = 1.3 V, I_{OUT} = 25 A f_{SW} = 500 kHz L_{OUT} = 0.3 µH, T_J = 25ºC		3.7		W
I_{QVIN}	V_{IN} Quiescent Current	T_G to T_{GR} = 0 V B_G to P_{GND} = 0 V		10		µA

(1) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5 V driver IC.

5.4 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (Min Cu) (1)			153	°C/W
	Junction-to-ambient thermal resistance (Max Cu) (2)(1)			67	
$R_{\theta JC}$	Junction-to-case thermal resistance (Top of package) (1)			3.0	
	Junction-to-case thermal resistance (P_{GND} Pin) (1)			1.25	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

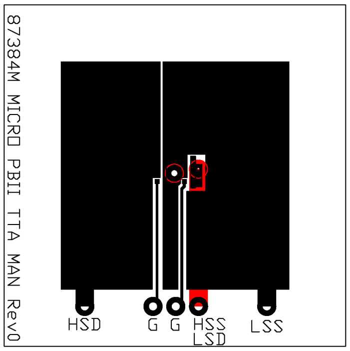
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2) Cu.

5.5 Electrical Characteristics

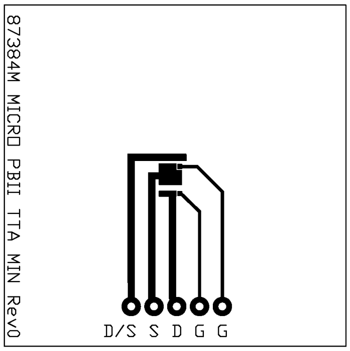
T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 Control FET			Q2 Sync FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	30			30			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1			1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 10 V			100			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	1.1		1.9	1.1		1.7	V
$R_{DS(on)}$	Drain-to-Source On-Impedance	V_{GS} = 4.5 V, I_{DS} = 25 A		7.5	8.9		2.15	2.6	mΩ
		V_{GS} = 8 V, I_{DS} = 25 A		6.4	7.7		1.95	2.4	
g_{fs}	Transconductance	V_{DS} = 10 V, I_{DS} = 25 A		67			240		S
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input Capacitance (1)	V_{GS} = 0 V, V_{DS} = 15 V, f = 1MHz		884	1150		3760	4890	pF
C_{OSS}	Output Capacitance (1)			452	588		1110	1440	pF
C_{RSS}	Reverse Transfer Capacitance (1)			19.4	25.2		87	114	pF
R_G	Series Gate Resistance (1)			1.0	2.0		0.7	1.4	Ω
Q_g	Gate Charge Total (4.5 V) (1)	V_{DS} = 15 V, I_{DS} = 25 A		7.1	9.2		31	40	nC
Q_{gd}	Gate Charge – Gate-to-Drain			1.5			8.6		nC
Q_{gs}	Gate Charge – Gate-to-Source			2.7			8.6		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.3			5.4		nC
Q_{OSS}	Output Charge	V_{DD} = 12 V, V_{GS} = 0 V		11.3			37		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 25 A, R_G = 2 Ω		8.7			17.5		ns
t_r	Rise Time			56			49		ns
$t_{d(off)}$	Turn-Off Delay Time			14			29		ns
t_f	Fall Time			7.6			8.2		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode Forward Voltage	I_{DS} = 25 A, V_{GS} = 0 V		0.85			0.80		V
Q_{rr}	Reverse Recovery Charge	V_{dd} = 15 V, I_F = 25 A, di/dt = 300 A/μs		21			51		nC
t_{rr}	Reverse Recovery Time			21			32		ns

(1) Specified by design



Max $R_{\theta JA}$ = 67°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 153°C/W when mounted on minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.6 Typical Power Block Device Characteristics

T_J = 125°C, unless stated otherwise. For Figure 3 and Figure 4, the Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0 inches (W) × 3.5 inches (L) × 0.062 inch (H) and 6 copper layers of 1 oz. copper thickness. See *Application and Implementation* for detailed explanation.

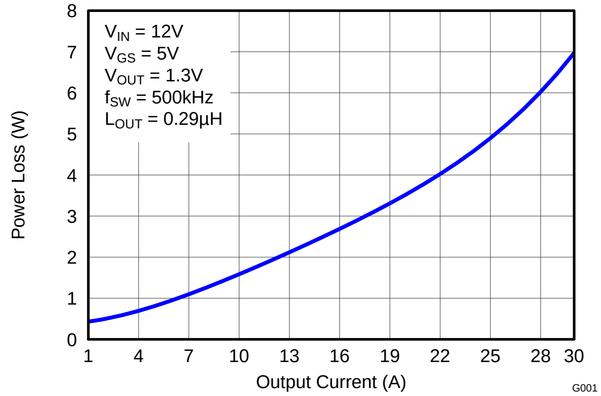


Figure 1. Power Loss vs Output Current

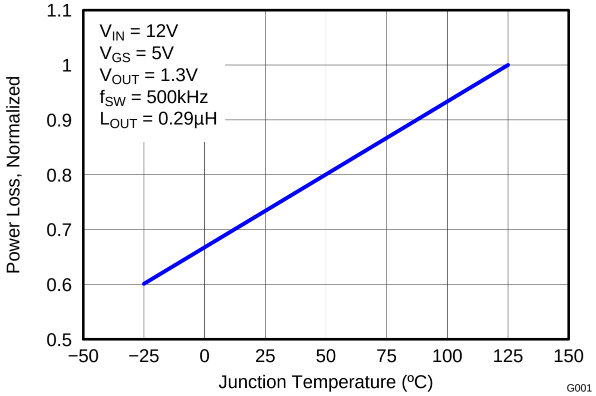


Figure 2. Normalized Power Loss vs Temperature

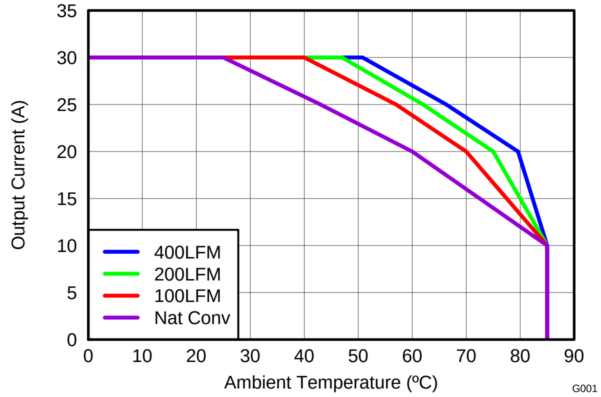


Figure 3. Safe Operating Area – PCB Horizontal Mount

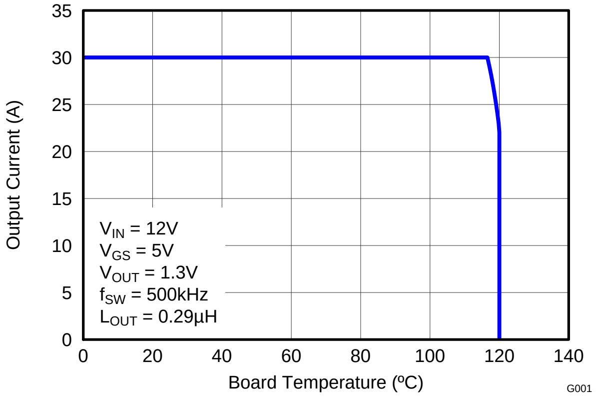


Figure 4. Typical Safe Operating Area

Typical Power Block Device Characteristics (continued)

T_J = 125°C, unless stated otherwise. For Figure 3 and Figure 4, the Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0 inches (W) × 3.5 inches (L) × 0.062 inch (H) and 6 copper layers of 1 oz. copper thickness. See *Application and Implementation* for detailed explanation.

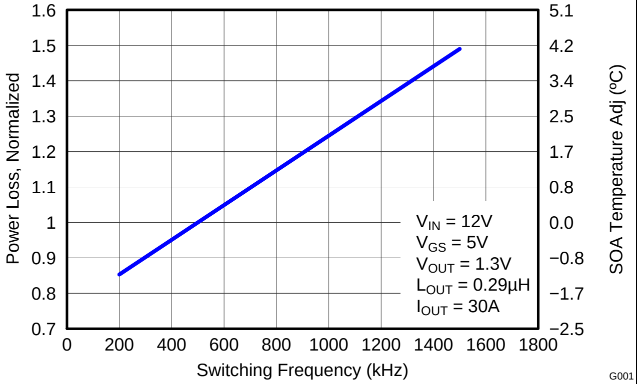


Figure 5. Normalized Power Loss vs Switching Frequency

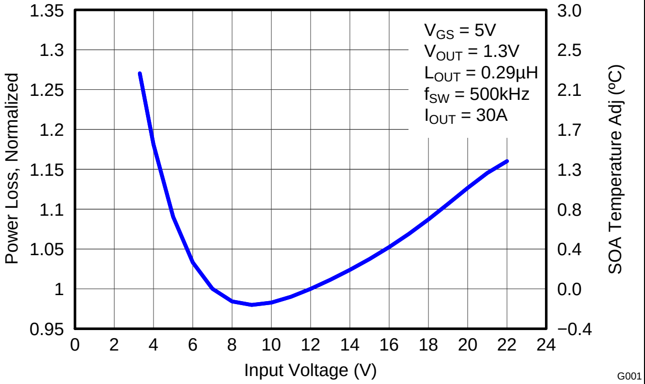


Figure 6. Normalized Power Loss vs Input Voltage

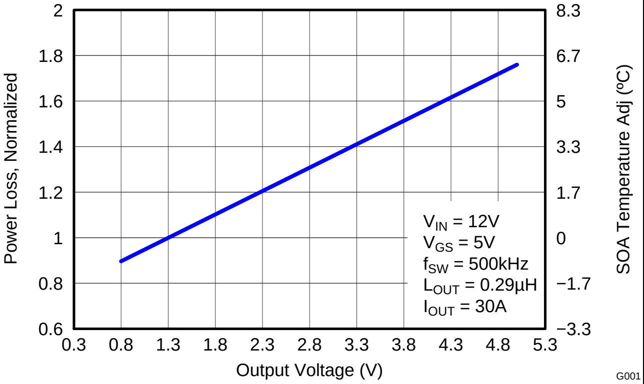


Figure 7. Normalized Power Loss vs Output Voltage

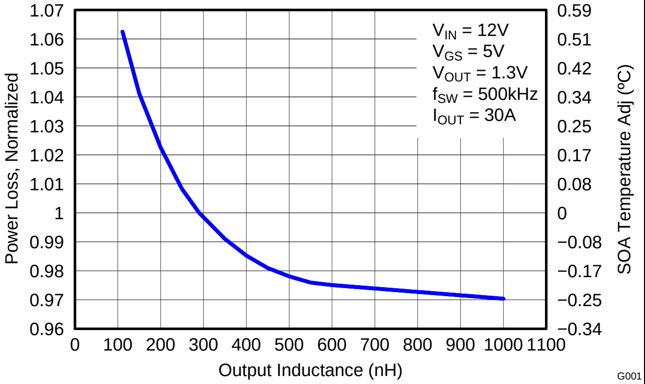


Figure 8. Normalized Power Loss vs Output Inductance

5.7 Typical Power Block MOSFET Characteristics

T_A = 25°C, unless stated otherwise.

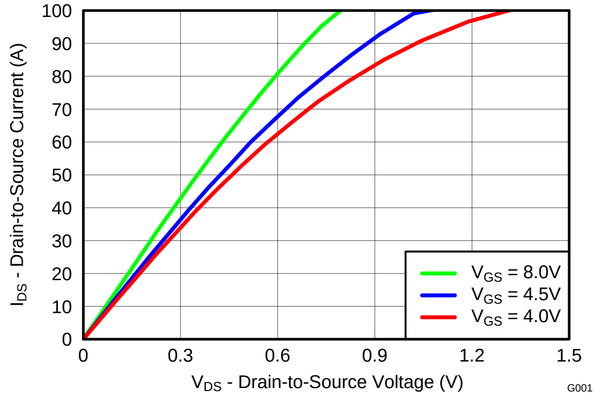


Figure 9. Control MOSFET Saturation

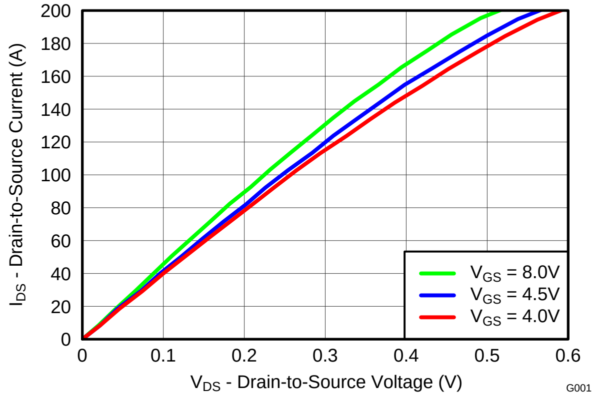


Figure 10. Sync MOSFET Saturation

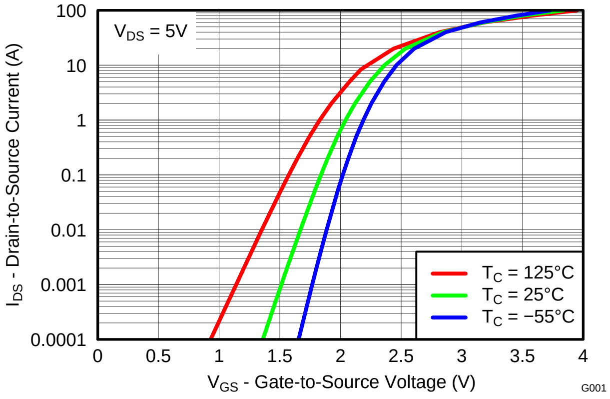


Figure 11. Control MOSFET Transfer

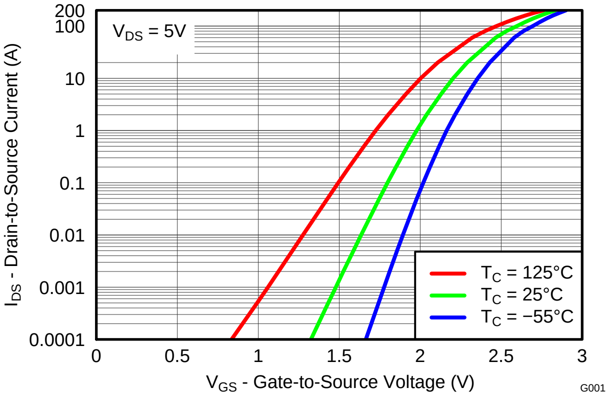


Figure 12. Sync MOSFET Transfer

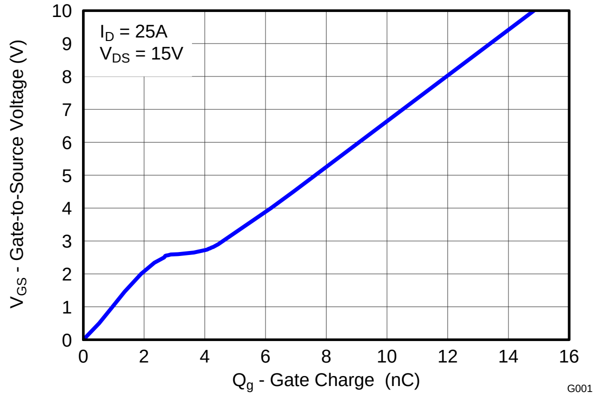


Figure 13. Control MOSFET Gate Charge

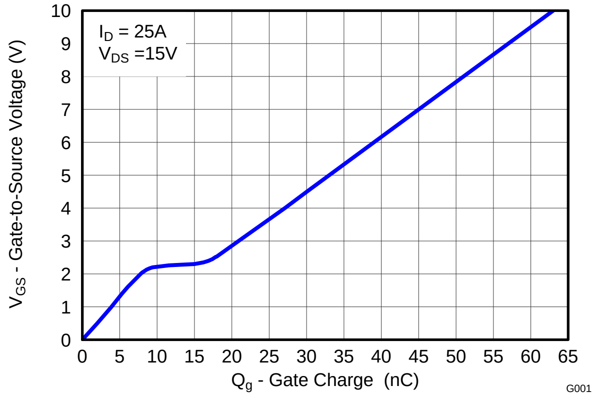


Figure 14. Sync MOSFET Gate Charge

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

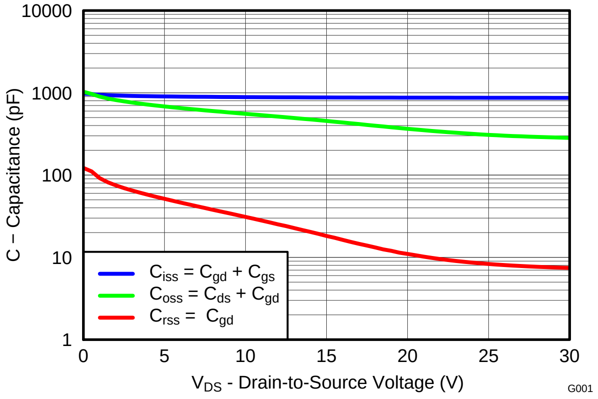


Figure 15. Control MOSFET Capacitance

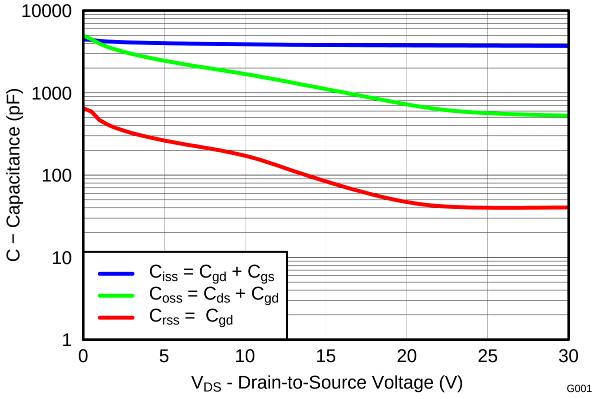


Figure 16. Sync MOSFET Capacitance

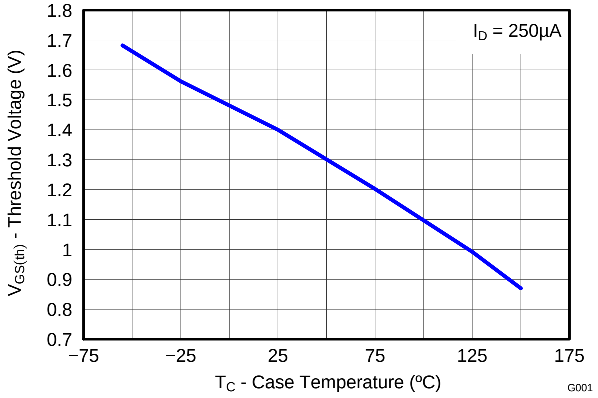


Figure 17. Control MOSFET $V_{GS(th)}$

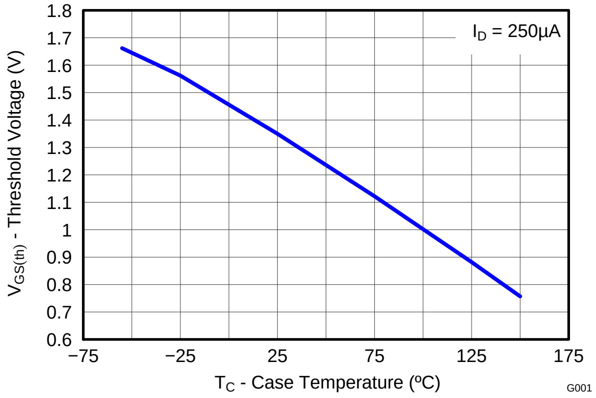


Figure 18. Sync MOSFET $V_{GS(th)}$

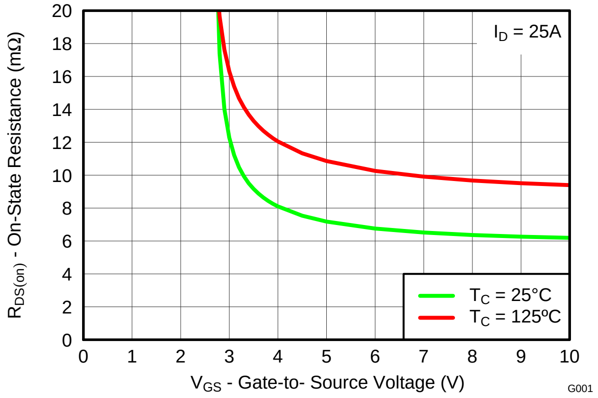


Figure 19. Control MOSFET $R_{DS(on)}$ vs V_{GS}

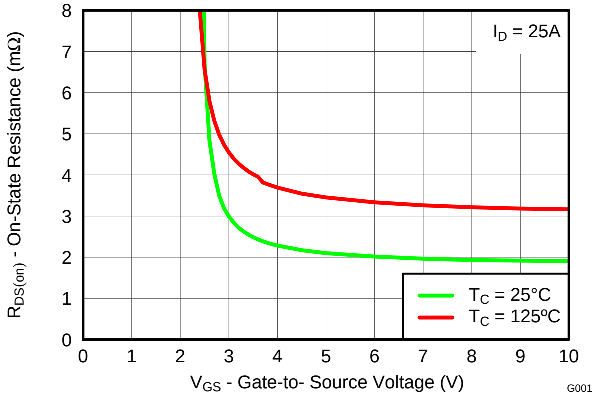


Figure 20. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

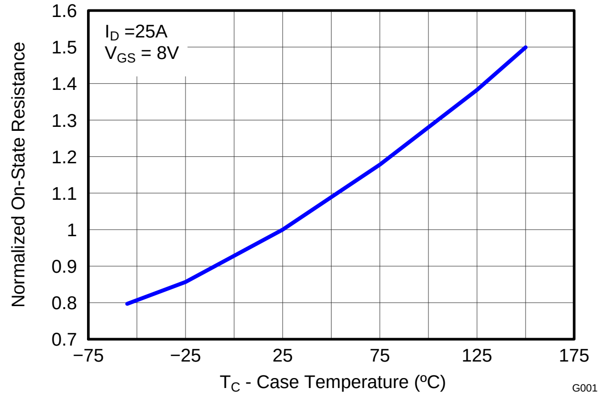


Figure 21. Control MOSFET Normalized $R_{DS(on)}$

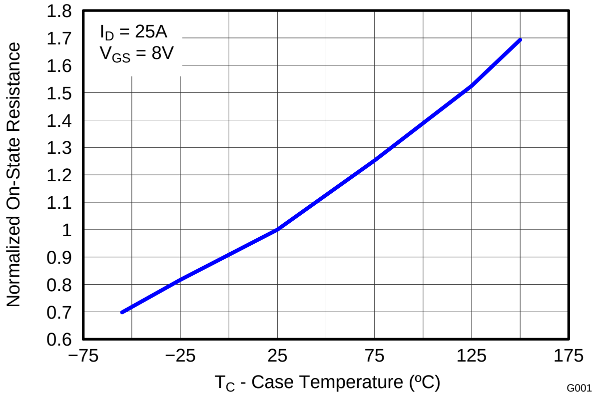


Figure 22. Sync MOSFET Normalized $R_{DS(on)}$

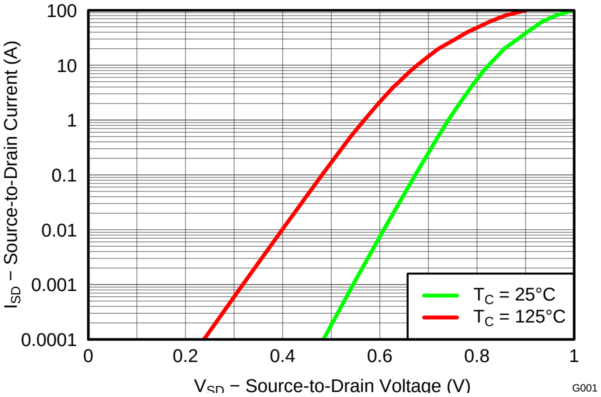


Figure 23. Control MOSFET Body Diode

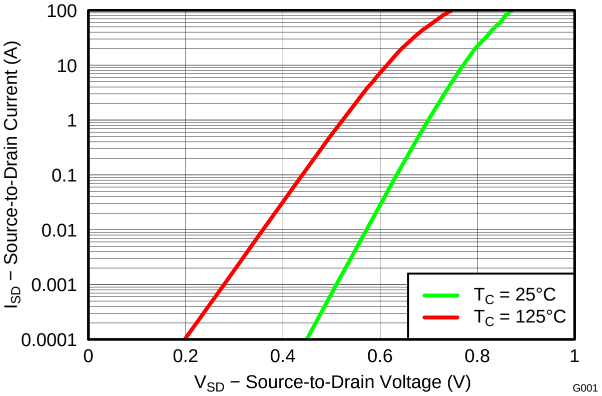


Figure 24. Sync MOSFET Body Diode

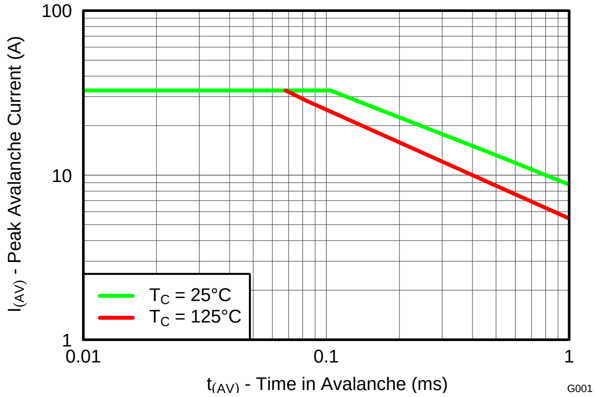


Figure 25. Control MOSFET Unclamped Inductive Switching

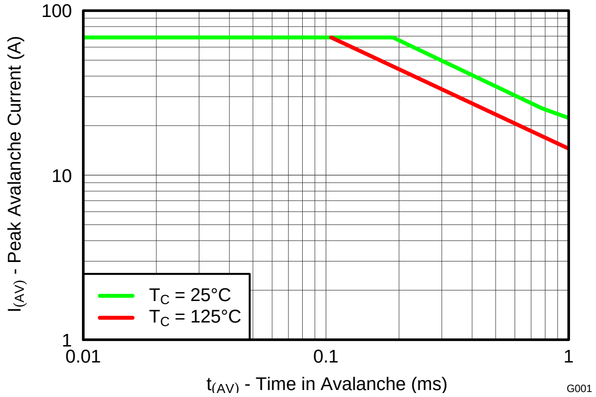


Figure 26. Sync MOSFET Unclamped Inductive Switching

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI ’ s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The CSD87384M NexFET™ power block is an optimized design for synchronous buck applications using 5 V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored toward a more systems-centric environment. System level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

6.2 Power Loss Curves

MOSFET-centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. To simplify the design process for engineers, TI has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87384M as a function of load current. This curve is measured by configuring and running the CSD87384M as it would be in the final application (see Figure 27). The measured power loss is the CSD87384M loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{Power Loss} \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.3 Safe Operating Curves (SOA)

The SOA curves in the CSD87384M data sheet provide guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 4 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 inches (W) × 3.5 inches (L) × 0.062 inch (T) and 6 copper layers of 1 oz. copper thickness.

6.4 Normalized Curves

The normalized curves in the CSD87384M data sheet provide guidance on the Power Loss and SOA adjustments based on their application-specific needs. These curves show how the power loss and SOA boundaries adjust for a given set of systems conditions. The primary y-axis is the normalized change in power loss and the secondary y-axis is the change in system temperature required to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

Normalized Curves (continued)

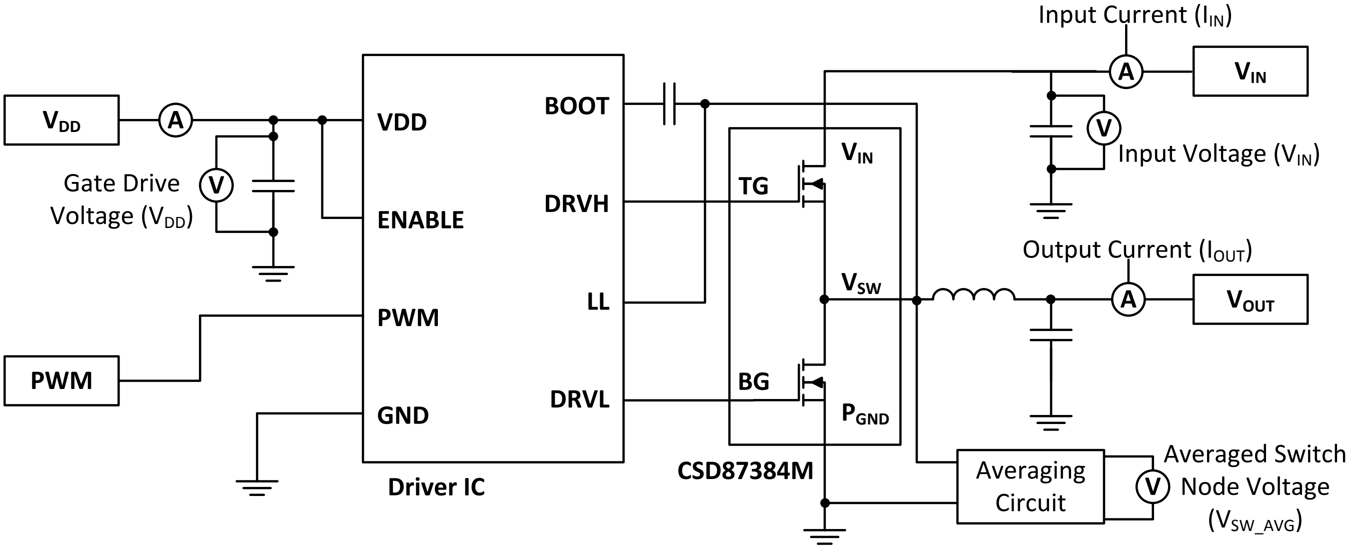


Figure 27. Typical Application

6.5 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Design Example*). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps the user should take to predict product performance for any set of system conditions.

6.5.1 Design Example

Operating Conditions:

- Output Current = 20 A
- Input Voltage = 4 V
- Output Voltage = 1 V
- Switching Frequency = 800 kHz
- Inductor = 0.2 µH

6.5.2 Calculating Power Loss

- Power Loss at 20 A = 3.5 W (Figure 1)
- Normalized Power Loss for input voltage ≈ 1.18 (Figure 6)
- Normalized Power Loss for output voltage ≈ 0.94 (Figure 7)
- Normalized Power Loss for switching frequency ≈ 1.15 (Figure 5)
- Normalized Power Loss for output inductor ≈ 1.02 (Figure 8)
- **Final calculated Power Loss = 3.5 W × 1.18 × 0.94 × 1.15 × 1.02 ≈ 4.6 W**

6.5.3 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 1.5ºC (Figure 6)
- SOA adjustment for output voltage ≈ –0.5ºC (Figure 7)
- SOA adjustment for switching frequency ≈ 1.2ºC (Figure 5)
- SOA adjustment for output inductor ≈ 0.2ºC (Figure 8)
- **Final calculated SOA adjustment = 1.5 + (–0.5) + 1.2 + 0.2 ≈ 2.4ºC**

In the previous design example, the estimated power loss of the CSD87384M would increase to 4.6 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 2.4ºC. Figure 28 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board or ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 2.4ºC. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board or ambient temperature.

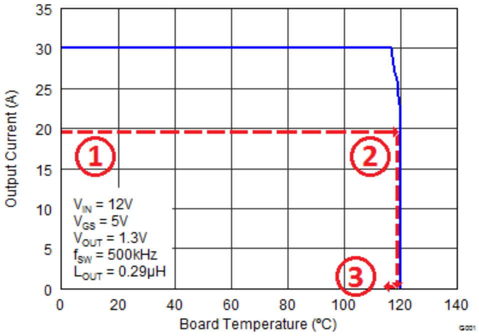


Figure 28. Power Block SOA

7 Layout

7.1 Layout Guidelines

7.1.1 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout yields maximum performance in both areas. A brief description on how to address each parameter is provided.

7.1.2 Electrical Performance

The CSD87384M has the ability to switch voltages at rates greater than 10 kV/µs. Take special care with the PCB layout design and placement of the input capacitors, inductor, and output capacitors.

- The placement of the input capacitors relative to VIN and PGND pins of CSD87384M device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 29). The example in Figure 29 uses 1 × 10 nF 0402 25 V and 4 × 10 µF 1206 25 V ceramic capacitors (TDK part number C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Stage C21, C5, C8, C19, and C18 should follow in order.
- The switching node of the output inductor should be placed relatively close to the Power Block II CSD87384M VSW pins. Minimizing the VSW node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. See Figure 29. (1)

7.1.3 Thermal Performance

The CSD87384M has the ability to utilize the PGND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that wicks down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 29 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

The number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

7.2 Layout Example

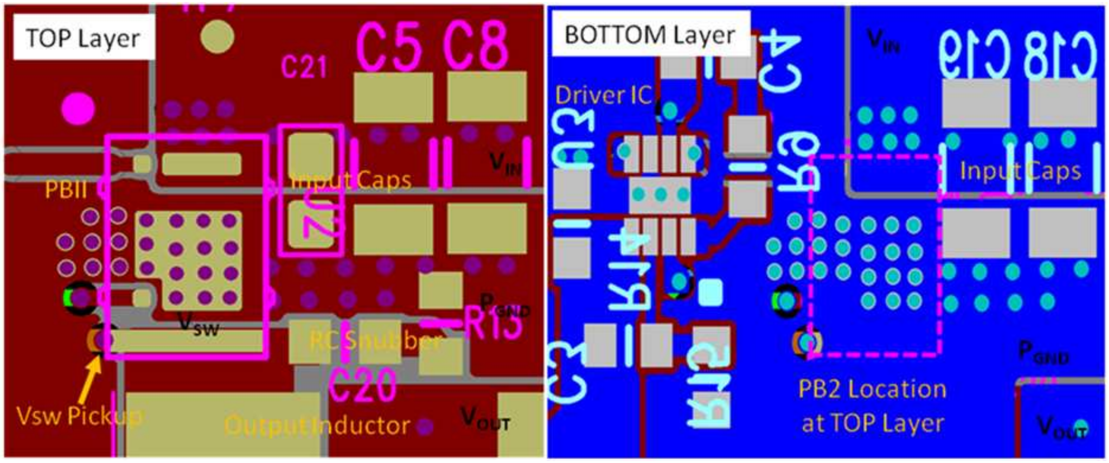


Figure 29. Recommended PCB Layout (Top Down View)

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(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

8 Device and Documentation Support

8.1 Trademarks

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8.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.3 Glossary

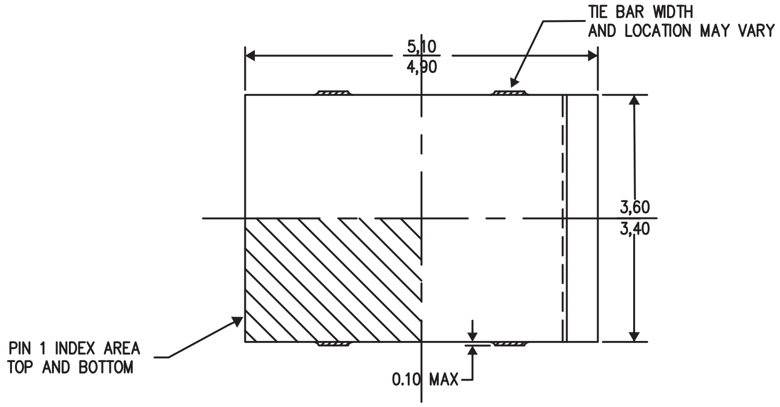
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

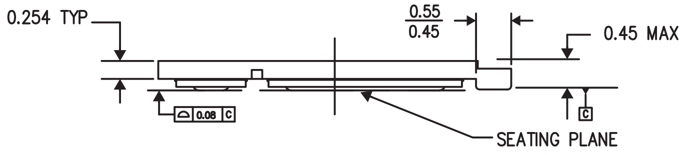
9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation

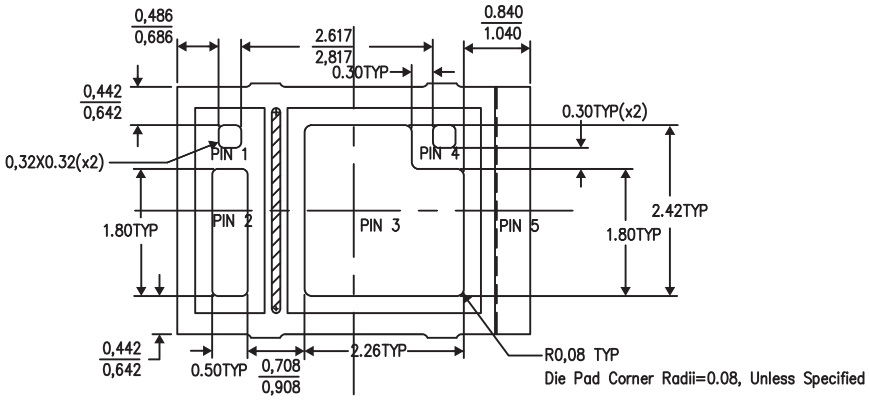
9.1 CSD87384M Package Dimensions



Top View



Side View

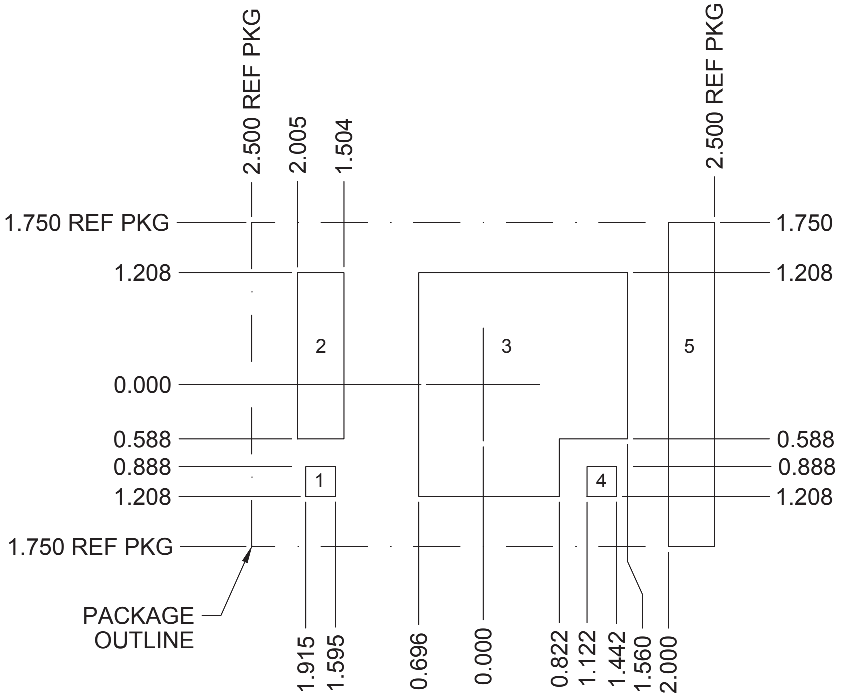


Bottom View

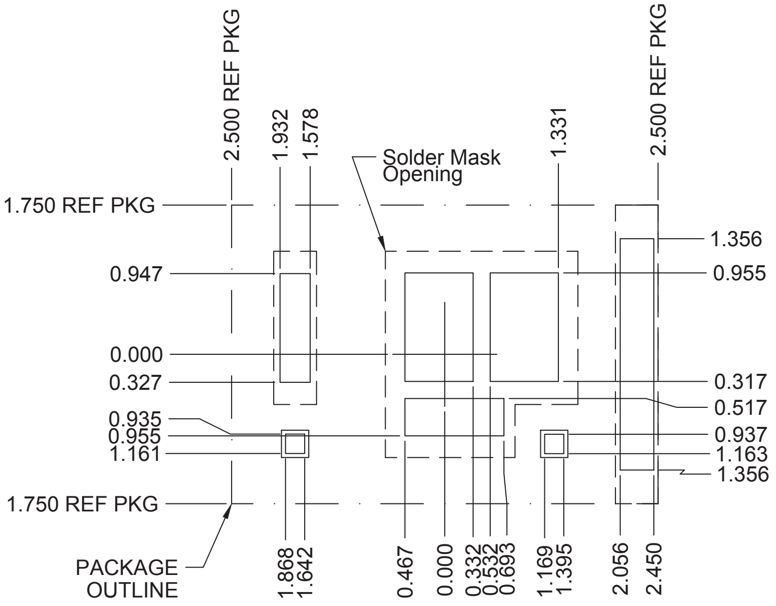
Pin Configuration

Position	Designation
Pin 1	TG
Pin 2	V_{IN}
Pin 3	P_{GND}
Pin 4	BG
Pin 5	V_{SW}

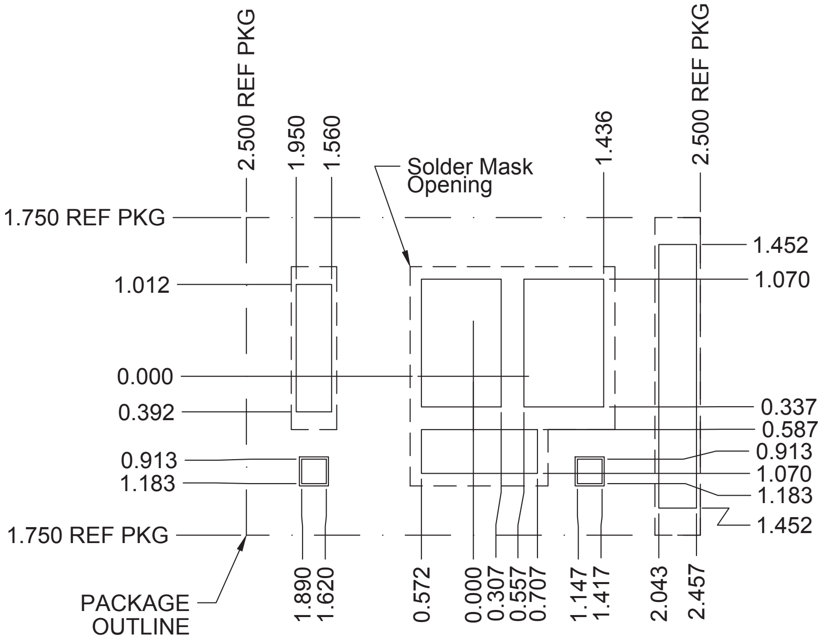
9.2 Land Pattern Recommendation



9.3 Stencil Recommendation (100 µm)

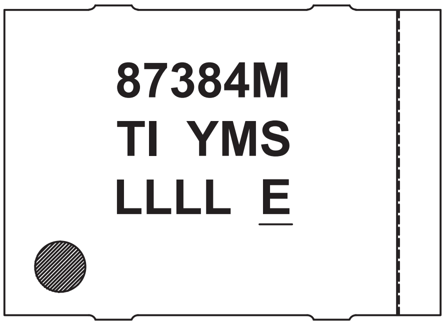


9.4 Stencil Recommendation (125 µm)

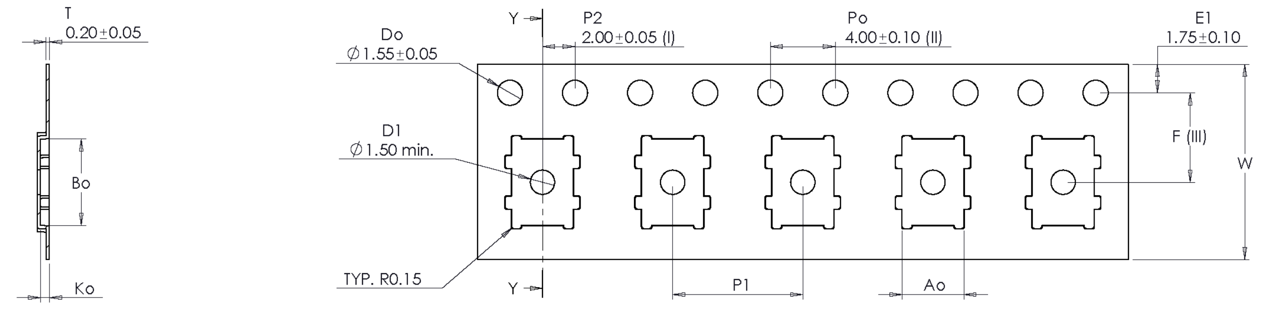


For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

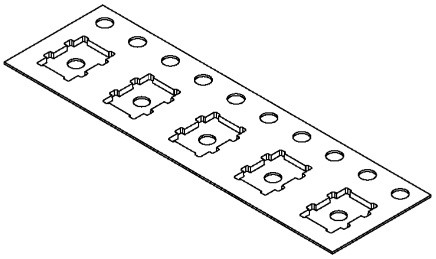
9.5 Pin Drawing



9.6 CSD87384M Embossed Carrier Tape Dimensions



SECTION Y-Y
SCALE 3.5 : 1



Ao	3.80	+/- 0.10
Bo	5.30	+/- 0.10
Ko	0.55	+/- 0.05
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

Forming format : Press Form - 17
Estimated max. length : 278 meter/22B3 reel

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

(1) Pin 1 is oriented in the top-left quadrant of the tape enclosure (closest to the carrier tape sprocket holes).

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87384M	ACTIVE	PTAB	MPB	5	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 150	87384M	Samples
CSD87384MT	ACTIVE	PTAB	MPB	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 150	87384M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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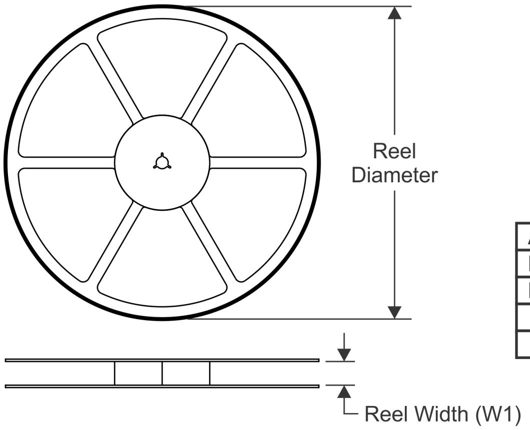
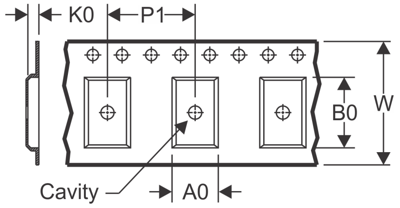
TAPE AND REEL INFORMATION

REEL DIMENSIONS

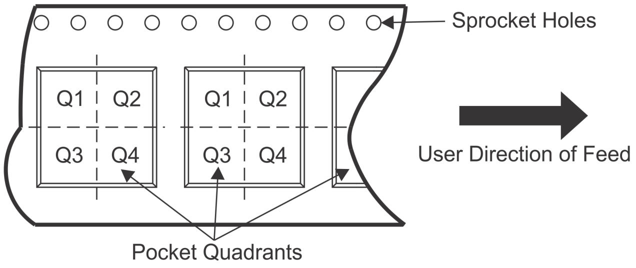


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

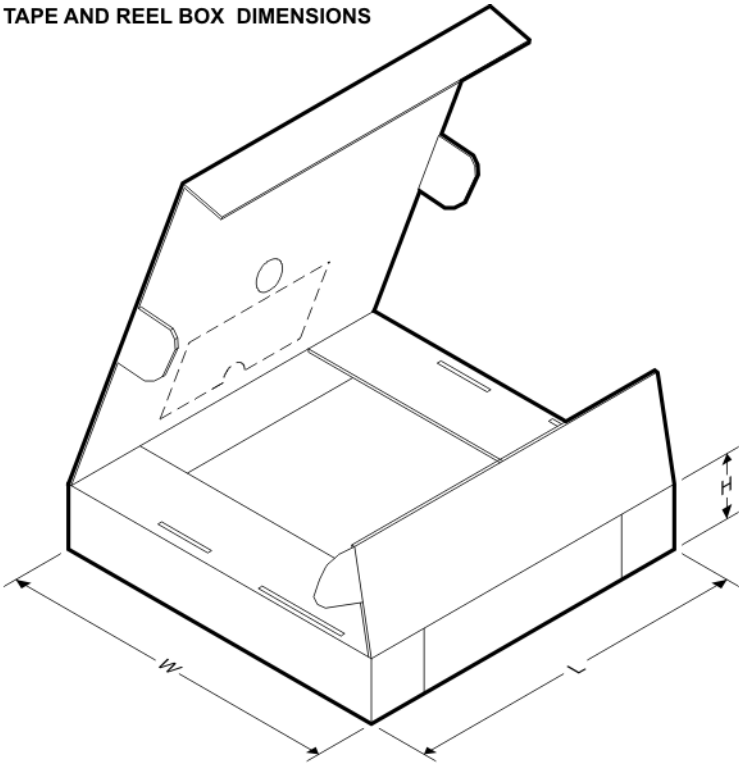
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87384M	PTAB	MPB	5	2500	330.0	12.4	3.8	5.3	0.55	8.0	12.0	Q1
CSD87384MT	PTAB	MPB	5	250	180.0	12.4	3.8	5.3	0.55	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87384M	PTAB	MPB	5	2500	367.0	367.0	35.0
CSD87384MT	PTAB	MPB	5	250	210.0	185.0	35.0

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