

DUAL DIGITAL ISOLATOR

Check for Samples: [ISO7221C-HT](#)

FEATURES

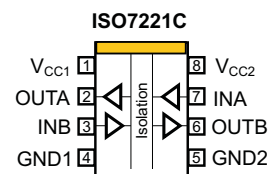
- 1-, 5- and 25-Mbps Signaling Rate Options
 - Low Channel-to-Channel Output Skew; 1 ns max
 - Low Pulse-Width Distortion (PWD); 1 ns max
 - Low Jitter Content; 1 ns Typ at 150 Mbps
- 4000- V_{peak} Isolation, 560 V_{peak} V_{IORM}
 - UL 1577 Approved
 - 50-kV/ μs Typical Transient Immunity
- Operates with 3.3-V or 5-V Supplies
- 4-kV ESD Protection
- High Electromagnetic Immunity

APPLICATIONS

- Down-Hole Drilling
- High Temperature Environments

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Extreme (-55°C to 175°C) Temperature Range ⁽¹⁾ ⁽²⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.



- (1) Custom temperature ranges available.
- (2) Device is qualified to ensure reliable operation for 1000 hours at maximum rated temperature. This includes, but is not limited to temperature bake, temperature cycle, electro migration, bond inter metallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DESCRIPTION

The ISO7221 is a dual-channel digital isolator. To facilitate PCB layout, the channels are oriented in the opposite directions. This device has a logic input and output buffer separated by TI's silicon-dioxide (SiO_2) isolation barrier, providing galvanic isolation of up to 4000 V. Used in conjunction with isolated power supplies, this device blocks high voltage, isolates grounds, and prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received every 4 μs , the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state.

The small capacitance and resulting time constant provide fast operation with signaling rates available from 0 Mbps (dc) to 150 Mbps. ⁽³⁾ The A-, B- and C-option devices have TTL input thresholds and a noise filter at the input that prevents transient pulses from being passed to the output of the device. The M-option devices have CMOS $V_{\text{CC}}/2$ input thresholds and do not have the input noise-filter and the additional propagation delay.

(3) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ISO7221C-HT

SLLSE78A – APRIL 2011 – REVISED OCTOBER 2012

www.ti.com

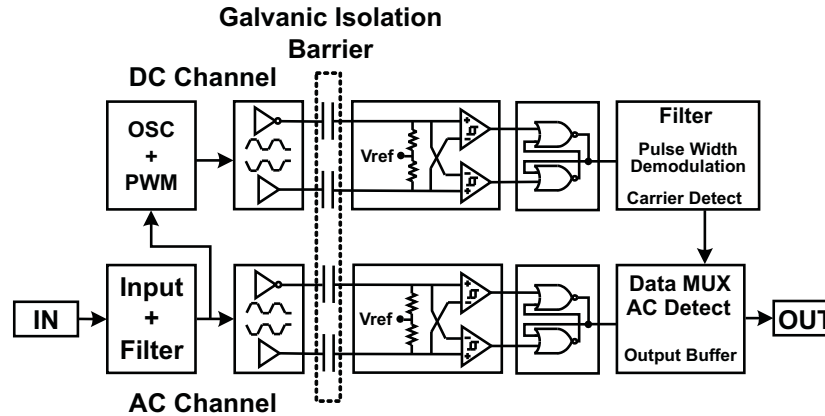
This device requires two supply voltages of 3.3 V, 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS.

The ISO7221 is characterized for operation over the ambient temperature range of –55°C to 175°C.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SINGLE-CHANNEL FUNCTION DIAGRAM



AVAILABLE OPTIONS⁽¹⁾

PRODUCT	MAX SIGNALING RATE	PACKAGE ⁽²⁾	INPUT THRESHOLD	MARKED AS	ORDERING NUMBER
ISO7221C	25 Mbps	SOIC-8	≈ 1.5 V (TTL) (CMOS compatible)	I7221H	ISO7221CHD

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

REGULATORY INFORMATION

UL
Recognized under 1577 Component Recognition Program ⁽¹⁾
File Number: E181974

- (1) Production tested ≥3000 VRMS for 1 second in accordance with UL 1577.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		VALUE	UNIT
V _{CC}	Supply voltage ⁽²⁾ , V _{CC1} , V _{CC2}	–0.5 to 6	V
V _I	Voltage at IN, OUT	–0.5 to 6	V
I _O	Output current	±15	mA
ESD	Electrostatic discharge	Human Body Model	Electrostatic discharge JEDEC Standard 22, Test Method A114-C.01
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101
		Machine Model	ANSI/ESDS5.2-1996
T _J	Maximum junction temperature	180	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage ⁽¹⁾ , V_{CC1} , V_{CC2}	3		5.5	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current	–4			mA
t_{ui}	Input pulse width ⁽²⁾	40	33		ns
$1/t_{ui}$	Signaling rate ⁽²⁾	0	30	25	Mbps
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
T_A	Operating temperature	–55		175	°C

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.

For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

(2) Typical signaling rate and Input pulse width are measured at ideal conditions at 25°C.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT					
I_{CC1} 25 Mbps	$V_I = V_{CC}$ or 0 V, no load		12	22	mA
I_{CC2} 25 Mbps	$V_I = V_{CC}$ or 0 V, no load		12	22	
V_{OH} High-level output voltage	$I_{OH} = -4$ mA, See Figure 1	$V_{CC} - 0.8$	4.6		V
	$I_{OH} = -20$ μ A, See Figure 1	$V_{CC} - 0.1$	5		
V_{OL} Low-level output voltage	$I_{OL} = 4$ mA, See Figure 1		0.2	0.4	V
	$I_{OL} = 20$ μ A, See Figure 1		0	0.1	
$V_{I(HYS)}$ Input voltage hysteresis			150		mV
I_{IH} High-level input current	IN from 0 V to V_{CC}			11	μ A
I_{IL} Low-level input current	IN from 0 V to V_{CC}	–11			μ A
C_I Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin(4E6\pi t)$		1		pF
CMTI Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 3	25	50		kV/ μ s

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.

For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH} , t_{pHL} Propagation delay	See Figure 1	21	32	43	ns
PWD Pulse-width distortion $ t_{pHL} - t_{pLH} $ ⁽¹⁾	See Figure 1		1	2	ns
$t_{sk(pp)}$ Part-to-part skew ⁽²⁾				10	ns
$t_{sk(o)}$ Channel-to-channel output skew ⁽³⁾			0.2	5	ns
t_r Output signal rise time	See Figure 1		1		ns
t_f Output signal fall time	See Figure 1		1		ns
t_{fs} Failsafe output delay time from input power loss	See Figure 2		3		μ s

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ISO7221C-HT

SLLSE78A – APRIL 2011 – REVISED OCTOBER 2012

www.ti.com

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{CC1}	25 Mbps		V _I = V _{CC} or 0 V, no load		12	22	mA
I _{CC2}	25 Mbps		V _I = V _{CC} or 0 V, no load		6	12	mA
V _{OH}	High-level output voltage	(5-V side)	I _{OH} = −4 mA, See Figure 1	V _{CC} − 0.8			V
			I _{OH} = −20 μA, See Figure 1	V _{CC} − 0.1			
V _{OL}	Low-level output voltage		I _{OL} = 4 mA, See Figure 1			0.4	V
			I _{OL} = 20 μA, See Figure 1			0.1	
V _{I(HYS)}	Input voltage hysteresis				150		mV
I _{IH}	High-level input current		IN from 0 V to V _{CC}			11	μA
I _{IL}	Low-level input current		IN from 0 V to V _{CC}		−11		μA
C _I	Input capacitance to ground		IN at V _{CC} , V _I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V _I = V _{CC} or 0 V, See Figure 3		15	40	kV/μs

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH} , t_{pHL}	Propagation delay		24	36	49	ns
PWD	Pulse-width distortion $ t_{pHL} - t_{pLH} $ ⁽¹⁾			1	2	ns
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾				10	ns
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾			0.2	10	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time	See Figure 1		2		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 2		3		μ s

- (1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{CC1}	25 Mbps		V _I = V _{CC} or 0 V, no load		6	12	mA
I _{CC2}	25 Mbps		V _I = V _{CC} or 0 V, no load		12	22	mA
V _{OH}	High-level output voltage	(3.3-V side)	I _{OH} = −4 mA, See Figure 1	V _{CC} − 0.4			V
			I _{OH} = −20 μA, See Figure 1	V _{CC} − 0.1			
V _{OL}	Low-level output voltage		I _{OL} = 4 mA, See Figure 1			0.4	
			I _{OL} = 20 μA, See Figure 1	0		0.1	
V _{I(HYS)}	Input threshold voltage hysteresis			150			mV
I _{IH}	High-level input current		IN from 0 V or V _{CC}			11	μA
I _{IL}	Low-level input current		IN from 0 V or V _{CC}	−11			μA
C _I	Input capacitance to ground		IN at V _{CC} , V _I = 0.4 sin (4E6πt)	1			pF
CMTI	Common-mode transient immunity		V _I = V _{CC} or 0 V, See Figure 3	15	40		kV/μs

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH} , t_{pHL} Propagation delay		24	36	49	ns
PWD Pulse-width distortion $ t_{pHL} - t_{pLH} ^{(1)}$			1	3	ns
$t_{sk(pp)}$ Part-to-part skew ⁽²⁾				10	ns
$t_{sk(o)}$ Channel-to-channel output skew ⁽³⁾			0.2	10	ns
t_r Output signal rise time	See Figure 1		1		
t_f Output signal fall time			1		
t_{fs} Failsafe output delay time from input power loss	See Figure 2		3		μs

- (1) Also referred to as pulse skew.
- (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT					
I_{CC1} 25 Mbps	$V_I = V_{CC}$ or 0 V, no load		6	12	mA
I_{CC2} 25 Mbps	$V_I = V_{CC}$ or 0 V, no load		6	12	mA
V_{OH} High-level output voltage	$I_{OH} = -4$ mA, See Figure 1	$V_{CC} - 0.4$	3		V
	$I_{OH} = -20$ μA, See Figure 1	$V_{CC} - 0.1$	3.3		
V_{OL} Low-level output voltage	$I_{OL} = 4$ mA, See Figure 1		0.2	0.4	V
	$I_{OL} = 20$ μA, See Figure 1		0	0.1	
$V_{I(HYS)}$ Input voltage hysteresis			150		mV
I_{IH} High-level input current	IN from 0 V or V_{CC}			11	μA
I_{IL} Low-level input current	IN from 0 V or V_{CC}	-11			
C_I Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin(4E6\pi t)$		1		pF
CMTI Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 3	15	40		kV/μs

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH} , t_{pHL} Propagation delay		25	40	53	ns
PWD Pulse-width distortion $ t_{pHL} - t_{pLH} ^{(1)}$			1	3	ns
$t_{sk(pp)}$ Part-to-part skew ⁽²⁾				10	ns
$t_{sk(o)}$ Channel-to-channel output skew ⁽³⁾			0.2	5	ns
t_r Output signal rise time	See Figure 1		2		ns
t_f Output signal fall time	See Figure 1		2		ns
t_{fs} Failsafe output delay time from input power loss	See Figure 2		3		μs

- (1) Also referred to as pulse skew.
- (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

PARAMETER MEASUREMENT INFORMATION

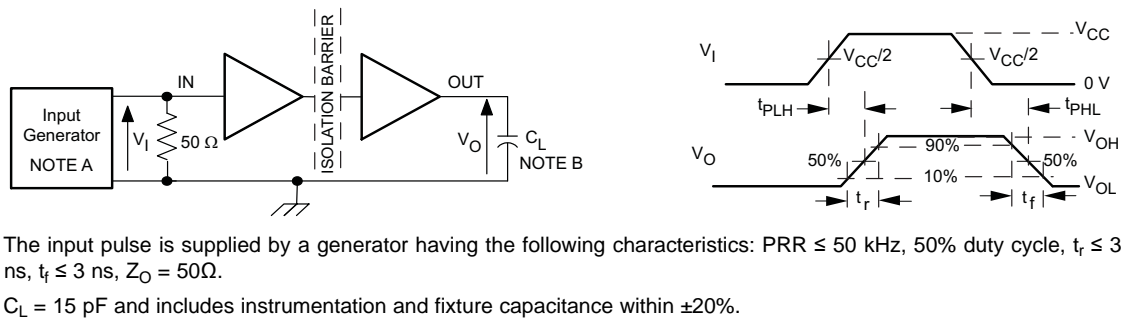


Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms

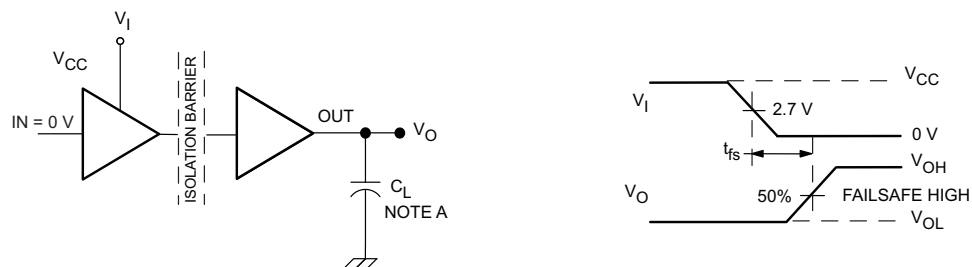


Figure 2. Failsafe Delay Time Test Circuit and Voltage Waveforms

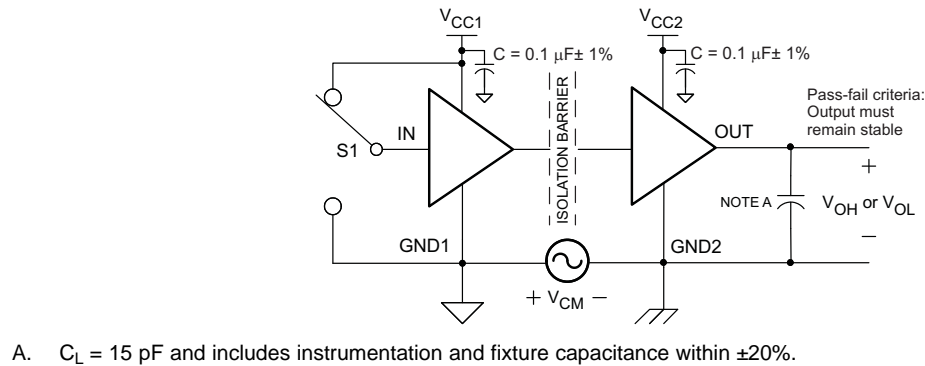


Figure 3. Common-Mode Transient Immunity Test Circuit

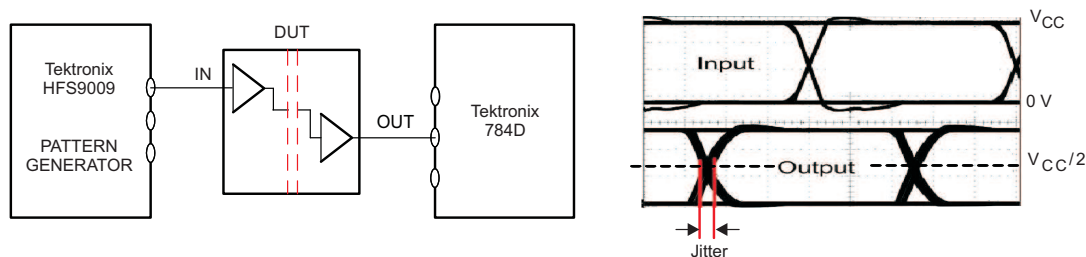
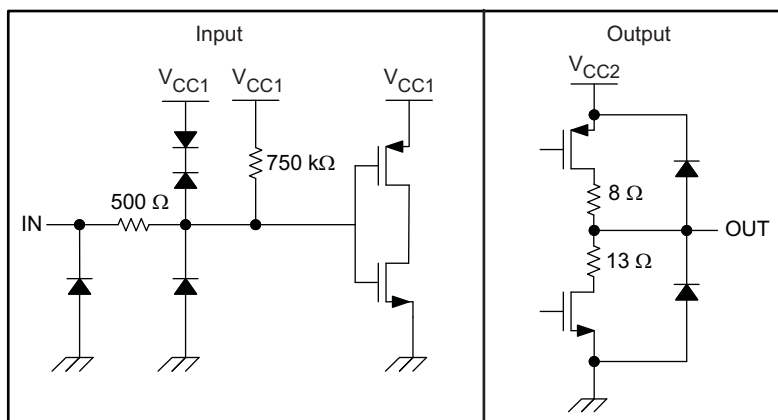


Figure 4. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

DEVICE I/O SCHEMATICS



SOIC-8 PACKAGE THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA} Junction-to-air	Low-K Thermal Resistance ⁽¹⁾		212		°C/W
	High-K Thermal Resistance		122		
θ_{JB} Junction-to-Board Thermal Resistance			37		
θ_{JC} Junction-to-Case Thermal Resistance			69.1		

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

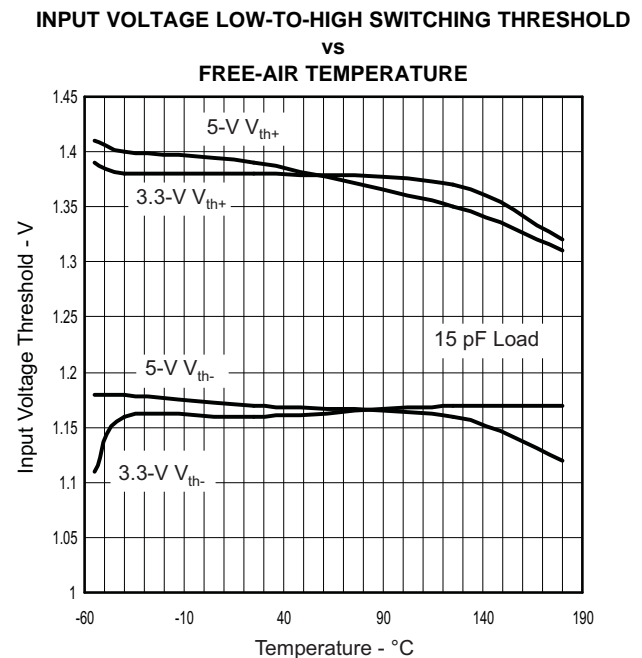
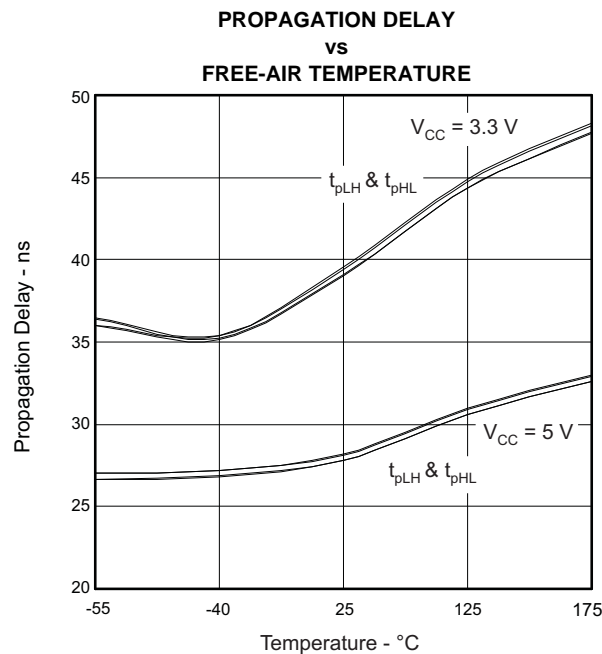
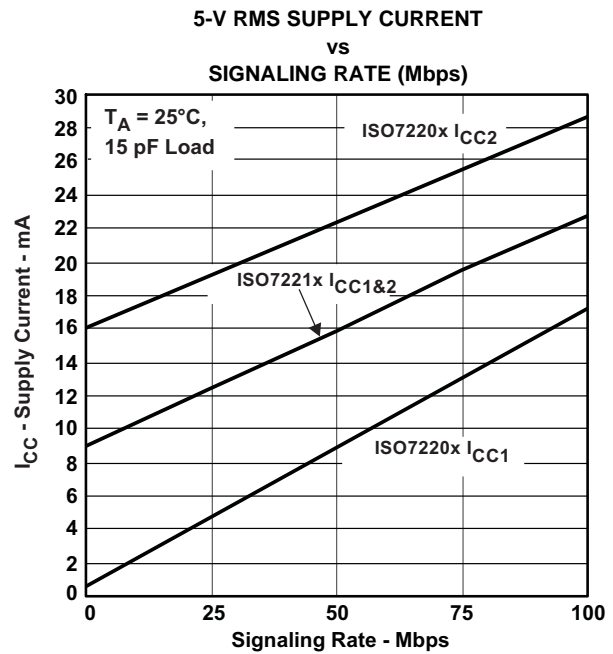
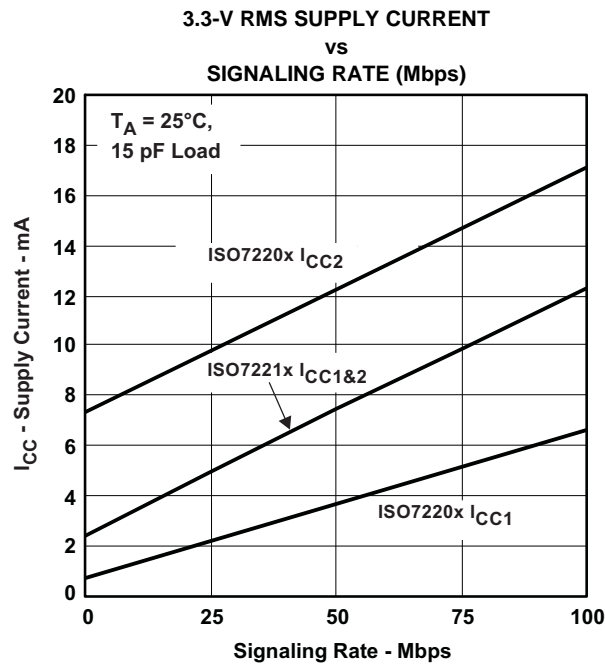
DEVICE FUNCTION TABLE

Table 1. Function Table⁽¹⁾

INPUT SIDE V _{CC}	OUTPUT SIDE V _{CC}	INPUT IN	OUTPUT OUT
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered Up (V_{CC} ≥ 3.0V); PD = Powered Down (V_{CC} ≤ 2.5V); X = Irrelevant; H = High Level; L = Low Level

TYPICAL CHARACTERISTIC CURVES



TYPICAL CHARACTERISTIC CURVES (continued)

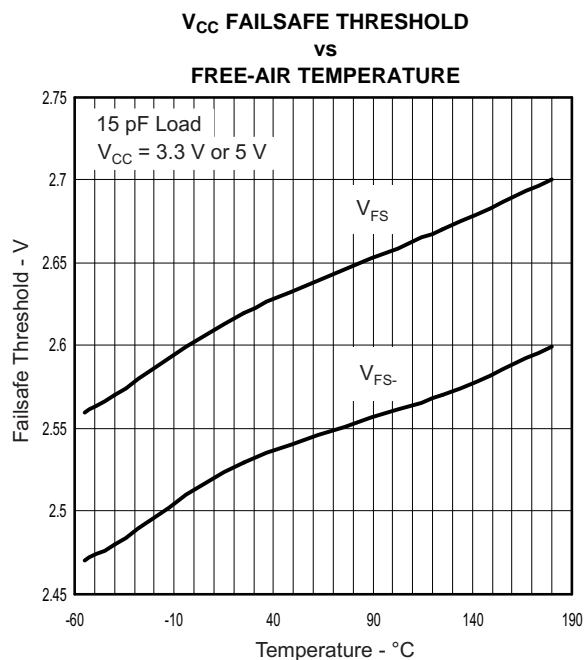


Figure 9.

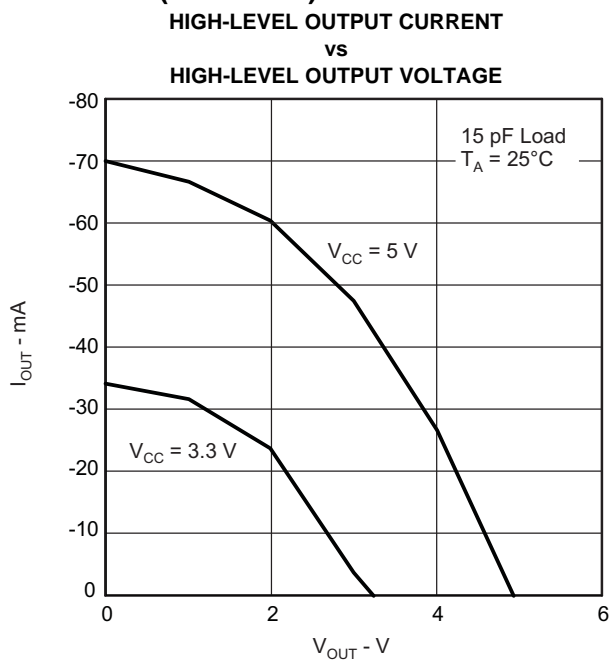


Figure 10.

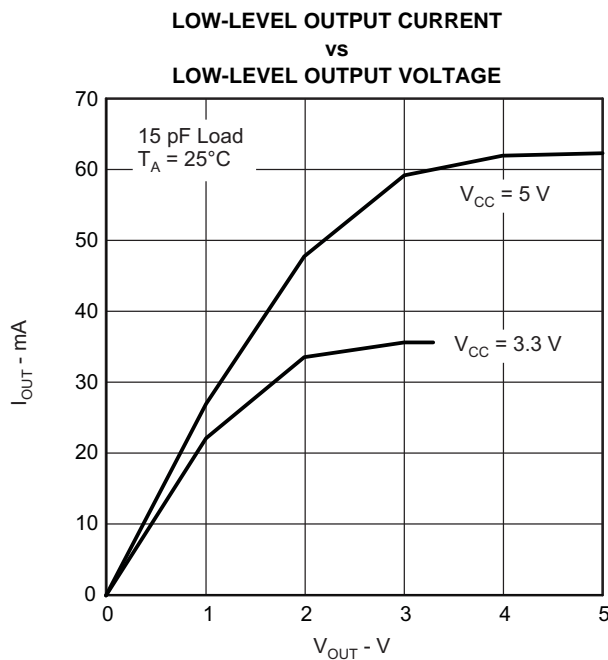


Figure 11.

APPLICATION INFORMATION

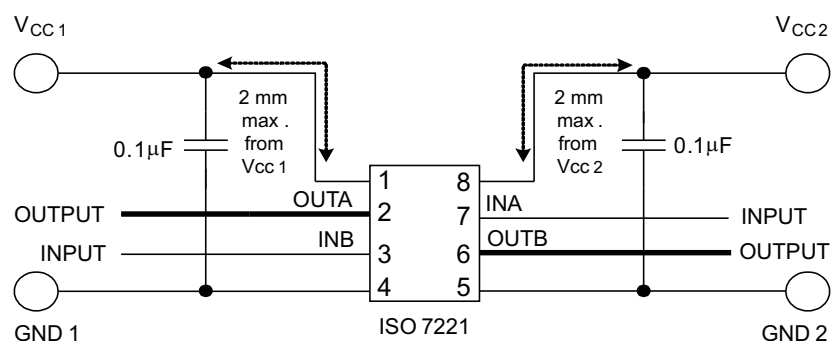
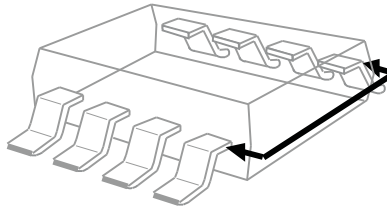


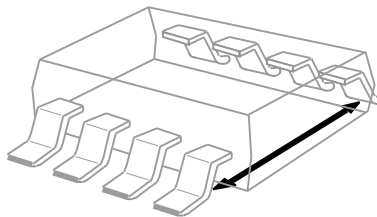
Figure 12. Typical ISO7221 Application Circuit

ISOLATION GLOSSARY

Creepage Distance — The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



Clearance — The shortest distance between two conductive input to output leads measured through air (line of sight).



Input-to Output Barrier Capacitance — The total capacitance between all input terminals connected together, and all output terminals connected together.

Input-to Output Barrier Resistance — The total resistance between all input terminals connected together, and all output terminals connected together.

Primary Circuit — An internal circuit directly connected to an external supply mains or other equivalent source which supplies the primary circuit electric power.

Secondary Circuit — A circuit with no direct connection to primary power, and derives its power from a separate isolated source.

Comparative Tracking Index (CTI) — CTI is an index used for electrical insulating materials which is defined as the numerical value of the voltage which causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface -- the higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

ISO7221C-HT

SLLSE78A – APRIL 2011 – REVISED OCTOBER 2012

www.ti.com

Insulation:

Operational insulation — Insulation needed for the correct operation of the equipment.

Basic insulation — Insulation to provide basic protection against electric shock.

Supplementary insulation — Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation — Insulation comprising both basic and supplementary insulation.

Reinforced insulation — A single insulation system which provides a degree of protection against electric shock equivalent to double insulation.

Pollution Degree:

Pollution Degree 1 — No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence.

Pollution Degree 2 — Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation must be expected.

Pollution Degree 3 — Conductive pollution occurs or dry nonconductive pollution occurs which becomes conductive due to condensation which is to be expected.

Pollution Degree 4 — Continuous conductivity occurs due to conductive dust, rain, or other wet conditions.

Installation Category:

Overvoltage Category — This section is directed at insulation co-ordination by identifying the transient overvoltages which may occur, and by assigning 4 different levels as indicated in IEC 60664.

I: Signal Level — Special equipment or parts of equipment.

II: Local Level — Portable equipment etc.

III: Distribution Level — Fixed installation

IV: Primary Supply Level — Overhead lines, cable systems

Each category should be subject to smaller transients than the category above.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7221CHD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 175	I7221H	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO7221C-HT :

- Catalog: [ISO7221C](#)
- Automotive: [ISO7221C-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com