

# OPA165x SoundPlus™ Low Noise and Distortion, General-Purpose, FET-Input Audio Operational Amplifiers

## 1 Features

- Low Noise:
  - 4.5 nV/ $\sqrt{\text{Hz}}$  at 1 kHz
  - 3.8 nV/ $\sqrt{\text{Hz}}$  at 10 kHz
- Low Distortion: 0.00005% at 1 kHz
- Low Quiescent Current: 2 mA Per Channel
- Low Input Bias Current: 10 pA
- Slew Rate: 10 V/ $\mu\text{s}$
- Wide Gain Bandwidth: 18 MHz (G = +1)
- Unity Gain Stable
- Rail-to-Rail Output
- Wide Supply Range:  $\pm 2.25$  V to  $\pm 18$  V, or +4.5 V to +36 V
- Dual and Quad Versions Available
- Small Package Sizes:
  - Dual: SO-8 and MSOP-8
  - Quad: SO-14 and TSSOP-14

## 2 Applications

- Analog and Digital Mixers
- Audio Effects Processors
- Musical Instruments
- A/V Receivers
- DVD and Blu-Ray™ Players
- Car Audio Systems

## 3 Description

The OPA1652 (dual) and OPA1654 (quad) FET-input operational amplifiers achieve a low 4.5-nV/ $\sqrt{\text{Hz}}$  noise density with an ultralow distortion of 0.00005% at 1 kHz. The OPA1652 and OPA1654 op amps offer rail-to-rail output swing to within 800 mV with a 2-k $\Omega$  load, which increases headroom and maximizes dynamic range. These devices also have a high output drive capability of  $\pm 30$  mA.

These devices operate over a very wide supply range of  $\pm 2.25$  V to  $\pm 18$  V, or +4.5 V to +36 V, on only 2 mA of supply current per channel. The OPA1652 and OPA1654 op amps are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions.

These devices also feature completely independent circuitry for lowest crosstalk and freedom from interactions between channels, even when overdriven or overloaded.

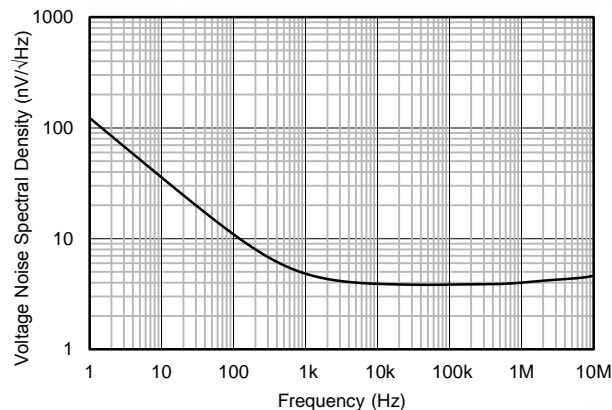
The OPA1652 and OPA1654 temperature ranges are specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA1652	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
OPA1654	SOIC (14)	8.65 mm x 3.91 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Input Voltage Noise Spectral Density



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Original (December 2011) to Revision A

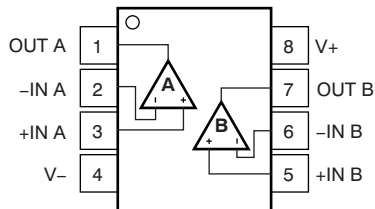
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- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section .....

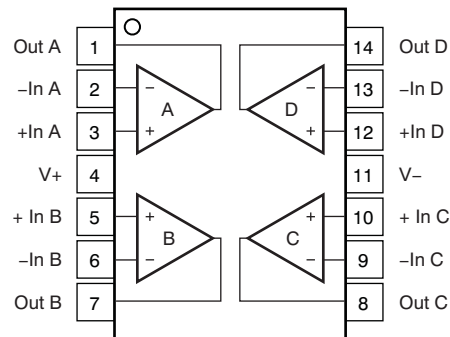
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## 5 Pin Configuration and Functions

**OPA1652: D and DGK Packages**  
8-Pin SOIC and VSSOP  
Top View



**OPA1654: D and PW Packages**  
14-Pin SOIC and TSSOP  
Top View



**Pin Functions: OPA1652**

NAME	PIN		I/O	DESCRIPTION
	OPA1652			
	SOIC	VSSOP		
-IN A	2		I	Inverting input, channel A
+IN A	3		I	Noninverting input, channel A
-IN B	6		I	Inverting input, channel B
+IN B	5		I	Noninverting input, channel B
OUT A	1		O	Output, channel A
OUT B	7		O	Output, channel B
V-	4		—	Negative (lowest) power supply
V+	8		—	Positive (highest) power supply

**Pin Functions: OPA1654**

NAME	PIN		I/O	DESCRIPTION
	OPA1654			
	SOIC	TSSOP		
-IN A	2		I	Inverting input, channel A
+IN A	3		I	Noninverting input, channel A
-IN B	6		I	Inverting input, channel B
+IN B	5		I	Noninverting input, channel B
-IN C	9		I	Inverting input, channel C
+IN D	10		I	Noninverting input, channel C
-IN D	13		I	Inverting input, channel D
+IN D	12		I	Noninverting input, channel D
Out A	1		O	Output, channel A
Out B	7		O	Output, channel B
Out C	8		O	Output, channel C
Out D	14		O	Output, channel D
V-	11		—	Negative (lowest) power supply
V+	4		—	Positive (highest) power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply voltage, $V_S = (V+) - (V-)$		40	V
	Input	$(V-) - 0.5$	$(V+) + 0.5$	V
Current	Input (all pins except power-supply pins)	-10	10	mA
	Output short-circuit <sup>(2)</sup>	Continuous		
Temperature	Operating, $T_A$	-55	125	°C
	Junction, $T_J$		200	°C
	Storage, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to  $V_S/2$  (ground in symmetrical dual supply setups), one amplifier per package.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000
		Machine model (MM)	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Supply voltage	4.5 (±2.25)		36 (±18)	V
$T_A$	Operating temperature	-40		85	°C

## 6.4 Thermal Information: OPA1652

THERMAL METRIC <sup>(1)</sup>		OPA1652		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	143.6	218.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.9	78.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.8	103.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	27.8	14.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	61.3	101.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the application report, [Semiconductor and IC Package Thermal Metrics](#).

## 6.5 Thermal Information: OPA1654

THERMAL METRIC <sup>(1)</sup>		OPA1654		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.1	126.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.8	46.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	58.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	19.9	5.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	44.2	57.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the application report, [Semiconductor and IC Package Thermal Metrics](#).

## 6.6 Electrical Characteristics: $V_S = \pm 15\text{ V}$

At  $T_A = 25^\circ\text{C}$ ,  $R_L = 2\text{ k}\Omega$ , and  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>AUDIO PERFORMANCE</b>						
THD+N	Total harmonic distortion + noise		0.00005%			
		$G = +1$ , $f = 1\text{ kHz}$ , $V_O = 3 V_{RMS}$	-126			dB
IMD	Intermodulation distortion	$G = +1$ , $V_O = 3 V_{RMS}$	SMPTE/DIN Two-Tone, 4:1 (60 Hz and 7 kHz)	0.00005%		
				-126		dB
			DIM 30 (3-kHz square wave and 15-kHz sine wave)	0.00005%		
				-126		dB
CCIF Twin-Tone (19 kHz and 20 kHz)		0.00005%				
				-126		dB
<b>FREQUENCY RESPONSE</b>						
GBW	Gain-bandwidth product	$G = +1$	18			MHz
SR	Slew rate	$G = -1$	10			V/ $\mu\text{s}$
	Full power bandwidth <sup>(1)</sup>	$V_O = 1 V_P$	1.6			MHz
	Overload recovery time	$G = -10$	1			$\mu\text{s}$
	Channel separation (dual and quad)	$f = 1\text{ kHz}$	-120			dB
<b>NOISE</b>						
$e_n$	Input voltage noise	$f = 20\text{ Hz to } 20\text{ kHz}$	5.4			$\mu\text{V}_{PP}$
	Input voltage noise density	$f = 1\text{ kHz}$	4.5			$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$	3.8			$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 1\text{ kHz}$	3			$\text{fA}/\sqrt{\text{Hz}}$
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$	$\pm 0.5$	$\pm 1.5$		mV
		$V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$ , $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ <sup>(2)</sup>	2	8		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = \pm 2..25\text{ V to } \pm 18\text{ V}$	3	8		$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$V_{CM} = 0\text{ V}$	$\pm 10$	$\pm 100$		pA
$I_{OS}$	Input offset current	$V_{CM} = 0\text{ V}$	$\pm 10$	$\pm 100$		pA
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range		$(V-) + 0.5$	$(V+) - 2$		V
CMRR	Common-mode rejection ratio		100	110		dB
<b>INPUT IMPEDANCE</b>						
	Differential		100    6			M $\Omega$    pF
	Common-mode		6000    2			G $\Omega$    pF
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$(V-) + 0.8\text{ V} \leq V_O \leq (V+) - 0.8\text{ V}$ , $R_L = 2\text{ k}\Omega$	106	114		dB
<b>OUTPUT</b>						
$V_{OUT}$	Voltage output	$R_L = 2\text{ k}\Omega$	$(V-) + 0.8$	$(V+) - 0.8$		V
$I_{OUT}$	Output current		See <a href="#">Typical Characteristics</a>			mA
$Z_O$	Open-loop output impedance	$f = 1\text{ MHz}$	See <a href="#">Typical Characteristics</a>			$\Omega$
$I_{SC}$	Short-circuit current <sup>(3)</sup>		$\pm 50$			mA
$C_{LOAD}$	Capacitive load drive		100			pF

(1) Full-power bandwidth =  $SR / (2\pi \times V_P)$ , where SR = slew rate.

(2) Specified by design and characterization.

(3) One channel at a time.

**Electrical Characteristics:  $V_S = \pm 15\text{ V}$  (continued)**

 At  $T_A = 25^\circ\text{C}$ ,  $R_L = 2\text{ k}\Omega$ , and  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
$V_S$	Specified voltage		$\pm 2.25$		$\pm 18$	V
$I_Q$	Quiescent current (per channel)	$I_{OUT} = 0\text{ A}$		2	2.5	mA
		$I_{OUT} = 0\text{ A}$ , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ <sup>(2)</sup>			2.8	mA
<b>TEMPERATURE</b>						
	Specified range		-40		85	$^\circ\text{C}$
	Operating range		-55		125	$^\circ\text{C}$

OPA1652, OPA1654

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6.7 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.

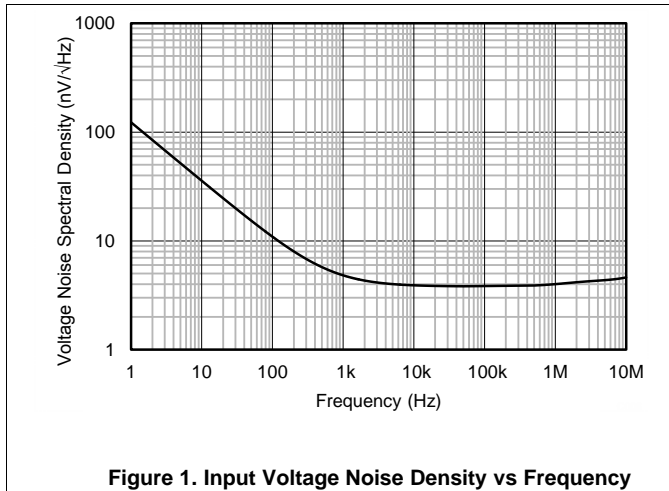


Figure 1. Input Voltage Noise Density vs Frequency

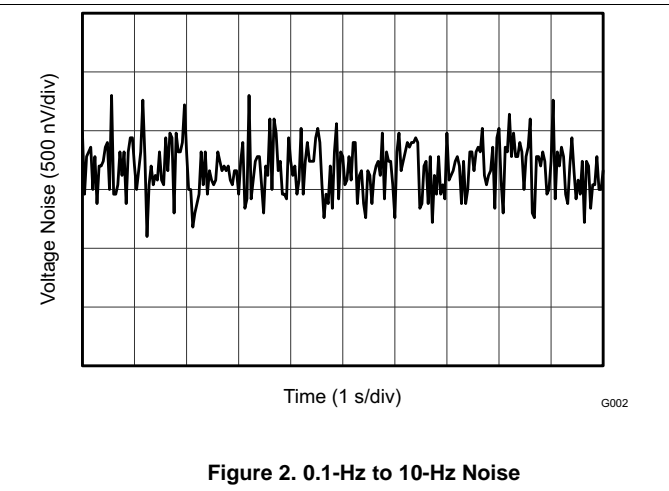


Figure 2. 0.1-Hz to 10-Hz Noise

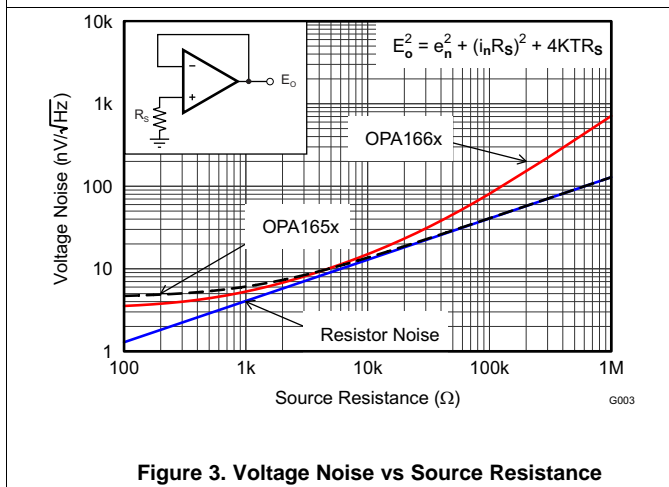


Figure 3. Voltage Noise vs Source Resistance

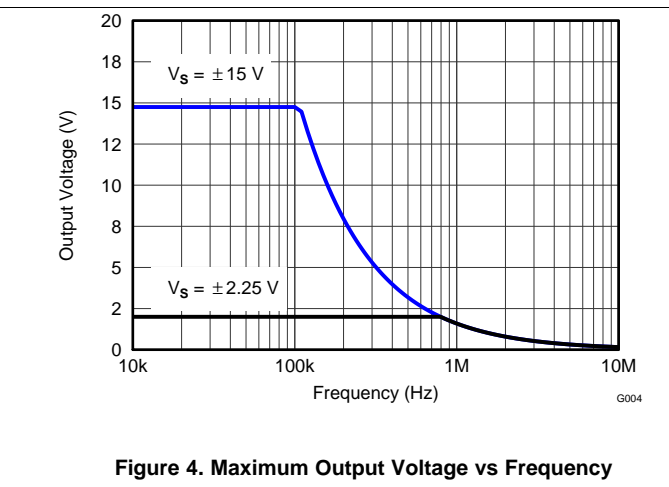


Figure 4. Maximum Output Voltage vs Frequency

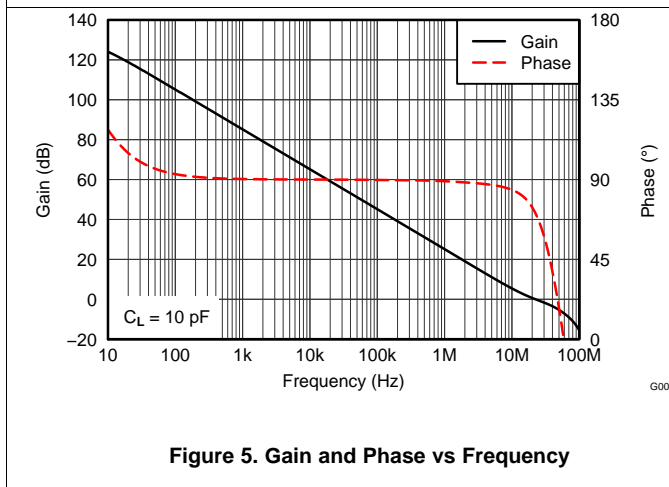


Figure 5. Gain and Phase vs Frequency

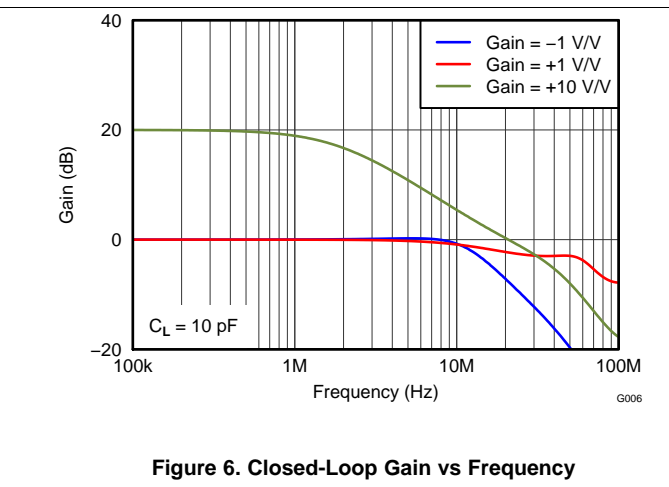


Figure 6. Closed-Loop Gain vs Frequency



Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.

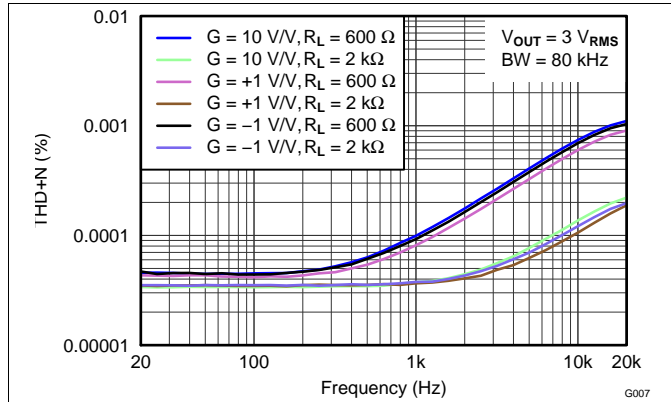


Figure 7. THD+N Ratio vs Frequency

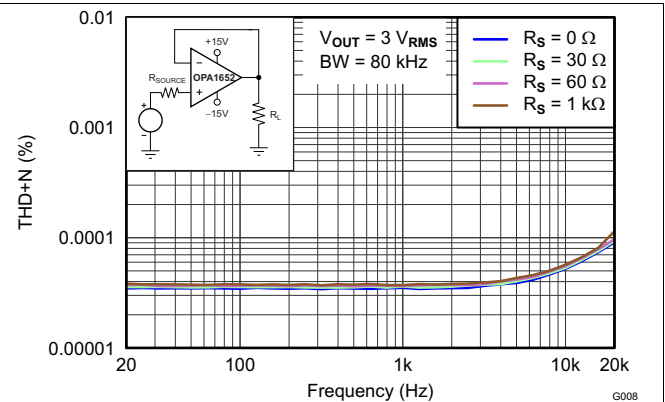


Figure 8. THD+N Ratio vs Frequency

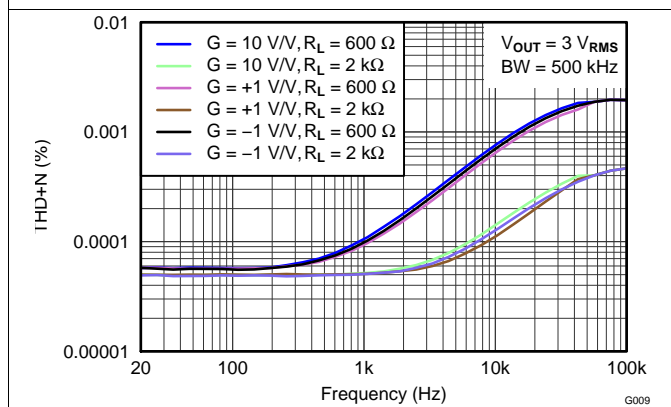


Figure 9. THD+N Ratio vs Frequency

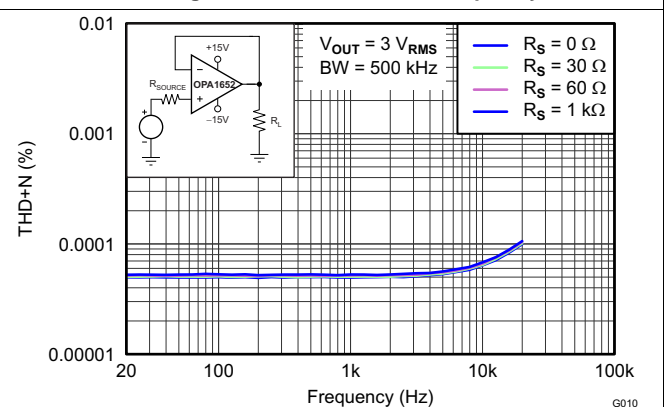


Figure 10. THD+N Ratio vs Frequency

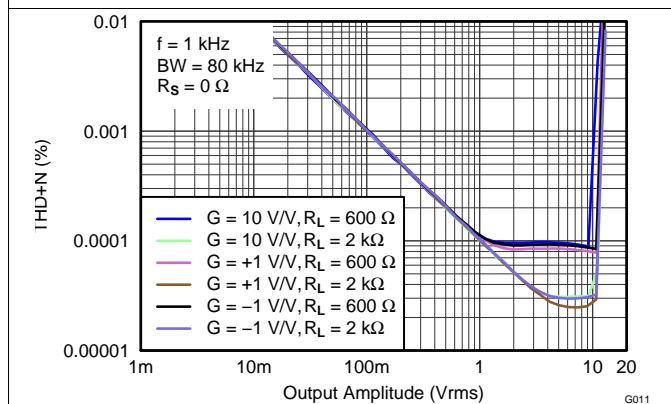


Figure 11. THD+N Ratio vs Output Amplitude

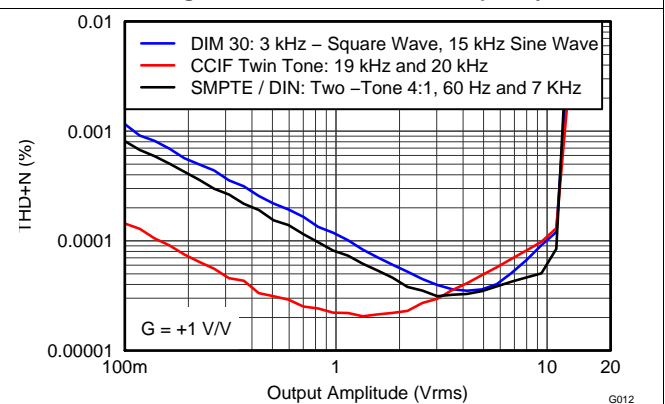
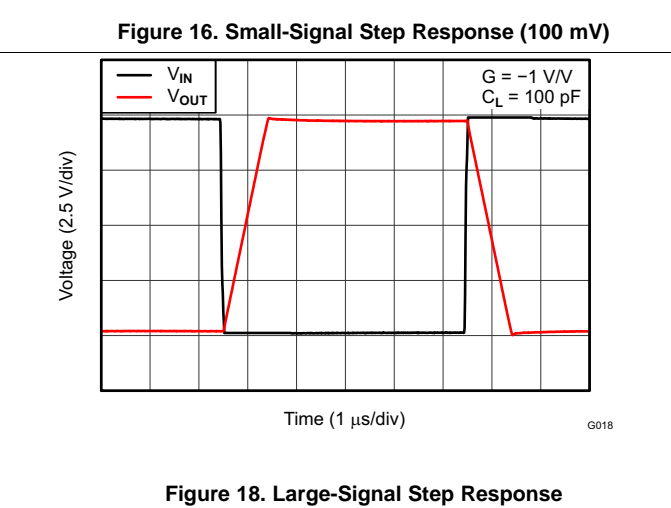
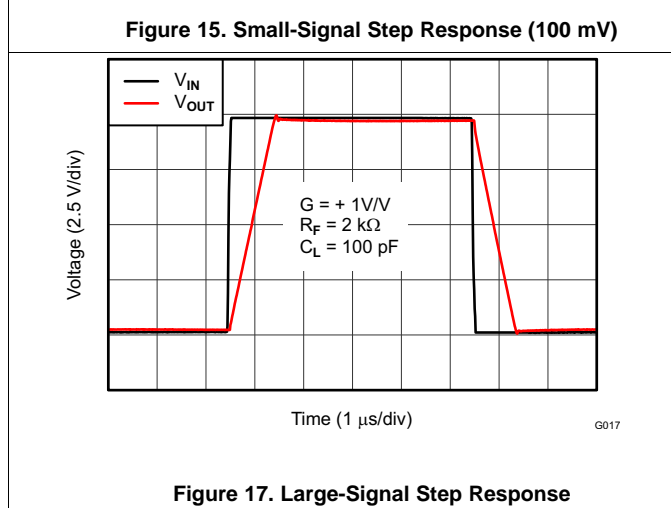
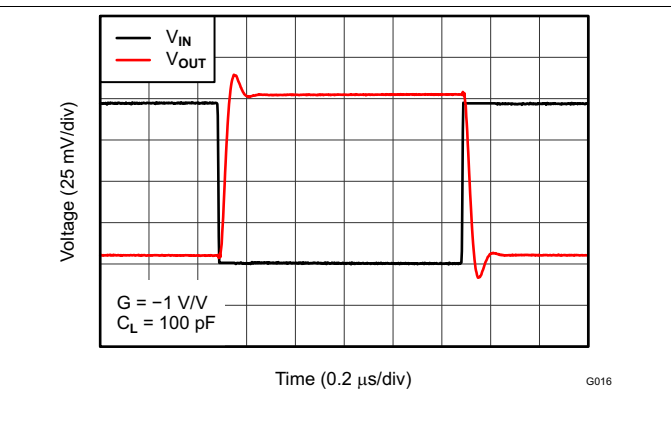
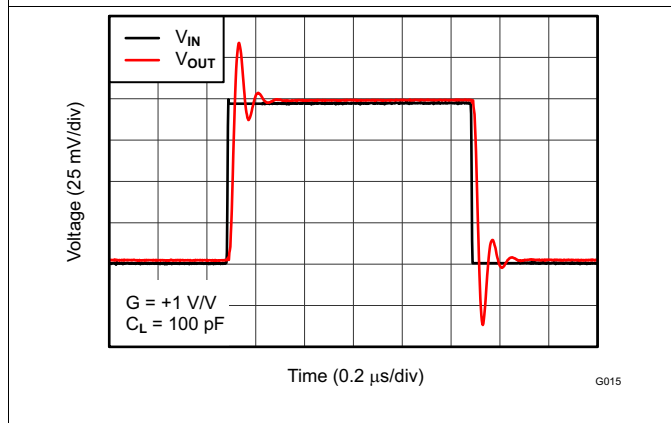
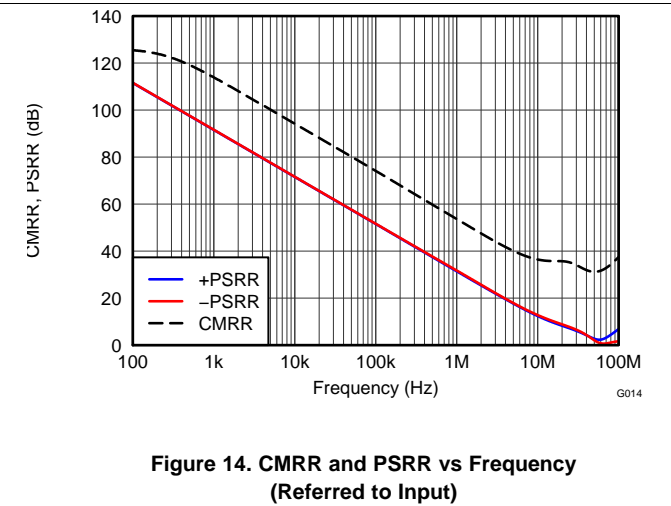
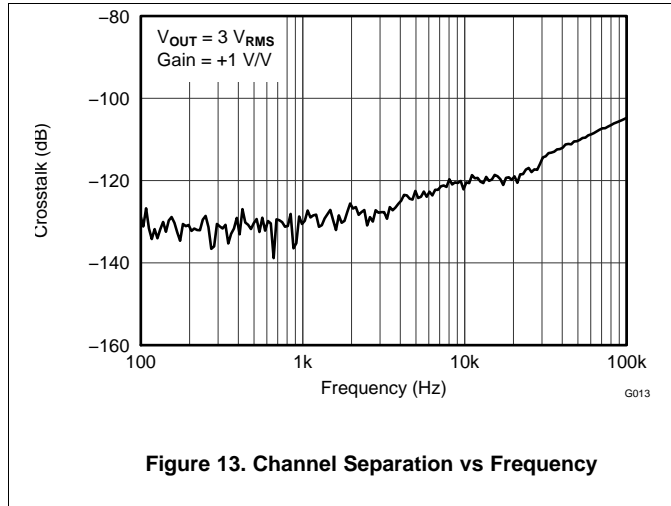


Figure 12. Intermodulation Distortion vs Output Amplitude

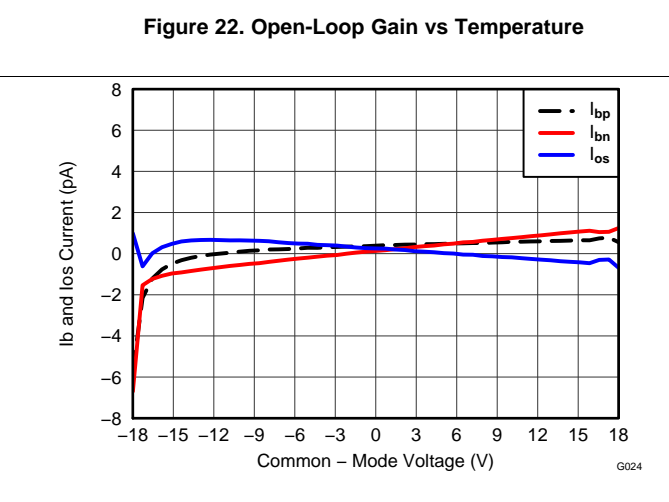
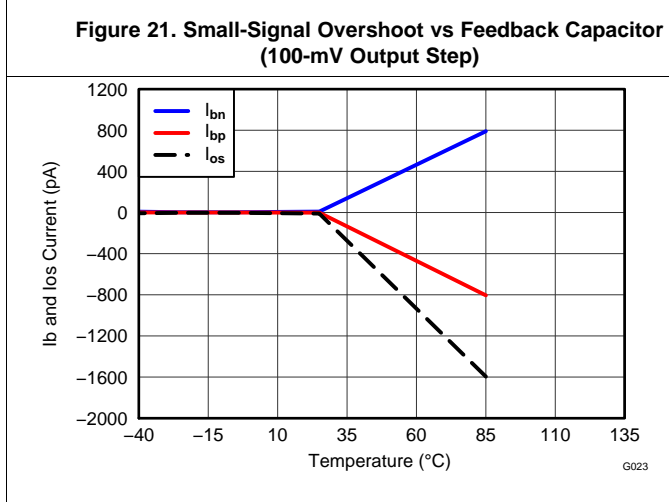
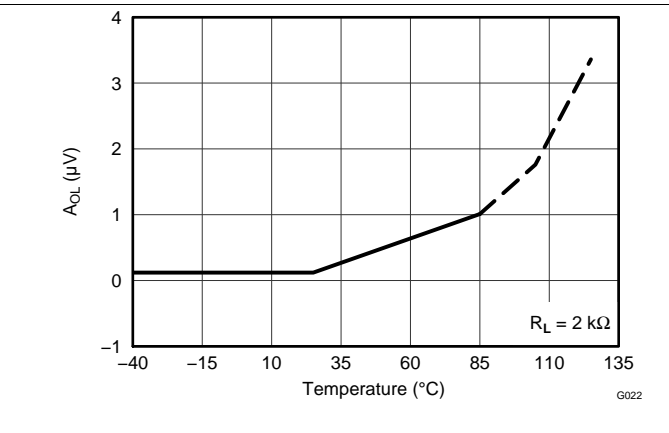
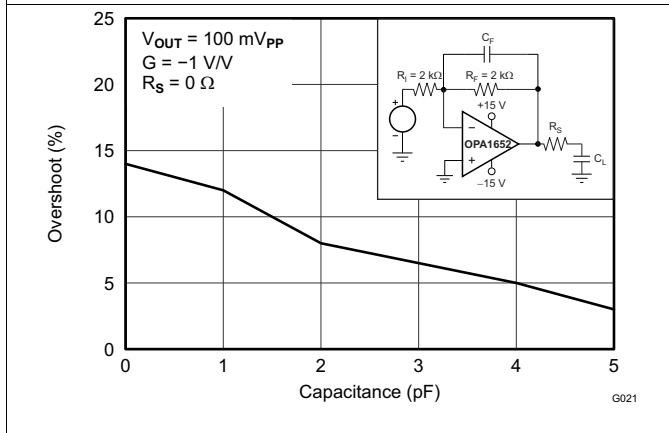
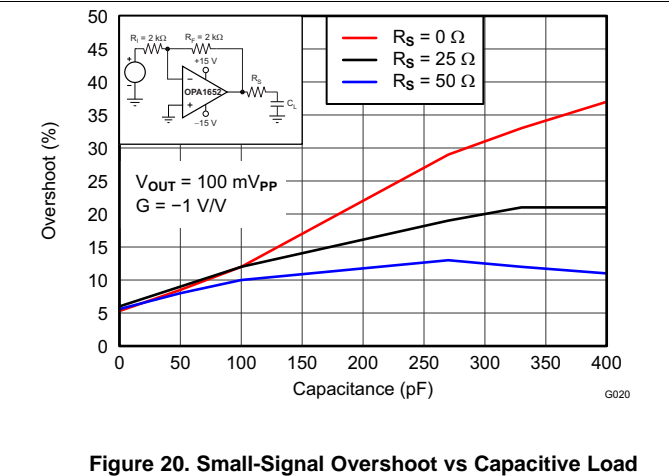
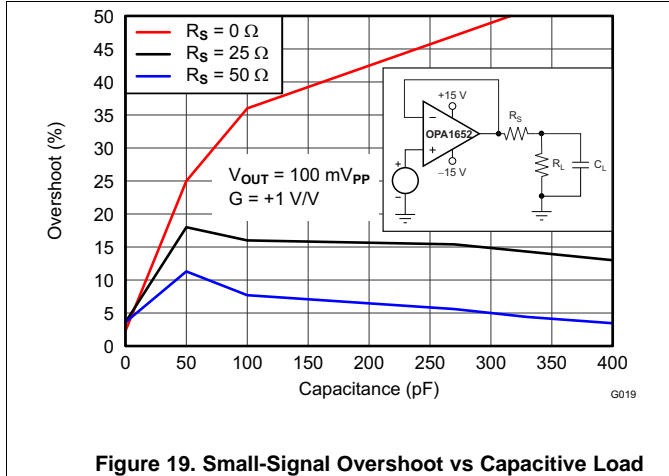
### Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.



Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.



**Typical Characteristics (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.

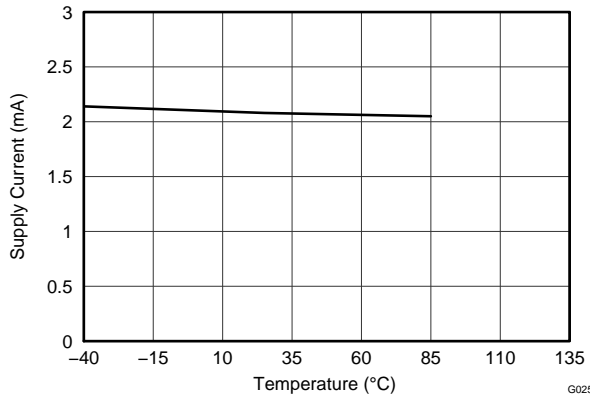


Figure 25. Supply Current vs Temperature

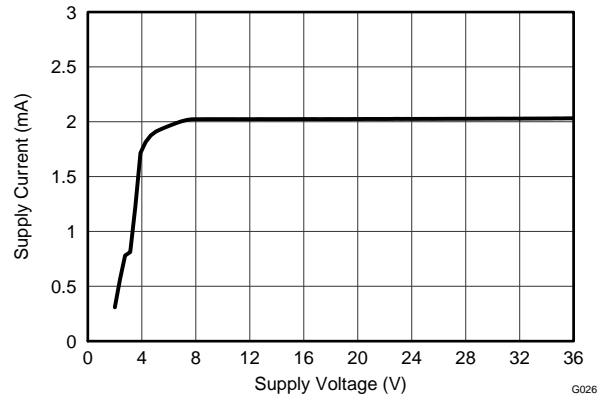


Figure 26. Supply Current vs Supply Voltage

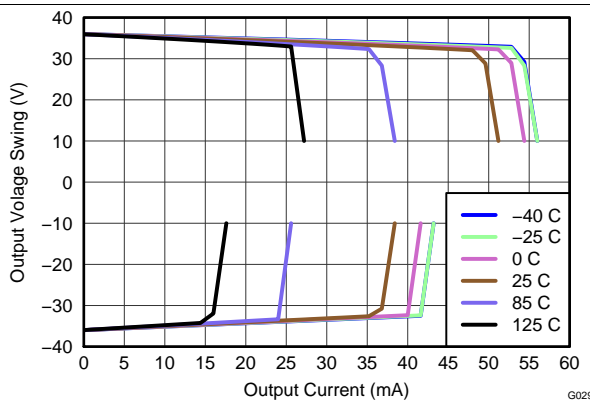


Figure 27. Output Voltage vs Output Current

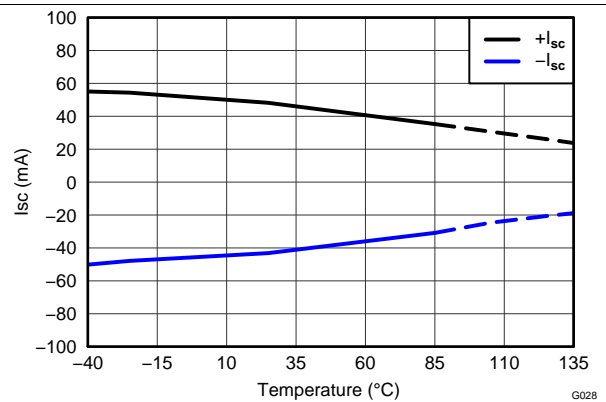


Figure 28. Short-Circuit Current vs Temperature

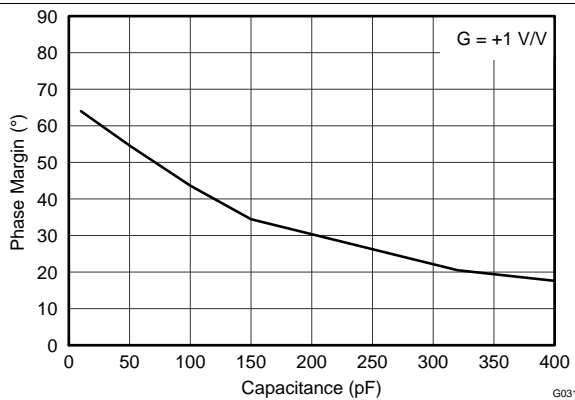


Figure 29. Phase Margin vs Capacitive Load

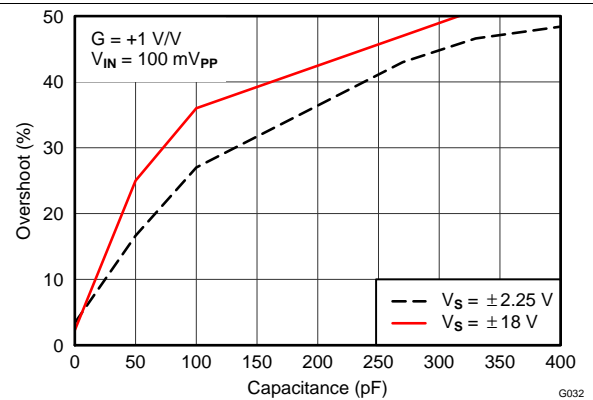
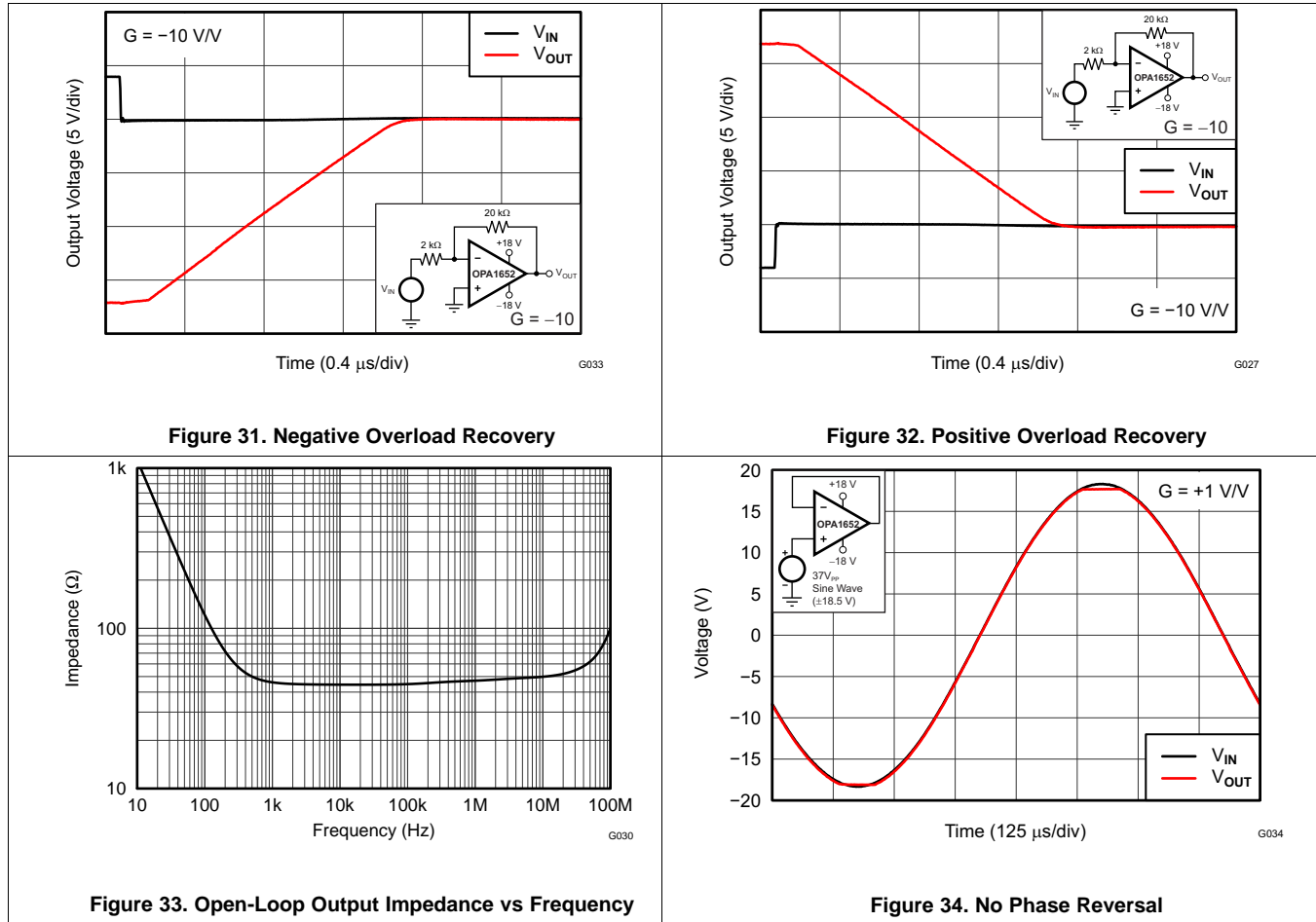


Figure 30. Percent Overshoot vs Capacitive Load

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.

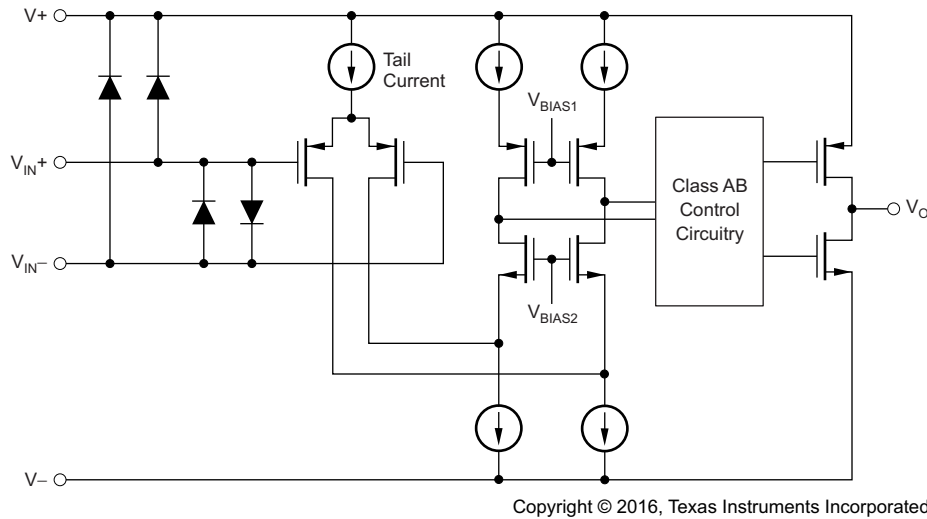


## 7 Detailed Description

### 7.1 Overview

The OPA1652 and OPA1654 are unity-gain stable, precision dual and quad op amps with very low noise. The [Functional Block Diagram](#) shows a simplified schematic of the OPA165x (one channel shown). The device consists of a very low noise input stage with a folded cascode and a rail-to-rail output stage. This topology exhibits superior noise and distortion performance across a wide range of supply voltages not previously delivered by audio operational amplifiers.

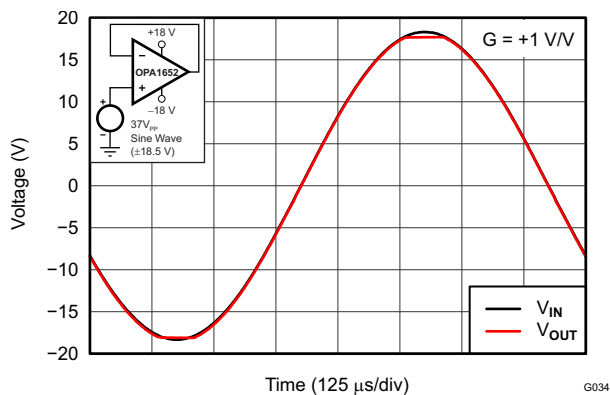
### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Phase Reversal Protection

The OPA165x family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA165x prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in [Figure 35](#).

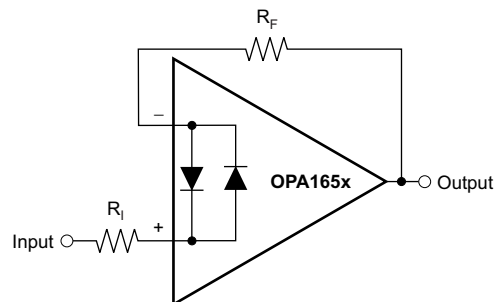


**Figure 35. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition**

## Feature Description (continued)

### 7.3.2 Input Protection

The input terminals of the OPA1652 and OPA1654 are protected from excessive differential voltage with back-to-back diodes, as [Figure 36](#) illustrates. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or  $G = +1$  circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor ( $R_I$ ) and/or a feedback resistor ( $R_F$ ) can be used to limit the signal input current. This resistor degrades the low-noise performance of the OPA165x and is examined in the following [Noise Performance](#) section. [Figure 36](#) shows an example configuration when both current-limiting input and feedback resistors are used.



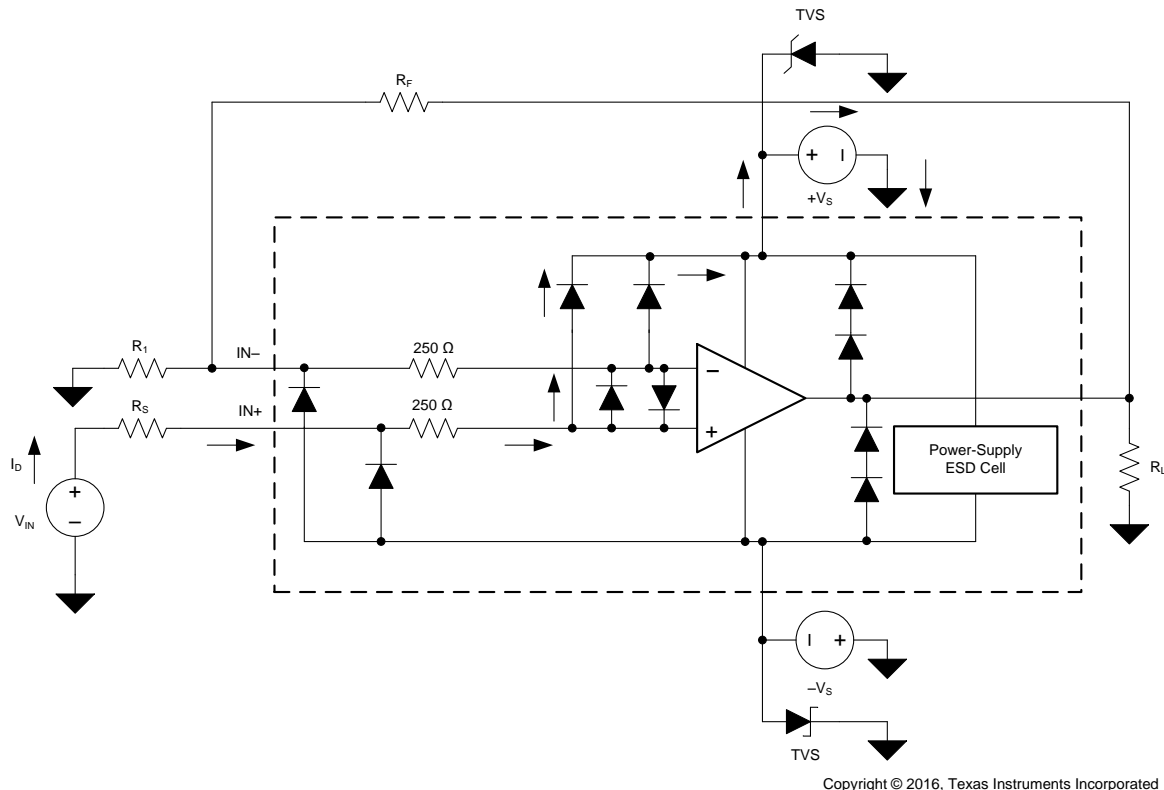
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**Figure 36. Pulsed Operation**

### 7.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. [Figure 37](#) illustrates the ESD circuits contained in the OPA165x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

**Feature Description (continued)**


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**Figure 37. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA165x but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (refer to [Figure 37](#)), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

[Figure 37](#) shows a specific example where the input voltage ( $V_{IN}$ ) exceeds the positive supply voltage ( $V+$ ) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If  $V+$  can sink the current, one of the upper input steering diodes conducts and directs current to  $V+$ . Excessively high current levels can flow with increasingly higher  $V_{IN}$ . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current,  $V_{IN}$  can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.



## Feature Description (continued)

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies ( $V+$  or  $V-$ ) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see [Figure 37](#). Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

## 7.4 Device Functional Modes

### 7.4.1 Operating Voltage

The OPA165x series op amps operate from  $\pm 2.25$  V to  $\pm 18$  V supplies while maintaining excellent performance. The OPA165x series can operate with as little as +4.5V between the supplies and with up to +36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA165x series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25 V with the negative supply at  $-5$  V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range of  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ . Parameters that vary significantly with operating voltage or temperature are shown in the [Typical Characteristics](#).

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

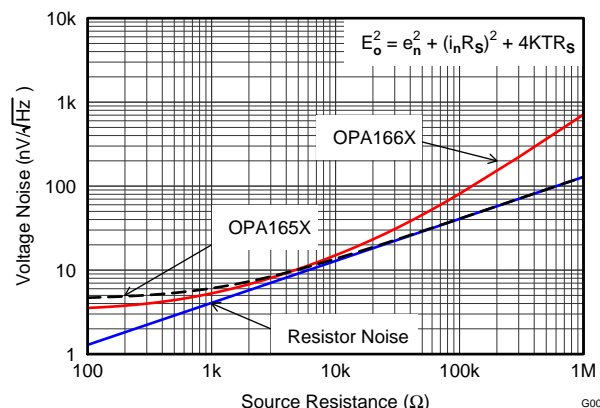
#### 8.1.1 Noise Performance

Figure 38 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions).

The OPA165x (GBW = 18 MHz, G = +1) is shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The voltage noise of the OPA165x series op amps makes them a better choice for source impedances greater than or equal to 1 kΩ.

The equation in Figure 38 shows the calculation of the total circuit noise, with these parameters:

- $e_n$  = Voltage noise
- $i_n$  = Current noise
- $R_s$  = Source impedance
- $k$  = Boltzmann's constant =  $1.38 \times 10^{-23}$  J/K
- $T$  = Temperature in Kelvins (K)



**Figure 38. Noise Performance of the OPA165x in Unity-Gain Buffer Configuration**

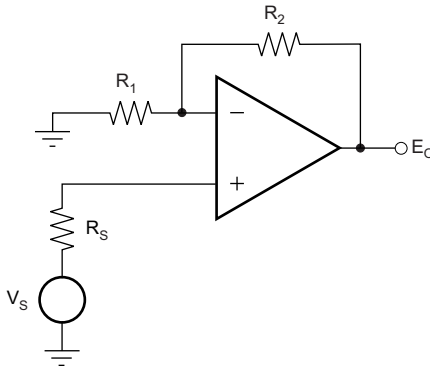
Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. Figure 38 plots this equation. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 39 illustrates both inverting (Figure 39 B) and noninverting (Figure 39 A) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

**Application Information (continued)**

**A) Noise in Noninverting Gain Configuration**



Noise at the output:

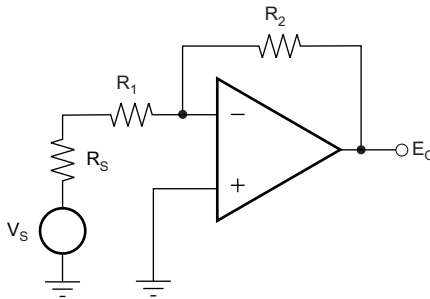
$$E_o^2 = \left[ 1 + \frac{R_2}{R_1} \right]^2 e_n^2 + \left[ \frac{R_2}{R_1} \right]^2 e_1^2 + e_2^2 + \left[ 1 + \frac{R_2}{R_1} \right]^2 e_s^2$$

Where  $e_s = \sqrt{4kTR_s}$  = thermal noise of  $R_s$

$e_1 = \sqrt{4kTR_1}$  = thermal noise of  $R_1$

$e_2 = \sqrt{4kTR_2}$  = thermal noise of  $R_2$

**B) Noise in Inverting Gain Configuration**



Noise at the output:

$$E_o^2 = \left[ 1 + \frac{R_2}{R_1 + R_s} \right]^2 e_n^2 + \left[ \frac{R_2}{R_1 + R_s} \right]^2 e_1^2 + e_2^2 + \left[ \frac{R_2}{R_1 + R_s} \right]^2 e_s^2$$

Where  $e_s = \sqrt{4kTR_s}$  = thermal noise of  $R_s$

$e_1 = \sqrt{4kTR_1}$  = thermal noise of  $R_1$

$e_2 = \sqrt{4kTR_2}$  = thermal noise of  $R_2$

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Note: For the OPA165x series of op amps at 1 kHz,  $e_n = 4.5 \text{ nV}/\sqrt{\text{Hz}}$ .

**Figure 39. Noise Calculation in Gain Configurations**

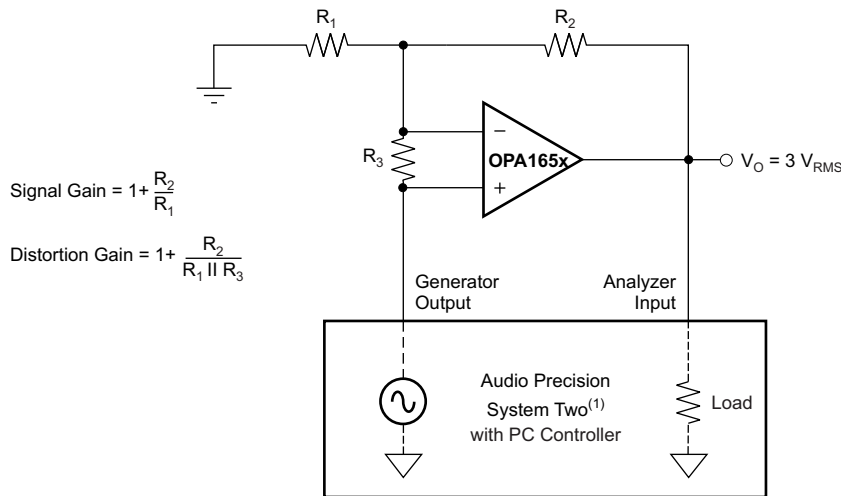
**8.1.2 Total Harmonic Distortion Measurements**

The OPA165x series op amps have excellent distortion characteristics. THD + noise is below 0.0002% ( $G = +1$ ,  $V_o = 3 V_{RMS}$ ,  $BW = 80 \text{ kHz}$ ) throughout the audio frequency range, 20 Hz to 20 kHz, with a 2-k $\Omega$  load (see [Figure 7](#) for characteristic performance).

The distortion produced by the OPA165x series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as [Figure 40](#) shows) can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. [Figure 40](#) shows a circuit that causes the op amp distortion to be gained up (refer to the table in [Figure 40](#) for the distortion gain factor for various signal gains). The addition of  $R_3$  to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by the distortion gain factor, thus extending the resolution by the same amount. Note that the input signal and load applied to the op amp are the same as with conventional feedback without  $R_3$ . The value of  $R_3$  should be kept small to minimize its effect on the distortion measurements.

The validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

**Application Information (continued)**


SIGNAL GAIN	DISTORTION GAIN	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>
+1	101	∞	1 kΩ	10 Ω
-1	101	4.99 kΩ	4.99 kΩ	49.9 Ω
+10	110	549 Ω	4.99 kΩ	49.9 Ω

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 (1) For measurement bandwidth, see [Figure 7](#) through [Figure 12](#).

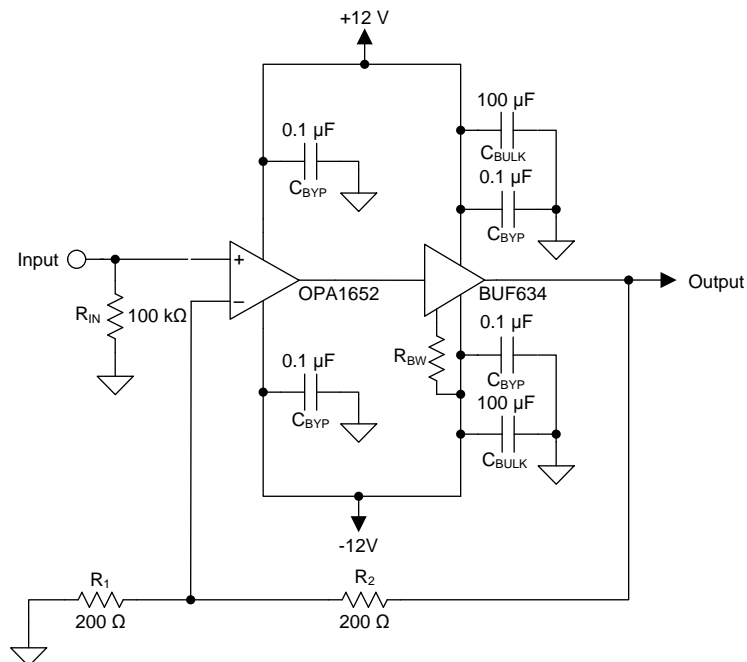
**Figure 40. Distortion Test Circuit**
**8.1.3 Capacitive Loads**

The dynamic characteristics of the OPA1652 and OPA1654 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor ( $R_S$  equal to 50 Ω, for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device becomes shorted. [Figure 19](#) illustrates a graph of *Small-Signal Overshoot vs Capacitive Load* for several values of  $R_S$ . Also, refer to [Feedback Plots Define Op Amp AC Performance](#) (SBOA015), available for download from the TI website, for details of analysis techniques and application circuits.

## 8.2 Typical Application

The low noise and distortion of the OPA165x family of audio operational amplifiers make them an excellent choice for a number of analog audio circuits. One such circuit is shown in Figure 41 which illustrates a power amplifier circuit suitable for high-fidelity headphone applications.



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Figure 41. Composite Power Amplifier for Headphones

### 8.2.1 Design Requirements

- Gain: 6 dB
- Output Voltage: > 2 V<sub>RMS</sub>, 32-Ω Load
- Output Impedance: < 1 Ω
- THD+N: < -110dB (1 kHz, 2 V<sub>RMS</sub>, 32-Ω Load)

### 8.2.2 Detailed Design Procedure

The power amplifier circuit (single channel shown) features a BUF634 high-speed buffer amplifier inside the feedback loop of an OPA1652 to increase the amount of available output current. The bandwidth and power consumption of the BUF634 can be set with an external resistor, R<sub>BW</sub>. For this circuit, a 0-Ω resistor was used for R<sub>BW</sub>, which configures the BUF634 for its widest bandwidth and highest performance. The gain of the circuit is determined by the feedback resistors R<sub>1</sub> and R<sub>2</sub> as shown in Equation 1:

$$A_V = 1 + \frac{R_2}{R_1} \quad (1)$$

To achieve the design goal of 6-dB voltage gain (2 V/V), R<sub>1</sub> and R<sub>2</sub> must have equal values. These resistors also contribute noise thermal noise to the circuit. The voltage noise spectral density of the feedback resistors, referred to the amplifier input, is given in Equation 2:

$$e_{NR} = \sqrt{4kT(R_2 \parallel R_1)} \quad (2)$$

Ideally, the thermal noise contributions of the resistors would not significantly degrade the noise performance of the circuit. Selecting resistor values such that the resistor noise is less than one-third the input voltage noise of the op amp (Equation 3) ensures that any increase in the circuit noise as a result of the feedback resistor contributions is minimal.

**Typical Application (continued)**

$$e_{NR} \leq \frac{e_{OA}}{3} \tag{3}$$

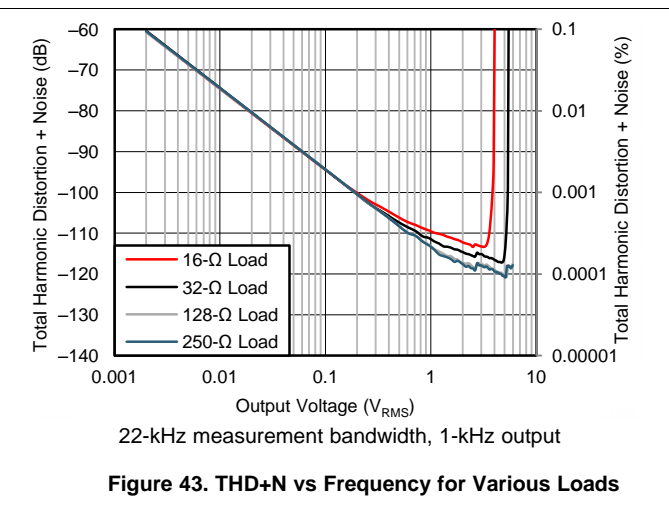
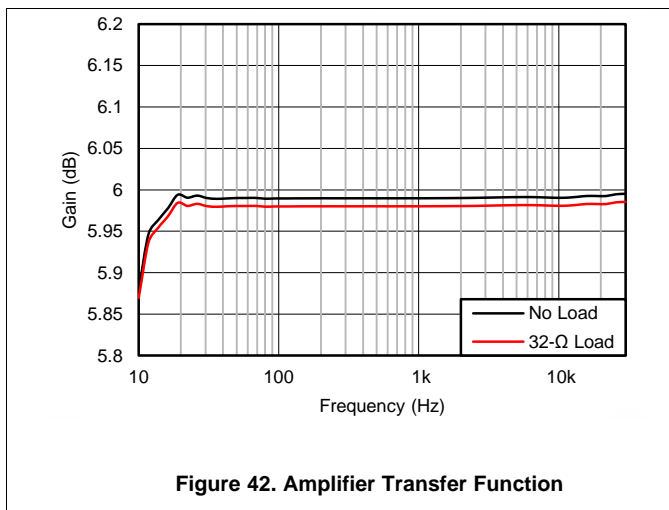
To calculate the required resistor values, Equation 3 is inserted into Equation 2, and the resulting equation is rearranged to solve for the parallel combination of  $R_1$  and  $R_2$  as shown in Equation 4. Using a value of 3.8 nV/ $\sqrt{\text{Hz}}$  as the broadband voltage noise of the OPA1652 results in a value of 96.8  $\Omega$  for the parallel combination of  $R_1$  and  $R_2$ . Standard value 200- $\Omega$  resistors were used for  $R_1$  and  $R_2$ , resulting in a parallel value of 100  $\Omega$ , which is suitably close to the required value.

$$R_1 || R_2 \leq \frac{e_{OA}^2}{36kT} \leq \frac{(3.8 \text{ nV}/\sqrt{\text{Hz}})^2}{36 \times 1.381 \times 10^{-23} \times 300} \leq 96.8 \Omega \tag{4}$$

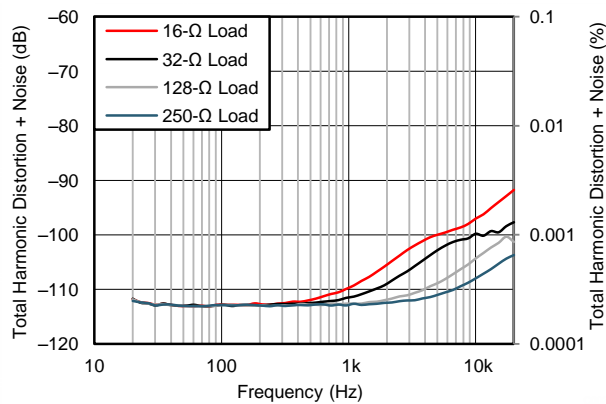
Because of the extremely wide bandwidth and high slew rate of the BUF634, no additional components were required to maintain stability in the circuit or prevent latch-up conditions. This circuit was found to be stable with capacitive loads over 1 nF, which is suitable for headphone applications.

**8.2.3 Application Curves**

The measured performance of the circuit is shown in Figure 42 through Figure 46. The frequency response is extremely flat over the full audio bandwidth, deviating only 0.004 dB over the audible range. The decrease in gain shown at low frequency is a result of the test equipment and not the amplifier circuit. The amplifier output impedance, calculated from the change in gain in the loaded and unloaded conditions, is 0.036  $\Omega$ . The maximum output power before clipping is displayed in Figure 43. For a 32- $\Omega$  load, the power amplifier was able to deliver 781 mW before clipping. The best THD+N performance achieved with a 32- $\Omega$  load was -117.2 dB at 678 mW (1 kHz, 22-kHz measurement bandwidth). THD+N vs frequency is shown in Figure 44 for a 2- $V_{RMS}$  output level measured in a 90-kHz bandwidth. The worst-case measurement was for a 16- $\Omega$  load (250 mW), 20-kHz input frequency, -91.8 dB (0.0026%). Two FFTs are also shown of the amplifier output spectrum for a 2- $V_{RMS}$ , 1-kHz, fundamental into two different loads. All distortion harmonics are below -120 dB relative to the fundamental for both loading conditions.

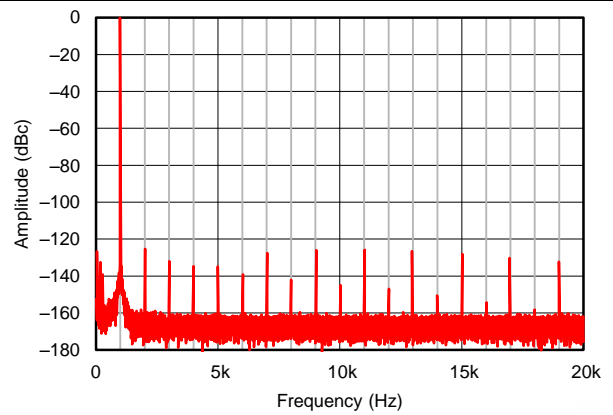


Typical Application (continued)



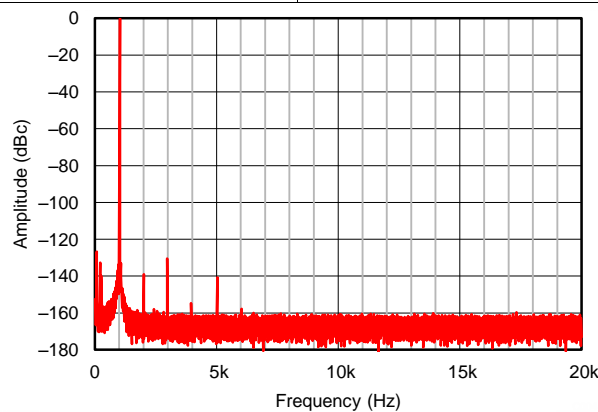
90-kHz measurement bandwidth, 2- $V_{RMS}$  output

Figure 44. THD+N vs Frequency for Various Loads



1 kHz, 32- $\Omega$  load, 2- $V_{RMS}$  output

Figure 45. Output Spectrum



1 kHz, 250- $\Omega$  load, 2  $V_{RMS}$

Figure 46. Output Spectrum

## 9 Power Supply Recommendations

The OPA165x are specified for operation from 4.5 V to 36 V ( $\pm 2.25$  V to  $\pm 18$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1- $\mu\text{F}$  capacitors are adequate.

## 10 Layout

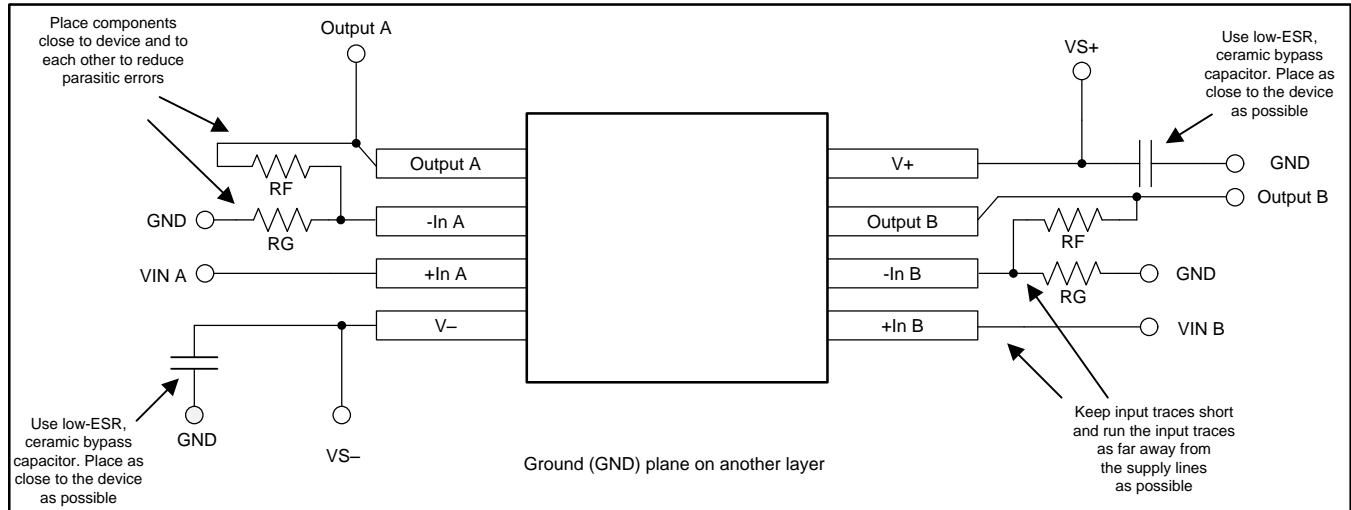
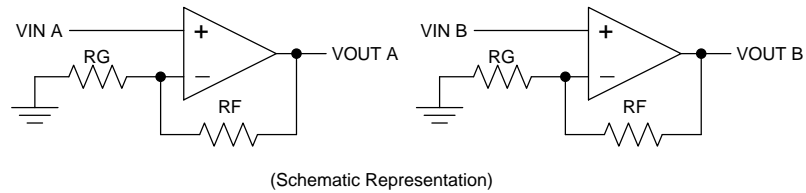
### 10.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V+$  to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Physically separate digital and analog grounds, observing the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 47](#), keeping  $R_F$  and  $R_G$  close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at  $85^{\circ}\text{C}$  for 30 minutes is sufficient for most circumstances.



## 10.2 Layout Example



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Figure 47. Operational Amplifier Board Layout for Noninverting Configuration

## 10.3 Power Dissipation

The OPA1652 and OPA1654 series op amps are capable of driving 2-k $\Omega$  loads with a power-supply voltage up to  $\pm 18$  V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA165x series op amps improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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#### NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

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##### 11.1.1.2 DIP Adapter EVM

The [DIP Adapter EVM](#) tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

##### 11.1.1.3 Universal Operational Amplifier EVM

The [Universal Op Amp EVM](#) is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP and SOT-23 packages are all supported.

---

#### NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

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##### 11.1.1.4 Smart Amplifier Speaker Characterization Board Evaluation Module

The [Smart Amplifier Speaker Characterization Board](#), when used in conjunction with a supported TI Smart Amplifier and PurePath Console software, provides users the ability to measure speaker excursion, temperature and other parameters for use with a TI Smart Amplifier products.

##### 11.1.1.5 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at <http://www.ti.com/ww/en/analog/precision-designs/>.

##### 11.1.1.6 WEBENCH® Filter Designer

[WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, [WEBENCH® Filter Designer](#) allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

The following documents are relevant to using the OPA165x, and recommended for reference. All are available for download at [www.ti.com](http://www.ti.com) unless otherwise noted.

- [OPA1652, OPA1654 EMIR Immunity Performance](#) (SBOT007)
- [Source resistance and noise considerations in amplifiers](#) (SLYT470)
- [Single-Supply Operation of Operational Amplifiers](#) (SBOA059)
- [Op Amp Performance Analysis](#) (SBOA054)
- [Compensate Transimpedance Amplifiers Intuitively](#) (SBOA055)
- [Tuning in Amplifiers](#) (SBOA067)
- [Feedback Plots Define Op Amp AC Performance](#) (SBOA015)
- [Active Volume Control for Professional Audio](#) (TIDU034)

### 11.3 Related Links

[Table 1](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA1652	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
OPA1654	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.5 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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### 11.7 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1652AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652	<a href="#">Samples</a>
OPA1652AIDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OUP1	<a href="#">Samples</a>
OPA1652AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OUP1	<a href="#">Samples</a>
OPA1652AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652	<a href="#">Samples</a>
OPA1652AIDRGR	PREVIEW	SON	DRG	8	3000	TBD	Call TI	Call TI	-40 to 85		
OPA1652AIDRGT	PREVIEW	SON	DRG	8	250	TBD	Call TI	Call TI	-40 to 85		
OPA1654AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654	<a href="#">Samples</a>
OPA1654AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654	<a href="#">Samples</a>
OPA1654AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654	<a href="#">Samples</a>
OPA1654AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1652AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1652AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1654AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA1654AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1652AIDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
OPA1652AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA1654AIDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA1654AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. JEDEC MO-229 package registration pending.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
 E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
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Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
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Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
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